The 2026 IEEE 76th Electronic Components and Technology Conference

May 26 – 29, 2026

2026 Conference Program & Exhibitor Listings

Sponsored by IEEE ELECTRONICS PACKAGING SOCIETY, IEEE

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WELCOME TO THE IEEE 76th ECTC FROM THE GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program and Executive Committees, we are pleased to welcome you to the IEEE 76th Electronic Components and Technology Conference (ECTC). Sponsored by the IEEE Electronics Packaging Society, this premier event is held May 26–29, 2026, at the JW Marriott & The Ritz-Carlton Grande Lakes in Orlando, Florida. As the world's leading microelectronics packaging conference, ECTC unites over 2,000 global professionals—including top manufacturers, design houses, foundries, researchers, and investors. Join us to engage with key stakeholders and explore the breakthrough technologies shaping the future of the industry.

The 76th ECTC returns with an exceptional program, building on last year's record-breaking attendance to deliver another premier experience for the microelectronics community. The conference starts with eight special sessions held on Tuesday, featuring parallel tracks where industry-leading panelists tackle the field's most pressing challenges and emerging technical innovations.

Following the successful debut of the ECTC Student Challenge, the 2026 conference features the second issue of this competition. An updated format includes three distinct categories for BSc, MSc, and PhD candidates, with winners to be officially announced during the Friday Luncheon.

Additionally, the Start-Up Competition takes place on Thursday. This event provides a platform for emerging companies to pitch their business ideas to a professional jury, followed by an audience Q&A, jury deliberation, and award presentation.

The conference concludes its major networking activities with the ECTC Reception Gala on Thursday evening. This hallmark event gathers all attendees for high-level networking and technical exchange in a collaborative environment.

At the 76th ECTC, approximately 450 technical papers are presented in 36 oral sessions and five interactive sessions. Authors from over 20 countries share their latest research on topics including: 3D integration, 2.5D architectures, bridge and chiplet integration, hybrid bonding, wafer-to-wafer and chip-to-wafer bonding, novel substrate materials, high-density RDL, next-generation interconnections, warpage management of large panels, and large-package manufacturing, additive manufacturing, wearable and medical applications, AI/ML, and advanced RF and antenna designs, thermal management, interconnect reliability, advanced characterization, and process simulations, eco-friendly packaging, and secure designs. The 76th ECTC serves as a global platform for exploring cutting-edge advancements in microelectronic packaging, fostering innovation, and addressing industry challenges.

This year, the conference features a total of twelve special sessions with industry experts, including nine on Tuesday, each lasting 90 minutes.

Following last year's successful model, the Tuesday schedule includes two concurrent tracks of special sessions. The first special session, exploring Quantum Infrastructure for AI Applications, will be co-chaired by Rabindra Das (MIT Lincoln Laboratory) and Pavel Roy Paladhi (NVIDIA). The second special session, which focuses on New Packaging Technologies for Panel Level Integration, is chaired by Venkata Mokkapati and Markus Leitgeb (AT&S), with Rozalia Beica (Rapidus) serving as moderator. Tuesday morning also features two additional parallel tracks. Special Session 5 addresses System Integration Challenges for Large-Scale, High-Power Components in HPC and AI Applications, led by chairs Tae-Kyu Lee (Cisco Systems, Inc.) and Michael Gallagher (Qnity Electronics). Following this at 10:30 a.m., Special Session 6 focuses on Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging, chaired by Tiwei Wei (UCLA) and Ning Ye (Sandisk). The first afternoon special session, AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging, is co-chaired by Ian O'Connor (Ecole Centrale de Lyon) and Jose Schutt-Aine (University of Illinois at Urbana-Champaign). In parallel, Special Session 7 explores Enabling Next Generation Advanced Technology From Wafer to Panel chaired by Kuldip Johal (MKS Instruments), Beth Keser (Volantis Semiconductor), and Lihong Cao (ASE).

Concluding the afternoon, two final special sessions are planned in parallel starting at 3:30 p.m. Special Session 4, titled Photonics-Based Systems for AI and Exascale Computing, is chaired by Stephane Bernabé (CEA-LETI) and Lars Brusberg (Corning, Inc.). Simultaneously, an additional special session explores Innovative Materials for Advanced Packaging, led by chairs Zia Karim (Yield Engineering Systems) and Ksenija Varga (EV Group).

Parallel to the special sessions, the Heterogeneous Integration Roadmap (HIR) workshop is chaired by Ravi Mahajan (Intel), Subu Iyer (UCLA), Anne Meixner (HIR Fellow), Benson Chan (Binghamton University), Rockwell Hsu (Cisco), and Jose Schutt-Aine (UIUC), carrying on the legacy of Dr. William (Bill) Chen (ASE). Four sessions are planned: Additive Electronics Manufacturing (AME) for Advanced Packaging moderated by Felippe Pavinatto (GE Aerospace); Metrology for Advanced Packaging: Challenges, Innovations, and Industry Impact moderated by Benson Chan (Binghamton University) and Antara Nandi (NIST); Emerging Technologies moderated by Rockwell Hsu (Cisco) and Zhichao Zhang (Intel); and Neuromorphic Computing moderated by Shaloo Rakheja and Jose Schutt-Aine (both with UIUC).

Tuesday evening offers additional opportunities to engage. Aakrati Jain (IBM) leads a Young Professionals Networking Event from 6:45 p.m. to 7:45 p.m. Following this, Takashi Hisada and Yasumitsu Orii (both with Rapidus) chair the IEEE EPS Seminar on Redefining System Integration: The Rise of Organic Substrates from 7:45 p.m. to 9:15 p.m.

On Wednesday morning, May 27, 2026, ECTC features its keynote presentation on Advanced Packaging & the Future of System Optimization by Dr. Tien Wu, CEO of Advanced Semiconductor Engineering (ASE), invited by General Chair Michael Mayer (University of Waterloo).

The Student Engagement Program, chaired by Ibrahim Guven (Virginia Commonwealth University) and Przemyslaw Gromala (Robert Bosch Kft), also takes place throughout the day, welcoming undergraduate students from local universities and colleges.

On Thursday, May 28, 2026, from 8:00 to 9:15 a.m., a Plenary Session asks the question "Efficiency Is Not Enough – Are We Solving the Wrong Problem in the Data Center Energy Use?". The discussion is chaired by Jan Vardaman (TechSearch International) and Masha Gorchichko (Marvell Technologies, Inc.)

Finally, the IEEE EPS President's Panel also covers data centers with a discussion entitled "Data Centers in the Age of AI – Challenges and Solutions" organized by IEEE EPS President Jeff Suhling (Auburn University) and EPS Members, David McCann (Amkor Technology), Benson Chan (Binghamton University) and Kanad Ghose (Binghamton University). It is held on Friday morning, May 29, 2026.

The IEEE ITherm Conference is co-located with the 76th ECTC. There are 16 CEU-approved, expert-led courses held on Tuesday, May 26, 2026. These Professional Development Courses (PDCs) are organized by Kitty Pearsall and Jeffrey Suhling.

The ECTC Exhibits, running Wednesday, May 27, and Thursday, May 28, showcase cutting-edge technologies and products from over 100 leading companies in electronic components, materials, packaging, and services. Starting daily at 9 a.m., the exhibits provide excellent opportunities for networking during coffee breaks, luncheons, and evening receptions.

Whether you are an engineer, manager, student, or executive, ECTC offers unique experiences for everyone in the microelectronics packaging and components industry. We invite you to join us for the 76th ECTC and to be a part of all the exciting technical and professional opportunities.

We want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 76th ECTC a success. We look forward to meeting you at JW Marriott & The Ritz-Carlton Grande Lakes Resort, Orlando, Florida, from May 26 to 29, 2026.

As many of you know, our community recently lost a truly respected leader with the passing of Dr. William (Bill) Chen on March 27, 2026. Over his distinguished, decades-long career, Bill was instrumental in shaping ECTC into the conference it is today, notably leading the efforts in 2010 for IEEE EPS to become its sole owner. To honor his incredible legacy and his impact as a mentor, we are proud to dedicate the 76th ECTC to his memory.

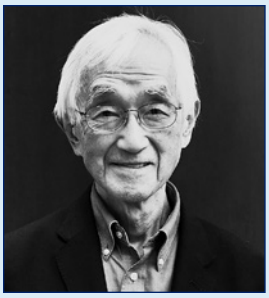
Michael Mayer
76th ECTC General Chair
mmayer@uwaterloo.ca

Bora Baloglu
76th ECTC Program Chair
borabal@ieee.org

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society (EPS), I am delighted to welcome you to the 2026 Electronic Components and Technology Conference. ECTC is widely recognized as the premier international event for electronics packaging. Building on a long history of annual events with a few conference name changes along the way, ECTC celebrated its 75th anniversary last year with a record setting attendance of over 2,500 semiconductor packaging technologists from across the globe. This year represents the 76th annual meeting, and it will be held in parallel with ITherm 2026 at the same venue. We expect to continue to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging.

As many of you have heard, the electronics packaging community lost one of its long-term and most widely respected leaders with the passing away of Dr. William (Bill) Chen on March 27, 2026. Bill was a visionary with a strategic world view, who successfully fostered strong bridges between industry and academia. He served as an invaluable mentor to many of us throughout our careers. We will pay tribute to his legacy at several events during the conference including the Heterogeneous Integration Roadmap (HIR) sessions on Tuesday, and the EPS Luncheon on Thursday. In addition to countless contributions throughout his career, Bill served as IEEE EPS President for two terms. While President, he led the team that negotiated for IEEE EPS to become the sole owner/sponsor of all future ECTC conferences in 2010, ensuring that it would be our flagship event for many years to come.



Remembering
William (Bill) Chen • March 27, 2026

Following ECTC this year, IEEE EPS will sponsor flagship events in Europe and Asia, including the ESTC Conference to be held in Helsinki, Finland in September, and the EPTC Conference to be held in Singapore in December. Additional major technically sponsored international events coming later in 2026 include ICEPT (China, August), IEMT (Malaysia, October), IMPACT (Taiwan, October), ICSJ (Japan, November), and IDSPS (India, December).

The success of ECTC would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year's exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community. I would also like to thank our authors, presenters, and sponsors for their contributions to ECTC 2026. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members.

In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website or at the EPS booth at ECTC. Finally, I would like to thank you for attending ECTC 2026. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Jeff Suhling, EPS President 2026 – 2027

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Conference organizers reserve the right to cancel or change this program without prior notice.

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all courses, sessions, seminars, meals, exhibits, Interactive Presentation areas, and all conference-sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff member may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables, particularly electronics, cash, and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities, including, but not limited to, functions, events, sessions, seminars, meals, exhibits, and IP areas, and all conference social functions. Thank you for your consideration and cooperation.

REGISTRATION AND MISCELLANEOUS INFORMATION

REGISTRATION LOCATION AND HOURS

ECTC registration will be open at the ECTC Registration Desk located in the JW Marriott Grande Lakes, lobby level, at the Grande Registration Desk.

Monday, May 25, 2026: 3:00 p.m. – 6:00 p.m.
Tuesday, May 26, 2026: 6:45 a.m. – 6:45 p.m.
Wednesday, May 27, 2026: 6:45 a.m. – 4:00 p.m.
Thursday, May 28, 2026: 7:00 a.m. – 4:00 p.m.
Friday, May 29, 2026: 7:00 a.m. – Noon

REGISTRATION FEES

Door Registration includes the digital Proceedings. A link for downloading the Proceedings will be emailed to you!

IEEE Member JOINT Registration (full ECTC + ITherm conference)	$1,750
IEEE Member Full Registration	$1,330
IEEE Member Speaker / Session Chair	$1,190
IEEE Member One Day	$875
IEEE Member Speaker One Day	$770
Non-Member JOINT Registration (full ECTC + ITherm conference)	$2,095
Non-Member Full Registration	$1,605
Non-Member Speaker / Session Chair	$1,190
Non-Member One Day	$875
Non-Member Speaker One Day	$770
Student	$480
Student Speaker	$480

TUESDAY PROFESSIONAL DEVELOPMENT COURSES

IEEE Members

Tuesday AM or PM Course with luncheon	$440
Tuesday All-Day Courses with luncheon	$625

Non-Members

Tuesday AM or PM Course with luncheon	$490
Tuesday All-Day Courses with luncheon	$675
Tuesday Student All-Day Courses with luncheon	$150
Extra Luncheon Tickets for Each Day	$105

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctors Briefing
Room Location: Palazzo C, JW Marriott

SESSION CHAIRS AND SPEAKERS BREAKFAST

Session chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, speakers and session chairs will get to meet each other and instructions for the day will be provided by the Program Chair.

7:00 a.m. Wednesday – Friday
Room Location: Valencia Tent, Lower Level, Outside, JW Marriott

SPEAKER PREP ROOM

Speakers should prepare and review their digital presentations within the allotted times below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday
Room Location: Brava, Lower Level, JW Marriott

GENERAL INFORMATION

Attendee Wi-Fi

Network SSID: ECTC 2026
Password: 2026OrlandoFL

Hotel Concierge

The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room

Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, eperfecto@gmail.com or +1-845-475-1290.

LUNCHEONS

Main Stage Room: Coquina Ballroom, JW Marriott

ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Your conference badge will be scanned for entry into lunch. Please come and enjoy time with other attendees and colleagues in the industry!

Lunch times will vary, see below for specific details for each day.

Tuesday: 12:00 Noon – 1:15 p.m.

Wednesday: 12:45 p.m. – 2:00 p.m.

Thursday: 12:45 p.m. – 2:00 p.m. – Sponsored by: The IEEE Electronics Packaging Society

Friday: 12:45 p.m. – 2:00 p.m. – Don't miss out on this lunch! We will be raffling off several prizes including a hotel stay, free conference registrations, and many other industry gadgets!

ECTC Student Reception

Tuesday, May 26, 2026 • 5:00 p.m. – 6:00 p.m.
Mediterranean Ballroom Porte Cochere, Outside, JW Marriott

Texas Instruments

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

General Chair's Speakers Reception

Tuesday, May 26, 2026 • 6:00 p.m. – 7:00 p.m.
Valencia Tent, Lower Level, Outside, JW Marriott
Invited session chairs and speakers are requested to attend the reception.

Exhibition Reception

Wednesday, May 27, 2026 • 5:30 p.m. – 6:30 p.m.
Mediterranean Ballroom, JW Marriott
All attendees and guests are invited.

76th ECTC Gala Reception

Thursday, May 28, 2026 • 7:30 p.m.
Main Stage: Coquina Ballroom, JW Marriott

Koh Young Technology

EPS Worldwide Chapter Officer Meet and Greet

Thursday, May 28, 2026 • 2:00 p.m. – 3:00 p.m.
Cordova 2, Lower Level, JW Marriott

ECTC Mobile App

ECTC is pleased to announce the use of the same free mobile app as last year. It is called eConference.io by X-CD Technologies. The app provides information on schedules for our technical program including the Professional Development Courses as well as exhibitors, sponsors, and venue maps. The app also features tools to create your personal itinerary by setting your schedule, so you never miss a presentation, special session, or social interaction function. Importantly, it enables you to participate in selecting the best paper awards by voting. The app is available for iOS and Android devices from their respective app stores by searching "eConference.io" in stores or scanning the QR code included here. Once downloaded, enter the code **ECTC2026** (not case-sensitive). Log into the app **using the email you registered with** and start browsing the content.

IEEE Transactions on Components, Packaging, and Manufacturing Technology

IEEE Electronics Packaging Society

If you are an author of a 76th ECTC paper, consider submitting an enhanced and extended version of your work to the *IEEE Transactions on Components, Packaging, and Manufacturing Technology* for journal publication after the conference. A journal manuscript needs to go beyond the conference paper by incorporating new results, deeper analysis, additional discussions, and expanded references that were not included in the original submission. The journal paper must cite the conference paper. For more details on submitting a Transactions paper, see **https://eps.ieee.org/publications/.**

76th ECTC SPECIAL SESSION OVERVIEW

2026 Special Session on Quantum Infrastructure for AI Applications

Quantum Infrastructure for AI Applications: Packaging Challenges and Roadmap

Tuesday, May 26, 2026, 8:30 a.m. – 10:00 a.m. • Palazzo D, JW Marriott

Chairs: Rabindra N. Das, MIT Lincoln Laboratory; Pavel Roy Paladhi, NVIDIA


Quantum computers can provide a platform to solve hard problems which are computationally intractable with traditional computer architecture. Packaging is a key bottleneck to scale quantum processors into AI-relevant accelerators. Major technical obstacles include cryogenics and thermal management, high-density low-loss interconnects, cryo-compatible control electronics, EMI/stray coupling, reliability and manufacturability. AI workloads demand high throughput, low latency, predictable QoS, and tight integration with classical accelerators and data pipelines — packaging must enable fast data movement and tight hybrid quantum-classical feedback. This special session will bring together industry and academy leaders working on quantum packaging hardware developments over the past two decades. The focus will be on future packaging challenges and the roadmap for quantum applications. Packaging areas that need to be researched and tailored to prepare for large scale quantum computation implementation of higher fidelity systems will be identified. Aspects of various quantum technologies and corresponding hardware development will be explored. Our panelists have over 80 years combined experience in quantum technology ranging from hardware built, quantum technology scope, and applications to performance, analysis etc. They are highly experienced with development of prototypes and mapping applications to existing technology. Panelists will present and discuss some of the key challenges and directions that the research should be focused on. It is anticipated that this topic will become very significant to the computer packaging industry as well as the quantum computing world and this panel gives an opportunity for the ECTC community to be informed, be engaged and ready to contribute.

Mark Gouker, MIT Lincoln Lab; Muir Kumph, IBM; Bart Machielse, IonQ; Brian Maertz, Google Quantum; Michael J. Manfra, Microsoft Quantum; Luu Nguyen, PsiQuantum

2026 Special Session on New Packaging Technologies and Panel-Level Integration

New Packaging Technologies Enabled by Panel Level Integration

Tuesday, May 26, 2026, 10:30 a.m. – 12:00 Noon • Palazzo D, JW Marriott

Chairs: Venkata Mokkapati, AT&S; Markus Leitgeb, AT&S; Rozalia Beica, Rapidus



Innovation in semiconductors is reaching another milestone where advanced IC substrates when crossing paths with panel level packaging (PLP) are opening new capabilities. With increasing technical, architectural/functional and market demands, new functionalities (power delivery, signal integrity, warpage control) are integrated into IC substrates through panel level solutions addressing evolving high-end applications like Si photonics, edge AI inference, automotive and HPC. Potential technologies that address these challenges, due to convergence, are embedded components, glass core and ultra-high density (UHD) layers on the substrate. This is essential for such applications where heterogeneous integration is scaled to the panel level resulting in denser, faster, smart and high-performing packages. Join the team of experts from IDM/OEM, foundry and OSATs where they discuss what is needed to converge IC substrates, PLP, and heterogeneous integration to build next generation intelligent systems.

Muhannad Bakir, Georgia Tech; Omar Bchir, Qualcomm; Habib Hichri, Ajinomoto; Shin-Puu Jeny, AMAT; Kuldip Johal, MKS Atotech; Gabriela Periera, Yole Group; Farhang Yazdani, Broadpak

2026 Special Session on AI-Enabled EDA

AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging

Tuesday, May 26, 2026, 1:30 p.m. – 3:00 p.m. • Palazzo D, JW Marriott

Chairs: Ian O'Connor, Ecole Centrale de Lyon, France; Jose Schutt-Aine, University of Illinois at Urbana-Champaign


The integration of multi-physics domains (mechanical, thermal, signal integrity, and electromagnetics) creates unprecedented challenges in electronic package design, requiring holistic and agile approaches beyond traditional methods. While AI has taken major strides in digital design, challenges in analog multi-physics packaging co-design are limiting progress.

This panel, organized jointly by IEEE CEDA and IEEE EPS, explores the transformative role and challenges of AI and machine learning in EDA including AI-driven optimization and agentic AI systems. Panelists will discuss how AI-assisted optimization and design space exploration merge with physical modeling to tackle challenges in memory wall, disaggregation to chiplets, advanced package architectures, sharing insights from industry leaders to define next-generation requirements. The discussion will emphasize practical applications of AI for design space exploration (DSE-AI), co-simulation, and cross-domain optimization, as well as emerging paradigms for training, inference, and workflow automation in EDA. Additionally, the role and impact of Application Design Kits (ADKs) in enabling collaborative, scalable multi-physics AI co-design will be examined.

David Atienza, EPFL; Christopher Bailey, Arizona State University; Henry Sheng, Synopsys; Hanzhi Ma, Zhejiang University; Nandish Mehta, NVIDIA Research; Madhavan Swaminathan, Pennsylvania State University; Jan Vardaman, TechSearch Intl.

2026 Special Session on Photonic-Based Systems

Photonic-Based Systems for AI and Exascale Computing

Tuesday, May 26, 2026, 3:30 p.m. – 5:00 p.m. • Palazzo D, JW Marriott

Chairs: Stéphane Bernabé, CEA-LETI; Lars Brusberg, Corning Inc.


Having emerged just a couple of years ago, co-packaged optics (CPO) has changed the paradigm of optical interconnects, driven by the artificial intelligence boom, and is on the way to realizing the electronics/photonics convergence promised by silicon photonics. As demonstrations based on the CPO approach multiply, the next stage is taking shape: photonic chiplet based architectures, photonic interposers, etc., opening the door to optical networks on chip, photonic switching or programmable photonics. The panel will present recent developments in CPO applied to AI, as well as challenges for these future applications: laser integration issues, development of silicon photonics, 3D co-integration methods as well as process implementation in foundries and OSATs.

Darius Bunandar, Lightmatter; Severine Cheramy, SCINTIL Photonics; Shang Y. Hou, TSMC; Farnood Rezaie, Cisco Systems; Rebecca Schaevitz, Mixx Technologies

2026 Special Session on System Integration Challenges

System Integration Challenges of Large-Size and High-Power Components for High-Performance Computing and AI Applications

Tuesday, May 26, 2026, 8:30 a.m – 10:00 a.m • Palazzo E, JW Marriott

Chairs: Tae-Kyu Lee, Cisco Systems, Inc.; Mike Gallagher, Qnity Electronics


Rapid advances in heterogeneous integration technologies are enabling the design and development of components with significantly larger form factors and substantially higher power densities than were feasible just a few years ago. As package sizes exceeding 100 mm x 100 mm and power levels approaching or surpassing 1,000 W become increasingly common in high-performance computing (HPC) and AI network systems, new challenges are emerging in system-level design and integration. These challenges span system manufacturing, component and PCB reliability, testing, and thermal management, all of which are experiencing heightened complexity and risk. At the same time, opportunities exist in component architecture, materials selection, and manufacturing processes to mitigate these challenges and accelerate the development of next-generation, highly integrated systems. This special session will present and discuss key system integration challenges associated with large-size, high-power components for HPC and AI applications.

Mudasir Ahmad, Cisco; Hemanth Dhavaleswarapu, AMD; Choong-Un Kim, University of Texas at Arlington; Richard Rao, Marvell; Dongji Xie, NVIDIA

2026 Special Session on Co-Design in High-Performance Packaging

Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging

Tuesday, May 26, 2026, 10:30 a.m. – 12:00 Noon • Palazzo E, JW Marriott

Chairs: Ning Ye, Sandisk; Tiwei Wei, University of California, Los Angeles


As packaging complexity increases to support AI, HPC, and heterogeneous integration systems, the interactions among thermal, mechanical, and electrical domains are becoming more tightly coupled—and more difficult to manage independently. Traditional design approaches that treat these domains in isolation are no longer sufficient for achieving system-level performance, reliability, and manufacturability required in advanced packaging.

This special session will focus on the growing need for co-design methodologies that bridge these domains. The session will feature panelists from key players across the supply chain, including EDA, OSATs, foundries, substrate suppliers, and system companies, who will share perspectives on real-world challenges, trade-offs, and co-optimization strategies.

Gang Duan, Samsung Electro-Mechanics; Bill En, AMD; C. P. Hung, ASE; Kelly Morgan, Synopsys; Kathy Yan, TSMC; Yu-Tao Yang, Mediatek

2026 Special Session on Wafer to Panel

Enabling Next-Generation Advanced Packaging Technology From Wafer to Panel

Tuesday, May 26, 2026, 1:30 p.m. – 3:00 p.m. • Palazzo E, JW Marriott

Chairs: Kuldip Johal, MKS Instruments; Beth Keser, Volantis Semiconductor; Lihong Cao, ASE



The fast growth of AI and HPC is driving demand for better performance, higher bandwidth, and improved power efficiency. The advanced chiplet integration combining CPU, GPU, ASIC, HBM, and co-packaged optics is becoming a key enabler. These designs require larger interposers and substrates, pushing the limits of traditional wafer-level packaging due to issues of large warpage, low yield, and limited wafer utilization. Panel-Level Packaging (PLP) is emerging as a promising solution, enabling larger format production with better scalability, yield, and cost efficiency. It also supports new technologies like embedded components, organic interposers, and glass core substrates that are the key for future systems in AI, HPC, automotive, and mobile devices. In this panel, experts from IDMs, fabless companies, foundries, OSATs, material and equipment suppliers will discuss how to bring panel-level integration into high-volume production.

Hidenori Abe, Resonac; Yin Chang, ASE; Gang Duan, Samsung Electro-Mechanics; Deepak Kulkarni, AMD; Lee Chee Ping, LAM Research

2026 Special Session on Innovative Materials for Advanced Packaging

Innovative Materials for Advanced Packaging – Materials for Packaging, Integration, and Performance

Tuesday, May 26, 2026, 3:30 p.m. – 5:00 p.m. • Palazzo E, JW Marriott

Chairs: Zia Karim, Yield Engineering Systems; Ksenija Varga, EV Group


This special session covers a wide range of topics from polyimide/EMC to build-up materials, hybrid-bonding dielectrics, exotic materials, adhesion and stress buffer layers, and interconnect materials (electroless, UBM, solder). The discussion will be to define "the necessity" and the "must" factor to introduce new innovative materials to improve performance, to address current node shortcomings, or to reduce cost. This special session will review new materials for different areas of advanced packaging from substrates, to RDL, to interposers, to chiplets, and the integration thereof.

Hidenori Abe, Resonac; Seiichiro Ohashi, Ajinomoto; Rama Puligadda, Brewer Science; Zsolt Tokei, IMEC; Kathy Yan, TSMC

2026 IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 26, 2026, 8:00 a.m. – 5:00 p.m. • Palazzo F-H, JW Marriott

Chairs: Ravi Mahajan, Intel Corporation; William Chen, ASE (in memoriam); Subu Iyer, UCLA; Anne Meixner, HIR Fellow; Benson Chan, Binghamton University; Rockwell Hsu, Cisco Systems; Jose Schutt-Aine, UIUC




8:00 a.m. – 8:30 a.m.: HIR Welcome, Introduction & Agenda Review

8:30 a.m. – 10:00 a.m.: Additive Electronics Manufacturing (AME) for Advanced Packaging

10:30 am – 12:00 Noon: Metrology for Advanced Packaging: Challenges, Innovations, and Industry Impact

1:15 p.m. – 3:15 p.m.: Emerging Technologies

3:30 p.m. – 5:00 p.m.: Neuromorphic Computing

2026 ECTC Young Professional Networking Event

Tuesday, May 26, 2026, 6:45 p.m. – 7:45 p.m. • Palazzo D, JW Marriott

Chair: Aakrati Jain, IBM

Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2026 IEEE EPS Seminar on Organic Substrates in the Chiplet Era

Redefining System Integration: The Rise of Organic Substrates in the Chiplet Era

Tuesday, May 26, 2026, 7:45 p.m. – 9:15 p.m.
Main Stage Room, Coquina Ballroom, JW Marriott

Chairs: Takashi Hisada, Rapidus; Yasumitsu Orii, Rapidus


As chiplet-based architectures rapidly become the mainstream design paradigm, the role of the package substrate has evolved from a passive interconnect carrier to a decisive enabler of system performance, power efficiency, and heterogeneous integration. Even with new approaches such as NVIDIA's recently proposed CoWoP (Chip on Wafer on PCB), organic substrates remain at the heart of advanced packaging, serving as the essential platform that connects chiplets with wafers, large panels, and ultimately the system board.

This special session brings together leaders from across the ecosystem — industry trend experts, EDA solution providers, and leading substrate manufacturers — to discuss the challenges and innovations driving the next generation of organic substrates. Topics will cover market and technology trends shaping chiplet-based systems, co-design methodologies bridging package and system-level optimization, and manufacturing breakthroughs needed to deliver ultra-fine line and large-panel organic substrates at scale.

By uniting perspectives from system architects, design tool innovators, and substrate manufacturers, this session underscores that organic substrates are no longer just passive carriers, but the critical foundation enabling chiplet integration and next-generation high-performance systems in the post-Moore era.

Yasushi Araki, Shinko; Y. H. Chen, Unimicron; C. P. Hung, ASE; Tarek Ibrahim, Intel; Kenneth Larsen, Synopsys

2026 ECTC Keynote Talk

Advanced Packaging and the Future of System Optimization

Wednesday, May 27, 2026, 8:00 a.m. – 9:15 a.m.
Main Stage Room, Coquina Ballroom, JW Marriott

Chair: Michael Mayer, University of Waterloo, Canada
Speaker: Tien Wu, CEO of Advanced Semiconductor Engineering, Inc.


Global AI infusion is redefining performance, power, and integration requirements, placing advanced packaging at the forefront of semiconductor innovation. As chip architecture complexity increases, the industry is progressing beyond device-level scaling toward system-level optimization. Advances in heterogeneous integration and packaging-enabled co-design are shaping more efficient, scalable, and resilient systems. Moving forward, system-centric strategies that align architecture, packaging, and collaboration across the ecosystem are paramount to shaping the golden era of AI and semiconductors.

2026 ECTC Student Competition

Wednesday, May 27, 2026, 6:45 p.m. - 8:00 p.m. • Palazzo D, JW Marriott

Chairs: Przemyslaw Gromala, Robert Bosch Kft; Ibrahim Guven, Virginia Commonwealth University


Finalists for the ECTC 2026 Student Innovation Challenges Competition in BSc/MSc and PhD level categories will make their presentations during this session. This competition allows participants to demonstrate their skills, apply their academic knowledge, and collaborate on innovative ideas in the field of electronic/photonic packaging. The winners in each category will be announced during the Friday luncheon.

2026 Plenary Session on Data Centers Needs

Efficiency Is Not Enough: Are We Solving the Wrong Problem in Data Center Energy Use?

Thursday, May 28, 2026, 8:00 a.m. – 9:15 a.m.
Main Stage Room, Coquina Ballroom, JW Marriott

Chairs: Masha Gorchichko, Marvell Technology, Inc.; Jan Vardaman, TechSearch International, Inc.


This session will explore the key challenges and opportunities in improving energy use in data center applications, spanning hardware, system architecture, software, and infrastructure to showcase the complexity of the issue and highlight the necessity to adopt a holistic framework for the energy use conversation. We will discuss the role of cutting-edge packaging technologies influencing the energy consumption of high-performance applications.

Ankur Agarwal, Celestial AI; Rich Bonner, Accelsius; John Knickerbocker, IBM; David Lo, Google; Raja Swaminathan, AMD; Dennis Trieu, Microsoft

2026 ECTC Start-Up Challenges

The Light Age: Strategic Investment in Photonics to Power the Next Computing Era

Thursday, May 28, 2026, 6:00 p.m. - 7:30 p.m. • Palazzo A-C, JW Marriott

Chairs: Rozalia Beica, Rapidus; Farhang Yazdani, Broadpak


Start-up companies will pitch their innovative ideas to a panel, followed by audience Q&A, jury deliberation, and then awards and a networking event.

Jurors: John Wei, Applied Ventures; Kevin Fahey, Market Operandi; Henry Huang, Micron Ventures; Isabel Klein, M-Ventures; Martijn Pierik, Southwest Strategies Group, Yik Yee Tan, Yole Group; Tobias Egle, Fine Structure Capital

2026 IEEE EPS President's Panel

Data Centers in the Age of AI: Challenges and Solutions

Friday, May 29, 2026, 8:00 a.m. – 9:15 a.m.
Main Stage Room, Coquina Ballroom, JW Marriott

Chairs: Benson Chan, Binghamton University; David McCann, Amkor Technology; Jeff Suhling, Auburn University

Moderator: Kanad Ghose, Binghamton University



Foundational/large language models for AI applications continue to drive the energy and natural resource demands for data centers. Projected energy demands of AI data centers are about to exceed the available energy sources. Hard-pressed utilities providing electricity to data centers have, in many cases, passed the cost of additional generation and distribution on to customers. The cooling needs for the AI data centers are also taxing the water sources. This is a crisis in the making and has to be addressed in a proactive manner to enable the society-at-large to capitalize on the benefits of AI without overtaxing natural resources and without financial burdens on the public. This panel features presentations and discussion by area experts on the technology, economic and environmental challenges posed by AI data centers and potential solutions in the systems, microelectronics, and advanced packaging realm to address these challenges.

Arvind Kumar, IBM; Nandish Mehta, NVIDIA; Farnood Rezaie, Cisco; Bahgat Sammakia, Binghamton University

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For more information on 2027 sponsorship opportunities, please contact Alan Huffman at alan.huffman@ieee.org

ECTC 2025 BEST PAPER AWARDS

BEST SESSION PAPER

Direct-to-Silicon Liquid Cooling Integrated on CoWoS® Platform

Yu-Jen Lien, Sing-Da Jiang, Cheng-Chieh Hsieh, Han-Jong Chia, Tsunyen Wu, Chien-Chih Lin,Ke-Han Shen, Szu-Wei Lu, Kathy Yan, Kuo-Chung Yee, Douglas C.H. Yu, Taiwan Semiconductor Manufacturing Company Ltd.

BEST INTERACTIVE PRESENTATION PAPER

An Effective 3D Thermal Network Integrated With Deep Learning for Improved Prediction of the 3D Thermal Properties of Complex Packaging Patterns

Jeong-Hyeon Park, Sungkyunkwan University, Jaechoon Kim, Sukwon Jang, Sungho Mun, Eun-Ho Lee, Samsung Electronics Co. Ltd

OUTSTANDING SESSION PAPER

Development of Glass Core Build-up Substrate With TGV

Masahiro Sunohara, Jun Yoshiike, Hiroshi Taneda, Yoko Nakabayashi, Noriyoshi Shimizu, Shinko Electric Industries Co., Ltd

OUTSTANDING INTERACTIVE PRESENTATION PAPER

Novel Packaging Platform Based on Bridge Dies With Top and Bottom I/O Connections on Standard Substrates

Jae-Sung Lim, Sangkyu Jang, Yong Gyu Jang, Yongnam Koh, Jin-Wook Jang, Jayden Donghyun Kim, HANA Micron Inc.

INTEL BEST STUDENT PAPER

Physics-Informed Neural Networks for SAM Image Enhancement With a Novel Physics-Constrained Metric for Advanced Semiconductor Packaging Inspection

Shajib Ghosh, Nitin Varshney, Antika Roy, Patrick Craig, Md Mahfuz Al Hasan, Sanjeev J. Koppal, Navid Asadizanjani; University of Florida, Rayhane Ghane-Motlagh, ficonTEC Service USA Inc.; Nelly Elsayed, University of Cincinnati

INTEL OUTSTANDING STUDENT PAPER AWARD

Packaging and Integration of Multifunctional Brain Computer Interface

Ziqi Jia, Ariel David Cerpa, Gloria J. Kim, Yong-Kyu Yoon, University of Florida

TI BEST IP STUDENT PAPER

Parasitic Extraction and Signal Integrity Analysis of Memristor-Based Crossbar Arrays for Neuromorphic Computing

Tahsin Binte Shameem, Yi Zhou, Zohreh Salehi, José Schutt-Ainé, University of Illinois at Urbana-Champaign; Hanzhi Ma, Zhejiang University

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 26, 2026

All Courses are Located in the JW Marriott

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Cordova 1, Lower Level **1. High Reliability Soldering in Advanced Semiconductor Packaging** *Course Leader(s): Ning-Cheng Lee, ShinePure Hi-Tech*	Cordova 1, Lower Level **9. Polymers for Advanced Packaging** *Course Leader(s): Jeff Gotro, InnoCentrix, LLC*
Cordova 2, Lower Level **2. Photonic Components and Packaging Technologies for Data Center, Communication, Sensing, and Displays** *Course Leader(s): Torsten Wipiejewski, Huawei Technologies Duesseldorf GmbH*	Cordova 2, Lower Level **10. Diamond Heat Spreaders and Heterogeneous Integration** *Course Leader(s): Joana-Catarina Mendes, Instituto de Telecomunicaciones*
Palazzo A, Lobby Level **3. Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Heterogeneous Integration and Advanced Packaging** *Course Leader(s): Viorel Dragoi, EV Group*	Palazzo A, Lobby Level **11. Advanced Packaging for Chiplet, Heterogeneous Integration, and Co-Packaged Optics** *Course Leader(s): John H. Lau, Unimicron Technology Corp.*
Palazzo B, Lobby Level **4. Introduction to Quality and Reliability Engineering of Advanced Microelectronics Packaging** *Course Leader(s): Shubhada Sahasrabudhe, QuRIuS LLC; Shalabh Tandon, QuRIuS LLC*	Palazzo B, Lobby Level **12. Preventing Packaging Failure - Modeling and Mitigation Strategies for Warpage, Fatigue, and Thermal Issues** *Course Leader(s): Xuejun Fan, Lamar University*
Cordova 3, Lower Level **5. 2.5D/3D Package Failure Analysis - Failure Mechanisms and Analytical Tools** *Course Leader(s): Deepak Goyal, Carl Zeiss, Inc.*	Cordova 3, Lower Level **13. Failure Analysis of Engineering Materials for Advanced Electronic Packaging** *Course Leader(s): Kuan Yew Cheong, Universiti Sains Malaysia*
Cordova 4, Lower Level **6. AI-Applications in Semiconductor Packaging** *Course Leader(s): Pradeep Lall, Auburn University*	Cordova 4, Lower Level **14. Flip Chip Technologies** *Course Leader(s): Shengmin Wen, TATA Electronics Private Limited*
Cordova 5, Lower Level **7. Fundamentals of Fabrication Processes and RF Design of Advanced Packages Including Fan-Out, Chiplets, Glass and Polymer Interposers** *Course Leader(s): Ivan Ndip, Brandenburg University of Technology/Fraunhofer IZM; Markus Woehrmann, Fraunhofer IZM*	Cordova 5, Lower Level **15. Advanced Packaging for 5G/6G - RF Focus** *Course Leader(s): Premjeet Chahal, Michigan State University*
Cordova 6, Lower Level **8. Electronics Cooling and Reliability for Data Centers** *Course Leader(s): Patrick McCluskey, University of Maryland, College Park*	Cordova 6, Lower Level **16. Thermal Management in the Age of AI** *Course Leader(s): Jaime Sanchez, Qualcomm*

Refreshment Breaks
10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Cordova and Palazzo Foyers, JW Marriott

COMMITTEE MEETINGS

ASSOCIATED COMMITTEE MEMBERS ONLY

All Rooms are Located in the JW Marriott

Tuesday, May 26, 2026

8:00 a.m. – 5:00 p.m.
EPS HIR Workshop
Palazzo F-H

9:00 p.m. – 10:30 p.m.
ECTC Photonics Committee
Marbella 1

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Marbella 2

Wednesday, May 27, 2026

7:00 a.m. – 8:00 a.m.
EPS Power TC
Cordova 1

7:00 a.m. – 8:00 a.m.
EPS Materials and Processes TC
Cordova 2

7:00 a.m. – 8:00 a.m.
EPS EDMC TC
Cordova 3

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Marbella 1

5:00 p.m. – 6:00 p.m.
EPS Technical Committee Chairs
Cordova 5 & 6

Thursday, May 28, 2026

7:00 a.m. – 8:00 a.m.
EPS Emerging Tech TC Meeting
Cordova 5

7:00 a.m. – 8:00 a.m.
EPS Photonics TC Meeting
Cordova 4

7:00 a.m. – 8:00 a.m.
EPS High Density Boards and Substrates TC Meeting
Cordova 3

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC Meeting
Cordova 2

8:00 a.m. – 10:00 a.m.
EPS Conference Organizers Meeting
Cordova 1

2:00 p.m. – 3:00 p.m.
EPS Chapter Chairs Meet & Greet
Cordova 2

3:00 p.m. – 4:00 p.m.
EPS T-CPMT SAE
Cordova 3

4:30 p.m. – 6:00 p.m.
EPS BoG Information Session
Cordova 5 & 6

5:15 p.m. – 6:00 p.m.
ECTC 2026 Program Committee Meeting
Palazzo D

6:30 p.m. – 7:30 p.m.
ECTC Program Subcommittee Chairs & Assistant Chairs Reception
(by invitation only)

9:30 p.m.
76th ECTC Governing/ Executive Committee Reception
(by invitation only)

Friday, May 29, 2026

7:00 a.m. – 8:00 a.m.
EPS RF & THz Tech. TC
Cordova 3

7:00 a.m. – 8:00 a.m.
EPS 3D/TSV TC
Cordova 2

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Cordova 4

9:00 a.m. – 10:00 a.m.
EPS T-CPMT SAE/AEs
Cordova 5 & 6

2:15 p.m. – 5:15 p.m.
ECTC Executive Committee
Cordova 5 & 6

5:00 p.m. – 6:00 p.m.
ECTC / EPS Steering Committee
Cordova 5 & 6

PROGRAM SESSIONS: WEDNESDAY, MAY 27, 9:30 A.M. - 12:35 P.M.

Session 1: Enabling Fan-In and Fan-Out Wafer/Panel Level Packaging Technology	Session 2: Co-Packaged Optics	Session 3: Advances in Low Temperature Hybrid Bonding
Committee: **Packaging Technologies**	**Committee:** **Photonics**	**Committee:** **Materials & Processing**
Palazzo A-C, JW Marriott	**Palazzo D, JW Marriott**	**Tuscany D, The Ritz-Carlton**
Session Co-Chairs **Young-Gon Kim – Renesas Electronics** **Email: young.kim.jg@renesas.com** **Steffen Kroehnert – ESPAT-Consulting** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs** **Ajey Jacob – University of Southern California** **Email: ajey@isi.edu** **Soon Jang – ficonTEC USA** **Email: soon.jang@ficontec.com**	**Session Co-Chairs** **Yoichi Taira –Keio University** **Email: taira@appi.keio.ac.jp** **Ksenija Varga – EV Group** **Email: k.varga@evgroup.com**
1. 9:30 AM - A Novel 600mm Panel Interposer with 300mm Panel Assembly Approach for Advanced Packaging Solution in HPC and AI Applications Teck Chong Lee, Yung Shun Chang, Ping-Feng Yang, Lihong Cao, Wiwy Wudjud, Powei Lu, Yihsien Wu – Advanced Semiconductor Engineering, Inc.	***1. 9:30 AM - Proposal of a Novel Opto-Electronic Fan-Out Wafer-Level Packaging Based on Optical RDL and Opto-Chiplets*** Siim Heinsalu, Fumi Nakamura, Satoshi Suda, Akihiro Noriki – National Institute of Advanced Industrial Science and Technology	***1. 9:30 AM - Hybrid Bonding With Ultra-low Temperature Annealing: Morphological and Electrical Validations*** Margot Faure, Agathe Lerat, Pablo Renaud, Floriane Baudin, Maria-Luisa Calvo-Munoz, Hadi Hijazi, Frank Fournel, Christophe Dubarry – CEA-LETI
2. 9:50 AM - Multi Stacked FOWLP Utilizing Extreme Aspect Ratio Cu Post for Mobile on-Device AI Memory Solution Eun Young Lee, Sangkyu Lee, Woosang Jung, Yongjin Seol, Yieok Kwon, Myeonghan Bae, Choi Dong-Jun, Jang EunJi, Sohyun Lee, Jeongseok Mun, Sungoh Ahn, Won Kyoung Choi – Samsung Electronics Co., Ltd.	***2. 9:50 AM - High-Density, Energy-Efficient CPO Platform with PIC-in-Mold Interposer Architecture for AI/ML Data Centers*** Sajay Gourikutty, JiaQi Wu, Zhonghua Yang, Mihai Rotaru, Ji Lin, Yong Han, Lai Yee Chia, Sharon Lim, Sandra San, Tai Chong Chai, Surya Bhattacharya – Institute of Microelectronics A*STAR	***2. 9:50 AM - Pressure-less Cu/Polymer Hybrid Bonding at Low Temperature and Fine Pitch Using a Novel Polymer Adhesive with Precisely Controlled Composition*** Ryo Hayakawa, Yuzo Nakamura, Satoshi Otsuka, Hajime Kato, Shigetaka Hori, Yutaka Hisamune, Satoshi Inada – Mitsui Chemicals, Inc.; Chih-Jing Hsu, Yung-Sheng Lin, Ren-Jieh Kao, Chih-Pin Hung, Yun-I Yeh – Advanced Semiconductor Engineering, Inc.
3. 10:10 AM - The Study and Challenges of Ultra-thin Chip Module for Fan-out Embedded Bridge Die Package (FO-EB) Kuei-Hsiao Kuo, Jui Teng Hung, Derrick Dai, Chun Sheng Ho, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.	***3. 10:10 AM - Photonic-Electronic Integration on Glass Substrate with Temperature-Stabilized Vertical Optical Coupling by Resin-Encapsulated Collimation Mirror*** Shingo Nakamura, Yasutaka Mizuno, Kunio Kobayashi, Takeru Naito, Tetsuya Nakanishi, Hiroshi Uemura, Keiji Tanaka, Katsumi Uesaka – Sumitomo Electric Industries, Ltd.; Mio Emura, Mami Miyairi, Yoshikatsu Ishizuki – FICT, Ltd.; Yoichiro Kurita – Institute of Science Tokyo	***3. 10:10 AM - Reliable Low-Temperature (≤ 250oC) Cu/Dielectric Hybrid Bonding for High-Bandwidth Memory (HBM) Stack Integration*** Tran Van Nhat Anh, B.S.S. Chandra Rao, Chaeeun Lee, Fujino Masahisa, Vempati Srinivasa Rao, Navab Singh – Institute of Microelectronics A*STAR; Prayudi Lianto, Nicholas Boon Leong Chua – Applied Materials, Inc.; Rong Ji, Ming Lin – Institute of Materials Research and Engineering A*STAR; Yong Hong Derrick Tan – WinTech Nano-Technology Services Pte. Ltd.
10:30 a.m. – 11:15 a.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 11:15 AM - Progress Towards a Fine-Pitch Multi-Layer Organic Substrate Enabled by Fan-out Technology Georgios Dogiamis, Timothy Takeuchi, Craig Bishop – Deca Technologies, Inc.; Matthew Magnavita, Michael Naujokaitis, Robert Naujokaitis, Gregory Johnson, Stanislau Niauzorau, Leslie Hwang, Binh Duong, Jason Conrad – Arizona State University	***4. 11:15 AM - Thin-Film Lithium Niobate Hybrid Integration for Co-packaged Optics*** Zhixing Lin – University of California; Tam Huynh, Ayed Sayem, K.W. Kim, Cuong Tran, Yang Liu, Manohar Bongarala, Sarwesh Parbat, Rishav Roy, Ting-Chen Hu, Alaric Tate, Mark Cappuzzo, Rose Kopf, Mark Earnshaw – Nokia Bell Labs; Alexander Rylyakov – Nokia Corporation	***4. 11:15 AM - Low-Temperature Chip Scale Cu-Cu Hybrid Bonding by Electroless Ag Passivation*** Cheng-Yan Yang, Ming-Hsuan Hsieh, Po-Shao Shih, Wei Choong Lee, Yu-Hsiang Lu, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.
5. 11:35 AM - A Novel Membrance-Based Adaptive Pressure Curing System for Warpage Suppression in Advanced Packaging HuanPing Su, Minghua Hsu, Chih-Horng Horng – Ableprint Technology Co., Ltd.	***5. 11:35 AM - High-Density Integration of III-V Devices and EICs Using Vertical-Coupled Photonic Packages with a Glass-IP and Redistribution Layers*** Kei Masuyama, Mizuki Shirao, Shinji Araki, Kiyotomo Hasegawa, Shinya Okuda, Seiu Higashide, Nobuo Ohata – Mitsubishi Electric Corporation	***5. 11:35 AM - Enabling Low-Temperature Fine-Pitch Hybrid Bonding: Role of Nanocrystalline Copper Microstructures and Pre-Bond Surface Treatments*** Mathieu Loyer – STMicroelectronics; Mathilde Gottardi, Maria-Luisa Calvo-Munoz – CEA-LETI; Christelle Rey, Emilie Deloffre, Sébastien Petitdidier – ST Microelectronics
6. 11:55 AM - Metal-Enhanced Waffle Wafer Design for Thermomechanical Warpage Reduction in Fan-out Wafer-Level Packaging Bonghak Lee, Sang Won Yoon – Seoul National University	***6. 11:55 AM - A 106-Gb/s × 8-Channel 1060-nm Single-Mode VCSEL-Based Ultra-Compact CPO Transceiver Enabling 2-km Parallel-Optical Links*** Wataru Yoshida, Kazuya Nagashima, Sho Yoneyama, Hideyuki Nasu – Furukawa Electric Co., Ltd.; Yuto Iwane, Kazutaka Takeda – Fujifilm Business Innovation Corp.; Fumio Koyama – Institute of Science Tokyo	***6. 11:55 AM - Polymer Fillet Integration to Improve Die Thinning and Inter-die Gap Fill Yield and Reliability in Die-to-Wafer Hybrid Bonding*** Alyssa Yaeger, Cristina Camagong – IBM Corporation; Roy Yu, Katsuyuki Sakuma – IBM Research
7. 12:15 PM - Additive Fan-Out Packaging for Discrete Components Arjun Wadhwa, Milan Saalmink, Marieke Burghoorn, Iris Kerkhof, Ruben Pranger, Luigi Gjergjaj, Bart van Goor, Jeroen van der Brand – Netherlands Organization for Applied Scientific Research (TNO); Edsger Smits, Francesca Chiappini – Chip Integration Technology Center/TNO	***7. 12:15 PM - Design and Packaging of a DWDM CW-DFB Laser Array for Co-Integrated Optical Interconnects*** Nandish Mehta, Ward Lopes, Benajmin G. Lee, C. Thomas Gray – NVIDIA; Ryosuke Hatai – Lumentum	***7. 12:15 PM - Scalable Low-Temperature Bonding for Packages Targeting Large-Format Interposers: High Throughput and High Reliability*** Sadaaki Katoh, Takeshi Saito, Keiko Ueno – Resonac Corporation; Daisuke Hashimoto, Haruya Suzuki – C.Uyemura & Co., Ltd.; Kiyoshi Oi, Goro Hasui – Shinko Electric Industries Co., Ltd.

PROGRAM SESSIONS: WEDNESDAY, MAY 27, 9:30 A.M. - 12:35 P.M.

Session 4: Breakthrough in Pitch Scaling With Advanced Bonding Technology	Session 5: RF and High-Speed Design for mmWave and Sub-THz	Session 6: Thermo-Mechanical Interactions With Reliability
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Tuscany E, The Ritz-Carlton	**Tuscany F-H, The Ritz-Carlton**	**Tuscany A-C, The Ritz-Carlton**
Session Co-Chairs **Pascale Gagnon – IBM Canada** **Email: pgagnon@ca.ibm.com** **Cong Zhao – Meta Platforms, Inc.** **Email: zhaocong@meta.com**	**Session Co-Chairs** **Harrison Chang – Advanced Semiconductor Engineering, Inc. (US)** **Email: Harrison_Chang@aseglobal.com** **Yong-Kyu Yoon – University of Florida** **Email: ykyoon@ece.ufl.edu**	**Session Co-Chairs** **Kuo-Ning Chiang – National Tsing Hua University** **Email: knchiang@pme.nthu.edu.tw** **Ning Ye – Sandisk** **Email: ning.ye@sandisk.com**
1. 9:30 AM - 100-nm-Level Post-Bond Accuracy and High-Yield Die-to-Wafer Hybrid Bonding System Using Non-Contact Die Transfer Kentaro Mihara, Takashi Hare, Hirofumi Sakai, Shimpei Aoki – Toray Engineering Co., Ltd.; Fumihiro Inoue – Yokohama National University; Akira Uedono – University of Tsukuba; Murugesan Mariappan, Hashimoto Hiroyuki, Takafumi Fukushima – Tohoku University	***1. 9:30 AM - Developments of Polymer Microwave Fiber Coupler in eWLB Package for Ultra-High-Speed Communication at D- and Y-Band*** Maciej Wojnowski, Ozan Yurduseven, Simon Kornprobst, Franz Xaver Engelsberger, Walter Hartner – Infineon Technologies AG; Parisa Aghdam, Sining An – Ericsson AB; Frida Strömbeck, Herbert Zirath – Chalmers University of Technology	***1. 9:30 AM - Predicting Long-Term Thermal Aging Behavior of Porous Sintered Layers via Hybrid Potts-Phase Field Model with Thermo-Mechanical Coupling*** Xiao Hu, Zichuan Li, Willem van Driel, Guoqi Zhang – Delft University of Technology; Chao Gu, Junwei Chen, Jiajie Fan – Fudan University; Jianlin Huang – Ampleon B.V.; Rene Poelma – Nexperia
2. 9:50 AM - A Study of Chiplet Distortion in Chip-to-Wafer (C2W) Hybrid Bonding Yi Shi, Charles El Helou, Mohammadreza Yaghoobi, Sheena Benson, Siyan Dong, Khant Minn, Tushar Talukdar, Haris Khan Niazi, Chytra Pawashe, Lance Hibbeler, Brandon Rawlings, Aleksandar Aleksov – Intel Corporation	***2. 9:50 AM - A Micro-3D Printed Helix for sub-THz Antenna-on-Chip Modules*** Genaro Soto Valle Angulo, Nikolas Roeske, Theodore Callis, Marvin Joshi, Manos M. Tentzeris – Georgia Institute of Technology	***2. 9:50 AM - Influence of Design and Liner Material on Reliability of Through Glass Vias Under Thermal Cycling: Numerical Modeling and Experimental Validation*** Dalei Yang, Junbo Yang, Karthik Arun Deo, Kewei Shou, Yuhan Gao, Yi Deng, Weichen Zhao, Yangyang Lai, Pengcheng Yin, Seungbae Park – Binghamton University
3. 10:10 AM - INTERCEPT - A Nondestructive Known Good Die Testing Probe and Reworkable Substrate Enabled by Liquid Metal Patterning Samuel Wang, Hsuan En Lee, Alexis Samoylov, Vineeth Harish, Subramanian Iyer – University of California, Los Angeles; Hsiao-Chen Lin, Mansi Sunil Sheth, Jui-Han Liu – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)	***3. 10:10 AM - Differentially fed Sub-THz Broadband Antenna Arrays Using Quartz Glass Cavity-Backed Bonding Technology*** Alexander Gäbler, Uwe Maaß, Wojciech Partyka – Fraunhofer IZM; Shoichiro Yamaguchi, Jungo Kondo, Kentaro Tani, Naotake Okada, Masato Tokai – NGK INSULATORS, LTD.; Makoto Iwai – NGK Europe GmbH; Ivan Ndip – Brandenburg University of Technology/Fraunhofer IZM	***3. 10:10 AM - Fracture Analysis for CoWoS Reliability Improvement*** Ming-Chih (Jason) Yew, Chia-Kuei Hsu, Chien-Yu Wang, Chieh-Ming Chang, Po-Chen Lai, Kuo-Chin Chang, Jia-Ming Yang, Chang-Fu Han, Jyun-Lin Wu, C.S. Chen, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.
10:30 a.m. – 11:15 a.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 11:15 AM - Assembly Process Optimization to Reduce Particle-Induced and non-Particle-Induced Voids in Chip-to-Wafer Hybrid Bonding Ling Xie, Ser Choong Chong, Hipona Randy Tupaen, Ignatius Lim, Vasarla Sekhar, Mishra Kumar, Chandra Bhesetti, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR; Fredimar Soliven, Evangelista Roy Anselmo, Chong Wei Lun, Nithyananda Hegde, Pavel Seroglazov, Hannes Kostner, Jonathan Abdilla, Chris Scanlan – BE Semiconductor Industries N.V.; Ramalingam Ranya, Ying Wang, Raymond Hung – Applied Materials, Inc.	***4. 11:15 AM - Advanced Scalable Modeling of High-Q Passives on a 300 mm RF Interposer Platform for mmWave and sub-THz Applications*** Côme Wallner, Xiao Sun – imec; Dimitri Lederer – UCLouvain	***4. 11:15 AM - Thermal Stress Reliability Optimization of TGV Density, Size, and Material Engineering for Glass Based Advanced Substrate Technology*** Jaesung Kim, Yujeong Kim, Eunbi Ko, Jun Soo Chang, Soon Gil Lee, Jaesung Oh, Chang Bo Jung, Ken Lee, Mun Sang You, Geonhee Lee – SIMMTECH; Hyunwoo Nam, Tae-Ik Lee – KITECH
5. 11:35 AM - Fluxless Vacuum Formic Acid Reflow of Indium Solder Thermal Interface Materials in Large Area BGA Packages Kyle Aserian, Ryan Mayberry, Andy Mackie – Indium Corporation; Phil Lehrer, David Heller, Xike Zhao, Fred Tarazi – Heller Industries	***5. 11:35 AM - Signal and Power Integrity Co-Analysis of Chiplet(UCIe)-Based GPU-HBM Interconnect for Reduced PHY Area*** Haeseok Suh, Jiwon Yoon, Youngsu Yoon, Junho Park, Hyunjun An, Junghyun Lee, Byeongmok Kim, Eunji Seo, Keunwoo Kim, Jaegeun Bae, Joungho Kim – Korea Advanced Institute of Science and Technology	***5. 11:35 AM - Thermal Storage Reliability Evaluation of Non-PFAS Potting Materials Used in Electronic Assemblies*** Yasitha Piyumal, Pradeep Lall – Auburn University; Ken Blecker – US Army CCDC-AC
6. 11:55 AM - Laser Assisted Bonding of InP Power Amplifier Chiplets on a 300 mm RF Si Interposer Damien Leech, Siddhartha Sinha, Hamideh Jafarpoorchekab, Nelson Pinho, Angel Uruena, Natalie Roels, Lili Wang, Nazia Fathima, Ehsan Shafahian, Punith Kumar Mudiger Krishne Gowda, Francois Chancerel, John Slabbekoorn, Akito Hiro, Luc van der Krabben, Alain Phommahaxay, Koen Kennes, Andy Miller, Eric Beyne, Nadine Collaert, Xiao Sun – imec	***6. 11:55 AM - Thermally Reconfigurable Split-Substrate Integrated Waveguide for Baseband and Broadband Signal Transmission*** Abdelrahman Omar, Md. Omar Faruk Noman – The University of North Carolina at Charlotte; Soumitra Joy – University of North Carolina	***6. 11:55 AM - Enhancing Warpage Predictability by Considering Thermal Aging Shrinkage of EMC in Heterogeneous Integration Wafer Level Packaging*** Ji Lin – Institute of Microelectronics A*STAR; Alfred Yeo, Wang Yifan, Chan Kai Chong – StatsChipPAC PTE. LTD
7. 12:15 PM - Pillar-Suspended Bridge (PSB); Fabrication Process Verification and Interconnect Design for 25-Micron Pitch Die-to-Die Interface Shinichi Arioka, Tanapun Srichanthamit, Koji Iwabu, Takashi Suzuki, Yoshiaki Aizawa – AOI Electronics Co., Ltd.; Yoichiro Kurita – Institute of Science Tokyo	***7. 12:15 PM - Fully Integrated mmWave MIMO Radar with Compact Antenna-on-Package Design*** Aditya Jogalekar, Mohammad Vatankhah Varnoosfaderani, Marc Dewilde, Zachary Crawford, Cathy Chi, Sunhwan Jang, Venkatesh Srinivasan – Texas Instruments, Inc.	***7. 12:15 PM - High Temperature Shock Testing on QFN, Flip-Chip and Chip Resistor Components*** Max Frank Haeusler, Karsten Meier, Karlheinz Bock – TU Dresden

PROGRAM SESSIONS: WEDNESDAY, MAY 27, 2:00 P.M. - 5:05 P.M.

Session 7: Heterogeneous Integration: The New Horizons	Session 8: Die-to-Wafer Hybrid Bonding: Current Advancements and Future Directions	Session 9: Advances in Thermal Materials and Encapsulation
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Palazzo A-C, JW Marriott	**Palazzo D, JW Marriott**	**Tuscany D, The Ritz-Carlton**
Session Co-Chairs **Luu Nguyen – PsiQuantum** **Email: lnguyen@psiquantum.com** **Subhash Shinde – Booz Allen Hamilton** **Email: sshinde@nd.edu**	**Session Co-Chairs** **Katsuyuki Sakuma – IBM Research** **Email: ksakuma@us.ibm.com** **Ilseok Son – TEL Technology Center, America, LLC** **Email: Ilseok.Son@us.tel.com**	**Session Co-Chairs** **Dwayne Shirley – Marvell Semiconductor, Inc.** **Email: shirley@ieee.org** **Ivan Shubin – Raytheon Technologies** **Email: ishubin@gmail.com**
1. 2:00 PM - Direct Bridge Multi-die (DBrM) Package: A Novel Silicon Bridge Chiplet Packaging Technology Using Die-Edge Gluing Technique for Chip Reconstitution Akihiro Horibe, Chinami Marushima, Takahito Watanabe, Atom Watanabe, Yasuharu Yamada, Sayuri Kohara, Risa Miyazawa, Hiroyuki Mori – IBM Research; Divya Taneja, Isabel De Sousa – IBM Canada, Ltd.	***1. 2:00 PM - Ultra-fine 1.4-µm Pitch Face-to-Back Chip-on-Wafer Cu–Cu Hybrid Bonding for the Chip-on-Wafer-on-Wafer Integration*** Itsuki Imanishi, Akihiro Urata, Masanori Chiyozono, Toru Osako, Kan Shimizu, Yoshihisa Kagawa – Sony Semiconductor Solutions	***1. 2:00 PM - Enhancement of Thermal Conductivity of the Advanced Packaging Materials by Using BNNT*** Changho Kim, Junha Hwang, Min Seok Kwak, Ji In Lee, Cheolwoo Kwak, Jaewoo Kim – Naieel Technology; Hikaru Uchida, Yuka Yamashita, Hiroki Ito – Denka Innovation Center
2. 2:20 PM - Scaling the EMIB-T Advanced Packaging Technology to Address the Future HPC/AI Demand Tarek Ibrahim, Zhiguo Qian, Jianyong Xie, Yidnekachew Mekonnen, Jung Kyu Han, Ali Lehaf, Tchefor Ndukum, Siddarth Kumar, Jason Gamba, Kaladhar Radhakrishnan, Kemal Aygun, Rahul Manepalli – Intel Corporation	***2. 2:20 PM - Process Optimization for Chip to Wafer Hybrid Bonding Using Inter Die Gap Fill Integration Approach*** Mishra Kumar, Vasarla Sekhar, Sasi Kumar Tippabhotla, Hipona Randy Tupaen, Norhanani Jaafar, Chandra Bhesetti, Daniel Ismael, Xie Ling, Ser Choong Chong, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR	***2. 2:20 PM - AlN-Based Chiplet Encapsulation: Enhancing Thermal Performance for High-Density Heterogeneous Integration*** Ashita Victor, Hansol Lee, Muhannad Bakir – Georgia Institute of Technology; Dohyun Go, Diego Mora, Andrew Kummel – University of California, San Diego
3. 2:40 PM - Large Reticle Size Advanced Packaging Selection Strategy Based on Warpage: FOCoS and FOCoS-B Wu-Lung Wang, Chung-Hung Lai, Wiwy Wudjud, Wei-Hong Lai, Hsin-Chih Shih, Chin-Li Kao, Chih-Yi Huang, Kai Jung Su, Hung Hsiang Cheng, Lihong Cao, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***3. 2:40 PM - Characterization of Bonding Behavior and Void Formation in Chip-on-Wafer Hybrid Bonding*** Zhao-Ze Jiang, Chih-Jing Hsu, Chen-Hung Lee, Che-Ming Hsu, Ren-Jieh Kao, Yun-I Yeh, Alexis Angelo Garcia, Po Hsiang Wang – Advanced Semiconductor Engineering, Inc.	***3. 2:40 PM - Interfacial Reaction of In-Ag Thermal Interface Materials With Ti/Ni/Ag Backside Chip Metallization and its Influence on Thermal Resistance*** Chunen Lin, Polina Leger, Keyen Ma, Thi Minh Anh Dao, Chun-Hao Chen – National Yang Ming Chiao Tung University; Anne Groth, Olaf Wittler – Fraunhofer Institute of Reliability and Microintegration IZM; Yu-Heng Hong – Semiconductor Research Center, Hon Hai Research Institute
3:00 p.m. – 3:45 p.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 3:45 PM - Demonstration of an Optical Packaged Substrate with Embedded Silicon Photonic Transceiver for High Performance Chiplet Packaging Fumi Nakamura, Akihiro Noriki, Kenta Suzuki, Satoshi Suda, Haruhiko Kuwatsuka, Takeru Amano – National Institute of Advanced Industrial Science and Technology; Naoki Matsui, Reona Motoji, Dan Maeda, Tomoya Sugita, Hiroki Yamamoto, Hirotaka Uemura – Kyocera Corporation	***4. 3:45 PM - Inverse Hybrid Bonding at 5 µm Pitch for High-Density Heterogeneous Integration*** Madison Manley, Wanshu Zeng, Ashita Victor, Danish Baig, Muhannad Bakir – Georgia Institute of Technology; Dipayan Pal, Andrew Kummel – University of California, San Diego	***4. 3:45 PM - Development of High Thermal Conductivity Molding Materials for Automotive Flip Chip Packages*** Hungyuan Li, Jerry Wang – Siliconware Precision Industries Co., Ltd.; Masahiro Iwai, Sean Kuo, Koichiro Uchida – Sumitomo Bakelite Co., Ltd.; Fa-Chuan Chen, Hsin-Long Chen, Bo-Kuan Yeh – MediaTek, Inc.; Song J. M – Department of Materials Science and Engineering, National Chung Hsing University
5. 4:05 PM - Process Integration Challenges in Heterogeneous Integration of XPU, HBM and Photonic Chiplets for AI/HPC Applications Lai Yee Chia, Tran Van Nhat Anh, Sandra San, Tai Chong Chai – Institute of Microelectronics A*STAR	***5. 4:05 PM - Development of Particle Robust Micro-Scale Interconnect by Cured-Polymer and Solder (MICS) Technology Down to 3 µm Pitch*** Mitsuru Ooida, Akiyoshi Aoyagi, Mamoru Sasaki, Shunsuke Akatsuka, Ayumi Nakajima, Kai Takagi, Toshihisa Nonaka – Rapidus Corporation	***5. 4:05 PM - In-Situ Cure Monitoring of EMC by Fiber Bragg Grating and Dielectric Sensors with Molecular Dynamics Validation for Accurate Warpage Prediction*** Woo-Jin An, Jeong-Hyeon Baek, Woong-Kyoo Yoo, Jun-Seop Song, Hak-Sung Kim – Hanyang University; Jihye Shim, Gyung-Hwan Oh – Samsung Electronics Co., Ltd.
6. 4:25 PM - Marvell cHBM Wiring Study Joshua Dillon, Ting Zheng, Arshiya Vohra, Kazin Blacklow, Eric Tremble, Wolfgang Sauter, Sid Allman – Marvell Technology, Inc.	***6. 4:25 PM - Initial Assessments of Fine Pitch Cu-Cu TCB for 3D Integration*** Vineeth Harish, Jui-Han Liu, Diana Cantini, Samuel Wang, Goutham Ezhilarasu, Subramanian Iyer – University of California, Los Angeles; Anton Turpault, Adeel Bajwa – Kulicke and Soffa Industries, Inc.	***6. 4:25 PM - Anisotropic 0D–1D Hybrid Molding Compound for Low Warpage and Enhanced Thermal Management in Advanced Packages*** Young-Joon Lee, Woong-Ryeol Yu – Seoul National University
7. 4:45 PM - Package Architectures for Hyper Large Form-Factors for AI and HPC Segment Mohit Khurana, Sujit Sharan, Aditya Vaidya, Kemal Aygun, Kaladhar Radhakrishnan, Jianyong Xie, Chinmay Potdar, Patrick Nardi, Sachin Deshmukh, Brandon Marin, Prasanna Raghavan, Satish Surana, Shripad Gokhale, Nisha Ananthakrishnan – Intel Corporation	***7. 4:45 PM - Next-Generation Optical-Electrical Co-Design Interconnect Using Low-Temperature Hybrid Bonding Technology*** Lin-Chun Su, Jou-Yun Yeh, Yu-Lun Liu, Chun-Ta Li, Chung-Jui Lee, You-Chia Chang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chien-Kang Hsiung – National Yang Ming Chiao Tung University/Applied Materials, Inc.; Yu-Tao Yang – MediaTek, Inc.; Shang-Hsuan Wu – Tokyo Electron America, Inc.; Kazuaki Ebisawa, Makiko Irie – Tokyo Ohka Kogyo Co., Ltd.	***7. 4:45 PM - Development of Negative Thermal Expansion Fillers for Next-Generation Advanced Semiconductor Encapsulation Materials*** Tetsuharu Yuge, Yutaro Tanaka, Kazuki Tsujikawa, Chie Matsunaga, Suresh Rao Nagendra Rao, Akihiro Ohara, Haruki Koshitouge, Masahiro Yokoyama – Mitsubishi Chemical Corporation

PROGRAM SESSIONS: WEDNESDAY, MAY 27, 2:00 P.M. - 5:05 P.M.

Session 10: - Reliability of Large Body High Performance Computing and AI Packaging Solutions	Session 11: Signal Integrity Design for High-Speed Interfaces	Session 12: Characterization and Modeling for Process and Multi-Domain Analyses
Committee: **Applied Reliability**	**Committee:** **Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Tuscany E, The Ritz-Carlton	**Tuscany F-H, The Ritz-Carlton**	**Tuscany A-C, The Ritz-Carlton**
Session Co-Chairs **Keith Newman – AMD** **Email: keith.newman@amd.com** **Paul Tiner – Texas Instruments, Inc.** **Email: p-tiner@ti.com**	**Session Co-Chairs** **Amit P. Agrawal – Advanced Micro Devices, Inc.** **Email: ap_agrawal@yahoo.com** **Xiao Sun – imec** **Email: xiao.sun@imec.be**	**Session Co-Chairs** **Rui Chen – Eastern Michigan University** **Email: rchen7@emich.edu** **Ruiyang Liu – Tenstorrent Inc.** **Email: ruiyang.liu9@gmail.com**
1. 2:00 PM - Reliability Prediction Model for the Solder Joint Bridging Failure of Large-Body BGA Packages Under System-Level Heatsink Compression Hsueh-Ying Liu, Siao-Yu Chen, Tz-Cheng Chiu – National Cheng Kung University	***1. 2:00 PM - Enabling 12+Gb/s HBM4E with EMIB-T Advanced Packaging Technology*** Yidnekachew Mekonnen, Jianyong Xie, Zhiguo Qian, Xenofon Konstantinou, Yunpeng Si, Yiran Cui, Kemal Aygun, Kaladhar Radhakrishnan – Intel Corporation	***1. 2:00 PM - Accelerated Multi-Physics Simulation of Moisture-Induced Stress in Electronic Packages via Sequential Coupling*** Liangbiao Chen, Yong Liu – ON Semiconductor; S. M. Yeasin Habib, Xuejun Fan – Lamar University
2. 2:20 PM - Systematic Reliability Study of a Large Size 2.5D Package with RDL Interposer for AI Processor Richard (Shiguo) Rao, Ivan Tan, Rich Graf, Tushar Chauhan, Dwayne Shirley, Theo Anemikos, Tim Hayes, Susan Li, Kevin Caffey – Marvell Technology, Inc.	***2. 2:20 PM - Scalable Electroplated Cu and Co Metaconductor for Low Loss 112 to 400 Gbps Wired Communication Interconnects*** Saeyeong Jeon, Ariel David Cerpa, Yong-Kyu Yoon – University of Florida	***2. 2:20 PM - Micro/Nanostructural Stress Characterization for Advanced 3D Integration Technologies*** Tatsumasa Hiratsuka, Masaki Haneda, Shoji Kobayashi, Masashi Nakazawa – Sony Semiconductor Solutions Corporation; Mario Gonzalez, Peng Zhao, Eric Beyne – imec; Yoshiya Hagimoto – Sony Semiconductor Solutions
3. 2:40 PM - The First Report of Si Bridge Type 2.5D Package's Reliability for Automotive Applications Tomoko Takahashi, Ken Imai, Ryota Morimoto, Yasuhiko Maki – Socionext; Mitsufumi Ishii – Socionext Inc.; Shiro Machida, Shuuichi Kariyazaki – Renesas Electronics Corporation; Takuya Nakamura – MIRISE	***3. 2:40 PM - Advanced SI/PI Interposer Design Solution Enabling High-Performance HBM4e at up to 12Gbps*** Taeyun Kim, Sungwook Moon, Seungki Nam, Kyoungseok Oh – Samsung Electronics Co., Ltd.	***3. 2:40 PM - Mechanics-Based Sequential Fabrication Model of Glass-Core Packages with Embedded Chiplets in Redistribution Layers*** Alexander King, Hyunggyu Park, Muhannad Bakir, Suresh K. Sitaraman – Georgia Institute of Technology
3:00 p.m. – 3:45 p.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 3:45 PM - Reliability Assessment of Multilayer Glass Core Packages With Polymer and Inorganic Through Glass Via (TGV) Liner And Fully Plated TGVs Meghna Narayanan, Pragna Bhaskar, Kaushik Godbole, Lakshmi Narasimha Vijay Kumar, Lila Dahal, Durga Gajula, Kyoung-Sik Moon, Muhannad Bakir, Suresh K. Sitaraman, Mark Losego, Mohan Kathaperumal – Georgia Institute of Technology	***4. 3:45 PM - Temperature and Yield-Aware Design of UCIe Die-to-Die Interconnects for Advanced Packaging*** Ram Krishna, Xu Chen, Elyse Rosenbaum – University of Illinois; Ashita Victor, Zhonghao Zhang, Muhannad Bakir – Georgia Institute of Technology; Atom Watanabe – IBM Research	***4. 3:45 PM - A Study of Electromigration Failure Criteria and Contributing Damage Factors*** Choong-Un Kim, Harikrishnan Kumarasamy, Dong Seok Lee – University of Texas, Arlington; Tae-Kyu Lee – Cisco Systems, Inc.; Sylvester Ankamah-Kusi – Texas Instruments, Inc.; Yan Li – MediaTek, Inc.
5. 4:05 PM - Reliability of SAC PBGA Assemblies Using Constitutive and Failure Models Incorporating Damage Mechanics Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Omma Sumaiya, Jeffrey Suhling, Pradeep Lall – Auburn University	***5. 4:05 PM - Figures of Merit to Characterize the Signal Integrity Performance of Interposer Interconnect for High Bandwidth Memory (HBM)*** Taeil Bae, Jinwon Lee, Hyunggon Bae, Hyunsik Kim, Inchul Jeong, Hyungsoo Kim – SK hynix Inc.	***5. 4:05 PM - Experimental Studies Towards Better Understanding of RDL Microstructure and Built-Up Stresses for Reliable Glass-Enabled Advanced Packaging*** Chukwudi Okoro, Rajesh Vaddi – Corning Research and Development Corp.; Mandakini Kanungo, Diego Prado, Robert Schaut – Corning, Inc.
6. 4:25 PM - Chip-Package-Board Interconnects Reliability Challenges and Solutions in Large Die Fan-in Wafer Level Package Varun Thukral, Gaurav Sharma, Michiel van Soestbergen, Amar Mavinkurve, Nishant Lakhera, Abdullah Fahim, Greta Terzariol – NXP Semiconductor, Inc.	***6. 4:25 PM - Cross-Topology Transfer Learning Using Bayesian Optimization for Scalable Surrogate Modeling of 3D Packaging Structures*** Md Sultan Mahmud, Madhavan Swaminathan – Pennsylvania State University; Xianbo Yang – IBM Corporation; Priyank Kashyap – Hewlett Packard Enterprise	***6. 4:25 PM - Mechanical Impact of Embedded Capacitor Array on Processor Module for High Performance Computing Applications*** Robert Darveaux – TMBS LLC; Richard Sheridan, Imran Khan, Maryam Rezaie – Saras Micro Devices
7. 4:45 PM - Predictive Reliability Modeling of Hybrid Bonding Through Warpage and Interfacial Defect Correlation Liton Kumar Biswas, Himanandhan Reddy Kottur, Istiaq Firoz Shiam, Pavanbabu Arjunamahnthi, Navid Asadizanjani – University of Florida; Neil Hubble, Paul Handler – Akrometrix LLC; Victor Vilar, Dadi Setiadi, Charles Woychik – NHanced Semiconductors, Inc.	***7. 4:45 PM - Analytical Approach to Statistical Modeling of Power Supply Induced Jitter*** Hyunjun An, Junghyun Lee, Haeseok Suh, Jiwon Yoon, Byeongmok Kim, Junho Park, Youngsu Yoon, Jaegeun Bae, Joungho Kim – Korea Advanced Institute of Science and Technology	***7. 4:45 PM - Experimental and Computational Fracture Strength Characterization at BEOL Structure Sharp Corners for Chip-Package Interaction Reliability Assessment*** Jehun Youn, Jonathan Whitby, Pei-En Chou, Ganesh Subbarayan – Purdue University

PROGRAM SESSIONS: THURSDAY, MAY 28, 9:30 A.M. - 12:35 P.M.

Session 13: Advances in Thermal Design and Characterization	Session 14: RDL and Fan-Out Interconnections	Session 15: Optical Interconnects
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Photonics**
Palazzo A-C, JW Marriott	**Palazzo D, JW Marriott**	**Tuscany D, The Ritz-Carlton**
Session Co-Chairs **Monita Pau – Onto Innovation** **Email: monita.pau@ontoinnovation.com** **Eric Tremble – Marvell Technology, Inc.** **Email: etremble@marvell.com**	**Session Co-Chairs** **Takafumi Fukushima – Tohoku University** **Email: fukushima-tak@tohoku.ac.jp** **Srinivas Pietambaram – Intel Corporation** **Email: srinivas.v.pietambaram@intel.com**	**Session Co-Chairs** **Richard Pitwon – Resolute Photonics, Ltd.** **Email: rpitwon@resolutephotonics.com** **Ping Zhou – LDX Optronics, Inc.** **Email: pzhou@ldxoptronics.com**
1. 9:30 AM - Process Development and Thermal Characterization of Micropillar Direct-to-Silicon Liquid Cooling Solution on CoWoS-R Platform Sing-Da Jiang, Chun-Yu Ou, Chi-Shiang Chiou, Yu-Sheng Tsai, Chang-Yi Tsai, Chuan-Chang Wu, Tsunyen Wu, Ying-Ju Chen, Wen-Hsiung Lu, Tzong-Huann Yang, Ren-Yu Chang, Kathy Yan, Rick Lien, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Low Warpage Double Side RDL Interconnection With Electrical Compensation for Panel Level Package*** Terry Wang, Cheng-Yueh Chang, Chien-Ming Tseng, Yu-Jhen Yang, Pei-Pei Cheng, Wendy Chou – Industrial Technology Research Institute; Hungyu Wu – Applied Materials, Inc.; Austin Cheng – FAVITE, Inc.; Hsin-Yi Huang – Everlight Chemical Industrial Corp.; Simon Zhong – TAIWAN TAIYO INK CO., Ltd.; Chi-hua Huang – Alliance Material Co., Ltd.; Kent Chen – CSUN, Ltd.	***1. 9:30 AM - Low-Loss Optical Interconnect Designs in Optimized Glass for Co-Packaged Optics*** Lars Brusberg, Jorge Holguín-Lerma – Corning, Inc.; Matthew Dejneka, Lucas W. Yeary, Chad Terwilliger, Betsy Johnson, Charisse Spier, Jonathan Walter, Katerina Rousseva, Sean Garner – Corning Research and Development Corp.
2. 9:50 AM - Toward Reliable and Thermally Robust BSPDN: A Dual-Path Design Based on BN–BN Bonding Chi Hsueh, Mu-Ping Hsu, Chun-Che Cheng, Jia-Rui Lin, Kuan-Neng Chen – National Yang Ming Chiao Tung University	***2. 9:50 AM - Panel CMP Co-Planarization of Heterogeneous Interfaces for Damascene Organic Interposers (L/S = 2/2 µm)*** Katsuaki To, Masashi Minami, Sadaaki Katoh – Resonac Corporation	***2. 9:50 AM - Detachable Glass Waveguide Connector for Co-Packaged Optics on Silicon Photonics Platform with <1.5 dB/Facet Passive Coupling and 280 mW Power Handling*** Arpan Dasgupta, A.K.M. Zahidur Chowdhury, Takako Hirokawa, Brian Popielarski, Yusheng Bian, Kevin Eaton, Jae Cho, Yarong Lin, Geng Ni, Keith Donegan, John Garant, Helen Wong, Robert Katz, Ryan Sporer, Michelle Zhang, Janet Tinkler, Asli Sahin, Norman Robson, Jean-Baptiste Laloe, Kevin Dezfulian, Jean Trewhella, Bob Mulfinger, Ken Giewont, Ted Letavic, Koushik Ramachandran, Rick Carter, Vikas Gupta – GlobalFoundries, Inc.; Sean Garner, Rajesh Vaddi – Corning Research and Development Corp.; Jasmeet Singh, Martin Spreemann, Robert Lee, Chuan Che Wang, Tim Grygriel, Andreas Matiss – Corning Incorporated
3. 10:10 AM - System-Level Thermal Validation of 2.5D Packages in GPU Servers: Impact of TCB vs HCB HBM Platforms Linus Park – Samsung Semiconductor, Inc.; Youchang Na, Seongjin Hong, Yoko Tomo, Hae Jung Yu, Yanggyoo Jung, Gyoungbum Kim, Heeyoub Kang, Yeonghyeon Gim, Eduardo Hernandez Pacheco, Jaechoon Kim, Yun Seok Choi – Samsung Electronics Co., Ltd.	***3. 10:10 AM - 3D Integration of an SRAM Chiplet in Fan-out Embedded Bridge Platform Achieving Low Energy Read/Write*** Dany-Sebastien Ly-Gagnon, Li Chen, Dwight Lee, Max Wu, Jiajing Wang, Ping-Chen Liu, CH Yang, Chung-Ching Peng – Intel Corporation; Steven Lin, Bruce Xu, Chung Kang Cai – Siliconware Precision Industries Co., Ltd.	***3. 10:10 AM - Laser Cleaning of Optical Couplers on Photonic Integrated Circuits*** Jean-Philippe Berube, Alexandre Douaud, Feng Liang, Loic Arias, Philippe Gagnon, Simon Duval, Louis-Rafael Robichaud – Femtum; Philippe Lassonde – Femtum/INRS; Francois Legare – National Institute for Scientific Research (INRS)
10:30 a.m. – 11:15 a.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 11:15 AM - High Performance Direct Liquid Jet Impingement Cooling on Structured Silicon Herman Oprins, Georg Elsinger, Vladimir Cherman, Geert Van der Plas, Zsolt Tokei, Eric Beyne – imec	***4. 11:15 AM - Influence of Metal Surface Characteristics on Auto Focus Reference Position and Pattern Fidelity in Fine-Pitch RDL Applications*** Jaehyuk Chang, Seokhun Choi, Kyung Chan Hwang, Zhongchuan Zhang, Chang I Su, Wen Fu, CC Chuang, YingChiao Wang – Applied Materials, Inc.; Hyunseok Yang, Youmin Chang, Chanjin Park, Mingu Kang – Samsung Electro-Mechanics Co., Ltd.	***4. 11:15 AM - Development of a High-Efficiency, Wide-Temperature-Range Optical Coupling Structure for CPO Modules*** Shuhei Sudo, Megumi Oishi, Misa Takahashi, Shogo Enomoto, Kono Sasaki, Tomoyuki Akahoshi – Kyocera Corporation
5. 11:35 AM - Process Development of Two-Stacked Chips with a Backside Embedded Two-Phase Cooling Solution Xiaowu Zhang, Boon Long Lau, Huicheng Feng, Gongyue Tang, Ming Chinq Jong, Surya Bhattacharya, Vempati Srinivasa Rao, B.S.S. Chandra Rao, Van Nhat Anh Tran – Institute of Microelectronics A*STAR	***5. 11:35 AM - Study of SeWaRe Failure in a Glass-Core Substrate with Redistribution Layers*** Kaushik Godbole, Nirvan Patel Masini, Alexander King, YongWon Lee, Suresh K. Sitaraman – Georgia Institute of Technology	***5. 11:35 AM - High-Density Polymer Waveguide Integration on Glass Substrate for CPO*** Takuya Kitainui, Yujiro Saito, Naoki Fukuda, Kenichi Ogawa – Dai Nippon Printing Co., Ltd.
6. 11:55 AM - Advances in Direct-to-Chip Liquid Cooling Integration Laura Mirkarimi, Ron Zhang, Gill Fountain, KM Bang, Suhail Sadiq, Arianna Avellan, Bongsub Lee, Helen Katske – Adeia	***6. 11:55 AM - Low-Cost Process of Organic RDL-Based Packaging Platform Enabling UCIe 32 GT/s Link Speed*** Donggyu Kim, Jun-Su Kim, Kwang Il Kim, Jun-Beom Kim, Yong-Gyu Jang, Yeon Ji Shin, Jae-Sung Lim, Sang Gyu Jang, Jin-Wook Jang – HANA Micron, Inc.; Sangyong Park, Seungho Lee, Jaeyoung Kim – Qualitas Semiconductor Co., Ltd.	***6. 11:55 AM - Low-Loss Polymer Waveguide Device for Fiber-to-Chip and Chip-to-Chip Connection*** Kai Yokoyama, Haruka Nakajima, Takaaki Ishigure – Keio University
7. 12:15 PM - Diamond-on-Chip Integration for Enhanced Thermal Management and Warpage Control in 2.5D Chiplets Packaging Zeming Tao, Ningning Xu, Dongchen Fan, Jinbao Zhang, Yixiong Wu, Weiyi Lin, Rongbin Xu, Dongxue Liang, Yi Zhong – Xiamen University; Delong Qiu – Jiashan Fudan Research Institute	***7. 12:15 PM - FOWLP-Enabled 3D Package-Level Heterogeneous Integration with Advanced Heat Spreading Architecture for Next-Generation Mobile Device*** Kyung Don Mun, Jihwang Kim, Sangjin Baek, Wooyoung Kim, Bong-Soo Kim, Dahye Kim, Bongju Cho, Se Hoon Jang, Jaechoon Kim, Suk Won Jang, Eun Young Lee, Daewoo Kim – Samsung Electronics Co., Ltd.	***7. 12:15 PM - Integrated Assembly Process For Pluggable Fiber Connector For Co-Packaged Optics*** Jelena Pesic, Lily Yuan, Joy Zhan, Shuhe Li, Dehua Xiao, Subal Sahni, Ankur Aggarwal – Celestial AI; Digvijay Raorane – Celestial AI/Marvell Technology, Inc.; Masha Gorchichko, Suresh Pothukuchi – Marvell Technology, Inc.

PROGRAM SESSIONS: THURSDAY, MAY 28, 9:30 A.M. - 12:35 P.M.

Session 16: Assembly and Manufacturing: 3D Stacking and Thermal Solutions	Session 17: Digital Twin and AI in Advanced Packaging and Interconnect Security	Session 18: Hybrid Bonding: Advanced Processing and Modeling
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committees: Materials & Processing and Thermal/Mechanical Simulation & Characterization**
Tuscany E, The Ritz-Carlton	**Tuscany F-H, The Ritz-Carlton**	**Tuscany A-C, The Ritz-Carlton**
Session Co-Chairs **Wenhao (Eric) Li – Applied Materials** **Email: liwenhao2010@gmail.com** **Jobert Van Eisden – MKS Instruments** **Email: Jobert.van-Eisden@MKS.com**	**Session Co-Chairs** **Masha Gorchichko – Marvell Technology, Inc.** **Email: maria.gorchichko@gmail.com** **Xinpei Cao – Henkel Corporation** **xinpei.cao@henkel.com**	**Session Co-Chairs** **Ercan (Eric) Dede – Toyota Research Institute North America** **Email: eric.dede@toyota.com** **Vidya Jayaram – Chipletz** **Email: vidya.jayaram@chipletz.com**
1. 9:30 AM - Selective Layer Transfer to Enable Fine-Grain Mixed Front-End Devices with Monolithic Interconnects Tushar Talukdar, Paul Nordeen, Thomas Sounart, Mohammadreza Yaghoobi, Abhishek Sharma, Andrey Vyatskikh, Brandon Rawlings, Clifford Engel, Lei Jiang, Felipe Bedoya, Siyan Dong, Charles El Helou, Mudit Bhargava, Adel A Elsherbini, Shawna Liff, Aleksandar Aleksov, Myung-Hee Na – Intel Corporation	***1. 9:30 AM - SUBSTRATE-CLOAK: A MEMS-Enabled Reconfigurable Obfuscation Framework for Secure Substrate Interconnects*** Himanandhan Reddy Kottur, Pavanbabu Arjunamahnthi, Mohammad Shafkat Khan, Pragyna Titty, Liton Kumar Biswas, Katayoon Yahyaei, Md Shah Imran Shovon, Istiaq Firoz Shiam, Navid Asadizanjani – University of Florida; Liam Hayes, Bo Liu, Joshua Hihath – Arizona State University; Michael Delany – BuildEmber LLC	***1. 9:30 AM - Pushing the Envelope in Mechanical Characterization of Copper in Hybrid-Bonding Patterns for Advanced Packaging: From Instrumented Indentation to Multimodal Atomic Force Microscopy*** Nicolas Alderete, Yvonne Gerbig, Gheorghe Stan – National Institute of Standards and Technology; Paresh Daharwal – Intel Corporation; Cristian Ciobanu – Colorado School of Mines/NIST
2. 9:50 AM - First Demonstration of MicroBump-based Massive Orthogonal Stacking Assembly IC (MOSAIC) Cube for SoC-DRAM Direct Stacking Hung-Chih Huang, Yuki Mitarai, Masaya Kawano, Mototsugu Hamada, Atsutake Kosuge – University of Tokyo; Takafumi Fukushima – Tohoku University	***2. 9:50 AM - Cryogenic Via-last TSVs for 2.5D Qubit Chip Implementation Demonstrating DC–20 GHz Signal Transmission at Millikelvin Temperatures*** Misato Taguchi, Takuji Miki – Kobe University	***2. 9:50 AM - Nanoindentation-Based Analysis of Wafer-to-Wafer Bond Strength Using Cohesive Zone Modeling and Machine Learning*** Yusuf Ozdemir, Oguzhan Orkut Okudur, Kris Vanstreels, Mario Gonzalez, Clement Merckling, Eric Beyne – imec
3. 10:10 AM - Electroplated Cu-Diamond Composite Thermal Vias for Interposer-Level Heat Management in 2.5D/3D Packages Ye Yang, Tiwei Wei – University of California, Los Angeles; James Chien – Taiwan Foresight Co. Ltd.	***3. 10:10 AM - Demonstration of Superconducting-Material-Filled TSV on Cryogenic Packaging Platform*** Hong Yu Li, Norhanani Jaafar, Ya-Ching Tseng, Anh Tran Van Nhat, Yong Chyn Ng – Institute of Microelectronics A*STAR	***3. 10:10 AM - Effects of the Chip Geometry and Bonding Initiation Point on Bonding Distortion in Die-to-Wafer Hybrid Bonding*** Takaaki Hirano, Tatsumasa Hiratsuka, Shoji Kobayashi, Masashi Nakazawa – Sony Semiconductor Solutions Corporation; Taichi Yamada, Yoshiya Hagimoto – Sony Semiconductor Solutions
10:30 a.m. – 11:15 a.m. • Refreshment Break: Exhibition Hall – Mediterranean Ballroom		
4. 11:15 AM - Optical Engine (OE) Integration Challenges for Next-Generation CPO on Networking and HPC Application Mike Tsai, Ming Zhuang, Shane Lin, Steven Lin, Michael Fu, Bruce Xu, Yih Jiang, Don Son Jiang – Siliconware Precision Industries Co., Ltd.	***4. 11:15 AM - Fabrication and Experimental Characterization of Embedded Multi-Terminal Capacitors With Ultra-Low Parasitics for Integrated Vertical Power Delivery*** Ramin Rahimzadeh Khorasani, Mohammad Al-Juwhari, Mahin Ahamed, Madhavan Swaminathan – Pennsylvania State University; Xingchen Li – Georgia Institute of Technology; Wisnu Murti, Tae Dong Kim – ELSPES	***4. 11:15 AM - First Demonstration of 450nm Pitch Cu-Cu Hybrid Bonding with 98% Yield Across 20M Interconnects for Ultra-Dense 3D Integration*** Ying Trickett, Roger Quon, Yoocharn Jeon, Amit Prakash, Raghav Sreenivasan, Raghuveer Patlolla, Joan Chung, JuSeon Goo, Shashank Sharma, Jeremiah Hebding, Siddarth Krishnan, Michael Chudzik – Applied Materials, Inc.; Sang Jin Kim, Norman Tam – Applied Materials; Barbara Weis, David Goldberger – EV Group
5. 11:35 AM - High Power System Scaling Using Double-Sided Connection in Embedded Substrate Sheng Li – Advanced Semiconductor Engineering, Inc. (US); Chu Jie Yang, Min Lung Huang, Yue Nung Lin, Jen-Kuang Fang – Advanced Semiconductor Engineering, Inc.	***5. 11:35 AM - Hidden in Traffic: Timing Leakage in Heterogeneous Integrated Processors*** Abir Ahsan Akib, Ankur Srivastava – University of Maryland; Sanjay (Jay) Rekhi, Kostas Amberiadis – National Institute of Standards and Technology	***5. 11:35 AM - System-Level Thermal Characterization of Hybrid Cu Bonded HBM on 2.5D Advanced Packaging*** Seongjin Hong, Hae Jung Yu, Hyuek Jae Lee, YoungLyong Kim, Jin Hyuk Chang, Mingyu Kang, Sangho Shin, Eunhee Jung, Youchang Na, Yooseok Jeong, Hyungjoon Jun, Seonghyun Park, Yeonghyeon Gim, Jaechoon Kim, Yun Seok Choi – Samsung Electronics Co., Ltd.; Linus Park – Samsung Semiconductor, Inc.
6. 11:55 AM - Top-Side Silicon Capacitor for Co-Optimized Thermal and Power Delivery in Fan-out Wafer Level Package Based PoP for Mobile SoCs Kyojin Hwang – Murata Manufacturing Co., Ltd.; Woobin Jung, Youngsang Cho, Jisoo Hwang, Heeseok Lee, Daehyun Kim, Seung Wook Yoon – Samsung Electronics Co., Ltd.	***6. 11:55 AM - Surface-Mounted Conformal Adhesive Electrodes for Impedance-Based Crack Detection in Composite Materials*** Riadh Al-Haidari, Babatunde Falola, Mousa Al-Zanina, Stephen Gonya, Mark Poliks – Binghamton University; Andrew Stemmermann, Daniel Balder – SunRay Scientific, Inc.	***6. 11:55 AM - Near-IR Excited Upconversion Nanoparticles for Optical Wafer-to-Wafer Bonding*** Aparnaa Iyer, Eren Özmen, Mohan Kathaperumal, Mark Losego, Ching-Ping Wong – Georgia Institute of Technology
7. 12:15 PM - High-Thermal-Conductivity (1.0 W/(m·K)) Dry-Film Solder Resist at 20 µm: Compatible with Standard Process Flow and Steady-State Thermal Validation Takumi Suzuki, Kohei Kitagawa, Ryohei Nojima, Fumitaka Kato, Daichi Okamoto – Taiyo Ink Mfg. Co., Ltd.; Zihao Lin, Kyoung-Sik Moon, Mohan Kathaperumal, Ching-Ping Wong – Georgia Institute of Technology	***7. 12:15 PM - AI-Driven Inverse Design and Vision Fusion Framework for Automated Signal Integrity Optimization of Organic RDL Interposers*** Minsun Cho, Taeheon Lee, Jiho Yu, Dayeong Kim, Sungyeop Jung – Korea University	***7. 12:15 PM - Fine-pitch Cu-Cu Hybrid Bonding Using Electroless-deposited (111) Nanotwinned Cu*** Wei Choong Lee, Po-Shao Shih, I-En Chen, Cheng-Yan Yang, Yu-Hsiang Lu, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

PROGRAM SESSIONS: THURSDAY, MAY 28, 2:00 P.M. - 5:05 P.M.

Session 19: Substrate Core Innovations: Glass, Ceramic, and Silicon

Committee:
Packaging Technologies

Palazzo A-C, JW Marriott

Session Co-Chairs
Kuldip Johal – MKS Instruments
Email: kuldip.johal@mks.com
Markus Leitgeb – AT&S AG
Email: m.leitgeb@ats.net

1. 2:00 PM - Glass Core Substrates – Next Generation Advanced Packaging Platform for AI and HPC
Srinivas Pietambaram, Tarek Ibrahim, Nicholas Psaila, Hiroki Tanaka, Vinith Bejugam, Dhruba Pattadar, Praveen Sreeramagiri, Manohar Konchady, Jeff Kaplan, Izabela Murtagh, Changhua Liu, Rahul Manepalli – Intel Corporation

2. 2:20 PM - Optimization of Glass Substrate CTE for Warpage Control and Solder Joint Reliability in Large HPC Packages
Pengcheng Yin, Junbo Yang, Yangyang Lai, Karthik Arun Deo, Kewei Shou, Dalei Yang, Seungbae Park – Binghamton University

3. 2:40 PM - First Demonstration of Low-loss W-/D-Band Vertical Interconnects on Multi-stacked Ceramic-Glass Substrate for 6G Antenna-in-Package Modules
Chenhao Hu, Genaro Soto Valle Angulo, Kyoung-Sik Moon, Manos M. Tentzeris – Georgia Institute of Technology

Session 20: Performance Analysis and Metrology of High-Bandwidth Electrical and Optical Interconnects

Committee:
Interconnections

Palazzo D, JW Marriott

Session Co-Chairs
Yu-Tao Yang – MediaTek, Inc.
Email: yu-tao.yang@mediatek.com
Chaoqi Zhang – Apple Inc.
Email: chaoqi.gt.zhang@gmail.com

1. 2:00 PM - Hybrid Bonding Surface Roughness Characterization: A RHEED Approach With High Speed and Atomic Scale (sub-nm) Sensitivity at Wafer Level
Weichang Lin, James Lu, Toh-Ming Lu, Gwo-Ching Wang – Rensselaer Polytechnic Institute; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research

2. 2:20 PM - Signal and Power Integrity of Organic, Silicon, and Hybrid Interposer in HPC Chiplet-Based System
Ming-Hung Wu, Yaotsu Chen, Yi-Chin Tsai, Po-Yuan Wei, Liang-Kai Chen, ChungHsuan Wu, Chun-Hong Chen, Sheng-Fan Yang – Global Unichip Corporation

3. 2:40 PM - Novel Metrology For Experimentally Visualizing Cu-Cu Bonding Induced Thermal Stress
Jie Li, Keyu Wang, Shuhang Lyu – Purdue University; Tiwei Wei – University of California, Los Angeles

Session 21: Novel Laser-Based Technologies and Fine-Pitch Interconnects

Committee:
Materials & Processing

Tuscany D, The Ritz-Carlton

Session Co-Chairs
Bing Dang – IBM Corporation
Email: dangbing@us.ibm.com
Mark Poliks – Binghamton University
Email: mpoliks@binghamton.edu

1. 2:00 PM - Fabrication and Transfer of Fine Pitch RDL Using Si Temporary Carrier Combined With IR Laser Release Approach
Francois Chancerel, Gilberto Casillas, John Slabbekoorn, Steven Brems, Koen Kennes, Arnita Podpod, Alain Phommahaxay, Zsolt Tokei, Eric Beyne – imec; Peter Urban, Simon Halas, Mario Gram, Thomas Uhrmann, Markus Wimplinger – EV Group

2. 2:20 PM - IR Laser Debond Process Modeling
Thomas Sounart, Henning Braunisch, Paul Nordeen, Tushar Talukdar, Md Mahbubul Hasan, Karan Prabhakar – Intel Corporation

3. 2:40 PM - Novel Organic Temporary Bonding Material for High-Temperature Semiconductor Processing Applications
Taichi Kikkawa, Yutaka Hisamune, Satoshi Inada, Yuzo Nakamura – Mitsui Chemicals, Inc.

Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Mediterranean Ballroom

4. 3:45 PM - The Impact of Glass Materials and Embedded Silicon on 2.3D and 2.5D Package Performance
Heeyoub Kang, Seulgi Yu, Gyung-Hwan Oh, Seongjin Hong, Dongwon Yoo, Gyoungbum Kim, Yoonha Jung, Kang Joon Lee, Jaechoon Kim, Yun Seok Choi – Samsung Electronics Co., Ltd.

5. 4:05 PM - Development of Long-Term Reliability for Glass Core Substrates with Build-up Layers
Koji Fujimoto, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.

6. 4:25 PM - Scaling Interconnect Density with Silicon-Core-Substrate Nano-Integrated Via Technology
Seann Ayers, Steven Verhaverbeke, Han-Wen Chen, Suresh Ramalingam – Applied Materials, Inc.

7. 4:45 PM - InfinityBoard A Panel-Level Glass-Core Packaging Platform for Ultra-Fine RDL and Vertical Interconnect Integration
Roland Rettenmeier, Laurent Nicolet, Michael Kothe, Udo Kirsch, Christian Schmid, Sven Seren, Thomas Widmann, Christian Buchner, Dian Zhang – SCHMID Group

4. 3:45 PM - Vertical Interconnects Characterization for 448 Gbps/lane Co-Packaged Optics Using Double-Sided Probing Method
JiaQi Wu, Sajay Gourikutty, Teck Guan Lim, Surya Bhattacharya – Institute of Microelectronics A*STAR

5. 4:05 PM - Photonic Interconnects in Glass Core for AI Data Center Applications
Md Rayid Hasan Mojumder, Ziyu Guo, Ning Li, Madhavan Swaminathan – Pennsylvania State University

6. 4:25 PM - Photonic Fabric™ Interconnect for a Scale-up Network Solution in Accelerated Computing
Dan Oh, Ankur Aggarwal, Jelena Pesic, Subal Sahni, Parmanand Mishra, Phil Winterbottom, David Lazovsky – Celestial AI; Suresh Pothukuchi, Ganesh Balamurugan, Trung Diep – Marvell Technology, Inc.

7. 4:45 PM - Advanced 3D Packaging Optics Engine with Integrated Micro-VCSEL Array for Ultra-High Bandwidth Optical Interconnect
Yuk-Tong Cheng, Murphy Lee, Tzu-Hung Lin, Wang Shi Yu, Chih-Hsiang Ho, Jr-Hau He – Rayleigh Vision Intelligence

4. 3:45 PM - Study of Sn Damascene Process for Novel Fine Pitch Micro-Bump Formation and Bonding
Kosuke Yamashita, Eric Turner, Haiying Zhou – Fujifilm Electronic Materials; John Slabbekoorn, Jaber Derakhshandeh – imec; Kazuki Tomota – Fujifilm Corp.

5. 4:05 PM - Thin Cleanable Organic Laser Release Layer With Ultralow Laser Transmittance Below 360 nm Wavelength for TBDB
Hanlin Chen, Loyde Braidlow, Amit Kumar, Alice Guerrero, Elliott Fitch, Deborah Blumenshine, Luna Liang, Christopher Bakker, Arthur Southard – Brewer Science, Inc.

6. 4:25 PM - Novel Temporary Bonding Film and Debonding Method Adapted for the Fabrication Process of Large Size Panel Packages
Motohiro Negishi, Yuta Akasu, Koji Yukimatsu, Emi Miyazawa, Tetsuya Enomoto, Tomohiro Ohkubo, Saeko Ogawa, Masanori Natsukawa, Tomohiko Kotake – Resonac Corporation

7. 4:45 PM - Electroplated Indium Micro-Bumps: Toward Scalable Low Temperature Ultra-Fine Pitch Interconnects
Maria-Luisa Calvo-Munoz, Yacoub Sahouane, Erwan Mekadem-Belaid, Mathilde Gottardi, Abdelhak Hassaine, Marie Maubert, Laurence Gabette, Laurence Andreutti, Catherine Pellissier, Chafik Mhamdi, Thierry Mourier – CEA-LETI; Alain Gueugnot – Grenoble Alps University/CEA-LETI

PROGRAM SESSIONS: THURSDAY, MAY 28, 2:00 P.M. - 5:05 P.M.

Session 22: Reliability of High Current and High Power Packaging Solutions

Committee:
Applied Reliability

Tuscany E, The Ritz-Carlton

Session Co-Chairs
Nokibul Islam – STATS ChipPAC, Ltd.
Email: Nokibul.ISLAM@jcetglobal.com
Yan Li – MediaTek, Inc.
Email: yanli7274@gmail.com

1. 2:00 PM - ENEPES as an Effective Surface Finish for Enhancing Electromigration Reliability in Solder Joints
Mai Yokota, Tsuyoshi Maeda, Katsuhisa Tanabe – C. Uyemura & Co., Ltd.

2. 2:20 PM - Direct to Silicon Microfluidic Cooling for Datacenters
Sashikanth Majety, Baris Dogruoz, Venkata Chivukula, Cam Turner, Bharath Ramakrishnan, Husam Alissa, Srikant Bharadwaj, Camille Couturier – Microsoft Corporation; Malik Fahrni, Yann Meier, Remco van Erp, Samuel Higginbotham – Corintis

3. 2:40 PM - Enabling Reliability Testing of Solder Interconnects Under Extreme Current
Choong-Un Kim, Jorge Mendoza, Dong Seok Lee, Harikrishnan Kumarasamy – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen – Texas Instruments, Inc.; Tae-Kyu Lee – Cisco Systems, Inc.; Patrick Thompson – TTFS

4. 3:45 PM - Cu-Core Solder Interconnect Mechanical Shear Strength Under High Current Density
Tae-Kyu Lee, Yujin Park, Adnan Mahmud, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.; Young-Woo Lee, Hui-Joong Kim, Jae-Yeol Son, Seul-Gi Lee – MK Electron Co., Ltd.

5. 4:05 PM - Evolution and Correlation of Microstructure and Mechanical Properties in Aged SAC/LTS Hybrid Solder Joints
Mahbub Alam Maruf, Souvik Chakraborty, Jeffrey Suhling, Pradeep Lall – Auburn University

6. 4:25 PM - Time-Resolved 3D X-ray Imaging of Electromigration Void Evolution in 2.5D Package
Junbo Yang, Stephen Cain, Yuhan Gao, Dalei Yang, Karthik Arun Deo, Yi Deng, Kewei Shou, Seungbae Park – Binghamton University

7. 4:45 PM - Effects of Plating Current Density on Electrochemical Reliability of RDL: In-Situ Electrochemical Migration Testing and Time-to-Failure Prediction
Hojin Lee, Jeong-Hyeon Baek, Haesu Ahn, Hak-Sung Kim – Hanyang University; Taehoon Kim, Jihye Shim – Samsung Electronics Co., Ltd.; Hyoc-Min Youn, Hakgee Jung – Dongjin Semichem Co., Ltd

Session 23: Power Integrity Analysis for High-Performance Computing

Committee:
Electrical Design and Analysis

Tuscany F-H, The Ritz-Carlton

Session Co-Chairs
Markondeya Raj Pulugurtha – Florida International University
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Atom Watanabe – IBM Research
Email: atom@ibm.com

1. 2:00 PM - Deep Coordination Graph-Based Reinforcement Learning for Multi-Domain PDN Optimization
Junho Park, Seonguk Choi, Inyoung Choi, Gwantaek Lee, Jiwon Yoon, Junghyun Lee, Youngsu Yoon, Byeongmok Kim, Jaegeun Bae, Joungho Kim – Korea Advanced Institute of Science and Technology; Chulhee Cho, Jinwook Song – Samsung Electronics Co., Ltd.

2. 2:20 PM - Design Methodology and Power Integrity Analysis of Staggered Current Pattern for Voltage Drop Mitigation in High-Power Multi-Core HPC System
Hyunwoong Kim, Sungwook Moon, Jungil Son, Chaewon Baek, Seungki Nam – Samsung Electronics Co., Ltd.

3. 2:40 PM - Dynamic Power Management Methodology for Distributed Vertical Power Delivery in High-Performance Computing Systems
Sriharini Krishnakumar – University of Illinois, Chicago; Inna Partin-Vaisband – University of Illinois

4. 3:45 PM - Neural Surrogates for Fast Signal and Power Integrity Co-Simulation and Co-Design of Chiplets Integration
En-Xiao Liu, Richard Xian-Ke Gao, Jun Liu, Dingjie Lu, Sridhar Narayanaswamy – Institute of High Performance Computing A*STAR; Zaifeng Yang – A*STAR Institute of High Performance Computing; Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR

5. 4:05 PM - Design Space Exploration of Chiplet and Interposer PDNs for 2.5D AI Systems
Seungmin Woo, Madison Manley, Muhannad Bakir – Georgia Institute of Technology; Taehoon Kim – Samsung Electronics Co., Ltd.

6. 4:25 PM - Fast Signal and Power Integrity Analysis Algorithm of UCIe-Based High-Speed Links with Transistor-Level Equalizers
Yi Zhou, Lewei Tang, Tahsin Shameem, Bobi Shi, Jose Schutt-Aine – University of Illinois

7. 4:45 PM - PINS: Power Integrity-Aware Power Delivery Network Synthesis in Interposer-Based Advanced Packaging
Tzu Han Hsu, Iris Hui-Ru Jiang – National Taiwan University

Session 24: AI and Machine Learning for Electronics Packaging

Committee: Thermal/Mechanical Simulation & Characterization

Tuscany A-C, The Ritz-Carlton

Session Co-Chairs
Pradeep Lall – Auburn University
Email: lall@auburn.edu
Karsten Meier – TU Dresden
Email: karsten.meier@tu-dresden.de

1. 2:00 PM - Multi-Agent Automation for Design-for-Reliability: From Literature to Auditable Knowledge and Experimental Design
Jialong Liang, Jiajie Fan, Guoqi Zhang, Willem van Driel – Delft University of Technology

2. 2:20 PM - Physics-Informed Neural Network Approach for Fast Prediction of Temperature Distribution and Hot Spots in Co-Packaged Optics
Sohrab Sheikh Sofla, Madhavan Swaminathan – Pennsylvania State University; Keng Tuan Chang, Meiju Lu, William Chen, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.; C. M. Hung, Yu-Tao Yang, Chinq-Shiun Chiu – MediaTek, Inc.

3. 2:40 PM - StressScore: Evaluating AI Predicted Stress Contours in Advanced Packaging With Contrastive Learning
Kart Leong Lim – Institute of Microelectronics A*STAR; Thanmaya Bharadwaj Puvvada – Nanyang Technological University (NTU)

4. 3:45 PM - AI-Driven Surrogate Modeling and Uncertainty Quantification for Active Power Cycling in Power Electronics Packages
Dharshan Barkur – TU Dresden/Robert Bosch GmbH; Przemyslaw Gromala – Robert Bosch Kft; Karsten Meier, Karlheinz Bock – TU Dresden

5. 4:05 PM - In-Situ Anomaly Detection for Power MOSFET's Degradation Based on Unsupervised LSTM-Autoencoder
Shaojian Xie, Jiajie Fan – Fudan University; Mesfin Ibrahim, Hiu Hung Lee, Chang Lu – Centre for Advances in Reliability and Safety, New Territories, Hong Kong; Jialong Liang, Guoqi Zhang – Delft University of Technology

6. 4:25 PM - Cross-Domain Integrated Digital Twin for Heterogeneous Integrated CPUs
Mumtahina Islam Sukanya, Aniket Bharamgonda, Abhijit Dasgupta, Ankur Srivastava – University of Maryland

7. 4:45 PM - A Physics-Informed AI Platform for Warpage Prediction and SMT Feasibility in Versatile 2.5D Packaging
Kewei Shou, Junbo Yang, Karthik Arun Deo, Dalei Yang, Pengcheng Yin, Yangyang Lai, Weichen Zhao, Yi Deng, Yuhan Gao, Seungbae Park – Binghamton University

Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Mediterranean Ballroom

PROGRAM SESSIONS: FRIDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 25: Optical and Electrical Design for High-Performance Computing	Session 26: Advanced Wafer-to-Wafer Hybrid Bonding	Session 27: Innovation in Glass and Dielectric Materials for Heterogeneous Integration
Committees: Electrical Design and Analysis and Packaging Technologies	**Committee: Interconnections**	**Committee: Materials & Processing**
Palazzo A-C, JW Marriott	**Palazzo D, JW Marriott**	**Mediterranean 4, JW Marriott**
Session Co-Chairs **Nicolas Boyer – Ciena Corporation / Email: nboyer@ciena.com;** **Michael Gallagher – Qnity Electronics, Inc. / Email: michael.gallagher@qnityelectronics.com; Srikrishna Sitaraman – Marvell Technology, Inc. / Email: srikrishna.sitaraman@gmail.com**	**Session Co-Chairs** **Anne Jourdain – imec** **Email: anne.jourdain@imec.be** **Tiwei Wei – University of California, Los Angeles** **Email: tiwei32@ucla.edu**	**Session Co-Chairs** **Jay Cho – GlobalFoundries, Inc.** **Email: jay.cho@gf.com** **Ziyin Lin – Intel Corporation** **Email: ziyin.lin@intel.com**
1. 9:30 AM - Advancing Interconnect Performance and Reliability with Innovations in 3D Photonic Integration Packaging and Fiber Coupling Sufi Ahmed, Sandeep Sane, Reza Baghdadi – Lightmatter; Bradley Snyder – PHIX; Suresh Jayaraman – Amkor Technology, Inc.	***1. 9:30 AM - Novel Process Integration for Highly Reliable and Manufacturable 0.4-µm-Pitch 50 M Cu-Cu Connections*** Yukako Ikegami, Ken Arano, Masanori Chiyozono, Kengo Kotoo, Kan Shimizu, Yoshihisa Kagawa – Sony Semiconductor Solutions	***1. 9:30 AM - Non-Destructive Characterization of Laser-Induced Molecular Modification in Glass for Selective Etching to Fabricate Through-Glass Vias (TGV) in Advanced Packaging*** Mruga Panse, Kyoung-Sik Moon, Mohan Kathaperumal, Ching-Ping Wong – Georgia Institute of Technology; Stefan Janssen, Youngho Suh, Myungjoo Park, Jehhoon Bhang – LG Electronics
2. 9:50 AM - Photonic Fabric™ Chiplets for Co-Packaged Optics in AI Data Centers Suresh Pothukuchi, Rekha Govindaraj – Marvell Technology, Inc.; Jared Farr, Sagar Dubey, Ankur Aggarwal, Dan Oh – Celestial AI; Digvijay Raorane – Celestial AI/Marvell Technology, Inc.	***2. 9:50 AM - Reducing Wafer-to-Wafer Bonding Misalignment to Enable 140nm Pitch Hybrid Bonding*** Christopher Netzband, Andrew Tuchman, Joshua Greklek, Sayantan Das, Brittany Hedrick, Hirokazu Aizawa, Ilseok Son – TEL Technology Center, America, LLC; Shinichi Tan, Yuki Taniguchi, Nathan Ip – Tokyo Electron Ltd.; Atsushi Nagata, Angelique Raley – Tokyo Electron, Ltd.	***2. 9:50 AM - Crack-Free Through-Hole Drilling of 400 µm-Thick Aluminosilicate Glass by Direct Laser Processing*** Toshio Otsu, Tsubasa Endo, Hiroharu Tamaru, Yohei Kobayashi – University of Tokyo
3. 10:10 AM - V-Groove Based Edge Coupling Enabled by Optical Glass Coupler Attach for Co-Packaged Optics Zhou Yang, Fan Fan, Timothy Gosselin, Ryan Mcqueen, Pratyasha Mohapatra, Anita Dey, Anurag Tripathi, Shan Zhong, Bohan Shan, Jesus Nieto Pescador, Corey Logston, Nicholas Psaila – Intel Corporation	***3. 10:10 AM - Wafer-to-Wafer Hybrid Bonding Technology with 200nm Interconnect Pitch*** Stefaan Van Huylenbroeck, Lieve Bogaerts, Koen D'have, Soon Aik Chew, Hung-Chieh Tsai, Serena Iacovo, Sven Dewilde, Shuo Kang, Joeri De Vos, Zsolt Tokei, Eric Beyne – imec	***3. 10:10 AM - Development of Low-Modulus Primer "Cbla" to Prevent SeWaRe in Glass-Core Substrates*** Daichi Kobayashi, Marie Ohuchi, Satoshi Takayasu, Yuzuru Kobayashi, Masahiro Miyasaka, Kosuke Urashima, Tomohiko Kotake – Resonac Corporation
10:30 a.m. – 11:15 a.m. • Refreshment Break: Palazzo and Mediterranean Foyers		
4. 11:15 AM - Power Distribution Network (PDN) Design and Analysis for Multi-Stack 3D Heterogeneous Integrated High Bandwidth Memory (3D-HI-HBM) Module Jiwon Yoon, Haeseok Suh, Eunji Seo, Junghyun Lee, Hyunjun An, Youngsu Yoon, Chaemin Yang, Jaegeun Bae, Hyunseo Uhm, Joungho Kim – Korea Advanced Institute of Science and Technology	***4. 11:15 AM - Robust Wafer-to-Wafer Cu Direct Bonding Process for Multi-Stacked CMOS Directly Bonded to Array (CBA) Technology in Future 3D Flash Memory*** Masayoshi Tagami, Hiroyuki Ashidate, Mitsuhiko Noda, Ryo Tanaka, Mamoru Watanabe, Ryuta Mizumoto, Genki Sawada, Yoshiharu Ono, Tomoyuki Takeishi, Katsuyuki Sekine – KIOXIA Corporation	***4. 11:15 AM - Novel Photosensitive Material with Low Shrinkage and Low Dielectric Properties for High-Density RDL in Glass Packaging*** Ritsuya Kawasaki, Kazuya Nakashima – Sumitomo Bakelite Co., Ltd.; Yu-Chieh Lin, Hyunggyu Park, Kyoung-Sik Moon, Mohan Kathaperumal, Ching-Ping Wong – Georgia Institute of Technology
5. 11:35 AM - Thermal-Aware Power Integrity Analysis of Embedded Integrated Voltage Regulator (IVR) in Interposer for 2.5D High-Power HPC Hyunwoong Kim, Sungwook Moon, Jungil Son, Jinho Kim, Seungki Nam – Samsung Electronics Co., Ltd.	***5. 11:35 AM - Process Integration for 300-nm-Pitch Hybrid Bonding with SiCN: 50nm Bonding Overlay, Fine-Grain Cu Metallurgy, and Reliability Assessment*** Kai Ma, Nikolaos Bekiaris, Jingting Chen, Jing Xu, Huixiong Dai – Applied Materials, Inc.; Jakob Haimberger, David Goldberger, Gernot Probst, Thomas Uhrmann, Markus Wimplinger – EV Group	***5. 11:35 AM - Digital Lithography Patterning of Novel Dry Film Resists for High Aspect Ratio Cu Pillar Applications on 310×310mm2 Panel Substrates*** Ksenija Varga, Lisa Berger, Tobias Zenger – EV Group; Hajime Furutani, Masayuki Kishino – Asahi Kasei Corporation
6. 11:55 AM - Multi-physics Design Methodology for Enlarged Chiplets Interconnections in Advanced Packaging Yung-Sheng Lin, Chih-Yi Huang, Teck Chong Lee, Smith Chen, Po-Chih Pan, Fu-Chen Chu, Tsung-Tang Tsai, Chung-Hung Lai, Wei-Hong Lai, Chin-Li Kao, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***6. 11:55 AM - Synchrotron-Based Characterization of Cu/SiCN Pretreatment for Hybrid Bonding via Ozone/Ethylene Radical Activation*** Bungo Tanaka, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Soichiro Motoda, Tetsuya Nishiguchi, Yuma Okadome – MEIDEN NANOPROCESS INNOVATIONS, INC.	***6. 11:55 AM - Low-Warpage Multilayer RDL Technology Using Thin Dry Film Dielectric with Reduced Curing Shrinkage and Dry-Etched Ultrafine Via*** Yusuke Naka, Tadahiko Hanada – Taiyo Ink Mfg. Co., Ltd.; Osamu Okada, Yoichiro Kurita – Institute of Science Tokyo; Takafumi Fukushima, Hashimoto Hiroyuki – Tohoku University; Yasuhiro Morikawa, Fumito Ootake – ULVAC, Inc.; Masahiro Sawa, Yasuhiro Ogo – JCU Corporation
7. 12:15 PM - Topology-Driven Organic Interposer Design for RDL Layer Reduction in Automotive UCIe-A 2.5D Chiplet Packages Shuuichi Kariyazaki, Hiroki Shibuya, Tatsuaki Tsukuda – Renesas Electronics Corporation	***7. 12:15 PM - Nanostructured Porous Cu for Ultralow-Temperature Direct Bonding*** Su-Ching Hsiao, Wei-Lan Chiu, Shih-cheng Yu, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo, Shih-Chieh Chang, Shih-Chieh Chang – Industrial Technology Research Institute	***7. 12:15 PM - Inkjet-Printed Photo-Imageable Dielectric for Large-Area Uniform Coating and High-Resolution Patterning in Advanced Packaging*** Wanhyuk Chang, Youngho Suh, Keejoon Kim, Beomsoo Kim, Myungjoo Park – LG Electronics; Hyunsoon Lim, Wooram Oh, Minyoung Lim – LG Chem

PROGRAM SESSIONS: FRIDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 28: Beyond Silicon: Innovation in Glass Substrates and Panel Level Packaging

Committee:
Assembly & Manufacturing Technology

Mediterranean 5, JW Marriott

Session Co-Chairs
Timo Henttonen – Microsoft Corporation
Email: timo.henttonen@microsoft.com
Venkata Mokkapati – AT&S AG
Email: v.mokkapati@ats.net

1. 9:30 AM - RDL Interposer Scheme Optimization for Electrical Performance with Varied RDL and Dielectric Layer Thicknesses
Chia-Hsiang Lin, Kathy Yan, Chien-Hsun Lee, Eric Chen, Yu-Wei Chen, Rachel Lu – Taiwan Semiconductor Manufacturing Company, Ltd.

2. 9:50 AM - First Demonstration of Stitching-Free Exposure Over an Ultra-Large 18-Reticle Area With High-Resolution 1.5µm Line/Space on Glass Substrates
Naoya Sohara, Toshimitsu Arai, Ryotaro Takahashi, Naoki Gotou, Hirosuke Takamatsu – USHIO

3. 10:10 AM - Demonstration of a 200×200 mm2 Glass Substrate for Large Area Packages
Jaewon Lee, Hyunggyu Park, Seungwoo Cha, Jinsun Yoo, Tushar Krishna, Muhannad Bakir – Georgia Institute of Technology; Srujan Penta – Georgia Institute of Technology/Marvell Technology, Inc.

Session 29: Innovation in Metallization, Alignment, Additive Manufacturing, and Low Temperature Interconnection

Committee:
Emerging Technologies

Mediterranean 1-3, JW Marriott

Session Co-Chairs
Benson Chan – Binghamton University
Email: chanb@binghamton.edu
Chukwudi Okoro – Corning Research and Development Corp. / Email: okoroc@corning.com

1. 9:30 AM - Game-Changing Nanosolder Technology: Self-Assembling Adhesives for Sub-10 µm Ultra-Fine Interconnects
Jin Woo Huh, Seol Kim, Changhoon Sim, Kyungsub Lee – Nopion Co., Ltd.; Tae-Wan Kim, Hyeong-Bin Park, Hak-Sung Kim – Hanyang University

2. 9:50 AM - Additively Manufactured Foldable Interconnects for 4D/Morphing Origami-Inspired mm-Wave Arrays
Hani Al Jamal, Manos M. Tentzeris – Georgia Institute of Technology

3. 10:10 AM - Rapid Additive Manufacturing of Multi-Layered Redistribution Layers and Interconnects Enabled by Hybrid Metal-Polymer Resin
Natalya K Crawford, Jaden Wang, Daria Holoman, Jarrett Bealer, Seungjun Lee, James Garcia, Zachariah Page, Michael Cullinan – The University of Texas at Austin

Session 30: Thermal Management and Cooling Simulation

Committee: Thermal/Mechanical Simulation & Characterization

Mediterranean 6-8, JW Marriott

Session Co-Chairs
Yong Liu – ON Semiconductor
Email: Yong.Liu@onsemi.com
Patrick McCluskey – University of Maryland, College Park
Email: mcclupa@umd.edu

1. 9:30 AM - Mitigating the Thermal Bottleneck in Advanced BEOL Interconnects
Xinyue Chang – imec/KU Leuven; Herman Oprins, Melina Lofrano, Bjorn Vermeersch, Zsolt Tokei, Seongho Park, Ingrid De Wolf – imec

2. 9:50 AM - Multiscale Thermal Simulator Development for High Resolution Hot Spot Analysis
Hiroyuki Ryoson – Dexerials Corporation; Shinji Sugatani, Takayuki Ohba – Institute of Science Tokyo

3. 10:10 AM - Experimental Characterization of Thermal Transport in Cu/Sn–Diamond Microbumps
Keyu Wang, Zhengwei Chen, Devang Tavkari, Jie Li, Noah Opendo, Amy M. Marconnet – Purdue University; Shusmitha Kyatam, Miguel A. Neto – University of Aveiro; Joana-Catarina Mendes – Institute of Telecommunications; Tiwei Wei – University of California, Los Angeles

10:30 a.m. – 11:15 a.m. • Refreshment Break: Palazzo and Mediterranean Foyers

4. 11:15 AM - Technical Study of RDL in Advanced Package Using Ultra-Low Df Film-Type Photo Imageable Dielectric
Keigo Yamaguchi, Yuta Yamakawa, Megumi Tanaka, Masayuki Miura, Daisuke Ando, Naoki Sato, Takuya Komine, Eiichi Hayashi, Takashi Kariya – Samsung Japan Corporation

5. 11:35 AM - Dry-Film-Only Process for Panel-Level 2.xD Packaging Enabling 2/2-µm Line/Space RDL and 5-µm Microvias
Ryo Kikuta, Masashi Minami, Ryosuke Kimura, Sachiko Matsushita, Takeshi Yamada, Masahiko Suzuki, Sadaaki Katoh – Resonac Corporation

6. 11:55 AM - Tether-Free Micro-Transfer-Printing of Si-Based Micro-Inductors: Demonstration of on-Glass and in-Silicon Integration for PowerSoC Applications
Amit Tanwar, Muhammet Genc, Liang Ye, Rayan Bajwa, Somnath Pal, Iurii Efimenkov, Ranajit Sai, Cian O'Mathuna, Brian Corbett – Tyndall National Institute; Sambuddha Khan – Tyndall National Institute/University College Cork

7. 12:15 PM - Advanced Manufacturing Solutions for Large Form Factor Patch on Interposer (PoINT) Scaling
Andrew Carlson, Qichang Wang, Khalid Abdelaziz, Fatemeh Rahimi, Tingting Gao, Xiao Lu – Intel Corporation

4. 11:15 AM - High-Precision Wafer-Level Bonding in Thin-3D: A Moiré Pattern and Deep-Learning Alignment Approach
Chen-Chia Chang, Shie-Ping Chang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; TingRay Chung – Horace Greeley High School; Nien-Chih Lin, Po-Jung Sung, Chih-Chao Yang – Taiwan Semiconductor Research Institute

5. 11:35 AM - Metallization Challenges: Conformable Deposition for Super High-Aspect Ratio (> 100) Fine TGV and Cu Pillar Embedment for 1-mm-Deep Fat TGV
Chang Liu, Jiayi Shen, Bungo Tanaka, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Kiyoharu Mori – NICHe; Hidenori Miyauchi – Micro Technology Co., Ltd.

6. 11:55 AM - Glass-Stacked Interposers with Microdispensed Silver Nanopaste for Low-Temperature 3D Interconnection
Sam LeBlanc – nScrypt; Bryce Gray, Kenneth Church – Sciperio; Josue Fuentes, Jason Benoit – Sciperio, Inc.; Lance Sookdeo – Sciperio, inc.; Eduardo Rojas – Embry-Riddle Aeronautical University

7. 12:15 PM - Advancing Sustainable Die-attach Technologies with Filled Bio-Sourced Epoxy Resin Systems
Frederic A. Banville, Saria Berger, Cloe Druillole, David Danovitch, Serge Ecoffey – University of Sherbrooke; Catherine Marsan-Loyer – Centre de Collaboration MiQroInnovation (C2MI); Josée Labrecque, David Gendron – Kemitek; Benjamin Busseniers, Katherine Pilger, Valerie Oberson – IBM Canada, Ltd.

6. 11:55 AM - High-Fidelity Package-Level Conjugate Thermal-Flow Simulation for a Memory-on-Logic 3D System with Embedded Liquid-Cooling
Yujui Lin, Hongchi Liu, Luke Min, Mehdi Asheghi, Kenneth Goodson – Stanford University; Walker Turner, John Wilson, Tahir Cader, C. Thomas Gray – NVIDIA

7. 12:15 PM - Identification of Local Dryout Signatures in Two-Phase Microchannel Heat Sinks Using a Multi-Chip Module Thermal Test Vehicle
Rishav Roy, Yang Liu, Sarwesh Parbat, David J. Apigo, Manohar Bongarala, Syed Faisal, Todd Salamon, Mark Cappuzzo, Ting-Chen Hu, Rose Kopf, Ed Sutter, Nagesh Basavanhally, Alaric Tate, Bob Farah, Rick Papazian, Mark Earnshaw – Nokia Bell Labs

PROGRAM SESSIONS: FRIDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 31: 3D Integration, TSV, and Hybrid Bonding Innovations	Session 32: Solder and Through Via Interconnections: Material & Process Innovations	Session 33: Emerging Materials and Interconnect Technologies for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Palazzo A-C, JW Marriott	**Palazzo D, JW Marriott**	**Mediterranean 4, JW Marriott**
Session Co-Chairs **Lihong Cao – Advanced Semiconductor Engineering, Inc.** **Email: lihong.cao@aseus.com** **Peng Su – Hewlett Packard Enterprise** **Email: peng.su1@hpe.com**	**Session Co-Chairs** **Yoshihisa Kagawa – Sony Semiconductor Solutions** **Email: Yoshihisa.Kagawa@sony.com** **Jean-Charles Souriau – CEA-LETI** **Email: jcsouriau@cea.fr**	**Session Co-Chairs** **Fumihiro Inoue – Yokohama National University** **Email: inoue-fumihiro-ty@ynu.ac.jp** **Zhangming Zhou – IC Packaging Agent Inc.** **Email: founders@icpackagent.com**
1. 2:00 PM - Die-To-Wafer Hybrid Bonding Technology Down to 1 µm Pitch for Multi-Die Stacking Integration Melissa Najem, Agathe Lerat, Carine Ladner, Loic Sanchez, Julien Diaz, Renan Bouis, Jérôme Dechamp, Antonio Roman, Myriam Assous, Stéphane Nicolas – CEA-LETI; Damien Saint Patrice, Lilian Masarotto – CEA-LETI, Univ. Grenoble Alpes	***1. 2:00 PM - Fluxless Thermo-Compression Bonding of 4X Reticle Die Stack*** Kartik Srinivasan, Mine Kaya, Danis Nugroho, Nicholas Cool, Niranjan Parab, Karthik Visvanathan, Shan Zhong – Intel Corporation	***1. 2:00 PM - Optical RDL Interposer Technology Using Polymeric Hybrid Bonding and Waveguide for Integrated CPO*** Toshihiko Katayama, Kazuki Inoue, Kyohei Hayashi, Motoya Kaneta, Yuma Tanaka, Ryota Kinoshita – Sumitomo Bakelite Co., Ltd.; Takafumi Fukushima – Tohoku University
2. 2:20 PM - Enabling Scalable Die-to-Wafer Hybrid Bonding Through Die Distortion Correction and Grid Measurement Alex Hsu, Etienne De Poortere – ASML; Imene Jadli, Anne Jourdain, Samuel Suhard, Andy Miller, Koen Kennes, Victor Manuel Blanco Carballo, Amir-Hossein Tamaddon, Eric Beyne – imec	***2. 2:20 PM - Simplified Fluxless Bonding via Ultraviolet Activation: Enabling High-Reliability Fine-Pitch Interconnections*** You-Gwon Kim, Dong-Hoon Yoo, Hyeong-Bin Park, Seungchul Shin, Hak-Sung Kim – Hanyang University; Dongsuk Kang – Hanwha Semitech Co.	***2. 2:20 PM - Multi-Mode Polymer Waveguides for Co-Packaged Optics*** Ross Johnson, Yaming Jiang, Rui Zhang, Michael Gallagher – Qnity Electronics, Inc.; James Ryley, Barbara Roeske, Henry Cain, Nancy Tassi, John Allen, Zhou Lu, Elizabeth Brundage, Masaki Kondoh – DuPont Electronics and Imaging
3. 2:40 PM - Reworkable Die-to-Wafer Hybrid Bonding Process Rajan Gangadharan, Dominik Suwito, Thomas Workman, Cyprian Uzoh, Justin Chen, Pawel Mrozek, Arianna Avellan, Suhail Sadiq, Laura Mirkarimi – Adeia	***3. 2:40 PM - Fluxless TCB With in-Situ Atmospheric Pressure Plasma Surface Treatment Enabling 25-Micron Pitch Solder Micro-Bumps for 3D Integration*** Mohammed Alhendi, Luke Darling, Roy Yu, Katsuyuki Sakuma, Neng Liu – IBM Research; Ming Li, Zetao Ma, Kai Ming Yeung, Le Cheng – ASMPT	***3. 2:40 PM - Layer Transfer of Epitaxial Ru by Metal-Metal Bonding: Towards Single-Crystal Interconnects*** Christoph Adelmann, Francois Chancerel, Jean-Philippe Soulié, Steven Brems, Zsolt Tokei, Seongho Park – imec; Peter Kerepesi, Michael Dornetshumer, Florian Medl, Tobias Wernicke, Christoph Floetgen, Markus Wimplinger – EV Group
3:00 p.m. – 3:45 p.m. • Refreshment Break: Palazzo & Mediterranean Foyers		
4. 3:45 PM - Enabling Beyond-16-Layer 3D Stacking with Ultra-Thin Die Hybrid Bonding with Integrated Bonder Guan Huei See, Shin-Puu Jeng, Arvind Sundarrajan, Loke Yuen Wong, Patrick Lim, Xiaodong Chen, Santosh Kumar Rath, Xing Zhao, Prayudi Lianto, Ashok Muthukumaran, Michael Chudzik – Applied Materials, Inc.	***4. 3:45 PM - Processing and Cold Testing of Superconducting and Thermal Conducting TSVs*** Qian Yang, Jaber Derakhshandeh, Anish Dangol, Vadiraj Rao, Anne Jourdain, Geraldine Jamieson, Karl Ceulemans, Rami Chukka, Koen Kennes – imec	***4. 3:45 PM - Reflectivity-Tunable Localized Epitaxy for Multi-Tier Monolithic 3D ICs*** Ching-Lin Chen, Yu-Chun Chen, Yu-Ming Pan, Chiao-Yen Wang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chih-Chao Yang – Taiwan Semiconductor Research Institute; Chang-Hong Shen – National Tsing Hua University; Chenming Hu – University of California, Berkeley
5. 4:05 PM - Low Distortion Fusion Bonding Using Pneumatically Warped Wafers Utkarsh Jain, Koen D'have, Damien Leech, Serena Iacovo, Koen Kennes, Steven Brems, Eric Beyne – imec; Philipp Schmidt, Philippe Muller, Dennis Bumueller, Thomas Schmidt – SUSS MicroTec GmbH	***5. 4:05 PM - BBCube 2.5D: A Bumpless 2.5D Integration Technology Enabling High-Density Inter-Chiplet Interconnection Using Waffle-Wafer and Via-Last TSVs*** Norio Chujo, Shinji Sugatani, Koji Sakui, Masao Taguchi, Hiroyuki Ryoson, Takayuki Ohba – Institute of Science Tokyo	***5. 4:05 PM - Siloxane Elastomer-Based Zero-CTE Prepreg Substrates for Foldable FPCB and Stress-free Advanced Semiconductor Packaging*** Hyungshin Kweon, SungHun Park, Byung Jo Um, Seung-Mo Kang, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology
6. 4:25 PM - Wafer Bonder and Lithography Co-Optimization for Sub-5nm Post-Bonding Overlay in Backside Power Delivery Architectures Andrew Tuchman, Christopher Netzband, Sheldon Meyers, Sayantan Das, Ilseok Son – TEL Technology Center, America, LLC; Leon van Dijk, Niyam Haque, Manav Tiyagi, Lieneke Kusters – ASML; Nathan Ip – Tokyo Electron Ltd.; Angelique Raley – Tokyo Electron, Ltd.	***6. 4:25 PM - TSV Stress Prediction via Machine Learning Based on EBSD Grain Microstructure*** Zhenliang Pan, Jaden Li, Tiwei Wei – University of California, Los Angeles; Jie Li, Shuhang Lyu – Purdue University; Rui Yan – Semiconductor Integration & Multiphysics Reliability Laboratory	***6. 4:25 PM - Characterization of Solderless Connection by Laser Welding and Its Application on Power Module*** Ming-Hung Chen, Yi-Chun Chou, Chun-Yi Cheng, Ren-Jieh Kao, Yun-I Yeh – Advanced Semiconductor Engineering, Inc.
7. 4:45 PM - Enabling Ultra Low Temperature Hybrid Bonding for D2W Scaling Veronica Strong, Jeff Bielefeld, Arijit Koley, Felipe Bedoya, Richard Vreeland, Michael Njuki, Siyan Dong, Haris Khan Niazi, Brandon Rawlings, Trianggono Widodo, Satyajit Walwadkar, Pilin Liu, Saurabh Chauhan, Farhad Daneshvar, Tushar Talukdar, Aleksandar Aleksov – Intel Corporation	***7. 4:45 PM - Chemically Tailored Cu-Electroplating and Contactless Isostatic Annealing of 1-mm-Thick Full Glass Wafer Cu Through-Glass-Vias*** Murugesan Mariappan, Hashimoto Hiroyuki, Takamichi Miyazaki, Takafumi Fukushima – Tohoku University; Kiyoharu Mori – T-Micro; Masahiro Sawa, Jinta Nampo – JCU Corporation	***7. 4:45 PM - Extreme High-Temperature Evaluation of Printed Platinum Materials for Aerospace Applications*** Abdullah Obeidat, Waleed Alshaibani, Erik Busse, Olya Noruz Shamsian, Stephen Gonya, Mark Poliks – Binghamton University; Masoud Mahjouri-Samani – NanoPrintek, Inc.; Felippe Pavinatto – GE Aerospace Research

PROGRAM SESSIONS: FRIDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 34: Optimizing Power Delivery, Thermal Management, and Metrology Solutions for Next-Generation Devices	Session 35: Reliability of Advanced Automotive, AI, and Interconnect Packaging Solutions	Session 36: Flexible Electronics and Thin-Assembly Warpage
Committee: Emerging Technologies	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Mediterranean 5, JW Marriott	**Mediterranean 1-3, JW Marriott**	**Mediterranean 6-8, JW Marriott**
Session Co-Chairs **Premachandran Chirayarikathuveedu – Menlo Microsystems** **Email: 319prem@gmail.com** **Tengfei Jiang – University of Central Florida** **Email: tengfei.jiang@ucf.edu**	**Session Co-Chairs** **Tz-Cheng Chiu – National Cheng Kung University** **Email: tcchiu@mail.ncku.edu.tw** **Richard (Shiguo) Rao – Marvell Technology, Inc.** **Email: richardrao@marvell.com**	**Session Co-Chairs** **Xuejun Fan – Lamar University** **Email: xuejun.fan@ieee.org** **Suresh K. Sitaraman – Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 2:00 PM - 3D Analysis of Hybrid Copper Bonding Through X-Ray Photon-Counting Nano-CT Imaging Till Dreier, Julius Hållstedt – Excillum AB; Darius Rückert – Voxray GmbH; Spyridon Gkoumas – DECTRIS Ltd.	***1. 2:00 PM - Understanding the Effect of Bismuth and Surface Finish on Thermo-mechanical Reliability of Flip-Chip BGA Solder Joints*** Varun Thukral, Eleni Tsepi, Lara Reboucas, Pieter Gommers, Sharan Kishore, Abdullah Fahim, C.S. Foong – NXP Semiconductor, Inc.	***1. 2:00 PM - Printing Path Optimization for Reliability Enhancement in Direct-Writing Flexible Circuits*** Yusen Nie, Luke McGinnis, Rui Chen – Eastern Michigan University
2. 2:20 PM - Microchannel-Embedded 3D-Printed Ceramic Substrates for Liquid-Cooled Power Module Packaging Haksoon Jung – Korea Advanced Institute of Science and Technology; Seongju Kim – Hanbat National University; Nahyeon Kim, Jimin Kwon – Ulsan National Institute of Science & Technology; Seungjun Chung – Korea University	***2. 2:20 PM - A Real-Time Resistance Monitoring Architecture for Prognostics and Health Management of Electronic Packages*** Shaheen Pouya, Mostafa Rahgouy, Jeffrey Suhling – Auburn University; Saad Hamasha – Binghamton University	***2. 2:20 PM - Multilayer Additive Circuit Process-Performance-Reliability Interactions in Dynamic Flexing of Wearable Applications*** Shriram Kulkarni, Yasitha Piyumal, Pradeep Lall – Auburn University
3. 2:40 PM - 3D Stacked GPU Architecture with Ultra-Thin 3D DRAM Dies and Voltage Regulators Embedded into Glass Substrate Pin-Jun Chen, Janak Sharda, Po-Kai Hsu, Muhannad Bakir, Shimeng Yu – Georgia Institute of Technology; Min Gyu Park, Sung Kyu Lim – University of Southern California	***3. 2:40 PM - Automotive Reliability of Micro–Cu Pillar Bumps for 2.5D Chiplet Integration*** Koichi Ando, Yoshiaki Yamada, Hideaki Tsuchiya, Hiroki Shibuya – Renesas Electronics Corporation	***3. 2:40 PM - Interfacial Fracture Characterization Using Wedge Testing of Electroless Plated Films on Additively Manufactured Conductive Polymers*** Joshua Corbin, Nicholas Ginga – University of Alabama in Huntsville; Sharmin Jahan, Nathan Lazarus – University of Delaware
3:00 p.m. – 3:45 p.m. • Refreshment Break: Palazzo & Mediterranean Foyers		
4. 3:45 PM - Efficiency Meets Fidelity: A Computational Paradigm for 3D X-Ray Imaging of HBM Packages Yang Yu, Jie Wang, Richard Chang, Ramanpreet Pahwa, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong, Eva Wai Leong Ching – Institute of Microelectronics A*STAR	***4. 3:45 PM - Enhanced Fault Localization Approach for Advanced Packaging with RDL Interconnection Nano-Defects*** Yi-Sheng Lin, Wiwy Wudjud, Cheng-Hsin Liu, Yu-Ting Lin, Yu-Jing Cheng, Chen-Chao Wang, Chih-Pin Hung, Lihong Cao – Advanced Semiconductor Engineering, Inc.	***4. 3:45 PM - Mechanical Simulation of Stretchable Sensors Conforming to Non-Euclidean Surfaces Using ANSYS LS-DYNA*** Sara Lieberman, Riadh Al-Haidari, Mark Poliks – Binghamton University; Felippe Pavinatto – GE Aerospace Research
5. 4:05 PM - Chemical Vapor Deposition (CVD) Diamond-filled Through Vias for Enhanced Vertical Heat Transport in 3D Heterogeneous Integration Ye Yang, Tiwei Wei – University of California, Los Angeles; Joana-Catarina Mendes, Gil Cabral – Institute of Telecommunications; Miguel A. Neto – University of Aveiro	***5. 4:05 PM - Dependence of Leakage Current Characteristics on Bonding Dielectrics in Fine-Pitch Hybrid Cu Bonding*** Sohye Cho, Hyeonmin Lee, Sungjae Choi, Young-Chang Joo – Seoul National University; Seokho Kim, Hojin Lee, Seunghun Lee – Samsung Electronics Co., Ltd.	***5. 4:05 PM - Warpage Prediction After Compression Molding Using Cure-Dependent Viscoelastic Properties*** Sukrut Prashant Phansalkar, Bongtae Han – University of Maryland
6. 4:25 PM - Wafer-Level Integrated 1200 V SiC MOSFET Package with Room-Temperature Wafer Bonding and Embedded Microfluidic Cooling Jiajing Nie, Jiuyang Tang, Hao Guan, Xinyue Wang, Guangyin Lei, Pan Liu – Fudan University; Tao Jiang, Junran Zhang – Research Institute of Fudan University in Ningbo; Guoqi Zhang – Delft University of Technology; Fengwen Mu – iSABers Group Co., Ltd	***6. 4:25 PM - Reliability Enhancement of FC-QFN Packages Using Cu Pillar Bump with PSPI and Buffer RDL for ULK*** Daehyun Kim, Kisu Joo, Heeseok Lee, Seung Wook Yoon – Samsung Electronics Co., Ltd.; Yongju Lee, Soomoon Park, Kwangho Lee – S.LSI Business, Samsung Electronics Co. Ltd	***6. 4:25 PM - Warpage Prediction of PCB in Multi-Laminating Processes Considering Cure Shrinkage and Anisotropic Visco-Elastic Properties of Prepreg Core*** Sanjay Kumar, Woong-Kyoo Yoo, Jaesung Kim, Chae-Young Ahn, Hak-Sung Kim – Hanyang University; Jinwoong Kim, Chan Hyuk Park – Doosan Corporation Electro-Materials BG
7. 4:45 PM - An Innovative Automated Tracing Method for Defect Identification in Advanced FOCoS-Bridge Package Cheng-Hsin Liu, Yi-Sheng Lin, Yu-Jen Chang, Yu-Jing Cheng, Yu-Ting Lin, Chen-Chao Wang, Chih-Pin Hung, Fan-Ju Hsiao – Advanced Semiconductor Engineering, Inc.	***7. 4:45 PM - Reliability Evaluation of 10-Second Cu/Polymer Hybrid Bonding for Next-Generation 3D Integration*** Tzu-Yu Chen, Yu-Lun Liu, Jia-Rui Lin, Yuan-Chiu Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Kazuaki Ebisawa, Makiko Irie, Ya-Chien Chuang, Hsiaowei Yeh, Satoshi Fujimura – Tokyo Ohka Kogyo Co., Ltd.	***7. 4:45 PM - Coupled Thermo-Mechanical-Chemical Simulation Framework for Warpage and Stress Analysis in PMC*** Kyeong-Bin Kim, Eun-Ho Lee – Sungkyunkwan University

INTERACTIVE PRESENTATIONS: WEDNESDAY, MAY 27, 10:00 A.M. - 12:00 P.M. AND 2:30 P.M. - 4:30 P.M.

Wednesday May 27
10:00 a.m. - 12:00 Noon

Session 37: Interactive Presentations - Thermo-Mechanical Stress and Reliability Analysis for Materials in Future Packaging

Committee: Interactive Presentations

Mediterranean Hallway, JW Marriott

Session Co-Chairs
Joshua Dillon
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Mark Poliks
Binghamton University
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1. - Experimental Studies of Assembly Material Creep Behaviors and The Impact to Package Warpage
Ziyin Lin, Yanbiao Chu, Mohammad Kabiri, Cih Cheng – Intel Corporation

2. - Layout-Driven FEM for Thermal and Thermo-Mechanical Analysis of MPGA and BGA Packages
Hyunggyun Noh, Woongkee Kim, Youngbong Kim, Sanggon Lee – Samsung Electronics Co., Ltd.

3. - In-Situ Observation and Modeling of Crack Velocity at Wafer-to-Wafer Bonding Interface
Kyeong-Bin Kim, Ju-Yong Shin, Eun-Ho Lee – Sungkyunkwan University; Haeri Kim, Wonyeop Jeong, YoungSu Yun, Jong Han Shin – SK hynix Inc.; Jiho Kang – Absolics Inc.

4. - A Novel and Cost-Effective Evaluation Strategy for Solder Joints Reliability for HPC and AI Applications
Peng Su, Omar Ahmed – Hewlett Packard Enterprise; Leif Hutchinson, Bernard Glasauer – Juniper Networks

5. - Methodology for Root Cause Analysis of 3D Multi-Chip Module Severely Damaged in Data Center Application
Charles Odegard, Alfred Griffin, Kasey Adams, James McElrath, Venkat Kalyanaraman, Anagha Kulkarni – Texas Instruments, Inc.

6. - Finite Element Analysis Based Methodology to Predict Electrical Parameter Shifts due to Mechanical Stress
Siva Gurrum, Hung-Yun Lin, Alexander Gamez, Li Jen Choi, Benjamin Amey, Ann Concannon – Texas Instruments, Inc.

7. - Thermal Behavior of Hybrid Bonding Interfaces in Advanced Packaging Technologies
Bijan Nili, Charles El Helou, Hadi Zandavi, Siyan Dong, Yi Shi, Tushar Talukdar, Lynn Chen, Xavier Brun, Aleksandar Aleksov – Intel Corporation; Aarom Schmidt – Fourier Scientific LLC

8. - FEA-Integrated 3PB and BOR Testing for Fracture Strength Characterization of Ultrathin Dies: Effects of Thickness, Surface Conditions, and Anisotropy
Jun-Seop Song, Sang-Il Kim, Gyu-Won Kim, Woong-Kyoo Yoo, Hak-Sung Kim – Hanyang University; Jong-Woon Yoo, Sang-Hoon Ko – SK hynix Inc.

9. - Simulation-Based Corrective Strategies for Warpage Behavior in Automotive Electronic Assemblies
Chih-Yang Weng, Shih-Wei Huang – WNC Corporation; Shen-Yu Yang, Chao-Chieh Chan – Wistron NeWeb Corporation; Chang-Chun Lee – National Tsing Hua University

10. - Stress Analysis of Cu-Cu Hybrid Bonding Interface Under Thermal Loading
Haozhong Wang – Harbin Institute of Technology; Binxu Ma, Peijiang Liu, Wanchun Tian, Xiaofeng Yang – China Electronic Product Reliability and Environmental Testing Research Institute; Hongtao Chen – Harbin Institute of Technology (Shenzhen)

11. - Thermal Characterization and Power Dissipation Enhancement of Hybrid-Bonded Chip Stack
Yong Han, Boon Long Lau, Gongyue Tang – Institute of Microelectronics A*STAR

12. - Orientation-Engineered AlN for Lateral Heat Spreading and Hotspot Management in 2.5D/3.5D ASICs on the Cloud AI Platform
Jun-Nan Liu, Tzu-Tai Chiu, Kuan Chung Fu, Wan-Yun Lee, Chih Huang Lai – National Tsing Hua University; Chao-Chih Chen, Wen-Pin Hsieh – Academia Sinica

13. - AI Head-Node Socket Interconnect Yield, Warpage, and Functionality
Steven Klein, Amit Abraham, Alexander Huettis, Taylor Rawlings, Eric Erike, Jacob Schichtel, Sugadh Bakare, Srinivasa Aravamudhan, Renn Chan Ooi, Prasanna Raghavan – Intel Corporation

14. - Liquid Metal Cooling for High-Power Electronics Driven by Magnetohydrodynamic Effect
Huicheng Feng, Bin He, Gongyue Tang, Xiaowu Zhang, Javen Tan – Institute of Microelectronics A*STAR

15. - A Holistic Study of Board Level Reliability of CoWoS-R Advanced Packaging on OCP Accelerator Modules
Sing-Da Jiang, Jing-An Huang, Chi-Shiang Chiou, Shih-Wei Liu, Tsunyen Wu, Ying-Ju Chen, Kathy Yan, Rick Lien, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.

16. - Controlling the Reaction Pathway to Tune Packaging Epoxy Properties
Polette Centellas, Ran Tao, Andrew Korovich, Alexander Landauer, Amanda Forster, Huong Giang Nguyen, Jan Obrzut, Christopher Soles – National Institute of Standards and Technology; Siena Iavarone-Garza – University of Maryland; Dante Ribeiro – Pennsylvania State University; Stian Romberg – University of Tennessee

17. - Influence of Copper Pad Surface Finish on Electromigration Performance of High-Reliability SAC-Based Hybrid Fine-Pitched BGA Solder Joints
Karthik Arun Deo, Junbo Yang, Yangyang Lai, Dalei Yang, Kewei Shou, Weichen Zhao, Yi Deng, Pengcheng Yin, Yuhan Gao, Seungbae Park – Binghamton University

18. - Demonstration of Two-Phase Jet Impingement Cooling with Phase Separation Membrane using Water on High-Power AI GPU
Yunchun Yang, Tiwei Wei – University of California, Los Angeles; Sidharth Rajeev, Harish Kumar Lattupalli, Srikanth Rangarajan – Binghamton University; Ketan Yogi – Purdue University; Bahgat Sammakia – State University of New York at Binghamton

19. - Enhancing In-Package Thermal Management of 3D V-NAND Flash Memory Using Under-Periphery Thermal Pins (UPTPs) and Materials-and-Structure Co-Design
Eun Pyo Hong, Jungsu Yoon, Ho Beom Han, Sang Won Yoon – Seoul National University; Suk-Kang Sung – Samsung Electronics Co., Ltd.

20. - Reliability Characteristics of Through Glass Vias With Polymer Liners
Meghna Narayanan, Muhannad Bakir, Mark Losego, Mohan Kathaperumal – Georgia Institute of Technology; Loic Constantin, Marvin Brent, Poulomi Mukherjee, Sarah Wozny – Applied Materials, Inc.

21. - A Thermodynamic Continuum Framework for Electromagnetic–Mechanical Dissipation in Superconducting Qubit Systems
Sung-Hyun Oh, Jin-Woong Cha – Korea Research Institute of Standards and Science; Yonuk Chong, Eun-Ho Lee – Sungkyunkwan University

22. - Experimental and Simulation-Based Assessment of Die Attach and Solder Mask Material Influence on Substrate Trace Cracking in BGA Packages
Chu-Chung Stephen Lee, Jasmine Lim, Ryan Zhang, HY Liu, Hazika Samsol Bahri, Sharan Kishore, Abdullah Fahim, Jetse De Witte, Tu-Anh Tran – NXP Semiconductor, Inc.

23. - Impact of Microstructure and Current Management on Electromigration Reliability in BGA Solder Joints for High-Performance Computing
Andrea Molina Moreno, Junyoung Bang, Miftahul Nabila, Kaitlyn Munoz, Tengfei Jiang – University of Central Florida; Nicholas Rudawski – University of Florida; Omar Ahmed, Peng Su – Hewlett Packard Enterprise; Leif Hutchinson, Valery Kugel, Bernard Glasauer – Juniper Networks

24. - Multiphysics Phase-Field Modeling of IMC Evolution and Reliability in Cu/Sn SLID Fine-Pitch Interconnects
Haohan Guo, Shubhra Bansal – Purdue University

25. - Assembly and Reliability Characterization of Glass-Cored Substrate Package for AI/HPC Applications
JoonYoung Choi, YoungJoo Choi – STATSChipPAC Korea; Nokibul Islam – STATS ChipPAC, Ltd.

26. - Rapid Prediction of Effective Orthotropic Elastic Properties for 2.5D Chiplet Packaging RDL
Dingjie Lu, Jun Liu, Wenzu Zhang, Richard Xian-Ke Gao, En-Xiao Liu, Sridhar Narayanaswamy – Institute of High Performance Computing A*STAR; Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR

27. - Effect of Bi Concentration on the Creep Behavior and Reliability of Mixed SAC-LTS Solder Joints
Souvik Chakraborty, Mahbub Alam Maruf, Golam Rakib Mazumder, Jeffrey Suhling, Pradeep Lall – Auburn University

28. - Modeling and Simulation of Se-Wa-Re Failure in Glass Core Substrates
Eduardo Barros De Moraes, Stanislav Sikulskyi, Robert Schaut – Corning, Inc.

Wednesday May 27
2:30 p.m. - 4:30 p.m.

Session 38: Interactive Presentations - Photonics, mmWave Applications, and Emerging Technologies

Committee: Interactive Presentations

Mediterranean Hallway, JW Marriott

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1. - Heterogeneous Integration of Compound Infrared Focal Plane Arrays (FPAs) and Silicon Read-Out Integrated Circuits (ROICs) Using Laser-Assisted Bonding at a 15µm-Pitch
Ga-Eun Lee, Hak-Sung Kim – Hanyang University; Young-Sung Eom, Gwang-Mun Choi, Jungho Shin, Ki-Seok Jang, Chanmi Lee, Jin-Hyuk Oh, Seong Cheol Kim, Mi-Ri Yoon, Kwang-Seong Choi, Jiho Joo – Electronics and Telecommunications Research Institute; Sang Jun Lee, Dayoung Kim – Korea Research Institute of Standards and Science; Jungwon Yoon – IRSpectra Co., Ltd.

2. - Design and Optimization of 2-mm Staggered RDL Interposer Channels for UCIe 3.0 up to 64 GT/s
Hong Seok Kim, Youngeun Na, Yeon Ji Shin, Soo Jeong Kim, Jinsik Kim, Jae-Sung Lim, Sang Yeul Yeum, Jayden Donghyun Kim – HANA Micron, Inc.; Woojin Lee – Swevenz Inc.

3. - System-Level Framework for Co-Optimizing Electromigration and Voltage Drop in High-Power Packages
Jungil Son, Sungwook Moon, Hyunwoong Kim, Seungki Nam – Samsung Electronics Co., Ltd.

4. - Channel-Adaptive Generative Learning for Diverse Equalizer Design Space Exploration in High-Speed Links
Junghyun Lee, Hyunjun An, Jiwon Yoon, Haeseok Suh, Junho Park, Youngsu Yoon, Byeongmok Kim, Jaegeun Bae, Inyoung Choi, Hyunseo Uhm, Eunji Seo, Joungho Kim – Korea Advanced Institute of Science and Technology

5. - A Fully Printed Flexible Electrochemical DNA Sensor with 3D Printed Microfluidics for SoP Lab-on-Chip Applications
Theodore Callis, Manos M. Tentzeris – Georgia Institute of Technology

6. - Damascene Fine Pitch RDL Process Development of 1.0µm CD for Line/Space using High-NA i-Line Scanner
Lili Wang, Natalie Roels, Emile Schockaert, Carine Gerets, Denis Dochain, Nancy Heylen, Murat Pak – imec; Kosuke Yamashita – Fujifilm Electronic Materials; Kazuki Tomota, Tomoki Matsuda – Fujifilm Corp.

7. - PALTO: Physics-Informed Active Learning for Tri-Gate FinFET Design Optimization for Vertical Power Delivery
Ayoub Sadeghi, Leonid Popryho, Inna Partin-Vaisband – University of Illinois

8. - Low-Loss Polymer Waveguides Based Architecture for Co-Packaged Optics
Aparnaa Iyer, Sai Saravanan Ambi Venkataramanan, Pragna Bhaskar, Ethan Shackelford, Janagama Goud, Ching-Ping Wong, Muhannad Bakir, Mohan Kathaperumal – Georgia Institute of Technology; Yusuke Uraoka, Maki Tanaka, Atsushi Yamaguchi, Hirotaka Akiyama – Panasonic Industry Co., Ltd.; Tomo Mugurma, Tom Shin – Panasonic Industrial Devices Sales Company of America

9. - Laser Assisted Transfer (LAT) of Coupon of III-V Epitaxial Layer on Silicon Photonics Devices
Takenori Fujiwara, Junpei Oniki, Yukari Jo, Daichi Miyazaki – Toray Industries, Inc.; Takumi Ikehara, Haruka Fujishige, Yuichiro Tsuda, Tatsuya Okada, Yoshiyuki Arai – Toray Engineering Co., Ltd.; James O'Callaghan, Peter O'Brien – Tyndall National Institute

10. - Real-Time Lock-in Thermography and X-Ray CT for Early Failure Detection in Large-Size Packages
Yuji Inui, Donchoru Kan, Masaki Takahashi, Motoo Aoyama, Sojiro Isomura, Nao Matsuo, Sadaaki Katoh – Resonac Corporation

11. - 3D-Printed Coaxial-Fed Patch Antenna-Embedded Substrates for 5G Antenna-In-Package Applications
Kyungsun Kim, Nahyeon Kim, Jimin Kwon – Ulsan National Institute of Science & Technology; Haksoon Jung, Yongwoo Lee – Korea Advanced Institute of Science and Technology; Yunsik Park – Korea Electronics Technology Institute

Wednesday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Exhibition Hall - Mediterranean Ballroom

12. - High-Bandwidth UCIe 2.0 Routing on Fine-Line Organic RDL with Enhanced Signal and Power Integrity for Scalable 64-Bit Multi-Chiplet Integration
Amit Kumar, Jitesh Shah, Nandakumar Ravi – Renesas Electronics Corporation

13. - Ultra-High Optical Power ELSFP Modules for CPO SiPh-Based Transceivers
Tetsuya Matsuyama, Kohei Umeta, Taketsugu Sawamura, Yuki Shiroishi, Hideyuki Nasu – Furukawa Electric Co., Ltd.

14. - IR-Drop Analysis of Power Delivery Networks in 3D Stacked Dies Using Face-to-Face and Face-to-Back Integration
Taehoon Kim – Samsung Electronics Co., Ltd.; Seungmin Woo, Madison Manley, Muhannad Bakir – Georgia Institute of Technology

15. - Monolithic Passive Low-Loss Fiber Coupling to Photonic Glass Core Substrates using Ion-Exchanged Waveguides and SLE-Fabricated V-Grooves
Maurice Haffner, Julian Schwietering, Ulrike Gasnesh – Fraunhofer IZM; Tom Chojne, Hashem Al-Shami – Technical University Berlin

16. - Electrical Design Guidance of Chiplet Interface Channels to Achieve 2634 GB/s/mm Die Edge Bandwidth
Jiwoon Moon, Jonghyeon Lee, Yuchul Jung, Yeji Kim, Youngwoo Kim – Sejong University; Kyungho Park – Korea Advanced Nano Fab Center

17. - Multi-Channel and Multi-Scale Optical Performance Enabling for a Detachable Edge Coupling Connector with Glass Coupler and Expanded Beam in CPO
Zhichao Zhang, Yalong Gu, Dekang Chen, Fan Fan, Feifei Cheng, Nicholas Psaila, Benjamin Duong, Kumar Abhishek Singh, Kemal Aygun, Ravi Mahajan – Intel Corporation

18. - Interface Enhancement Method for Silver-Sintered Flexible Strain Sensors Toward Improved Reliability and Sensitivity
Jiayu Ge, Letao Bian, Xinyue Wang, Pan Liu – Fudan University; Guoqi Zhang – Delft University of Technology

19. - Multi-Agent Reinforcement Learning Driven Package PDN Design Automation
Haran Manoharan, Chulsoon Hwang – Missouri University of Science and Technology

20. - Inverse Design for Ion-Exchanged Waveguides in Photonic Glass Core Substrates
Tom Chojne – Technical University Berlin; Victor Doroshenko, Boris Bergues, Marc Schartmann – OmegaLambdaTec; Julian Schwietering, Maurice Haffner, Ulrike Gasnesh – Fraunhofer IZM

21. - 2.5D and Vertical Integration for Real-time Co-Optimization of Voltage Regulation and Power Gating in HPC Systems
Salma Abdelzaher, Inna Partin-Vaisband – University of Illinois

22. - A Digital Image Correlation-Based Research Platform for Cure Shrinkage and Thermal Expansion Measurements on Epoxy Test Materials
Alexander Landauer – National Institute of Standards and Technology

23. - 3D Heterogeneous Integration Packaging of 5G RF Systems using Additive Electronics
Waleed Alshaibani, Abdullah Obeidat, Riadh Al-Haidari, Zhi Dou, Sara Lieberman, Shiwantha Gunathilake, Yoga Vyas Viswanathan, Stephen Gonya, Mark Poliks – Binghamton University; Jason Case, Joseph Iannotti, Felippe Pavinatto – GE Aerospace Research

24. - Optical Multi-Chip Interconnect Bridge (OMIB™) Interposer Demonstration to Enable High-Density Photonic Interconnects for High-Performance Computing Applications
Digvijay Raorane – Celestial AI/Marvell Technology, Inc.; Ankur Aggarwal – Celestial AI; Suresh Pothukuchi, Saket Chadda – Marvell Technology, Inc.

25. - Additively Manufactured Interdigitated Capacitor for High Temperature Applications
Erik Busse, Mousa Al-Zanina, Abdullah Obeidat, Emuobosan Enakerakpo, Waleed Alshaibani, Stephen Gonya, Mark Poliks – Binghamton University; Matthew Erdtmann, Adrian Pyke – Micro-Precision Technologies, Inc.

26. - A Switchable Longitudinal & Shear BLS Microscope for Comprehensive Modulus Imaging of Semiconductor Packaging Materials
Andrew Gayle, Ran Tao, Andrew Korovich, Polette Centellas, Yvonne Gerbig, Christopher Soles, Chris Michaels – National Institute of Standards and Technology; Sebastian Engmann – Theiss Research

27. - Ultra High Resolution Micro-LED Display Enablement at 300mm Using W2W Hybrid Bonding for AI and AR Applications
Raghav Sreenivasan, Jason Appell, Sangwoo Lim – Applied Materials, Inc.; Abhishek Bhat – Mojo Vision

28. - Low-Temperature Ultrathin Al_2O_3–SiO_2 Direct Bonding: Development and Optimization for Heterogeneous Integration of All-Optical Neuromorphic Chips
Albert Anthony, Sajay Gourikutty, Eva Wai Leong Ching, Ser Choong Chong – Institute of Microelectronics A*STAR

29. - Piezo-Magnetostrictive Transducer-Powered Wireless Implanted Sensors for Monitoring Hemodynamics
Veeru Jaiswal, Reshmi Banerjee, Ghaleb Al-Duhni, Mohammad Mohtasim Pial, Okeoma Arinze, Angelique Dominguez, Geraldine Pineda Andrade, Markondeya Raj Pulugurtha – Florida International University

30. - High-Efficiency 2 by 1 Antipodal Vivaldi Array on Ultra-thin PTFE for sub-6 GHz 5G: Cricut-Based Rapid Prototyping and Characterization
Mohamad El Yassine, Mutaz Shannag, Amanpreet Kaur – Oakland University

31. - Modeling and Optimization of 2-Stage Power Delivery Systems for High-Performance, Large-Area Packages
Jin Woong Kwak, Juyeop Baek, Muhannad Bakir, Visvesh Sathe – Georgia Institute of Technology

32. - BEM-Based Characterization of a D-Band On-Chip Patch Antenna Array
Jonatan Aronsson, Hans Schreckenbach – CEMWorks, Inc.; Iaroslav Shilinkov, Rob Maaskant – Chalmers University of Technology

33. - A Design-Space Exploration of Active Interposer Architectures for Long-Reach Signaling in Large-Area Advanced Packages
Taesoo Kim, Seungmin Woo, Muhannad Bakir – Georgia Institute of Technology; Srujan Penta – Georgia Institute of Technology/Marvell Technology, Inc.

34. - Language-Model Interfaces for SerDes Design Optimization: Comparing Prompt-Based and Agentic Approaches
Nirjhor Rouf, Soumyadeep Chatterjee, Sounak Dutta, Paul Franzon – North Carolina State University; Priyank Kashyap, Chris Cheng – Hewlett Packard Enterprise

Thursday May 28
10:00 a.m. - 12:00 Noon

Session 39: Interactive Presentations - Bonding Processes and Analysis in Next Generation Interconnects

Committee: Interactive Presentations

Mediterranean Hallway, JW Marriott

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Kristina Young
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1. - Trace-Element Effects in SAC Alloys: Mitigating HIP Defects in 5G/Automotive SoC SMT Assemblies
Tai-Yin Lin, Che-Kuan Chu, Chien-Min Lin, Zhe-Cheng Xu – Advanced Semiconductor Engineering, Inc.; Fa-Chuan Chen, Bo-Kuan Yeh, Hsin-Long Chen – MediaTek, Inc.

2. - Electromigration Resistance of Fine-Pitch Copper Lines: Comparison of Fine-Grained, Nanotwinned, and Standard Structures
Wei-Lan Chiu, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo, Shih-Chieh Chang – Industrial Technology Research Institute; Tao-Chi Liu, Yun-Yu Chen,, Elie Najjar – MacDermid Alpha

3. - Design of UCIe-A x64 Chiplets Integration for 16-36 GT/s Using Organic Interposer
Sheng-Fan Yang, Liang-Kai Chen, Wei-Chiao Wang, Chih-Chiang Hung, Wen-Yi Jian, Justin Hsieh, Ming-Hung Wu – Global Unichip Corporation

4. - Unit Level Die-to-die Attach with Low Thermal Input Thermo-Compression Bonding Towards Co-Packaged Optics Applications
Liban Jibril, Anita Dey, Jesus Nieto Pescador, Madhu Krishna Murthy, Sungmin Han, Niranjan Parab, Anurag Tripathi, Timothy Gosselin, Shan Zhong – Intel Corporation

5. - Novel Microbump Structure of Direct Solder Bumping on Seed Layer with Barrier Functionality (SoSBF)
Yusuke Tanaka, Keiichiro Hattori, Yuji Ohba, Aya Kurokawa, Toshiki Furutani, Takashi Kariya – Samsung Japan Corporation

6. - Fine-Pitch Cu/Polymer Hybrid Bonding Using Excimer Laser Damascene Process
Rikuo Kajiwara, Taichi Mikami, Yuzo Nakamura, Yutaka Hisamune, Satoshi Inada – Mitsui Chemicals, Inc.

7. - High Density RDL Scaling Using Digital Lithography Technology
Peng Suo, Chi-Ming Tsai, CC Chuang, Frederick Lie, YingChiao Wang, Jingxuan Wang, Guan Huei See, Arvind Sundarrajan, Jang Fung Chen, Shin-Puu Jeng – Applied Materials, Inc.

8. - Simultaneous Surface Reduction and Self-Passivation via Ar-CH_4 Plasma for Cu Hybrid Bonding
Hoogwan Lee, Byeongchan Go, Sarah Kim – Seoul National University of Science and Technology

9. - Influences of Bonding Misalignment on Copper Bulge Out in Wafer-to-Wafer Hybrid Bonding
Ryohei Kojima, Yuriko Yamano, Kengo Kotoo, Taichi Yamada, Naoki Komai, Suguru Saito, Yoshiya Hagimoto – Sony Semiconductor Solutions

10. - Laser-Assisted Bonding with h-BN Filled Non-Conductive Film for Fine-Pitch Semiconductor Packaging
Seong Cheol Kim, Jiho Joo, Young-Sung Eom, Gwang-Mun Choi, Jungho Shin, Ki-Seok Jang, Jin-Hyuk Oh, Chanmi Lee, Mi-Ri Yoon, Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Ga-Eun Lee – Hanyang University; Seung-Yoon Lee – Hanbat National University

11. - A Plasma-Activated, Water-Assisted Glass Bonding Technology for Advanced Heterogeneous Integration
Kuan Chung Fu, Jun-Nan Liu, Ying Li Chen, Chih Huang Lai – National Tsing Hua University; Shih-Lian Cheng, Jin-Sheng Wang – Unimicron Technology Corp.

12. - Methodology for Fine Line Strength in Fan-out Architectures
Yung-Sheng Lin, Ting Chun Lin, Min-Yan Tsai, Chung-Hung Lai, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

13. - Contamination-Controlled Pre-Assembly for High-Density Die-to-Wafer Hybrid Bonding
Fabiana Tanaka, Marie Sano, Kenta Hayama, Fumihiro Inoue – Yokohama National University; Jun Maeda, Tomoko Iwatsubo – LINTEC Corporation; Takashi Ouchi, Tsuyoshi Nakayama – JX Metals Trading Co., Ltd.; Shinji Ishitani, Naoya Hirota – Panasonic Holdings Corporation

14. - Hierarchical 3D-Vertically Staking with Multi-Layer and Stacking with Novel Structure by Transferrable Cu/Polymer Hybrid Bonding and 3D-Vertically Stacking For High Speed Digital Applications
Ou-Hsiang Lee, Yu-Ping Chan, Wei-Lan Chiu, Hsiang-Hung Chang, Chia-Wen Chiang, Jr-Wei Peng, Meng-Hsuan Chen, Liang-Cyuan Chang, Jia-Wen Fan, Da-Cheng Chien, Tsung-Yu OuYang, Chin-Hung Wang, Kuan-Neng Chen, Wei-Chung Lo, Shih-Chieh Chang – Industrial Technology Research Institute; Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chia-Hsin Lee, Chung-An Tan – Brewer Science, Inc.

15. - Integration and Characterization of Two Connection Schemes for Backside Power Delivery Network
Peng Zhao – Interuniversity Microelectronics Centre; Liesbeth Witters, Michele Stucchi, Vladimir Cherman, Melina Lofrano, Rami Chukka, Kevin Vandersmissen, Farid Sebaai, Bart Kenens, Joeri De Vos, Gerald Beyer, Zsolt Tokei, Eric Beyne – imec; Jan Willem Maes – ASM International N.V.

16. - Proposal of a Novel Design Method for Inter-Channel Crosstalk in High-Density Optical Interconnects Toward Massively Parallel Co-Packaged Optics
Ryosuke Matsumoto, Yuki Atsumi, Takayuki Kurosu, Fumi Nakamura, Siim Heinsalu, Akihiro Noriki, Satoshi Suda, Takeru Amano – National Institute of Advanced Industrial Science and Technology

17. - Bumpless Flip-Chip (BFC) as a Next-Generation Interconnect Technology for the AI Era
Rabindra Das, Daniel Oates, Alex Wynn, David Kim, Ravi Rastogi, Neel Parmar, Leonard Johnson, Steven Weber, Mollie Schwartz – MIT Lincoln Laboratory

18. - Thermally Functional Self-Activated Bonding for EUV-Compatible Backside Integration
Hayato Kitagawa, Taisuke Yamamoto, Fumihiro Inoue – Yokohama National University; Jenyu Lee, Shuntaro Machida, Kazuhiro Yuasa – KOKUSAI ELECTRIC CORPORATION; Shunsuke Teranishi – DISCO Corporation; Joichi Nishimura – SCREEN Holdings Co., Ltd.

19. - Electrodeposition of Aluminum on Direct Bonded Copper Substrates for Power Module Packaging
Thi Minh Anh Dao, Phuong Thao Hoang, Chun-Hao Chen – National Yang Ming Chiao Tung University; Ming-Si Jian, Peng-Wei Chu – National Tsing Hua University

Wednesday & Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Exhibition Hall - Mediterranean Ballroom

20. - Direct Transfer Bonding of Ultra-Thin Warped Chips for Advanced Heterogeneous 3DIC Integration with Fine-Pitch Direct/Hybrid Bonding
Ichiro Sano, Jun Kaneyasu – TAZMO Co., Ltd.; Shinya Takyu, Tomoka Kirihata – LINTEC Corporation; Takafumi Fukushima – Tohoku University; Yoichiro Kurita – Institute of Science Tokyo

21. - Through-Glass Via and Substrate Recess Technologies: Enabling Embedded Devices and Co Packaged Optics in Advanced Glass Packaging
Nils Anspach, Jannis Heinz, Daniel Dunker, Norbert Ambrosius, Simon Hirt, Roman Ostholt – LPKF Laser & Electronics SE

22. - Void-Free, Low-Resistance Through-Glass Vias Formed Using a Reduction-Gas-Generating Sinterable Cu Paste
Murugesan Mariappan, Hashimoto Hiroyuki, Takafumi Fukushima – Tohoku University; Kiyoharu Mori, Harumi Hosogoe – T-Micro; Hirokatsu Sakamoto, Akihiko Happoya – Daicel Corporation

23. - Time and Environment Characterization of Biodegradable Materials for Transient RF Systems
Denitsa Dimitrova, Pagnaa Nantogmah, J. Carson Meredith, Manos M. Tentzeris – Georgia Institute of Technology

24. - Impact of Cu Density on Via-to-Via Hybrid Bonding: Morphological and Electrical Characterizations
Agathe Lerat, Pablo Renaud, Christophe Dubarry, Margot Faure, Floriane Baudin, Sebastien Dominguez, Hadi Hijazi, Yorrick Exbrayat, Frank Fournel – CEA-LETI

25. - A Low-Cost 2.5D Photonic Silicon Interposer Assembly Process for HPC Applications
Digvijay Raorane – Celestial AI/Marvell Technology, Inc.; Suresh Pothukuchi, Saket Chadda, Joy Zhan – Marvell Technology, Inc.; Ankur Aggarwal, Sagar Dubey, Dan Oh – Celestial AI

26. - Exploring Cu-Cu Hybrid Bonding Failure Mechanisms under Current Stress via 3D Focused Ion Beam Tomography
Sari Al Zerey – State University of New York at Binghamton; Junghyun Cho – Binghamton University; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research

27. - An Evaluation of Hybrid Bonding of Cu/SiO2 Using Vacuum Ultraviolet Light Under Redox Gases
Shinichi Endo, Wu Kejun, Kengo Nishio, Akihiro Shimamoto, Akihiro Shimizu – Ushio, Inc.

28. - Novel O_2/H_2 Plasma Treatment for Cu Oxide Removal and Dielectric Activation in Hybrid Bonding
Kazutaka Noda, Atsushi Nagata, Norifumi Kohama, Yoshihiro Kondo – Tokyo Electron, Ltd.; Christopher Netzband, Andrew Tuchman, Ilseok Son – TEL Technology Center, America, LLC

29. - Fine Pitch Thermally Resistive Superconducting 3D Interconnects for Quantum Systems
Pablo Renaud, Candice Thomas, Meriem Guergour, Charles Bon-Mardion, Hadi Hijazi, Laurent Truong, Richard Souil, François Aussenac, Jean Charbonnier – CEA-LETI; Nathan Portatiu-Cambusset – University of Technology of Troyes; Edouard Deschaseaux – CEA-LETI/Grenoble Alps University

30. - Comprehensive Characterization of Surface Activation for Chip-to-Wafer Hybrid Bonding in 3D Flash Memory
Jingqi Zhang, Bungo Tanaka, Murugesan Mariappan, Chang Liu, Tetsu Tanaka, Takafumi Fukushima – Tohoku University

31. - High-Throughput Metrology of CMP-Treated Surface Topography Using Fizeau Interferometry for Hybrid Bonding
Ryoichi Sato, Hashimoto Hiroyuki, Bungo Tanaka, Kota Sasaki, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Kohei Nishiyama, Yuki Fujii – Kobe Steel

32. - Interfacial Analysis of Hybrid Bonding Using Water Surface Tension-Driven Self-Assembly for HBM
Kota Sasaki, Bungo Tanaka, Ryoichi Sato, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Hayato Hishinuma – Yamaha Robotics Co., Ltd.

33. - Advanced Metrology for Heterogeneous Chiplet Integration with High-Speed 100% Bond Overlay Measurement
Tan Nguyen, Bhaskar Jyoti Krishnatreya, Siyan Dong, Madhav Gautam – Intel Corporation; Frank Boegelsack, Thomas Uhrmann, Elisabeth Brandl – EV Group

34. - Understanding Scaling and Temperature Limits in Cu Bulge-Out Mechanism for Hybrid Wafer-to-Wafer Bonding
Joke De Messemaeker, Boyao Zhang, Aleksandar Radisic, Zaid El-Mekki, Sven Dewilde, Stefaan Van Huylenbroeck, Koen Van Sever, Herbert Struyf, Joeri De Vos, Gerald Beyer, Eric Beyne, Zsolt Tokei – imec

35. - Die-Shift of Sub-20 µm Thickness Embedded Die in Glass-Core Package Redistribution Layers
Hyunggyu Park, Jaewon Lee, Muhannad Bakir – Georgia Institute of Technology

36. - Implanted Nanotwin Boundaries Enable Stable Hybrid-Bondable Copper Metallization
Abdelhamid El-Sawy, Pingping Ye, Jianwen Han, Stephan Braye, Harhsul Khanna, David Doughty, Veronica Lambert, Adam Letize, Kyle Whitten, Thomas Richardson, Elie Najjar – MacDermid Alpha

37. - A Compact Optical Engine With Novel 2D Thin Film Micro-VCSEL Array Architecture for CPO and LPO Application at 3.2 Tbps
Murphy Lee, Yuk-Tong Cheng, Tzu-Hung Lin, Wang Shi Yu, Chih-Hsiang Ho, Jr-Hau He – Rayleigh Vision Intelligence

38. - Introduction to High-Speed LVDS Twisted Pair Transmission Across PCB and Chiplet RDL Interfaces
Mayukh Nandy, James Doyle, Simon Mayberry, Siyang Liu, Anuj Sarode, Hongbin Yu – Arizona State University

Thursday May 28
2:30 p.m. - 4:30 p.m.

Session 40: Interactive Presentations - Materials, Manufacturing, and Assembly Techniques in Advanced Packaging Solutions

Committee: Interactive Presentations

Mediterranean Hallway, JW Marriott

Session Co-Chairs
Karan Bhangaonkar
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Pavel Roy Paladhi
NVIDIA
Email: rpaladhi01@gmail.com

1. - Direct Chip Bonding on Thin Glass Substrates for W-Band Applications Using Aerosol Jet Printing
Ethan Kepros, Bhargav Avireni, Premjeet Chahal – Michigan State University

2. - Low-Temperature Sintering and Bonding Performance of Gradient Oxidized Copper Nanoparticles
Tetsu Yonezawa – Hokkaido University

3. - Reliability Assessment of Liquid Metal Alloy Thermal Interface Materials in Fan-out Embedded Bridge (FO-EB) Packages
Wen-Yu Teng, Jyun-De Jhan, Dai-Fei Li, Shane Lin, Yung-Ta Lin, Andrew Kang, Don Son Jiang – Siliconware Precision Industries Co., Ltd.

4. - Electroless Noble Metal Passivation Enabling Oxidation-Free Cu Bonding through a Comparative Study of Au, Pd and Ru for Low-Temperature Hybrid Bonding Applications
Byeongchan Go, Hoogwan Lee, Sarah Kim – Seoul National University of Science and Technology; Keiyu Komamura, Takanori Kishida – EEJA Ltd.

5. - Metal–Polymer Hybrid Bonding for Contamination Mitigation in Polymer-Based Semiconductor Packaging
Dong Yun Sung, Jiyun Lee, Seoyeon Choi, Seoul Ki Hong – Seoul National University of Science and Technology

6. - Challenges and Solutions for Package-level Encapsulation of Ultra-Large Die Complexes
Yang Guo, Ziyin Lin, John Decker, James Breyfogle, Eylul Simsek, Hsin-yu Li, Yiqun Bai, Chengzi Huang, Wen Yang – Intel Corporation

7. - Evaluating Large Body Packaging Performance of Glass Core Substrates for AI and HPC Applications
Jongmin Park, DongSu Ryu, GookJin Jung, JaeMin Bae, YoungSeob Shin, YoungHo Oh, YeonKi Jeong – Amkor Technology, Inc.

8. - Current-Assisted Cu–Cu Bonding at Low Temperature: Process Window and Mechanism
Byungkwan Kwak, Jinmyeong Seo, Haneul Han, Sanghwa Yoon, Bongyoung Yoo – Hanyang University

9. - Correlation of Copper Pattern Surface Morphology and Insertion Loss for High-Speed Communication
Yasutaka Amitani, Shunsuke Arima, Keisuke Joko – MEC COMPANY LTD.

10. - Microstructure for Zero Void by Control of Cu2+ in Metallization for TGV of Glass Core Substrate
Sung-Bin Kim, Jae-Hyung Kim, Myung-Jun Kim, Kyeong-Seop Park – AnyCasting Co., Ltd.; So-Yeon Lee – Inha University

11. - Robust LCP Bonding for Medical Implants: Impact of Surface Roughness and Reactive Accelerated Aging
Ladan Jiracek-Sapieha, Ryan Wilkerson, Jack Judy – University of Florida

12. - A Study of Lithography Process Comparison for Co-Package Optics
Hironobu Fujishima, Koya Mita, Makoto Ogusu, Hiromi Suda, Ken-Ichiro Mori – Canon, Inc.

13. - Collective Die-to-Wafer Bonding of Si Dies and 4-Inch Polycrystalline Diamond Wafer with Ultralow Thermal Boundary Resistance and High Bonding Quality
Shuchao Bao, Ningning Xu, Yi Zhong, Daquan Yu – Xiamen University; Ran He – Huawei Technologies Co., Ltd.

14. - Overcoming BEOL Thermal Constraints Via Low-Temperature Cu–Cu and Cu–Oxide Bonding of a-Ga2O3 UV-C Photodetectors
Jiyun Lee, Dong Yun Sung, Seoyeon Choi, Seoul Ki Hong – Seoul National University of Science and Technology

15. - Scalable Construction of 3D Graphene Frameworks via Combined Foaming and Freeze-Drying in High-Performance Epoxy Nanocomposites for Advanced Packaging
Zihao Lin, Sung-Ting Chen, Jung Yi Chen, Kyoung-Sik Moon, Ching-Ping Wong – Georgia Institute of Technology

16. - A Low Profile DC-DC Converter on the Inductor-Embedded-Substrate as an Integrated Package Solution (L-type-iPaS) Substrate for Next Vertical Power Delivery
Nobuyoshi Adachi, Yoshimitsu Ushimi, Kenji Nishiyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.; Manabu Yano – Murata Electronics North America

17. - A Novel Capacitor Embedded Substrate Based on Capacitor-Type integrated Package Solution (iPaS) for Vertical Power Delivery in Advanced Semiconductor Packaging
Akitomo Takahashi, Shuhei Yamada, Yuuki Yabuhara, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.; Manabu Yano – Murata Electronics North America

18. - Technology for Sequential Integration of HPA and LNA on Stacked GaN Layers for 3D Packaging of Next Gen Miniaturized Power RF Transceiver Front Ends
Kai Zoschke, Hermann Oppermann – Fraunhofer IZM; Antonis Stavrinidis, Nikolaos Makris – Foundation for Research & Technology Hellas; Philomela Komninou, Nikoletta Florini – Aristotle University of Thessaloniki; Paolo Fioravanti, Errikos Lourandakis – Circuits Integrated Hellas; Bruno Heusdens, Adrien Hertay – Taipro Engineering; Mohamad Abo Ras – Nanotest; Afshin Ziaei – Thales Research & Technology

19. - Radar System-in-Package with Integrated Antennas Based on Fan-out Wafer-Level Packaging RDL-First Integration
Arnaud Garnier, Laetitia Castagne, Rémi Franiatte, Daniel Mermin, Alexandre Siligaris, Mykhailo Zarudniev, Maciej Smierzchalski, Francesco Foglia Manzillo – Grenoble Alps University/CEA-LETI; Jean-Charles Souriau, Perceval Coudrain – CEA-LETI

20. - Sub-Millimeter GaN-on-Si Dielet Fabrication in Advanced Packaging Substrates Using Femtosecond Laser for 3D Heterogeneous Integration Applications
Pradyot Yadav, Ulrich Rohde, Ruonan Han, Tomás Palacios – Massachusetts Institute of Technology; Xingchen Li, Danish Baig, Wanshu Zeng, Muhannad Bakir – Georgia Institute of Technology; Juan Pastrana-Gonzalez, Ahmad Islam – Air Force Research Laboratory; Madhavan Swaminathan – Pennsylvania State University

21. - Room-Temperature Reduction of Molybdenum Oxide via 172-nm Vacuum Ultraviolet Irradiation in an H2/N2 Atmosphere with H2O Vapor
Akihiro Shimizu, Shinichi Endo – Ushio, Inc.

22. - High-Performance Low-Temperature SiCN for Hybrid Bonding in Advanced 3D Integration
Guanyu Song, Ming Li, Yuchen Hou, Hu Kang, Chunhai Ji – Lam Research Corporation

23. - Silicon Bridges for Chiplets Heterogeneous Integration with Microbumps
John H. Lau, Ning Liu, Tzyy-Jang Tseng – Unimicron Technology Corp.

24. - Enhanced Bonding Strength via Single-Wafer Annealing with Reduced Thermal Budget
Yoocharn Jeon, Mariia Gorchichko, Shashank Sharma, Jacob Yagura, Vijay Sukumaran, Juniper Iler, Raghav Sreenivasan, Siddarth Krishnan, Michael Chudzik – Applied Materials, Inc.

25. - Assembly Process Development for Ultra-large 88x52mm² Size Fan-out Interposer with Bridge Chips to Integrate Multi-HPC, HBM, and Photonic Optical Engine Chiplets
Sharon Pei Siang Lim, Lai Yee Chia, Manyi Pan, Hipona Randy Tupaen, Ignatius Lim, Mohamed Zakir Hussain Mohamed Ishak, Jerald Soh, Sandra San, Yong Liang Ye, Tai Chong Chai – Institute of Microelectronics A*STAR

26. - Fine Pitch and Ultra Low Profile Double-side Molded LGA Solution
Ming-Hung Chen, Yu-Chang Chen, Ren-Jieh Kao, Yun-I Yeh – Advanced Semiconductor Engineering, Inc.

Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Exhibition Hall - Mediterranean Ballroom

27. - Thermo-Pressing Treatment to Enhance Conductivity of Printed Carbon on Flexible Substrates
Babatunde Falola, Riadh Al-Haidari, Olya Noruz Shamsian, Shiwantha Gunathilake, Mark Poliks – Binghamton University

28. - Integration of Novel PECVD Film as Inter-Die-Gap-Fill (IDGF) and Advanced Thermal Interface Materials (TIM) for Next Generation 3DICs
Vijay Sukumaran, Sean Seutter, Karthik Guda Vishnu, Yoocharn Jeon, Michel Khoury, Grayson Langham, Liu Jiang, Man-Ping Cai, Ying Trickett, El Mehdi Bazizi, Jinho An, Chris Lee, Tom Osterheld, Raghav Sreenivasan, Siddarth Krishnan, Michael Chudzik – Applied Materials, Inc.

29. - Evaluation of Electroless-Plated Copper Circuits on Polyethylene Terephthalate (PET) for Roll-to-Roll Manufacturing of Flexible Hybrid Electronics
Zhi Dou, Riadh Al-Haidari, Mousa Al-Zanina, Mark Schadt, Mark Poliks – Binghamton University; James Honan, Thomas LeBlanc, Emily Rej, Carolyn Ellinger – Eastman Kodak Company; Fabian Schnegg – Nextflex

30. - Temperature-Dependent Electrical Characterization of New ABF-Type A Material up to 220 GHz
Mahin Ahamed, Madhavan Swaminathan – Pennsylvania State University; Lakshmi Narasimha Vijay Kumar – Georgia Institute of Technology; Habib Hichri, Yoshio Nishimura, Takashi Yamanaka, Yuko Shibata – Ajinomoto Co., Inc.

31. - Modular 3D Heterogeneous Integration with Stacked-Via 3D Stitch-Chips (SV-3DSC)
Shane Oh, Zhonghao Zhang, Paul Jo, Muhannad Bakir – Georgia Institute of Technology

32. - 60GHz mmWave Radar in Fan-in Wafer-Level Chip Scale Package (FI-WCSP) Technology
Aditya Jogalekar, Mohammad Vatankhah Varnoosfaderani, Marc Dewilde, Karan Bhatia, Tim Davis, Sangamesh Anandwade, Sunhwan Jang, Arnab Das, Vivek Sridharan, Krishnanshu Dandu, Venkatesh Srinivasan – Texas Instruments, Inc.

Friday May 29
10:00 a.m. - 12:00 Noon

Session 41: Student Interactive Presentations

Committee: Interactive Presentations

Mediterranean Hallway, JW Marriott

Session Co-Chairs
Ibrahim Guven
Virginia Commonwealth University
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Alan Huffman
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Bhaskar Jyoti Krishnatreya
Intel Corporation
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Michael Mayer
University of Waterloo
Email: mmayer@uwaterloo.ca

1. - Organics-Free Porous Nano-Dendritic Cu Films for High-Power Packaging Interconnects
Fatin Battal, Jeroen Maasen, Peter Mulder, Elias Vlieg, John Schermer – Radboud University; Nikhil Gupta – Delft University of Technology; Ruben Pranger – Netherlands Organization for Applied Scientific Research (TNO); Rene Poelma – Nexperia

2. - Ground Resonance Suppression on 212.5-Gbps OSFP with FEM and Mixed-Mode dPBTL Circuit
Kewei Song, Shixuan Yuan, Yulin He, Milton Feng – University of Illinois; Xiangyi Kong – University of Illinois Urbana-Champaign; Joseph Wang – Foxconn Interconnect Technology

3. - Study of Moisture Analysis Technology Based on Fan-out Package
Yang Yang, Meiying Su, Rui Ma, Hualong Fu, Anqi Zhou, Jun Li, Jingyi Zhao, Yunyan Zhou, Qidong Wang, Liqiang Cao – Institute of Microelectronics of the Chinese Academy of Sciences

4. - Location-Dependent Microstructure and Mechanical Properties Evolution of TGV-Cu via an EBSD–Nanoindentation Co-Localization Characterization
Junwei Chen, Chao Gu, Xuyang Yan, Jiajie Fan – Fudan University; Xiao Hu, Guoqi Zhang – Delft University of Technology; Bin Yang, Chengqiang Cui – Guangdong Fozhixin Microelectronics Technology Research Co. Ltd

5. - CMP-Free and Low-Temperature Cu-PI Hybrid Bonding for Rapid Multi-Chip to Wafer Integration
Jinzhu Li, Xinyao Wang, Qichun Lou, Mingze Ban, Ziyu Liu, Lin Chen, Qingqing Sun – Fudan University; Yabin Sun – East China Normal University

6. - Ultrasonic-Assist Thermocompression Al-PI Hybrid Bonding Applied for Chiplet Heterogeneous Bonding
Jinzhu Li, Mingze Ban, Qichun Lou, Xinyao Wang, Ziyu Liu, Lin Chen, Qingqing Sun – Fudan University; Yabin Sun – East China Normal University

7. - Robust Design of Hybrid Bonding Considering Cu Pad Inelastic Deformation for Reliability
Sang-Hoon Kim, Eun-Ho Lee – Sungkyunkwan University; Yeoun-Soo Kim, Haeri Kim, Jong Han Shin – SK hynix Inc; Jiho Kang – Absolics Inc.

8. - Thermal Distribution Analysis of a 2.5D CPO Structure Integrated with a DFB Laser
Thu Huong Bui, Lucas Yang, Kung-An Lin, Chao-Hsin Wu – National Taiwan University

9. - Reliability Evaluation of Intense Pulsed Light Flip-Chip Bonding with Various Surface Finishes
Hyeong-Bin Park, Young-Min Ju, Yun-Joong Kim, Hak-Sung Kim – Hanyang University

10. - Enhancing SiO_2 Bond Strength with Minimized Cu Surface Oxidation via H_2O-Assisted Plasma Treatment
Gyeongyeol Lee, Youngjoon Cha, An Nguyen, Rino Choi – Inha University

11. - A Co-Optimization Method for IVR and PDN in Embedded Vertical Power Delivery Substrate
Lihao Ou – Institute of Microelectronics of the Chinese Academy of Sciences; Xiangan You, Fang Yang, Zhidan Fang, Yunyan Zhou, Shanjun Ding, Fengze Hou, Yuxin Ye – Institute of Microelectronics of the Chinese Academy of Sciences

12. - Low Temperature and Low Pressure Fine-Pitch Cu-Cu Bonding by Electroplated In-Sn-Passivation
Yu-Hsiang Lu, Po-Shao Shih, Wei Choong Lee, Cheng-Yan Yang, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

13. - Miniaturized 3D Marchand Balun on Glass for Wideband RF Integration
Seokyoung Hwang, Sojeong Kim, Gangtae Jin, Young-Joon Kim – Gachon University; Yubin Kim, Jongmin Yook, Jein Yu – Korea Electronics Technology Institute

14. - Next-Generation Scanning Electron Microscope for Advanced Packaging: Coating-Free, Ambient, and Ready-to-Use
Weichen Zhao, Junbo Yang, Yuhan Gao, Dalei Yang, Kewei Shou, Yi Deng, Karthik Arun Deo, Stephen Cain, Seungbae Park – Binghamton University; Donghwa Kwak, Young-Eun Kwon, Junhee Lee – Coxem Co., Ltd.

15. - High Fidelity Reliability Prediction of SAC Solder Under Drop Impact via High Strain Rate and Temperature Dependent Properties
Dong-Hoon Yoo, You-Gwon Kim, Hak-Sung Kim – Hanyang University; Jin-Young Bang, Jong-Bum Lee – Samsung Electronics Co., Ltd.

16. - 3D Interconnection Using TGVs on Glass Interposer for Vertical 32 Gbps High-Speed Transmission
Suin Chae, Seonwoo Kim, Yubin Kim, Jein Yu – Korea Electronics Technology Institute; Jaemyung Lim – Hanyang University

17. - Reliability Prediction of Automotive SiC MOSFET Packages Based on Degradation of EMC Viscoelasticity and Interfacial Strength
Semin Lee, Sejun Park, Heeju Han, Hongyun So, Hak-Sung Kim – Hanyang University; Hyun-Woo Jung, Kyung-Woo Lee, Dae-Un Sung – Hyundai Motor Company

18. - Towards High-Conductivity Aerosol Jet Printed Copper with Amine Surfactant
Cheng Zheng, Chee Lip Gan – Nanyang Technological University; Alfred Zinn – Kuprion, Inc.

19. - Ultra-low Coefficient of Thermal Expansion Spin-on Polymer for Deep Trench Gap-Filling for 3D-IC Heterogeneous Integration
Pin-Lin Chen, Chih Chen – National Yang Ming Chiao Tung University; Ya-Chien Chuang, Hsiao-Wei Yeh, Satoshi Fujimura – Tokyo Ohka Kogyo Co., Ltd.

20. - Design and Signal Integrity Analysis of PCIe 5.0 SFF-8639 (U.2) Connector for AI Data Servers
Byeongmok Kim, Eunji Seo, Jihun Kim, Junho Park, Jiwon Yoon, Jaegeun Bae, Youngsu Yoon, Hyunseo Uhm, Joungho Kim – Korea Advanced Institute of Science and Technology; Youngje Cho, Hyanggon Kim, Sungmin Choi – Korea Electric Terminal

21. - Novel CMP-Free Cu/Polymer Low Temperature Hybrid Bonding with Wide Process Window for Advanced Packaging and 3D Integration
Kai-Yu Chao, Mu-Ping Hsu, Yuan-Chiu Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Yen-An Chen – Feng Chia University; Chee Ping Lee, Audrey Charles – Lam Research

22. - Room-Temperature Au-Au Bonding of Rough-Surface Ceramics Smoothed by Au Thin Film Transfer and the Plastic Deformation of Intermediate Metal Layer
Shintaro Goto, Kai Takeuchi, Eiji Higurashi – Tohoku University

23. - High-Resolution Nanoscale X-Ray Imaging for Non-Destructive Inspection of Copper Grains in Fine-Pitch Pads for Hybrid Bonding
Nimish Nazirkar, James Lu, Edwin Fohtung – Rensselaer Polytechnic Institute; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research; Dmitry Karpov – European Synchrotron Radiation Facility

24. - Advanced Acoustic Emission (AE) Sensing and Analytics Scheme for In-situ Warpage Characterizations of Flip-Chip Packaging
Yigit Turan, Xinchen Wang – Binghamton University; Sathya Raghavan – IBM Research; Zimo Wang – State University of New York at Binghamton

25. - Board-Level Reliability of 100mm × 100mm Large Glass Packages: Die Placement Configuration Based Thermo-Mechanical Reliability for AI/HPC Applications
Kaushik Godbole, YongWon Lee, Suresh K. Sitaraman – Georgia Institute of Technology

26. - Direct Glass-Copper Vias Integrated with Blind-Cavity Embedded Chips Using Nanoscale Liner
Sai Saravanan Ambi Venkataramanan, Mohan Kathaperumal, Hyunggyu Park, Mruga Panse, Aparnaa Iyer, Ching-Ping Wong, Mark Losego – Georgia Institute of Technology; Zhaoxia Yang, Mark Broman – Thin Film Technology Corp.

27. - Plasma-Free Wafer-Level Hybrid Bonding Using iCVD Polymer Thin Film for Feasible 3D Multi-Chip Integration
HyungJun Kim, MinJu Kim – Dankook University; Taehun Jeon, Jongkyung Park – Seoul National University of Science and Technology

28. - Interfacial Engineering for Cost-Effective Cu-to-Cu Direct Bonding Using an Ultra-Thin Cu-Selective Passivation Coating
Kevin Antony Jesu Durai – Department of Chemistry, University of North Texas; Duwage Anushka Perera, Khanh Tuyet Anh Tran, Dinesh Kumar Kumaravel, Shinoj Sridharan Nair; Oliver Chyan – University of North Texas; Rachel Ko – Texas Academy of Mathematics and Science

29. - Photonic Dielet Integration into Electrically Active FlexTrate for High Bandwidth Connectors
Alexis Samoylov, Subramanian Iyer – University of California, Los Angeles

30. - Ultraprecise Additive Printing of Reliable Fine-Pitch Features
Olya Noruz Shamsian, Erik Busse, Abdullah Obeidat, Mark Poliks – Binghamton University

31. - Compact 6-GHz Microstrip Bandpass Filter with Folded-Arm Resonators and Dual Transmission Zeros: Design, Fabrication and Measurement
Jaehyuk Lee, Alexander Wilcher, Hanna Jang, Ariel David Cerpa, Yong-Kyu Yoon – University of Florida

32. - Strain Range Dependent Fatigue Behavior of High Temperature Solder Alloys
Sean Lai, Chung Shuo Lee, Lijia Xie, John Blendell, Carol Handwerker, Ganesh Subbarayan – Purdue University

33. - A Novel Hierarchical Global Multi-Scale Network for X-Ray Image Enhancement in Packaging
Hanwen Li, Nagarajan Raghavan – Singapore University of Technology and Design; Senthilnath Jayavelu – Institute for Infocomm Research A*STAR

34. - Die-level Via-last TSV Formation and Heterogeneous 3D Integration with Multi-Project Wafers Using Photosensitive Temporary Adhesives for Agile Prototyping
Jiayi Shen, Akihiro Tominaga, Bungo Tanaka, Chang Liu, Tetsu Tanaka, Takafumi Fukushima – Tohoku University

35. - Additively-Deposited Fan-Out Interconnects for Power/RF Co-Packaging with Glass-Laminate Hybrid Panels
Sajith Rathnayaka, Daniel Escobar, Arjuna Madanayaka, Markondeya Raj Pulugurtha – Florida International University; Gilbert Rodriguez, Ronald Olmen – Haiku Tech Inc.

36. - Novel Immersion-Sn Passivation Process to Address Nanoporous-Cu Seed Layer Etching Challenge for Scalable, Low-Temperature Panel-Level Cu-Cu Bonding
Ramón A. Sosa, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology; Jobert Van Eisden, Kuldip Johal – MKS Instruments

37. - Heterogeneous Integration of BEOL 22nm CMOS FDSOI AI to Cu Interposers by Direct Bonding
Kirthika Nahalingam, Mohammad Rezaeifer, Kamran Entesari, Linda Katehi – Texas A&M University

38. - Link Quality Aware Pathfinding for Chiplet Interconnects
Aaron Yen, Jooyeon Jeong, Puneet Gupta – University of California, Los Angeles

39. - Thermally-Aware System-Technology Co-Optimization for AI Systems
Dedeepyo Ray, George Karfakis, Alexander Graening, Puneet Gupta – University of California, Los Angeles; David Ratchkov – Anemoi Software

Friday Refreshment Break: 10:30 a.m. - 11:15 a.m. – Palazzo and Mediterranean Foyers

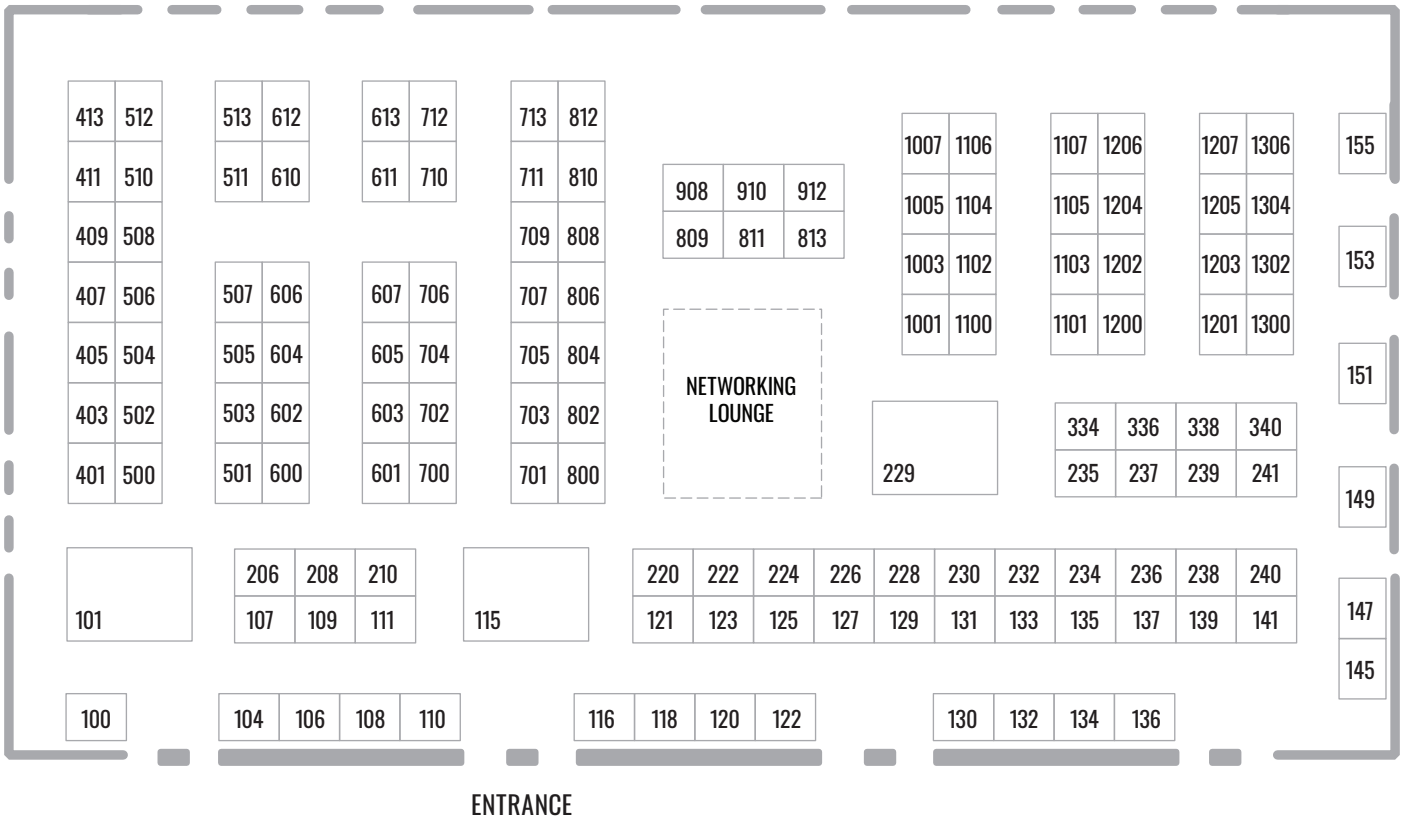
2026 ECTC EXHIBITION

Exhibit Hall Hours

Wednesday, May 27
9:00 a.m. – 12:30 p.m. / 2:00 p.m. – 6:30 p.m.

Thursday, May 28
9:00 a.m. – 12:30 p.m. / 2:00 p.m. – 4:00 p.m.

Mediterranean Ballroom, JW Marriott



2026 ECTC EXHIBITORS

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over 80 years of innovation and expertise. Headquartered in Niigata, Japan, NAMICS supports customers worldwide through subsidiaries in the United States, Europe, Taiwan, Singapore, Korea, Hong Kong, and China. Our portfolio includes industry-leading underfills, liquid molding compounds, glob top encapsulants, pressureless sintering die-attach materials, adhesives for sensor and camera modules, and stretchable printed materials for flexible interconnects, heating, and bonding. Known for unmatched quality and reliability, NAMICS partners closely with customers to deliver customized material solutions that enable next-generation electronic technologies.

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Technic Inc. is a Rhode Island based corporation with over 1,100 employees worldwide. For more than 80 years, Technic has been a global supplier of specialty chemicals, custom finishing equipment, engineered powders, and analytical control systems to the semiconductor, electronic component, printed circuit board, industrial finishing, and decorative industries.

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FIRST CALL FOR PAPERS

IEEE 77th Electronic Components and Technology Conference • www.ectc.net
to be held June 1 – June 4, 2027 at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, USA

The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee. Authors are encouraged to review the sessions of the previous ECTC programs to determine which committees to select for their abstracts.

Applied Reliability: 2D, 2.5D, 3D, chiplets/heterogenous integration, Si bridge, WLCSP, FOWLP, FOPLP, co-packaged optics (CPO), LED, memory devices, IOT, autonomous vehicles/automotive, wire bonded packages, sintered modules, micro-bump, micro-pillar, Cu-pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip interconnects, harsh environments, power modules, renewable energy systems, data center application, liquid cooling/ immersion cooling, thermal materials (TIM), medical electronics, wearable electronics, displays, AI application, computing, networking systems, HPC, mobile systems, fault isolation techniques, metrology, material characterization, use-condition, stress methodology

Assembly & Manufacturing Technology: Embedded, power, magnetics, embedded die and passives in substrates, controlling warpage, thermal dissipation, package stress, AI/ HPC/SerDes packages (2.5/3D), application of glass, hybrid materials, substrates, interposers for 2.5D/3D, innovations in conductive fine pitch traces, via manufacturing, AI/HPC SerDes packages, innovative packaging processes, methodologies, materials, tools enabling panel level packaging (PLP), cost-efficiency/yield perspective, high yield organic interposer 2.XD for panel level packaging (PLP)

Electrical Design & Analysis: Cloud computing, autonomous vehicles, AI/machine learning, large language models (LLMs)/generative AI, high-frequency (RF, mmWave, THz), 5G/6G, IoT, antennas, antenna-in/on-package (AiP/AoP), sensors, power transfer, wired/ wireless communications, RF to THz, multi-physics/multiscale modeling & characterization of interconnects, modules, components, systems, chiplet, heterogeneous integration, chip-to-chip/die-to-die, SiP/MCM/system co-design (chip/package/board), UCIe/HBM/HPC, SerDes, high-bandwidth, 3D integration/hybrid bonding, opto-electrical (OE) hybrid integration, co-packaged optics, analog packaging, power electronics modeling/characterization, signal integrity, power integrity, EMI/EMC

Emerging Technologies: Novel materials, packaging architectures, additive manufacturing, harsh environments, system technology co-optimization (STCO), smart manufacturing, digital twin, sensor integration/packaging, flexible electronics, implantable electronics, medical/ bio-electronics, integrated power challenges, power delivery, thermal solutions, high current/ high voltage devices, metrology and characterization, benchmarking, failure analysis, hardware security, quantum computing, cryogenic electronics, sustainability, emerging AI technologies

Interconnections: Chiplet heterogeneous integration, hybrid bonding (C2W & W2W), fan-out wafer level packaging, fan-out panel level packaging, through silicon via (TSV) and nano-TSV through glass via (TGV), through mold via (TMV), 2.5D/3D, silicon/glass/organic interposers, silicon bridges/local silicon interconnects, glass core substrate/advanced multi-core build-up substrate, fine-pitch/multi-layer RDLs, system-in-package (SiP), wafer-level system integration, panel-level system integration, thermo-compression/laser assisted/ transient liquid phase bonding, low temperature solders, flip-chip, micro-bump, Cu pillar, wirebond, Al ribbon bond, warpage mitigation, emerging technologies, optical interconnects, printable/flexible interconnects, interconnects for SiC/GaN and wide bandgap, materials/ chemistries, conductive/non-conductive adhesives, anisotropically conducting film (ACF), underfill materials and molding compounds, thermal interface materials and novel cooling techniques, metrologies, characterization techniques, thermal/mechanical/electrical tests and reliability, sustainable interconnects, chiplet interconnect design and validation, standards (UCIe/BoW etc.), design and characterization for backside power delivery network (BPDN), integrated IVR and passives

Materials & Processing: Hybrid bonding, fan-out packaging, silicon/glass interposer, 2.5D/3D integration, chiplet integration process, wafer-to-wafer bonding, through-silicon via (TSV), die-to-wafer stacking, wafer-level packaging (WLP), panel-level packaging (PLP), redistribution layer (RDL), die-embedding processes, panel-scale lithography, glass carriers, thinning and handling, system-level scaling, polymer TIMs, solder and liquid-metal TIMs, emerging TIMs, die-attach materials, thermo-mechanical reliability, high-temperature stable materials, hermetic sealing materials, shock-resistant compounds, low-k/low-loss dielectrics, dielectric deposition processes, dielectric patterning, capillary underfill (CUF), reworkable underfills, molded underfills (MUF), wafer-level molding materials, thermally conductive underfill/molding compounds, temporary bonding adhesives, temporary bonding carriers, UV-release adhesives, thermal-release adhesives, debonding processes, low-temperature adhesives, conductive adhesives, adhesive residue suppression, silicon/glass core substrates, substrate-like package (SLP), novel substrate materials, AI-enhanced materials and processes, low-temperature solders, high aspect ratio vias, electromagnetic interference (EMI) shielding materials, materials for co-packaged optics (CPO)

Packaging Technologies: Architectures, integration, thermal solutions of 2.XD, 3D heterogeneous packaging including co-packaged optics (CPO)/co-packaged copper (CPC), silicon/organic/glass/diamond interposers and related packaging technology including CPO/ CPC, hybrid/other die-to-die bonding, TSV, backside power delivery, embedded die/bridge/ passives, fan-out wafer/panel-level packaging, automotive, wireless power and power electronics including SiC/GaN/PMIC/SPS, bio/medical, RF, MEMS, sensors, wireless, flexible/ wearable, IoT

Photonics: Co-packaged optics (CPO), inverse design, hybrid bonding, heterogeneous materials, 2.5D/3D, PIC assembly, wafer-scale integration, interconnects, datacom, telecom, optical computing, high density I/O, data processing, 5G/6G, IoT, AI, space, radiation hard, low volatile organic compound (VOC) adhesives, high-temperature, vibration and shock resilience, atmospheric, automotive, defense, healthcare, green energy, agriculture, climate monitoring, underwater, low power, materials, connectors, packaging materials, fiber attach unit (FAU) and detachables, metamaterials, metasurfaces, fiber bundle connections, low size/ weight/power/cost (SWaP-C), characterization, equipment, packaging tools, 3D printing, micro-optics, free space optics, microscopy, fiber attach

Thermal/Mechanical Simulation & Characterization: Thermal and mechanical simulation and characterization across packaging technologies, package level, board level, system level, measurements & characterization, correlations, sensitivity & statistical analysis, reliability modeling and testing, material constitutive relations, fatigue, fracture mechanics, warpage, electromigration, vibration, shock and drop, moisture, modeling for harsh environments, thermo-mechanical, thermal management, cryogenic, humidity, chemical, chip-package interaction for heterogeneous integration, co-packaged optics, novel modeling techniques, multi-scale physics, model order reduction, AI/ML, digital twin, credible simulations for virtual release, co-design approaches, computational fluid dynamics (CFD) and process simulations, model verification

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract that describes the novelty, scope, content, and key points of your proposed manuscript via the website at www.ectc.net.

If you have any questions, contact:
Tanja Braun, 77th ECTC Program Chair
Fraunhofer IZM
tanja.braun@izm.fraunhofer.de

Abstracts cannot contain more than 700 words and must be received by October 5, 2026, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors. The authors are notified about the abstract selection outcome by December 11, 2026.

Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From the proposals received, 16 PDCs are selected for offering at the 77th ECTC on Tuesday, June 1, 2027.

Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 18, 2026. Authors are notified of course acceptance with instructions by December 11, 2026.

If you have any questions, contact:

Kitty Pearsall, 77th ECTC Professional Development Courses Chair – Capstan Technologies, Inc.
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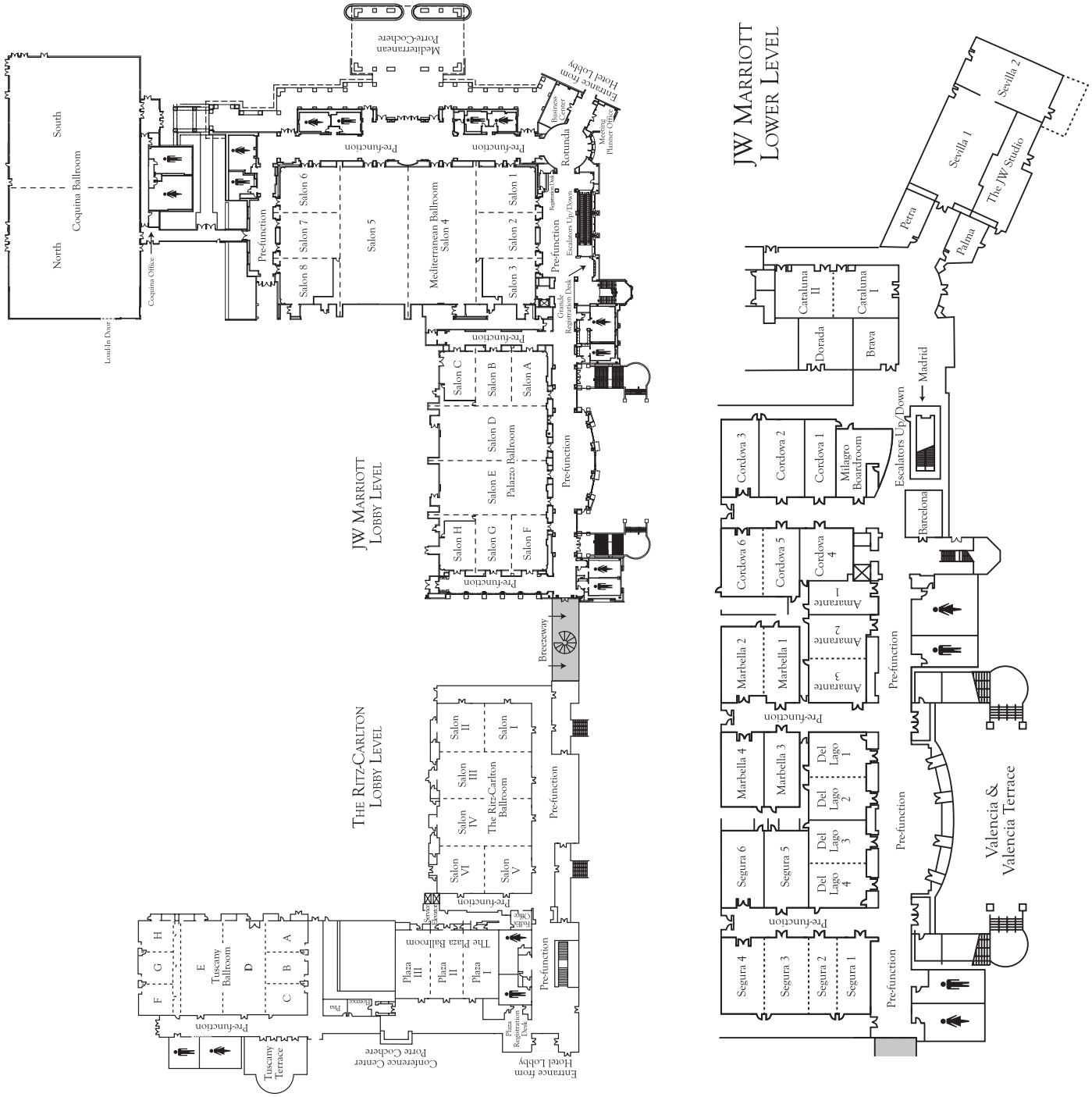

77TH ELECTRONIC COMPONENTS & TECHNOLOGY CONFERENCE

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Standing at the edge of the Front Range, Gaylord Rockies Resort & Convention Center showcases the state's alpine charm and offers guests a welcome reprieve from the typical mountain resort stay. From our thrilling Arapahoe Springs Water Park, to an exciting lineup of family-friendly activities and entertainment, there's something for the entire family to enjoy. Guests can explore the beautiful Grand Lodge and its stunning mountain views, five delicious restaurants, bars, the world-class Relâche Spa, and a state-of-the-art fitness center. For those planning or attending their next meeting or event, the resort features over 500,000 sq. ft. of flexible meeting space, 1,387 modern guest rooms, and 114 spectacular suites. With a fantastic water park, seasonal events, entertainment, and close proximity to local attractions, Gaylord Rockies Resort is the place where you can enjoy more of everything you love.

CONFERENCE AT A GLANCE

REGISTRATION

Monday, May 25, 2026
3:00 p.m. – 6:00 p.m.

Tuesday, May 26, 2026
6:45 a.m. – 6:45 p.m.

Wednesday, May 27, 2026
6:45 a.m. – 4:00 p.m.

Thursday, May 28, 2026
7:00 a.m. – 4:00 p.m.

Friday, May 29, 2026
7:00 a.m. – 12:00 Noon

JW Marriott Grande Lakes, lobby level, at the Grande Registration Desk

EXHIBITION HALL

Wednesday
9:00 a.m. – 12:30 p.m.
2:00 p.m. – 6:30 p.m.
Reception: 5:30 p.m. – 6:30 p.m.

Thursday
9:00 a.m. – 12:30 p.m.
2:00 p.m. – 4:00 p.m.
Mediterranean Ballroom, JW Marriott

SPEAKER PREPARATION ROOM

Tuesday – Friday
7:00 a.m. – 5:00 p.m.
Brava, Lower Level, JW Marriott

MAIN STAGE MORNING SESSIONS

Wednesday
ECTC Keynote

Thursday
EPS Plenary Session

Friday
IEEE EPS President's Panel
8:00 a.m. – 9:15 a.m.
Main Stage: Coquina Ballroom, JW Marriott

MAIN STAGE EVENING SESSIONS

Tuesday
IEEE EPS Seminar
7:45 p.m. – 9:15 p.m.
Main Stage: Coquina Ballroom, JW Marriott

Student Competition
Wednesday: 6:45 p.m. – 8:00 p.m.
Palazzo D, JW Marriott

Start-up Competition
Thursday 6:00 p.m. – 7:30 p.m.
Palazzo A-C, JW Marriott

GALA RECEPTION

Thursday
7:30 p.m.
Main Stage: Coquina Ballroom, JW Marriott

TUESDAY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m.
Palazzo C, JW Marriott

Professional Development Courses (PDCs)
8:00 a.m. – 12:00 Noon
1:30 p.m. – 5:30 p.m.
See page 9 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop
8:00 a.m. – 5:00 p.m.
Palazzo F-H, JW Marriott

Special Sessions
No. 1: 8:30 a.m. – 10:00 a.m.
No. 3: 10:30 a.m. – 12:00 Noon
No. 5: 1:30 p.m. – 3:00 p.m.
No. 7: 3:30 p.m. – 5:00 p.m.
Palazzo D, JW Marriott

No. 2: 8:30 a.m. – 10:00 a.m.
No. 4: 10:30 a.m. – 12:00 Noon
No. 6: 1:30 p.m. – 3:00 p.m.
No. 8: 3:30 p.m. – 5:00 p.m.
Palazzo E, JW Marriott

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Palazzo & Cordova Foyers, JW Marriott

Tuesday Lunch
12:00 Noon – 1:15 p.m.
Main Stage: Coquina Ballroom, JW Marriott

ECTC Exhibition Setup
1:00 p.m. – 5:00 p.m.
Mediterranean Ballroom, JW Marriott

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Mediterranean Ballroom Porte Cochere, Outside, JW Marriott

General Chair's Speakers & Session Chairs Reception
6:00 p.m. – 7:00 p.m.
Valencia Tent, Lower Level, Outside, JW Marriott
By invitation only

Young Professionals Networking Panel
7:00 p.m. – 7:45 p.m.
Palazzo D, JW Marriott

WEDNESDAY – FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Valencia Tent, Lower Level, Outside, JW Marriott

SESSIONS

9:30 a.m. – 12:35 p.m. and
2:00 p.m. – 5:05 p.m.
see pages 10–21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Palazzo A-C, JW Marriott

Sessions 2, 8, 14, 20, 26, 32
Palazzo D, JW Marriott

Sessions 3, 9, 15, 21
Tuscany D, The Ritz-Carlton

Sessions 4, 10, 16, 22
Tuscany E, The Ritz-Carlton

Sessions 5, 11, 17, 23
Tuscany F-H, The Ritz-Carlton

Sessions 6, 12, 18, 24
Tuscany A-C, The Ritz-Carlton

Sessions 27, 33
Mediterranean 4, JW Marriott

Sessions 28, 34
Mediterranean 5, JW Marriott

Sessions 29, 35
Mediterranean 1-3, JW Marriott

Sessions 30, 36
Mediterranean 6-8, JW Marriott

INTERACTIVE PRESENTATIONS

Sessions 37 – 41
10:00 a.m. - 12:00 p.m. and
2:30 p.m. - 4:30 p.m. (Wednesday & Thursday)
Mediterranean Foyer, JW Marriott
see pages 22–23 for specifics

LUNCH

12:45 p.m. – 2:00 p.m.
Main Stage: Coquina Ballroom, JW Marriott

REFRESHMENT BREAKS

10:30 a.m. – 11:15 a.m.
3:00 p.m. – 3:45 p.m.

Wednesday & Thursday Refreshment Break
Exhibition Hall – Mediterranean Ballroom, JW Marriott

Friday
Palazzo and Mediterranean Foyers, JW Marriott

The 2027 IEEE 77th Electronic Components and Technology Conference

June 1 – 4, 2027

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