ECTC at 75: Celebrating the Past, Innovating for the Future

The 2025 ECTC EPS President's panel

Panel overview

Moderator: Patrick Thompson, Texas Instruments, Inc

Panelists:

- Rao Tummala, Georgia Institute of Technology
- John Lau, Unimicron
- Bill Chen, ASE Group
- Kitty Pearsall, Capstan Technologies, Inc.

Agenda:

- Introduction
- ECTC history video
- Panelist presentations
- Discussion

Rao Tummala

- Rao Tummala invented or pioneered many technologies at IBM and Georgia Tech, including
  - the industry's 1st LTCC substrate, and the industry's 1st plasma display.
  - The industry's first 2.5D with up to144 chips that presaged today’s chiplets
  - The concept of SOP, system-on-package
- He set up Georgia Tech PRC as the largest and most comprehensive research, education and industry center in US, and created a consortium model for universities to develop manufacturable technologies.
- He published 800 articles, and 7 text books, and has 100 patents
- Rao received more than 50 awards from industry, academic and professional societies including the Davis Sarnoff Award from IEEE for industry’s 1st MCM
- For all of his contributions, he was named as the Father of Modern Packaging by IEEE which created a technical field award in his name, the IEEE Rao Tummala Electronic Packaging Award.

John Lau

- John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 530 peer-reviewed papers (385 are the principal investigator) and 24 textbooks.
- John has 52 issued and pending US patents (31 are the principal inventor)
- John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

Bill Chen

- William Chen (Bill) holds the position of ASE Fellow & Senior Technical Advisor at ASE Group. Prior to joining the ASE, he was Director at the Institute of Materials Research & Engineering (IMRE) in Singapore, following a distinguished career at IBM Corporation. Bill is a past President of the IEEE Electronics Packaging Society. He is a Life Fellow of IEEE and a Fellow of ASME. He received the ASME InterPACK Achievement Award in 2007. In 2018, he received the IEEE Electronics Packaging Field Award, recognizing his contribution to electronic packaging, from research & development through industrialization.
  Bill chairs the Heterogeneous Integration Roadmap initiative, co-sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division .

Kitty Pearsall

- KITTY PEARSALL earned her Ph.D. degree in Mechanical Engineering and Materials from the UT Austin in 1983. Kitty worked for IBM from 1972 to 2013, where she became both an IBM Distinguished Engineer and a member of the IBM Academy of Technology. Kitty was a process consultant and subject matter expert working on strategic initiatives impacting component qualification and end quality of procured commodities. She now works as an independent consultant for Capstan Technologies.
- Kitty received 4 IBM Outstanding Technical Achievement Awards and holds 12 US patents. Kitty is a licensed Professional Engineer (Texas since 1993). Kitty was the recipient of the UT Austin - Cockrell Engineering Distinguished Engineering Graduate Award in 2007 followed by induction as a charter member into the UT Mechanical Engineering Dept. Academy of Distinguished Alumni in 2008.
- Kitty is an active member in IEEE and EPS, as well as a member of TMS, American Society of Metals, and WIE. Kitty has been the Professional Development Course Chair since 2007. Kitty was the EPS President 2022 and 2023 and today serves a the EPS Junior Past President.

Early Memories

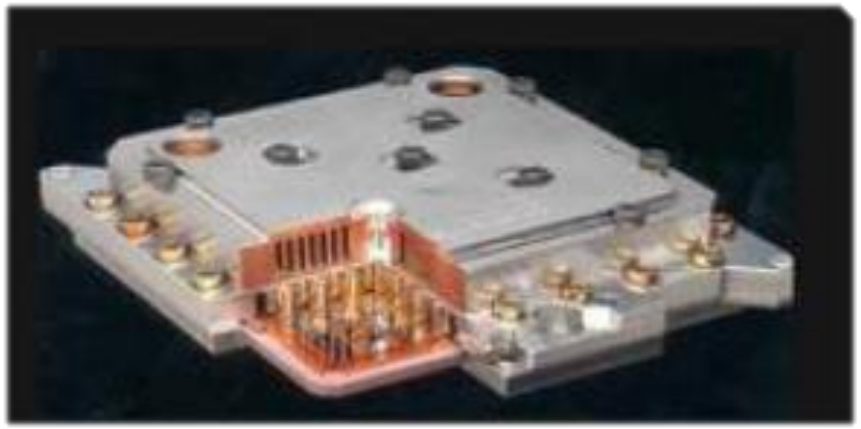
- Largest International Gathering of Packaging Technologists.
- Great Conference for Academics.
- Evening Sessions on Industry's1st Multichip Packaging in 1980s by:
  - IBM: Glass-Ceramic with Copper up to 61 layers(LTCC)
  - Fujitsu: Alumina+ Glass
  - NEC: Polymer-Cu Thin film RDL on 300 mm Alumina

Traditional vs. Integrated Systems Packaging

Traditional

IC Assembled on a Package Substrate

Packaging: Pre and Post Moore's law



Interconnected Module

Key Innovations that Revolutionized the Industry

- Flip Chip with Solders & Hybrid Bonding Without
- Multichip Substrates: Ceramic, Build up, Si interposers , EMIB, Glass
- 3D with TSV For Memory and 3D L+M for CMOS Image sensors
- Glass Panel Packaging to 1 Micron RDL Lithography
- Liquid Cooling near zero Thermal Interface Resistance
- Signal and Power Distribution with Decoupling Capacitors
- Design Tools, Methodologies and Algorithms

25 Years from Now

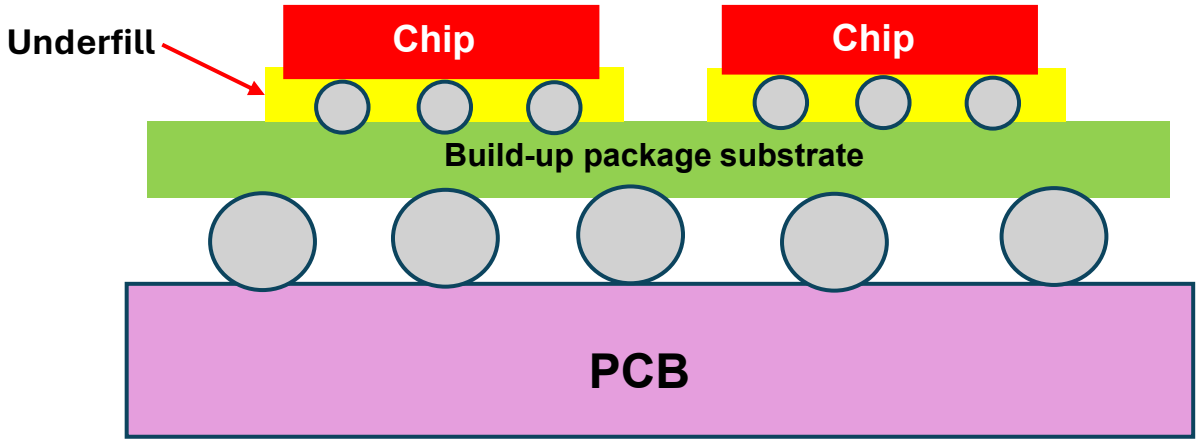
- Photonic- Based Computing In Products
- Quantum Computing In Products
- Neuromorphic Computing and Humans with Electronic Brains
- Robots Everywhere.

Early memories of ECTC and key innovations that revolutionized the industry (in high volume Production)

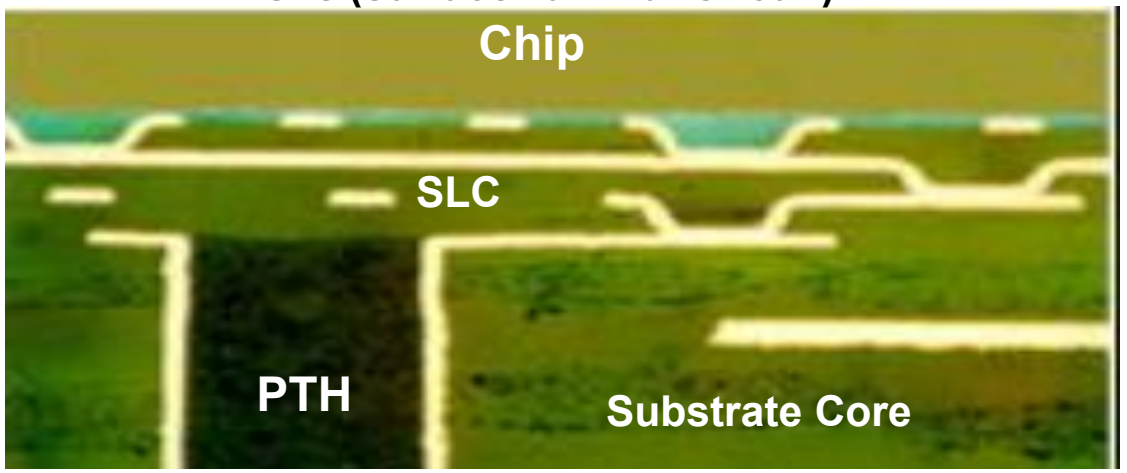
IEEE ELECTRONICS PACKAGING SOCIETY

ECTC
The 2025 IEEE 75th Electronic Components and Technology Conference

ECTC 1992 (IBM) Build-up Package Substrate

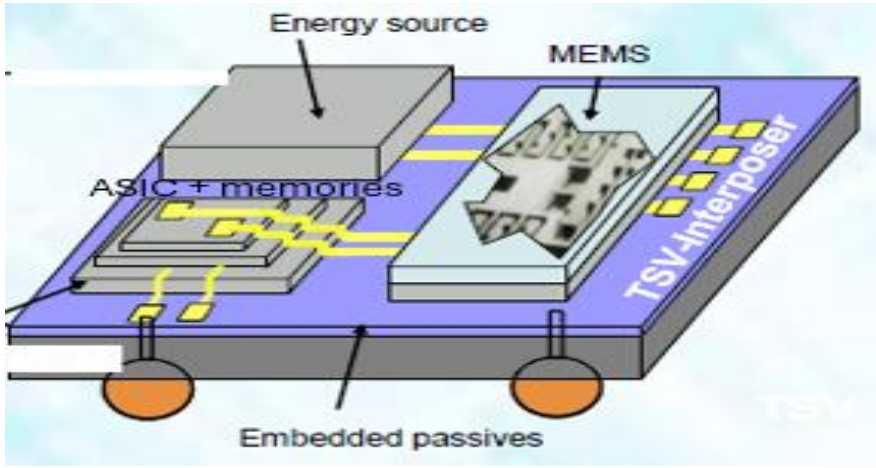


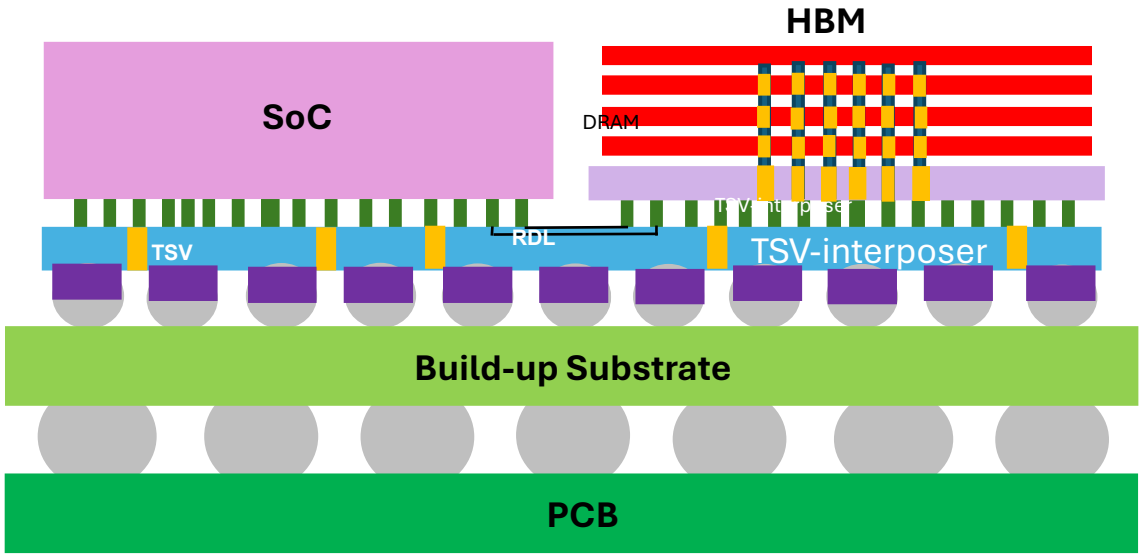
SLC (Surface Laminar Circuit)



Today, almost all electronic products use build-up package substrate

ECTC 2005 (CEA/Leti) 2.5D IC Integration





- **TSMC put it into production (2013)**
- **Today, all HPC products driven by AI use 2.5D**

Early memories of ECTC and key innovations that revolutionized the industry (in high volume Production)

IEEE ELECTRONICS PACKAGING SOCIETY

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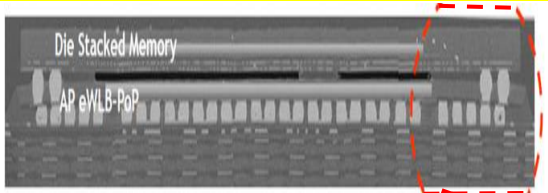
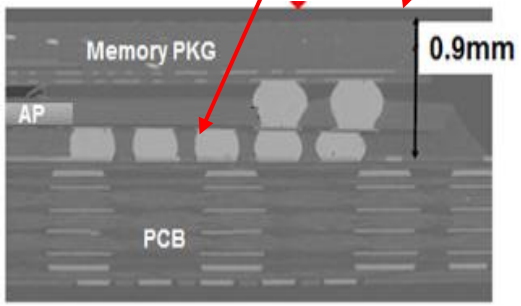
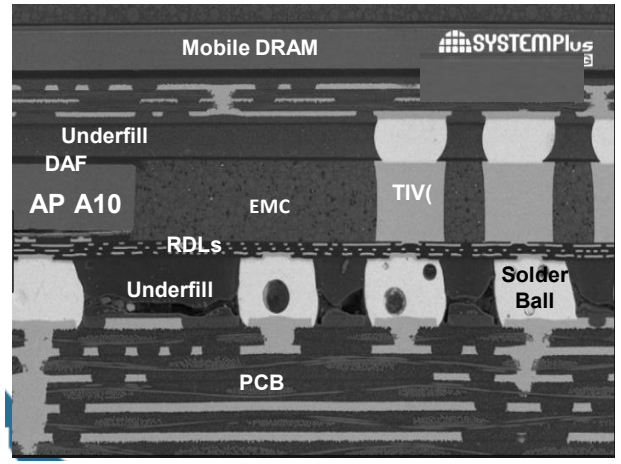
ECTC2010 (STATSChipPAC) AP Embedded in Fan-Out PoP



Fan-out RDLs

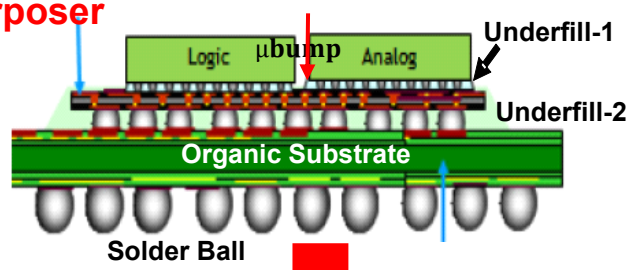




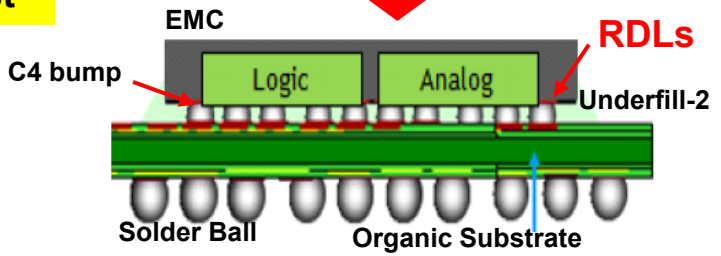
TSMC put it into production (2016)

ECTC2013 (STATSChipPAC) 2.3D IC Integration

TSV interposer

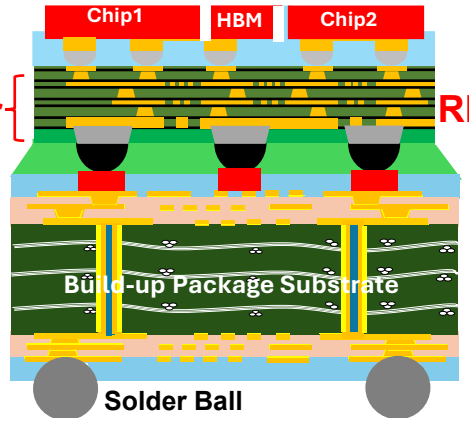


Chip first



Chip last

Organic Interposer



TSMC put 2.3D into production (2024)

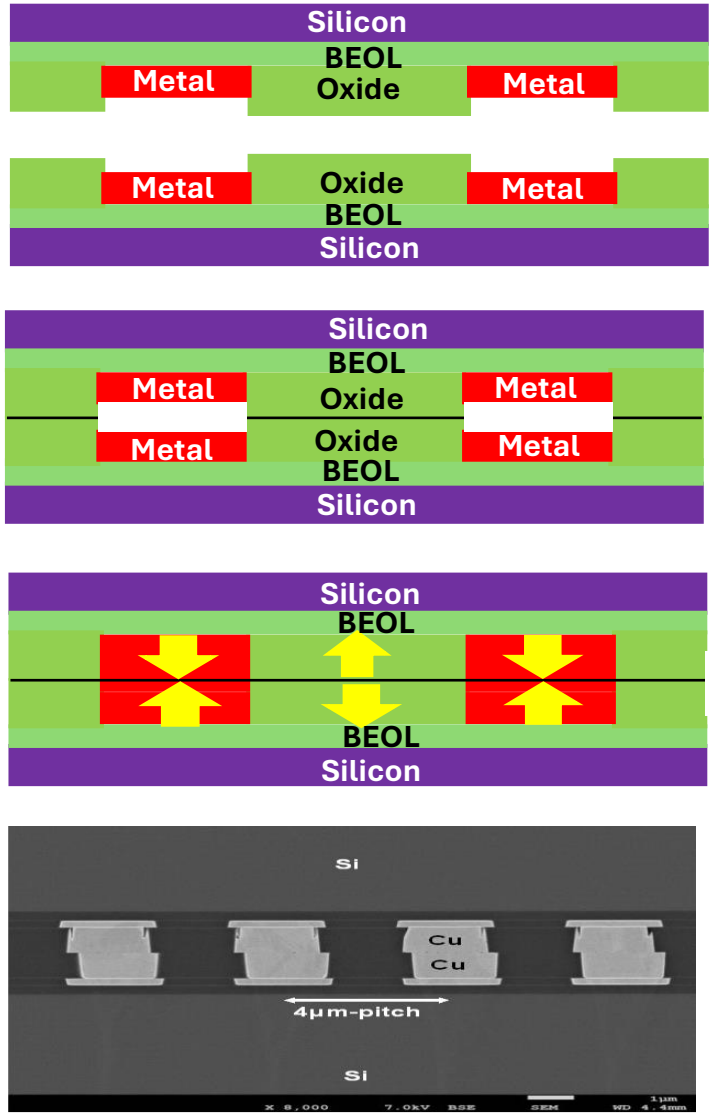
What's happening now that is exciting to you

IEEE ELECTRONICS PACKAGING SOCIETY

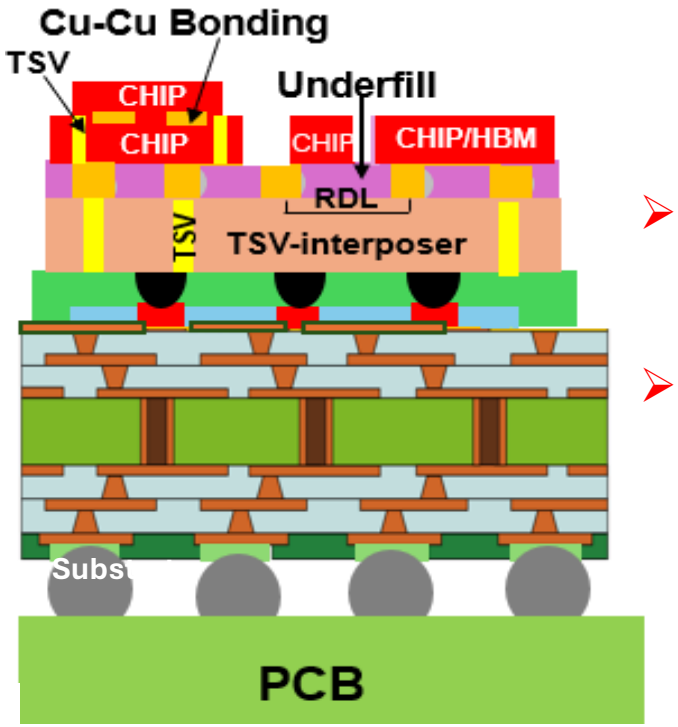
ECTC
The 2025 IEEE 75th Electronic Components and Technology Conference

- ECTC2022
  65 papers
- ECTC2023
  70 papers
- ECTC2024
  80 papers

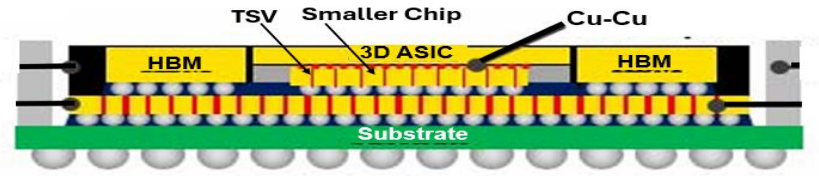
Cu-Cu Hybrid Bonding

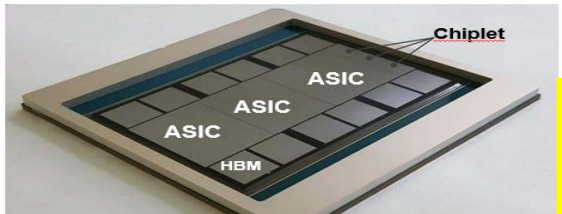


3.5D IC Integration



- Smaller Package Size
- Higher Electrical Performance





ECTC 2023 Samsung 3.5D

What's happening now that is exciting to you

IEEE ELECTRONICS PACKAGING SOCIETY

ECTC
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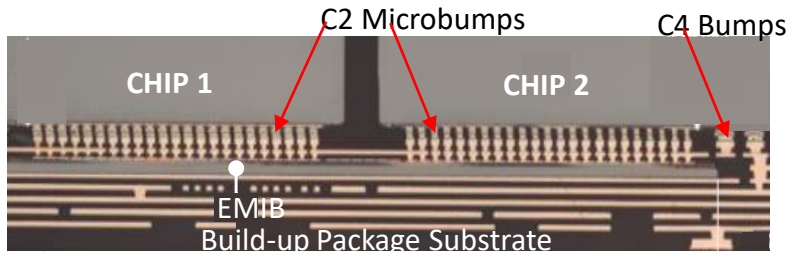
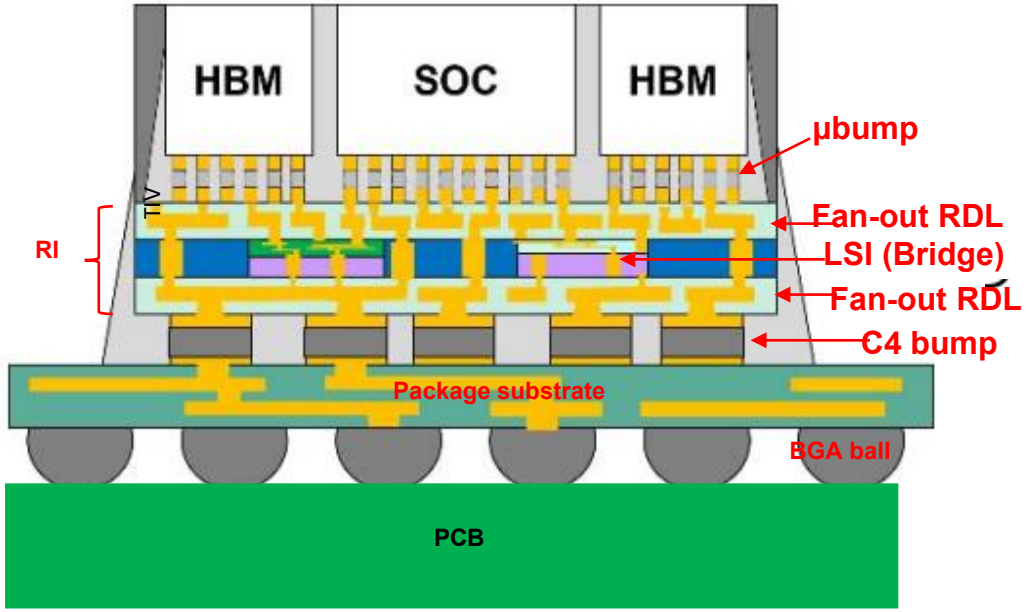
Bridges for Chiplets

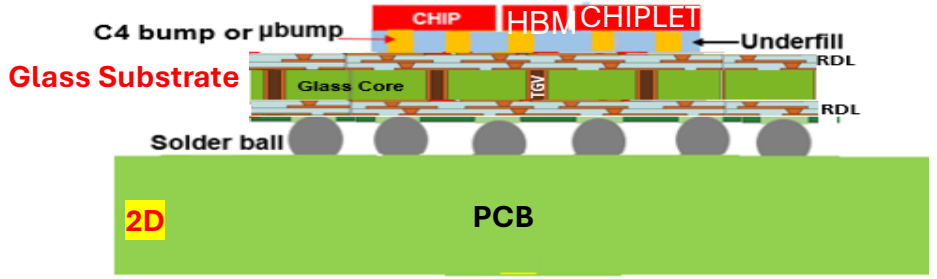


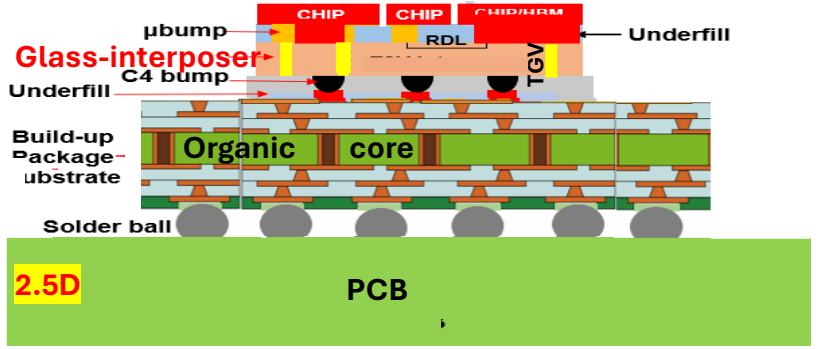
Bridges embedded in package substrate (Intel's EMIB)

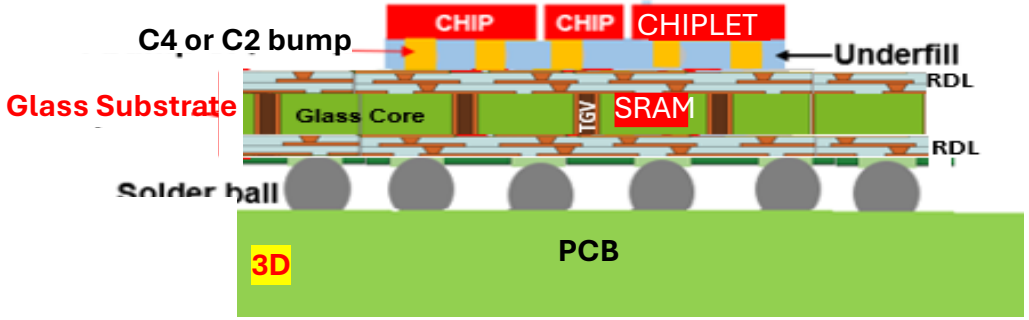


Bridges embedded in Fan-out EMC (TSMC's CoWoS-L)

Glass Packaging



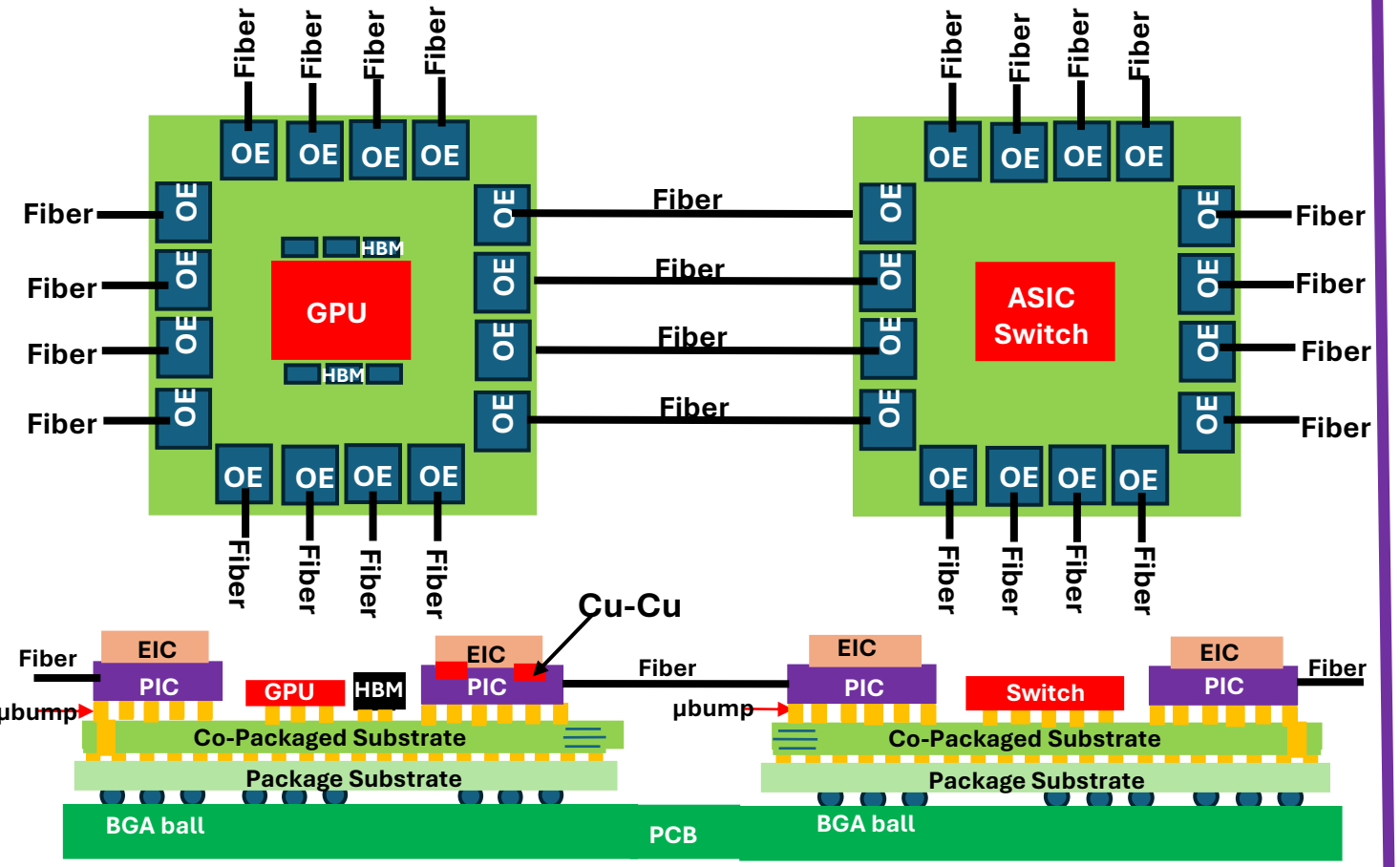




Seamlessly integrate optical interconnects

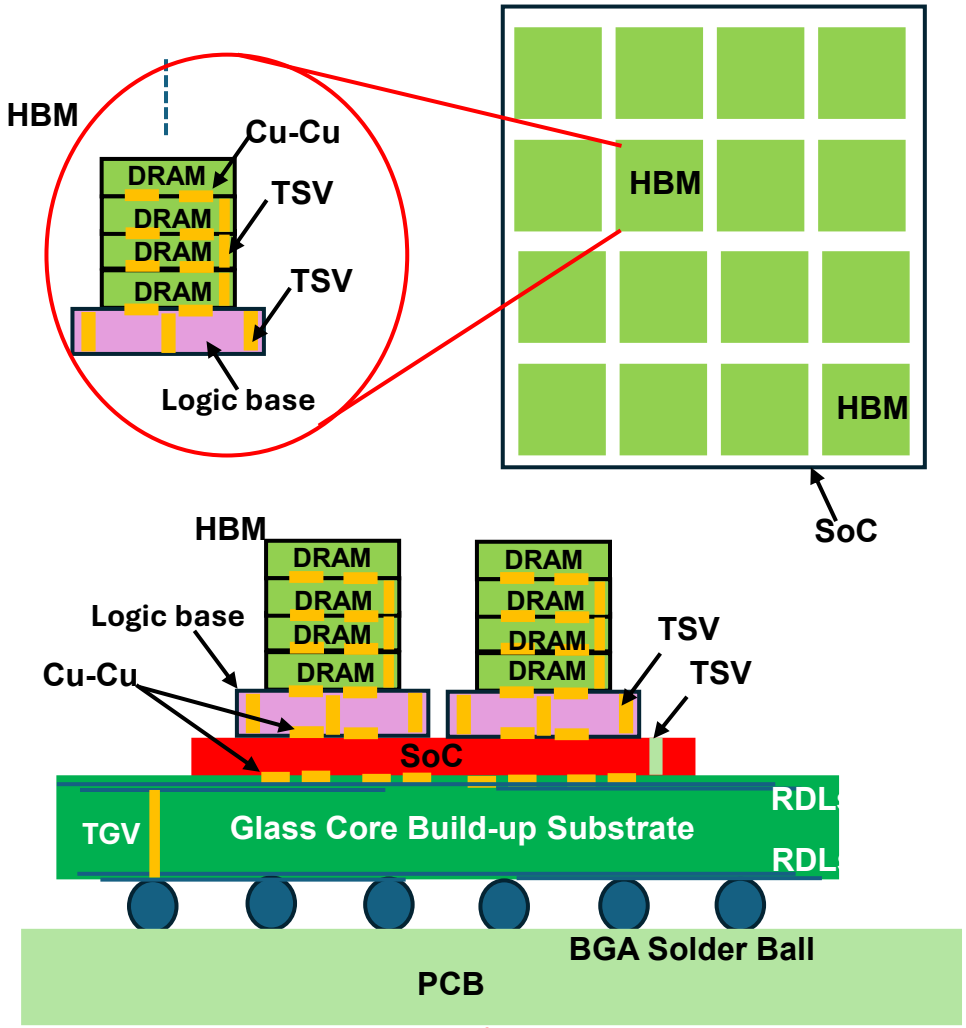
Your thoughts on what is coming on the road to the 100th ECTC

3D heterogeneous integration of GPU, HBM, ASIC switch, PIC, and EIC (Co-Packaged Optics)



HPC driven by AI + Communication

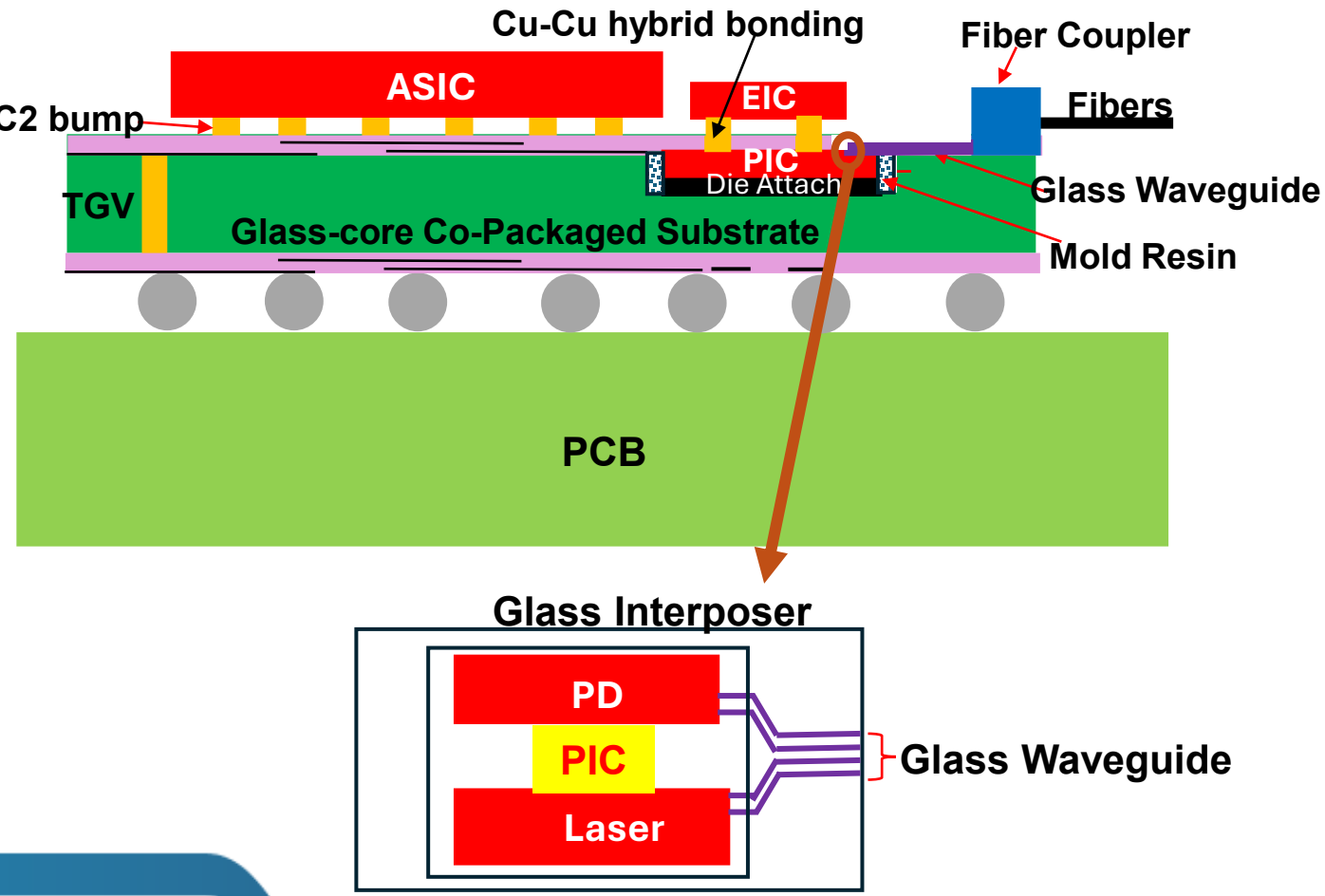
3.3D IC Integration for productors driven by AI



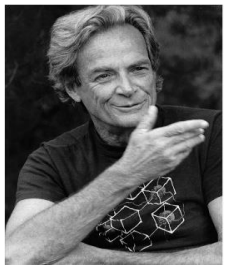
No TSV-interposer

Your thoughts on what is coming on the road to the 100th ECTC

3D heterogeneous integration of ASIC, EIC and PIC on a Glass-core co-packaged substrate



Quantum Computing



Quantum physics is so complex that even Richard Feynman,1965 Nobel Laureate in Physics and one of the fathers of quantum computing in the 1980s famously said:
"I think I can safely say that nobody understands quantum mechanics".

This statement excites many physicists working furiously on quantum computing!

Quantum computer is like a refrigerator (-273°C) with superconducting circuits. I'm wondering how are the packages work at this kind of environment.

EPS President's Panel

William Chen

May 30, 2025

Agenda

- ECTC 2010 Milestones
- Key Innovations that set the landscape today
- Future unlimited

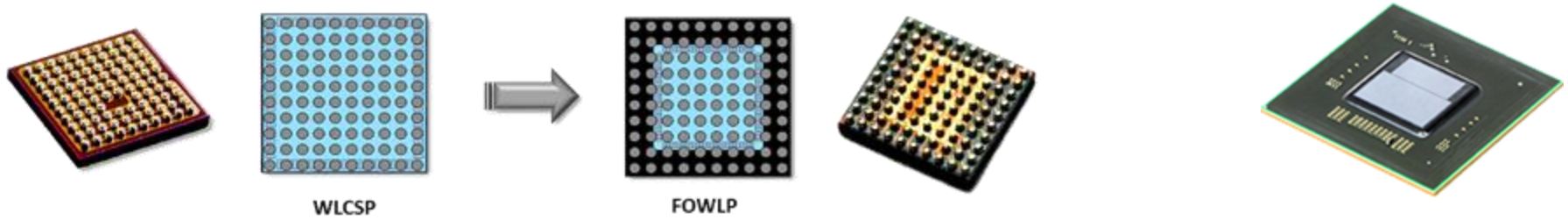
2010 ECTC Milestones

- At ECTC 2010, the Electronics Packaging Society (EPS) President, Rolf Aschenbrener signed an agreement with ECA for EPS to be the sole sponsor of ECTC, ending past years of dual sponsorship with ECA, together with ECTC General Chair Jean Trewhella.
- The “buyout” negotiation was led by EPS past presidents William Chen & Phil Garrou under the direction of EPS BoG*.
- This historic milestone established a deep and enduring partnership between EPS and ECTC, traversing 15 years of collaborative and innovative growth towards the outstanding ECTC 2025 we have today.

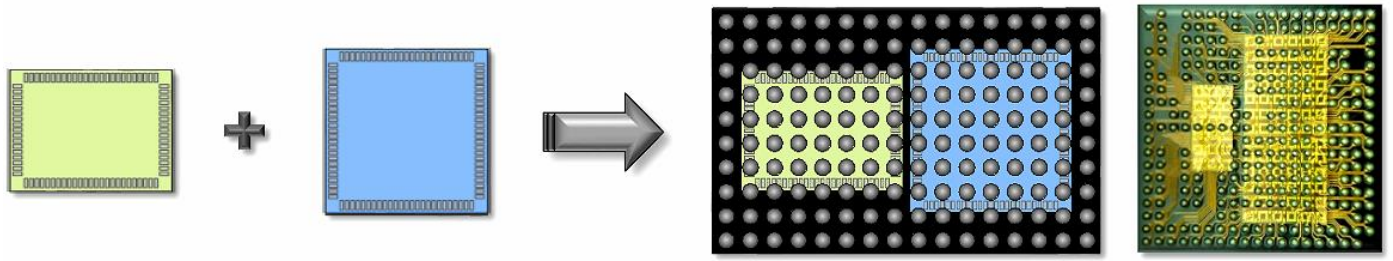
*Reference: Presentation to IEEE Electronics Packaging Society BoG June 5th ,2010.

Fan Out Developments from A to D

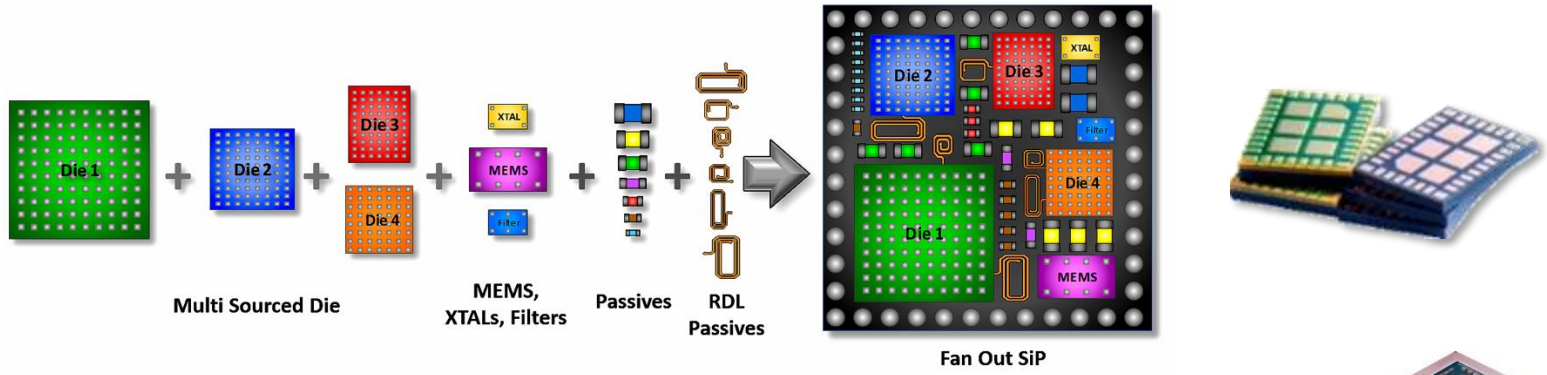
A. Die Shrinkage (2008)



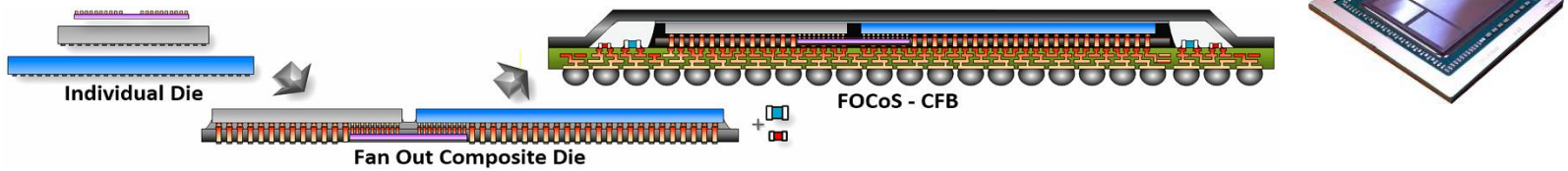
B. Heterogeneous Integration



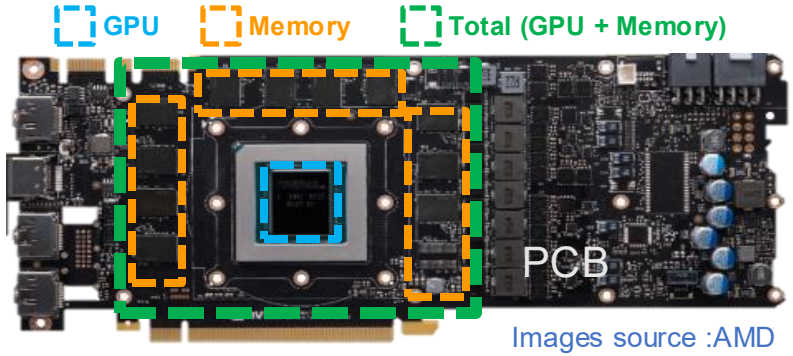
C. Fan Out SiP / Module



D. Fan Out Chip-on-Substrate FOCoS



2.5D with Si Interposer towards 3D Integration

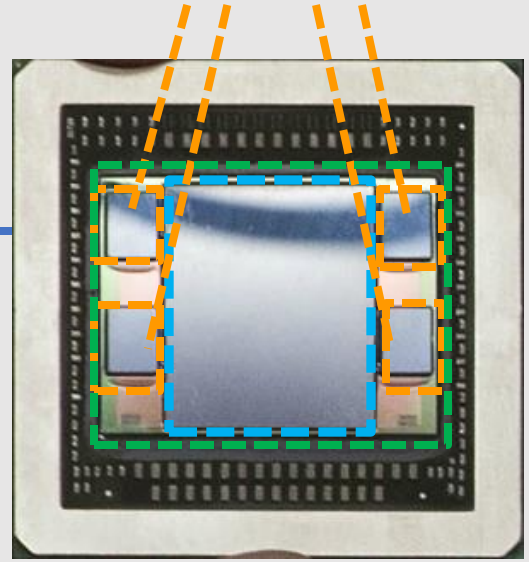


Images source :AMD

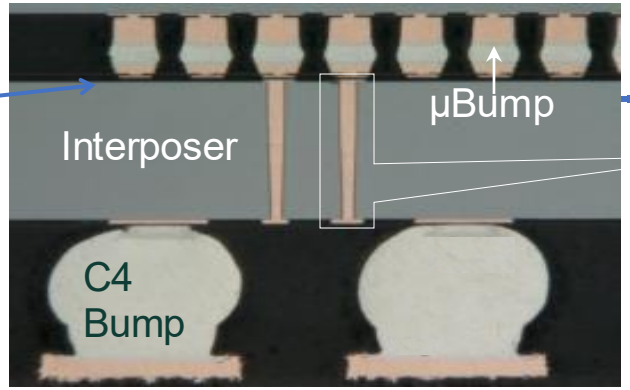
CHIPLETS INTEGRATION
70%
SYSTEM SIZE REDUCTION

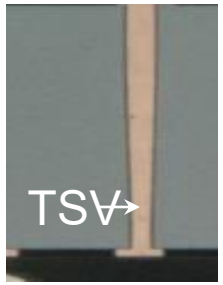
2.5D + 3D IC

HBM (High Bandwidth Memory)



Fine L/S:
0.5um/0.5um

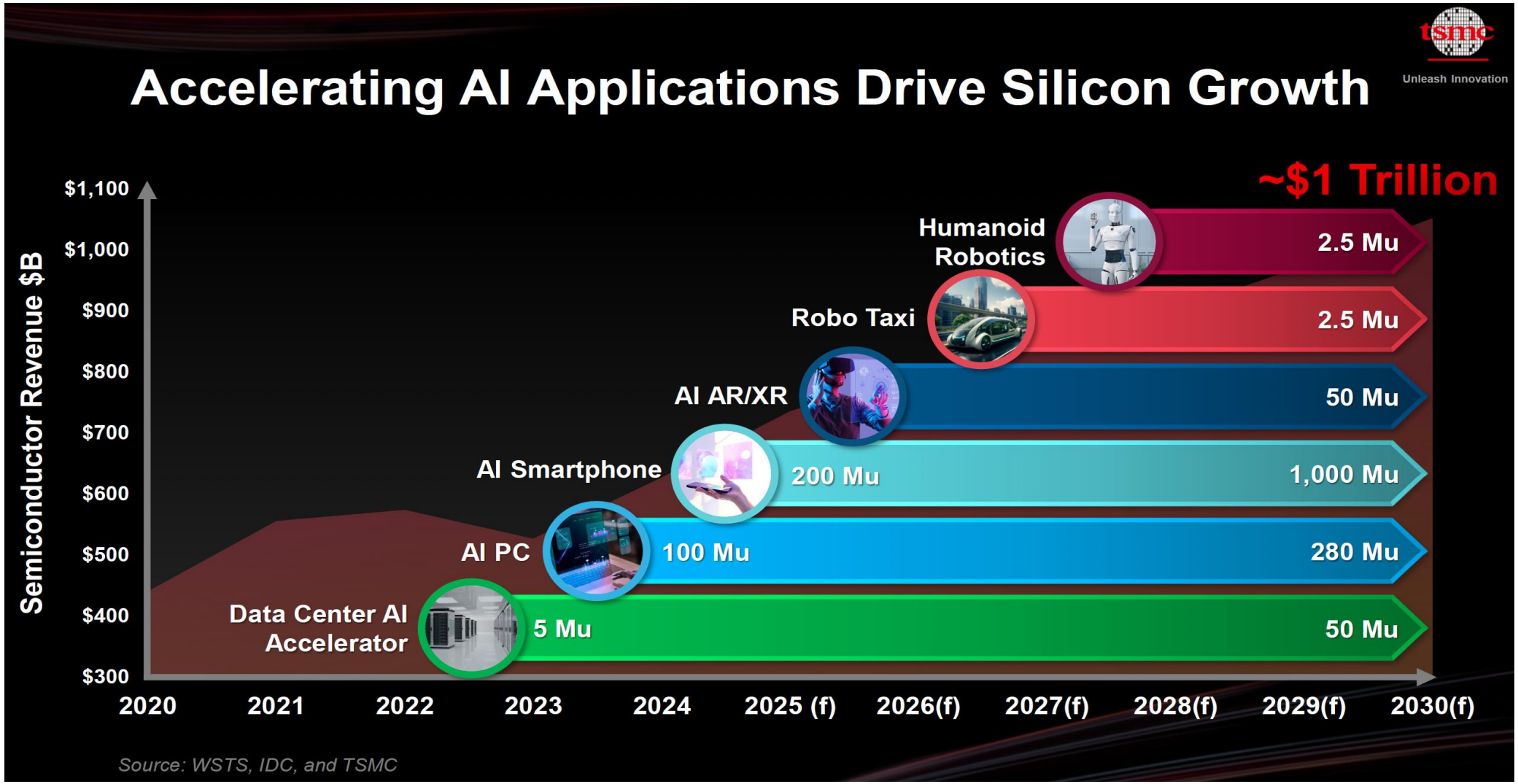




- > 20x more bumps vs. FCBGA
- Si Interposer line/space, 30x smaller vs. substrate

World's 1st 2.5D with x4 HBMs
Released June 2015
AMD & ASE Joint Collaboration

Unlimited potential for AI



Source: Kevin Zhang TSMC SVP Deputy CoCOO. April 2025 TSMC Press Briefing

Parting words

- Celebrating 15 years anniversary since the ‘Buy-out” to form Full EPS ECTC Sponsorship : ECTC 2025 continues to expand its scope in both innovation and application while remaining dedicated to the dynamic microelectronics profession with record high 2400 attendees.
- Incubated through close collaboration across the ecosystem, innovations in heterogeneous integration including (Fanout and 2.5D) thrive and evolve with new creativities & innovations across the packaging technologies & science landscape.
- The future is unlimited, with packaging enriched by AI driven innovations & creativity to help global impact and energy efficiency towards the betterment of the global society.
- I have no doubt that at 100th ECTC the new generation of sessions will feature AI /ML driven breakthroughs in science & technology unimaginable today.

Acknowledgements

Special acknowledgement to Dr CP Hung for sharing his excellent material from his OFC 2025 presentation, and to John Hunt for sharing his low/high density fanout development material.

Thanks to many colleagues & dear friends for the ECTC 2010 Collaboration & Transition to Full EPS ECTC Sponsorship.

How it was, is, and will be!
My Perspective

Kitty Pearsall
EPS Junior Past President
Capstan Technolgies

Component Hybrid Manufacturing Technology (now ECTC) – Late 80's to 2010

ECTC Technology Content in late 1987 to 2010 driven by:

Environmental regulations of manufacturing component assembly processes driven by restrictions:

- ✓ CFCs - Ozone depleting chemicals
- ✓ TRI – Toxic Release Inventory Chemicals

Assembly process Materials development driven by environmental regulations

- ✓ RoHS -- Restriction of Hazardous Substances (PbSn rosin-based solder transitions to water soluble PbSn and low residue PbSn to Pb free solder)
- ✓ WEEE -- Waste from Electrical and Electronic Equipment phased out/replaced

Component manufacturing processes PTH, SMT (ASICs, MCMs, Chip Scale Packages)

Dissemination of annual ECTC content:

ONLINE: Password protected ECTC 2024 digital proceedings for on-line browsing and download; Just Login here: https://conferences.computer.org/ectc

Innovations/Technologies are Plentiful - 2025

"… semiconductor manufacturers seeking innovative technologies and processes to stay competitive and meet ever-increasing consumer, and industrial demands turn to digital twin technology."

More focus on "smart manufacturing" in the semiconductor industry through integration of advanced technologies, AI, robotics, and machine learning

- ✓ Enhance automation
- ✓ Collect massive amounts of data through manufacturing assembly processes steps
- ✓ Utilize AI and IOT to analyze data gathered and through the use of many algorithms to drive process improvement and optimization

In-depth analysis applying digital twins to the semiconductor supply chain

- ✓ Enhance cybersecurity (cryptography) for semiconductor supply chain to protect supplier data, supplier process data, quality and reliability output of finished product
- ✓ Ensure continuity of supply for bill of materials

Introduction of new advanced packages

Projection → EV global car market share is expected to surpass 40% by 2030, with global sales projected to exceed 20 million by 2025, capturing over a quarter of the car market (International Energy Agency (IEA)).

- ✓ Expansion of EV charging stations by government/businesses to meet projected EV growth
- ✓ Increase of driving distance that is limited by current battery design by developing solid-state batteries
- ✓ Toyota SSB anticipated in 2027 with Volkswagen and Renault following 2027
- ✓ Smart electric vehicle charging technology will have to grow in the next decade to this increase
- ✓ Enhance ADAS Technology (Advanced driver-assistance systems)
- ✓ Standards developed for solid state batteries and smart electronic charging technology
- ✓ Ensure global supply challenges are met for “new materials and advanced packages” for EVs

Projection → Global Chip Packaging Market Size to grow from USD 45.87 billion to USD 82.03 billion by 2033 (McKinsey & Company)

Quantum Computing

- ✓ Anticipated to revolutionize semiconductor industry
- ✓ Not readily adopted today; requires time to mature
- ✓ Needs organizational readiness and proof-of-concept exploration

Quantum Computing sectors include AI, R&D in Technologies, Cybersecurity, Healthcare, Material Development, Energy, Finance, …

- ✓ Potential to decrease time for chip design by using algorithms developed by quantum computing
- ✓ Classical HPC continues to grow but because of Moore's Law winding down, the increasing costs of supercomputers, and the heavy power demand the HPC performance takes a hit. BUT Quantum computing can overcome HPC limitations
- ✓ Augment "classical" HPC by taking on specialized workloads

Materials more easily developed and analyzed (superconductivity, solid state batteries, …)