The 2026 IEEE 76th Electronic Components and Technology Conference

CALL FOR PAPERS

May 26 -29, 2026 • JW Marriott & The Ritz-Carlton Grande Lakes Resort, Orlando, Florida, USA

INTRODUCTION

On behalf of the IEEE Electronic Components and Technology Conference (ECTC) Program Committee, it is my pleasure to invite you to submit an abstract for the 76th ECTC, to be held May 26–29, 2026, at the JW Marriott & The Ritz-Carlton Orlando, Grande Lakes, Orlando, Florida. Recognized as the leading international conference in the semiconductor packaging industry, and sponsored by the IEEE Electronics Packaging Society (EPS), ECTC presents cutting-edge research and technical developments in electronics packaging including 2.5D and 3D heterogeneous integration, chiplet architectures, hybrid bonding, panel level packaging, flip-chip technologies, fan-out and fan-in packaging, integrated photonics, advanced materials such as glass substrates, and other critical aspects of system-level packaging.

The ECTC Program Committee consists of over 200 experts from diverse technical fields and is dedicated to creating an engaging technical program. ECTC regularly draws more than 2,000 attendees from over 20 countries and has become the event of the year for the whole electronics packaging community and the supply chain partners to get together once a year. The 75th Anniversary ECTC was an outstanding success and a memorable celebratory event, setting new records with 775 abstract submissions, a record number of exhibitors, and 2,517 registered attendees from 22 countries. It featured 390 technical papers presented in 36 oral sessions and five interactive sessions, including a session dedicated to students. Additionally, eight special sessions covered a variety of advanced packaging topics, such as ultra-high density interconnect technologies and supply chain readiness for artificial intelligence (AI) & high-performance computing (HPC), hybrid bonding, advancements in chiplet integration and the significance of utilizing glass core vs. redistribution layer (RDL) interposers as well as the thermal management solutions for next generation applications. These special sessions provided an open platform for subject matter experts to discuss current challenges and advancements in the packaging industry in an interactive format. On Wednesday morning, Sam Naffziger of AMD delivered an excellent keynote talking about tomorrow's compute needs for the AI era. The ECTC Exhibition showcased products and services from 136 exhibitors with invaluable support from our generous sponsors. The 76th ECTC will continue with the same tradition of being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become the enabler of tomorrow's compute needs versus just providing a protection and connection to the silicon chip.

The 76th ECTC will include special sessions such as an Heterogeneous Integration Roadmap (HIR) workshop and, concurrently, a diverse array of Professional Development Courses (PDCs) on the first day of the conference (Tuesday). Esteemed leaders in their respective fields will lead the special sessions discussing the cutting-edge topics within electronics packaging in an interactive platform where our attendees are encouraged to join the discussions with subject matter experts. Renowned experts will conduct the PDCs, enabling participants to expand their technical expertise. During the following three days, six parallel technical sessions will offer the most recent research and advancements in electronics packaging R&D, along with special panel discussions that highlight industry trends and best practices. Complementing the technical program, the ECTC Exhibition will feature leading companies specializing in electronic components, materials, and packaging, showcasing their latest innovations.

On behalf of the ECTC Program Committee, I look forward to seeing you at the 76th ECTC, during May 26–29, 2026, at the JW Marriott & The Ritz-Carlton Orlando, Grande Lakes, Orlando, Florida. Be there not to miss the only event that brings together the whole electronics packaging community and supply chain partners together from all over the world once a year!

Bora Baloglu, 76th ECTC Program Chair

MAJOR TOPICS

Highly rated abstracts are accepted for presentation at the ECTC conference. During abstract submission, authors are asked to choose the subcommittees whose topic areas best fit their abstracts. Please select two different program subcommittees in order of preference that should evaluate your submission for acceptance. Abstracts are rated according to the included original and previously unpublished, non-confidential, and non-commercial information on new developments, technology, and knowledge in the areas including, but not limited to, those given in the next ten paragraphs, one for each of ECTC's technical subcommittees.

Applied Reliability: 2D, 2.5D, 3D, chiplets/heterogenous integration, Si bridge, WLCSP, FOWLP, FOPLP, co-packaged optics (CPO), LED, memory devices, IOT, autonomous vehicles/automotive, wire bonded packages, sintered modules, micro-bump, micro-pillar, Cu-pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip interconnects, harsh environments, power modules, renewable energy systems, data center application, liquid cooling/ immersion cooling, thermal materials (TIM), medical electronics, wearable electronics, displays, AI application, computing, networking systems, HPC, mobile systems, fault isolation techniques, metrology, material characterization, use-condition, stress methodology

Assembly & Manufacturing Technology: Embedded, power, magnetics, embedded die and passives in substrates, controlling warpage, thermal dissipation, package stress, AI/HPC/SerDes packages (2.5/3D), application of glass, hybrid materials, substrates, interposers for 2.5D/3D, innovations in conductive fine pitch traces, via manufacturing, AI/HPC SerDes packages, innovative packaging processes, methodologies, materials, tools enabling panel level packaging (PLP), cost-efficiency/yield perspective, high yield organic interposer 2.xD for panel level packaging (PLP)

Electrical Design & Analysis: Cloud computing, autonomous vehicles, AI/machine learning, large language models (LLMs)/generative AI, high-frequency (RF, mmWave, THz), 5G/6G, IoT, antennas, antenna-in/on-package (AiP/AoP), sensors, power transfer, wired/wireless communications, RF to THz, multi-physics/multiscale modeling & characterization of interconnects, modules, components, systems, chiplet, heterogeneous integration, chip-to-chip/die-to-die, SiP/MCM/system co-design (chip/package/board), UCIe/HBM/HPC, SerDes, high-bandwidth, 3D integration/hybrid bonding, opto-electrical (OE) hybrid integration, co-packaged optics, analog packaging, power electronics modeling/characterization, signal integrity, power integrity, EMI/EMC

Emerging Technologies: Novel materials, packaging architectures, additive manufacturing, harsh environments, system technology co-optimization (STCO), smart manufacturing, digital twin, sensor integration/packaging, flexible electronics, implantable electronics, medical/bio-electronics, integrated power challenges, power delivery, thermal solutions, high current/high voltage devices, metrology and characterization, benchmarking, failure analysis, hardware security, quantum computing, cryogenic electronics, sustainability, emerging AI technologies

Interconnections: Chiplet heterogeneous integration, hybrid bonding (C2W& W2W), fan-out wafer level packaging, fan-out panel level packaging, through silicon via (TSV) and nano-TSV through glass via (TGV), through mold via (TMV), 2.5D/3D, silicon/glass/organic interposers, silicon bridges/local silicon interconnects, glass core substrate/advanced multi-core build-up substrate, fine-pitch/multi-layer RDLs, system-in-package (SiP), wafer-level system integration, panel-level system integration, thermo-compression/laser assisted/transient liquid phase bonding, low temperature solders, flip-chip, micro-bump, Cu pillar, wirebond, Al ribbon bond, warpage mitigation, emerging technologies, optical interconnects, printable/flexible interconnects, interconnects for SiC/GaN and wide bandgap, materials/chemistries, conductive/non-conductive adhesives, anisotropically conducting film (ACF), underfill materials and molding compounds, thermal interface materials and novel cooling techniques, metrologies, characterization techniques, thermal/mechanical/electrical tests and reliability, sustainable interconnects, chiplet interconnect design and validation, standards (UCIe/BoW etc.), design and characterization for backside power delivery network (BPDN), integrated IVR and passives

Materials & Processing: Hybrid bonding, fan-out packaging, silicon/glass interposer, 2.5D/3D integration, chiplet integration process, wafer-to-wafer bonding, through-silicon via (TSV), die-to-wafer stacking, wafer-level packaging (WLP), panel-level packaging (PLP), redistribution layer (RDL), die-embedding processes, panel-scale lithography, glass carriers, thinning and handling, system-level scaling, polymer TIMs, solder and liquid-metal TIMs, emerging TIMs, die-attach materials, thermo-mechanical reliability, high-temperature stable materials, hermetic sealing materials, shock-resistant compounds, low-k/low-loss dielectrics, dielectric deposition processes, dielectric patterning, capillary underfill (CUF), reworkable underfills, molded underfills (MUF), wafer-level molding materials, thermally conductive underfill/molding compounds, temporary bonding adhesives, temporary bonding carriers, UV-release adhesives, thermal-release adhesives, debonding processes, low-temperature adhesives, conductive adhesives, adhesive residue suppression, silicon/glass core substrates, substrate-like package (SLP), novel substrate materials, AI-enhanced materials and processes, low-temperature solders, high aspect ratio vias, electromagnetic interference (EMI) shielding materials, materials for co-packaged optics (CPO)

Packaging Technologies: Architectures, integration, thermal solutions of 2.XD, 3D heterogeneous packaging including co-packaged optics (CPO)/co-packaged copper (CPC), silicon/organic/glass/diamond interposers and related packaging technology including CPO/CPC, hybrid/other die-to-die bonding, TSV, backside power delivery, embedded die/bridge/passives, fan-out wafer/panel-level packaging, automotive, wireless power and power electronics including SiC/GaN/PMIC/SPS, bio/medical, RF, MEMS, sensors, wireless, flexible/wearable, IoT

Photonics: Co-packaged optics (CPO), inverse design, hybrid bonding, heterogeneous materials, 2.5D/3D, PIC assembly, wafer-scale integration, interconnects, datacom, telecom, optical computing, high density I/O, data processing, 5G/6G, IoT, AI, space, radiation hard, low volatile organic compound (VOC) adhesives, high-temperature, vibration and shock resilience, atmospheric, automotive, defense, healthcare, green energy, agriculture, climate monitoring, underwater, low power, materials, connectors, packaging materials, fiber attach unit (FAU) and detachables, metamaterials, metasurfaces, fiber bundle connections, low size/weight/power/cost (SWaP-C), characterization, equipment, packaging tools, 3D printing, micro-optics, free space optics, microscopy, fiber attach

Thermal/Mechanical Simulation & Characterization: Thermal and mechanical simulation and characterization across packaging technologies, package level, board level, system level, measurements & characterization, correlations, sensitivity & statistical analysis, reliability modeling and testing, material constitutive relations, fatigue, fracture mechanics, warpage, electromigration, vibration, shock and drop, moisture, modeling for harsh environments, thermo-mechanical, thermal management, cryogenic, humidity, chemical, chip-package interaction for heterogeneous integration, co-packaged optics, novel modeling techniques, multi-scale physics, model order reduction, AI/ML, digital twin, credible simulations for virtual release, co-design approaches, computational fluid dynamics (CFD) and process simulations, model verification

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

Visit the ECTC website (www.ectc.net) for additional conference information.

Abstract and Manuscript Submission

As the Program Chair of the 76th ECTC, I extend a warm invitation for you to electronically submit your abstract at www.ectc.net, utilizing the "Author Info" tab. Your abstract should provide comprehensive details of your proposed technical paper, including findings and results, within a maximum limit of 700 words. Additionally, please include a concise paragraph, not exceeding 50 words, highlighting the novelty of your work. You also have the option to submit a supporting figure or table if desired. The deadline for abstract submission is **October 6, 2025**.

During the submission process, please ensure to provide the affiliation, contact telephone number, and e-mail address for all co-authors in the desired order. Additionally, include the mailing address of the contact author and specify the name of the presenting author. Please note that only co-authors are permitted to serve as presenters at ECTC. Submitted abstracts become the property of ECTC, and ECTC reserves the right to publish the abstracts accepted for the conference. ECTC also reserves the right to prohibit, limit, or decline any editing of submitted abstracts.

Prior to all submissions, please ensure that you have received the necessary clearance from management and co-authors, where applicable. By December 8, 2025, authors are notified of abstract acceptance along with instructions for manuscript preparation and paper presentation. Contact authors of accepted abstracts are kindly requested to confirm the acceptance, which signifies the commitment to submit the manuscript within the specified timeframe and present the paper in-person as an author on-site at the conference. The Program Committee may, at their discretion, consider submitted abstracts for inclusion in the Interactive Presentation sessions.

Upon acceptance of your abstract, please submit your manuscript (4-8 full pages) for review by February 20, 2026. **Manuscripts not submitted by this date may be removed and replaced in the final program at the discretion of the Program Committee.** To be included in the Conference Proceedings, your abstract must be accepted, and your manuscript must fulfill all requirements, including timely response to reviewer requests following the manuscript submission deadline. Our Technical Committee members conduct a thorough review process to ensure content quality and scientific accuracy for all accepted manuscripts.

All abstracts and manuscripts must be original, previously unpublished, devoid of commercial content, and non-confidential. It is essential that your manuscript adheres to the specified ECTC format and upholds the principles of professional integrity by avoiding any instances of plagiarism and excessive redundancy (use of previously published work). All submitted manuscripts are checked for such plagiarism utilizing the IEEE CrossCheck service.

Similar to last year, first-time leading authors of successfully presented papers have the opportunity to participate in a special raffle prize drawing during the conference. Furthermore, following the conference, a collection of outstanding papers may be invited (with appropriate revisions) for peer-reviewed publication in special sections of the prestigious IEEE Transactions on Components, Packaging, and Manufacturing Technology.

If you have any questions, contact:
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Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose first author receives an ECTC personalized certificate and a check for $3,000.

Best Interactive Presentation Award: Each year the ECTC selects the best Interactive Presentation paper whose first author receives an ECTC personalized certificate and a check for $2,000.

Outstanding Paper Award: An outstanding conference paper is also selected for special recognition by the ECTC. The first author receives a personalized certificate and a check for $2,000.

Outstanding Interactive Presentation Award: An outstanding Interactive Presentation paper is also selected for special recognition by the ECTC. The first author receives a personalized certificate and a check for $1,500.

Intel Best Student Paper Awards: Intel Corporation is sponsoring awards for the best papers submitted and presented by a student at ECTC. The winning student will be presented with a certificate and a check for $2,500 (Best Student Paper) or $1,500 (Outstanding Student Paper).

Texas Instruments Outstanding Student Interactive Presentation Award: Texas Instruments is sponsoring an award for the best student Interactive Presentation at ECTC. The winning student will be presented with a certificate and a check for $1,500.

Sponsorship Opportunities to Enhance Your Presence at ECTC

ECTC offers many unique sponsorship opportunities that provide highly visible exposure for your company. Additional information is available at www.ectc.net under "Sponsors". Please contact:

Alan Huffman, ECTC Sponsorship Chair
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ECTC Exhibition

We invite you to be part of the ECTC Exhibition and showcase your products and services to engineers and managers from all areas of the microelectronics packaging industry. Again, over 2,000 attendees are expected for the 76th ECTC, representing companies from around the world.

Exhibit Dates: May 27–28, 2026

For more information, contact:
Chris Bower, ECTC Exhibits Chair
E-mail: chris.bower@ectc.net; exhibits@ectc.net

The 2026 exhibit information brochure will be posted online at www.ectc.net under the "Exhibits" section in August 2025. ECTC exhibit booth allocation is based on consecutive years of exhibit participation and/or Gold or Platinum sponsorship. Please contact Chris Bower at chris.bower@ectc.net and exhibits@ectc.net for more information or with any questions.

Call for Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on topics described on the previous page. From the proposals received, up to 16 PDCs will be selected for offering at the 76th ECTC on Tuesday, May 26, 2026. Instructors of selected PDCs will be given a minimum honorarium of $1,500. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. Attendees of the PDCs will be offered Continuing Education Units (CEUs) or Professional Development Hours (PDHs). These CEUs and PDHs are recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives, Course Outline, Who Should Attend," 200-word proposals must be submitted via the ECTC website at www.ectc.net by October 6, 2025. Authors will be notified of course acceptance with instructions by December 8, 2025. If you have any questions, contact:

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IEEE EPS Society Travel Grant Program

IEEE EPS is pleased to continue the IEEE EPS Travel Grant Program for the 76th ECTC. The goals of this award are to foster maximum student participation in ECTC and to recognize students with superior ECTC papers. We encourage all student authors to apply for this prestigious grant that will allow you to participate fully in the premier conference for electronic packaging.

Description: Grants are available to apply towards actual travel expenses, including airfare, hotel, and meals. Grants will be awarded competitively, based on abstracts submitted by student authors. The student who is named as the primary author of each winning abstract will receive a travel grant.

Eligibility: The competition is open to all full-time graduate students enrolled at an accredited institution in a program of study within the scope of ECTC. The student must be listed as the primary author on the abstract. A maximum of two authors (one per paper) from any one institution will receive a travel grant.

Application Process: To apply, check the "IEEE EPS Society Travel Grant" box in the "Awards" section of the online abstract submission form. Pre-selected abstracts based on technical committee scores will be requested to submit an extended abstract.

Intel Student Paper Awards

Intel Corporation is sponsoring awards for the best paper and an outstanding paper submitted, first authored, and presented by a student at the ECTC. The winning student will be presented with a certificate and a check for $2,500 for Best Student Paper and $1,500 for Outstanding Student Paper.

Eligibility: To be considered for the award, the student must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author (contact author and first author) and present the paper at the upcoming conference. Finalists will be determined by a review of the completed manuscripts by the judging committee. Manuscripts will be reviewed for relevance to the competition topics, technical content, and originality.

The author of the best and the outstanding student paper will be notified after the conference and must submit an affidavit from the student's faculty advisor certifying that the student meets the eligibility requirements.

Application Process: To enter the Intel Student Paper Awards competition, please check the "Intel Best Student Paper Award" box in the "Awards" section of the online abstract submission form.

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