The 2026 IEEE 76th Electronic Components and Technology Conference

May 26 – 29, 2026

2026 Advance Program

JW Marriott & The Ritz-Carlton Grande Lakes
Orlando, Florida, USA

Sponsored by IEEE Electronics Packaging Society, IEEE

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INTRODUCTION FROM THE IEEE 76TH ECTC PROGRAM CHAIR BORA BALOGLU

The 2026 IEEE 76th Electronic Components and Technology Conference (ECTC) at JW Marriott & The Ritz-Carlton Grande Lakes, Orlando, Florida • May 26 - 29, 2026

On behalf of the Program and Executive Committees, I am pleased to invite you to the IEEE 76th Electronic Components and Technology Conference (ECTC). Sponsored by the IEEE Electronics Packaging Society, this premier event will be held May 26–29, 2026, at the JW Marriott & The Ritz-Carlton Grande Lakes in Orlando, Florida. As the world's leading microelectronics packaging conference, ECTC unites over 2,000 global professionals—including top manufacturers, design houses, foundries, and researchers. Join us to engage with key stakeholders and explore the breakthrough technologies shaping the future of the industry.

The 76th ECTC returns with an exceptional program, building on last year's record-breaking attendance to deliver another premier experience for the microelectronics community. The conference will start with eight special sessions held on Tuesday, featuring parallel tracks where industry-leading panelists tackle the field's most pressing challenges and emerging technical innovations.

Following the successful debut of the Student Challenge, the 2026 conference will feature the second annual Student Innovation Challenge. The updated format includes three distinct categories for BSc, MSc, and PhD candidates, with winners to be officially announced during the Friday Luncheon.

Additionally, the Start-Up Competition Challenge will take place on Thursday. This event provides a platform for emerging companies to pitch their business ideas to a professional jury, followed by an audience Q&A, jury deliberation and award presentation.

The conference will conclude its major networking activities with the ECTC Reception Gala on Thursday evening. This hallmark event gathers all attendees for high-level networking and technical exchange in a collaborative environment.

At the 76th ECTC, approximately 450 technical papers will be presented in 36 oral sessions and five interactive sessions. Authors from over 20 countries will share their latest research on topics including: 3D integration, 2.5D architectures, bridge and chiplet integration, hybrid bonding, wafer-to-wafer and chip-to-wafer bonding, novel substrate materials, high-density RDL, next-generation interconnections, warpage management of large panels, and large-package manufacturing, additive manufacturing, wearable and medical applications, AI/ML, and advanced RF and antenna designs, thermal management, interconnect reliability, advanced characterization, and process simulations, eco-friendly packaging, and secure designs. The 76th ECTC serves as a global platform for exploring cutting-edge advancements in microelectronic packaging, fostering innovation, and addressing industry challenges.

This year, the conference features a total of twelve special sessions with industry experts, including nine on Tuesday, each lasting 90 minutes.

Following last year's successful model, the Tuesday schedule includes two concurrent tracks of special sessions. The first session, exploring Quantum Infrastructure for AI Applications, will be co-chaired by Rabindra Das (MIT Lincoln Laboratory) and Pavel Ray Palladi (NVIDIA). The second special session, which focuses on New Packaging Technologies for Panel Level Integration, will be chaired by Venkata Mokkapati and Markus Leitgeb (AT&S), with Rozalia Beica (Rapidus) serving as moderator. Tuesday morning also features two additional parallel tracks. Session five addresses System Integration Challenges for large-scale, high-power components in HPC and AI applications, led by chairs Tae-Kyu Lee (Cisco Systems, Inc.) and Peng Su (Hewlett Packard Enterprise). Following this at 10:30 AM, Session 6 focuses on Electrical-Thermal-Mechanical Co-design in high-performance packaging, chaired by Tiwei Wei (UCLA) and Ning Ye (Sandisk). The first afternoon session, AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging, will be co-chaired by Ian O'Connor (Ecole Centrale de Lyon) and Jose Schutt-Aine (University of Illinois at Urbana-Champaign). In parallel, session seven will explore Enabling Next Generation Advanced Technology from Wafer to Panel chaired by Kuldip Johal (MKS Instruments) and Beth Keser (Voltanis Semiconductor).

Concluding the afternoon, two final sessions will run in parallel starting at 3:30 PM. Session four, titled Photonics-Based Systems for AI and Exascale Computing, will be chaired by Stephane Bernabé (CEA-LETI) and Lars Brusberg (Corning, Inc.). Simultaneously, an additional session will explore Innovative Materials for Advanced Packaging, led by chairs Zia Karim (Yield Engineering Systems) and Ksenija Varga (EV Group).

Parallel to the special sessions, the Heterogeneous Integration Roadmap (HIR) workshop will be chaired by William Chen (ASE) and Ravi Mahajan (Intel).

Tuesday evening offers additional opportunities to engage. Aakrati Jain (IBM) will lead a Young Professionals Networking Event from 6:45 p.m. to 7:45 p.m. Following this, Takashi Hisada and Yasumitsu Orii (both with Rapidus) will chair the IEEE EPS Seminar on Redefining System Integration: The Rise of Organic Substrates from 7:45 p.m. to 9:15 p.m.

On Wednesday morning, May 27, 2026, ECTC will feature a keynote presentation on Advanced Packaging & the Future of System Optimization by Dr. Tien Wu, CEO of Advanced Semiconductor Engineering (ASE), invited by General Chair Michael Mayer (University of Waterloo).

The Student Engagement Program, chaired by Ibrahim Guven (Virginia Commonwealth University) and Przemyslaw Gromala (Robert Bosch Kft), will also take place throughout the day, welcoming undergraduate students from local universities and colleges.

On Thursday, May 28, 2026, from 8:00 to 9:15 a.m., a Plenary Session will ask the question and discuss "Efficiency Is Not Enough – Are We Solving the Wrong Problem in Data Center Energy Use?" which will be chaired by Jan Vardaman (TechSearch International) and Maria Gorchichko (Applied Materials)

Finally, the IEEE EPS President's Panel covering data centers with a discussion entitled "Data Centers in the Age of AI – Challenges and Solutions" organized by IEEE EPS President Jeff Shuling (Auburn University) and EPS Members David McCann (Amkor Technology) and Kanad Ghose (Binghamton University) will be held on Friday morning, May 29, 2026.

ECTC offers 16 CEU-approved Professional Development Courses (PDCs). These are organized by Kitty Pearsall and Jeffrey Suhling and taught by content experts. They will be held on Tuesday, May 26, 2026.

The ECTC Exhibits, running Wednesday, May 27, and Thursday, May 28, showcase cutting-edge technologies and products from over 100 leading companies in electronic components, materials, packaging, and services. Starting daily at 9 a.m., the exhibits provide excellent opportunities for networking during coffee breaks, luncheons, and evening receptions.

Whether you are an engineer, manager, student, or executive, ECTC offers unique experiences for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 76th ECTC and to be a part of all the exciting technical and professional opportunities.

I want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 76th ECTC a success. I look forward to meeting you at JW Marriott & The Ritz-Carlton Grande Lakes Resort, Orlando, Florida, from May 26 to 29, 2026.

Bora Baloglu
76th ECTC Program Chair
borabal@ieee.org

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76th ECTC ADVANCE REGISTRATION

Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions, **see page 32.**

Register early … save US$100 or more! All registrations received after May 8, 2026, will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the JW Marriott Grande Lakes Conference Center, Grande Registration Desk.

On-Site Registration Schedule

Registration is located at the Grande Registration Desk, JW Marriott Grande Lakes Conference Center.

Monday, May 25, 2026	3:00 p.m. – 6:00 p.m.
Tuesday, May 26, 2026	6:45 a.m. – 6:45 p.m.
Wednesday, May 27, 2026	6:45 a.m. – 4:00 p.m.
Thursday, May 28, 2026	7:00 a.m. – 4:00 p.m.
Friday, May 29, 2026	7:30 a.m. – 12:00 Noon

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. This conference, and the venue it is located in, are smoke-free environments, including vaping.

ITherm 2026

ITherm is co-located with ECTC. All ITherm sessions and exhibits will take place in the JW Marriott Grande Lakes Resort. For more information about ITherm 2026, please visit **www.ieee-itherm.net.**

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

ECTC Sponsors

With over seven decades of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 2,000 individuals and more than 150 organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company's interests. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors".

To sign up for sponsorship or to get more details, please contact **Alan Huffman at alan.huffman@ieee.org or +1-336-380-5124.**

Hotel Accommodations

Rooms for ECTC attendees have been reserved at The Grande Lakes Orlando Resort, including the JW Marriott and The Ritz-Carlton. The special conference rate for a single/double occupancy room is as follows:

JW Marriott: US $240++/night
The Ritz-Carlton: US $290++/night

Please note these rooms are on a first-come, first-served basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Room reservations must be made directly through the link at **www.ectc.net/location** or with the hotel by May 8, 2026, or until rooms run out, to ensure our preferred conference rate. All reservations made after the cutoff date of May 8, 2026, at 5 p.m. Eastern Time will be accepted on a space and rate availability basis. If you need to cancel a reservation, please do so by 5 p.m. Eastern Time, at least 5 days before arrival, for a full refund.

Check-in time: 4 p.m. & check-out time: 11 a.m.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2026 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2026 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (**www.ectc.net/location**). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there, and if it's too good to be true, it likely is. Should you have any questions about booking a hotel room, please contact ECTC staff at: **registration@ectc.net**.

Transportation Services

There is no complimentary transportation to and from the hotel and airport. All attendees must make their own transportation arrangements to the hotel upon arriving at the airport.

76th ECTC CONFERENCE OVERVIEW

2026 Special Session on Quantum Infrastructure for AI Applications

Quantum Infrastructure for AI Applications: Packaging Challenges and Roadmap

Tuesday, May 26, 2026, 8:30 a.m. – 10:00 a.m.

Chairs: Rabindra N. Das, MIT Lincoln Laboratory; Pavel Roy Paladhi, NVIDIA

Quantum computers can provide a platform to solve hard problems which are computationally intractable with traditional computer architecture. Packaging is a key bottleneck to scale quantum processors into AI-relevant accelerators. Major technical obstacles include cryogenics and thermal management, high-density low-loss interconnects, cryo-compatible control electronics, EMI/stray coupling, reliability and manufacturability. AI workloads demand high throughput, low latency, predictable QoS, and tight integration with classical accelerators and data pipelines — packaging must enable fast data movement and tight hybrid quantum-classical feedback. This special session will bring industry and academy leaders working on Quantum packaging hardware developments over the past two decades. The focus will be on future packaging challenges and roadmap for quantum applications. Packaging areas that need to be researched and tailored to prepare for large scale quantum computation implementation of higher fidelity systems will be identified. Aspects of various quantum technologies and corresponding hardware development will be explored. Our panelists have over 80 years combined experience in Quantum technology ranging from hardware built, quantum technology scope, applications, performance, analysis etc. They are highly experienced with development of prototypes, mapping applications to existing technology etc. Panelists will present and discuss some of the key challenges and directions that the research should be focused on. It is anticipated that this topic will become very significant to the computer packaging industry as well as the quantum computing world and this panel gives an opportunity for the ECTC community to be informed, be engaged and ready to contribute.

Brian Maertz, Google Quantum; Mark Gouker, MIT Lincoln Lab; William Oliver, MIT; Luu Nguyen, PsiQuantum; Michael J. Manfra, Microsoft Quantum; Bart Machielse, IonQ

2026 Special Session on New Packaging Technologies and Panel-Level Integration

New Packaging Technologies Enabled by Panel Level Integration

Tuesday, May 26, 2026, 10:30 a.m. – 12:00 Noon

Chairs: Venkata Mokkapati, AT&S; Markus Leitgeb, AT&S; Rozalia Beica, Rapidus

Innovation in semiconductors is reaching another milestone where advanced IC substrates when crossing paths with PLP (Panel Level Packaging) are opening new capabilities. With increasing technical, architectural/functional and market demands, new functionalities (power delivery, signal integrity, warpage control) are integrated into IC substrates through panel level solutions addressing evolving high-end applications like Si Photonics, Edge AI inference, Automotive and HPC. Potential technologies that address these challenges- due to- convergence are embedded components, glass core and UHD layers on the substrate. This is essential for such applications where heterogeneous integration is scaled to the panel level resulting in denser, faster, smart and high performing packages.

Join the team of experts from IDM/OEM, Foundry and OSATs where they discuss on what is needed to converge IC substrates, Panel Level Packaging and Heterogeneous integration, to build next-generation intelligent systems.

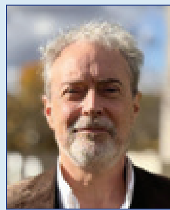
Omar Bchir, Qualcomm; Shin-Puu Jeng, AMAT; Muhannad Bakir, Georgia Tech; Habib Hichri, Ajinomoto; Kuldip Johal, MKS Atotech; Farhang Yazdani, Broadpak

2026 Special Session on AI-Enabled EDA

AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging

Tuesday, May 26, 2026, 1:30 p.m. – 3:00 p.m.

Chairs: Ian O'Connor, Ecole Centrale de Lyon, France; Jose Schutt-Aine, University of Illinois at Urbana-Champaign



The integration of multi-physics domains - mechanical, thermal, signal integrity, and electromagnetics - creates unprecedented challenges in electronic package design, requiring holistic and agile approaches beyond traditional methods. While AI has taken major strides in digital design, challenges in analog multi-physics packaging co-design are limiting progress.

This panel, organized conjointly by IEEE-CEDA and IEEE-EPS, explores the transformative role and challenges of AI and machine learning in EDA including AI-driven optimization and agentic AI systems. Panelists will discuss how AI-assisted optimization and design space exploration merge with physical modeling to tackle challenges in memory wall, disaggregation to chiplets, advanced package architectures, sharing insights from industry leaders to define next-generation requirements. The discussion will emphasize practical applications of AI for design space exploration (DSE-AI), co-simulation, and cross-domain optimization, as well as emerging paradigms for training, inference, and workflow automation in EDA. Additionally, the role and impact of Application Design Kits (ADKs) in enabling collaborative, scalable multi-physics AI co-design will be examined.

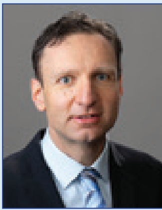
Christopher Bailey, Arizona State University; Madhavan Swaminathan, Pennsylvania State University; Hanzhi Ma, Zhejiang University; Nandish Mehta, NVIDIA Research; Jan Vardaman, TechSearch Intl.; David Atienza, EPFL; Norman Chang, Synopsys

2026 Special Session on Photonic-Based Systems

Photonic-Based Systems for AI and Exascale Computing

Tuesday, May 26, 2026, 3:30 p.m. – 5:00 p.m.

Chairs: Stéphane Bernabé, CEA-LETI; Lars Brusberg, Corning Inc.



Having emerged just a couple of years ago, CPO (Co-packaged Optics) has changed the paradigm of optical interconnects, driven by the artificial intelligence boom, and is on the way to realizing the electronics/photonics convergence promised by silicon photonics. As demonstrations based on the CPO approach multiply, the next stage is taking shape: photonic chiplet based architectures, Photonic Interposers, etc., opening the door to optical networks on chip, photonic switching or programmable photonics. The panel will present recent developments in CPO applied to AI, as well as challenges for these future applications: laser integration issues, development of silicon photonics, 3D co-integration methods as well as process implementation in foundries and OSATs.

Rebecca Schaevitz, Mixxtech; Severine Cheramy, Scintil Photonics; Farnood Rezaie, Cisco Systems; Shang Y. Hou, TSMC; Darius Bunandar, Lightmatter

2026 Special Session on System Integration Challenges

System Integration Challenges of Large-Size and High-Power Components for High-Performance Computing and AI Applications

Tuesday, May 26, 2026, 8:30 a.m – 10:00 a.m

Chairs: Tae-Kyu Lee, Cisco Systems, Inc.; Mike Gallagher, Qnity Electronics

Rapid advances in heterogeneous integration technologies are enabling the design and development of components with significantly larger form factors and substantially higher power densities than were feasible just a few years ago. As package sizes exceeding 100x100 mm^2 and power levels approaching or surpassing 1000 W become increasingly common in high-performance computing (HPC) and AI network systems, new challenges are emerging in system-level design and integration. These challenges span system manufacturing, component and PCB reliability, testing, and thermal management, all of which are experiencing heightened complexity and risk. At the same time, opportunities exist in component architecture, materials selection, and manufacturing processes to mitigate these challenges and accelerate the development of next-generation,

highly integrated systems. This special session will present and discuss key system integration challenges associated with large-size, high-power components for HPC and AI applications.

Hemanth Dhavaleswarapu, AMD; Mudasir Ahmad, Cisco: Richard Rao, Marvell; Dongji Xie, NVIDIA; Choong-Un Kim, University of Texas, Arlington

2026 Special Session on Co-Design in High-Performance Packaging

Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging

Tuesday, May 26, 2026, 10:30 a.m. – 12:00 Noon

Chairs: Ning Ye, Sandisk; Tiwei Wei, University of California, Los Angeles

As packaging complexity increases to support AI, HPC, and heterogeneous integration system, the interactions among thermal, mechanical, and electrical domains are becoming more tightly coupled—and more difficult to manage independently. Traditional design approaches that treat these domains in isolation are no longer sufficient for achieving system-level performance, reliability, and manufacturability required in advanced packaging.

This special session will focus on the growing need for co-design methodologies that bridge these domains. The session will feature panelists from key players across the supply chain, including EDA, OSATs, foundries, substrate suppliers, and system companies, who will share perspectives on real-world challenges, trade-offs, and co-optimization strategies.

Bill En, AMD; Gang Duan, Samsung Electro-Mechanics; CP Hung, ASE; Kathy Yan, TSMC; Kelly Morgan, Synopsys; Yu-Tao Yang, Mediatek

2026 Special Session on Wafer to Panel

Enabling Next-Generation Advanced Packaging Technology From Wafer to Panel

Tuesday, May 26, 2026, 1:30 p.m. – 3:00 p.m.

**Chairs: Kuldip Johal, MKS Instruments;
Beth Keser, Volantis Semiconductor; Liong Chao, ASE**

The fast growth of AI and HPC is driving demand for better performance, higher bandwidth, and improved power efficiency. The advanced chiplet integration combining CPU, GPU, ASIC, HBM, and co-packaged optics is becoming a key enabler. These designs require larger interposers and substrates, pushing the limits of traditional wafer-level packaging due to issues of large warpage, low yield, and limited wafer utilization. Panel-Level Packaging (PLP) is emerging as a promising solution, enabling larger format production with better scalability, yield, and cost efficiency. It also supports new technologies like embedded components, organic interposers, and glass core substrates that are the key for future systems in AI, HPC, automotive, and mobile devices. In this panel, experts from IDMs, Fabless, foundries, OSATs, Material and equipment suppliers will discuss how to bring panel-level integration into high-volume production.

Deepak Kulkarni, AMD; Abe Hidenori, Resonac; Ingu Yin Chang, ASE; Lee Chee Ping, LAM; Gang Duan, Samsung

2026 Special Session on Innovative Materials for Advanced Packaging

Innovative Materials for Advanced Packaging – Materials for Packaging, Integration, and Performance

Tuesday, May 26, 2026, 3:30 p.m. – 5:00 p.m.

Chairs: Zia Karim, Yield Engineering Systems; Ksenija Varga, EV Group

Special Session on "Innovative Materials for Advanced Packaging – Materials for Packaging, Materials for Integration, and Materials for Performance" which could cover a wide range of topics from Polyimide/ EMC to Build-up materials, HB Dielectrics, Exotic materials, Adhesion and Stress Buffer Layers, and Interconnect materials (Eless, UBM, Solder). The discussion will be to define well "the necessity" and the "must" factor to introduce new innovative materials to improve performance, to address a current node short-comings, or to reduce cost. This special session will review new materials for different areas of advanced packaging from substrates, to RDL, to Interposers, to chiplets and the integration thereof.

Kathy Yan, TSMC; Rama Puligadda, Brewer Science; Zsolt Tokei, IMEC; Seiichiro Ohashi, Ajinomoto Fine-Techno Co., Inc.; Hidenori Abe, Resonac Holding Corporation

2026 IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 26, 2026, 8:00 a.m. – 5:00 p.m.

Chairs: Ravi Mahajan, Intel Corporation and William Chen, ASE

This year's HIR Workshop at ECTC will feature four technical sessions, spanning Tuesday morning and afternoon, with the following preliminary agenda:

8:00 a.m. – 8:30 a.m.: HIR Welcome, Introduction, Agenda Review

8:30 a.m. – 10:00 a.m.: Additive Electronics Manufacturing (AME) for Advanced Packaging

10:30 a.m. – 12:00 Noon: CHIPS R&D Metrology

1:30 p.m. – 3:00 p.m.: Technical Session #3

3:30 p.m. – 5:00 p.m.: Technical Session #4

2026 ECTC Young Professional Networking Event

Tuesday, May 26, 2026, 6:45 p.m. – 7:45 p.m.

Chair: Aakrati Jain, IBM

Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2026 IEEE EPS Seminar on Organic Substrates in the Chiplet Era

Redefining System Integration: The Rise of Organic Substrates in the Chiplet Era

Tuesday, May 26, 2026, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada, Rapidus; Yasumitsu Orii, Rapidus

As chiplet-based architectures rapidly become the mainstream design paradigm, the role of the package substrate has evolved from a passive interconnect carrier to a decisive enabler of system performance, power efficiency, and heterogeneous integration. Even with new approaches such as NVIDIA's recently proposed CoWoP (Chip on Wafer on PCB), organic substrates remain at the heart of advanced packaging, serving as the essential platform that connects chiplets with wafers, large panels, and ultimately the system board.

This special session brings together leaders from across the ecosystem — industry trend experts, EDA solution providers, and leading substrate manufacturers — to discuss the challenges and innovations driving the next generation of organic substrates. Topics will cover market and technology trends shaping chiplet-based systems, co-design methodologies bridging package and system-level optimization, and manufacturing breakthroughs needed to deliver ultra-fine line and large-panel organic substrates at scale.

By uniting perspectives from system architects, design tool innovators, and substrate manufacturers, this session underscores that organic substrates are no longer just passive carriers, but the critical foundation enabling chiplet integration and next-generation high-performance systems in the post-Moore era.

2025 ECTC Keynote Talk

Advanced Packaging and the Future of System Optimization

Wednesday, May 27, 2026, 8:00 a.m. – 9:15 a.m.

**Chair: Michael Mayer, University of Waterloo, Canada
Speaker: Tien Wu, CEO of Advanced Semiconductor Engineering, Inc.**

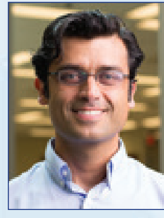
Global AI infusion is redefining performance, power, and integration requirements, placing advanced packaging at the forefront of semiconductor innovation. As chip architecture complexity increases, the industry is progressing beyond device-level scaling toward system-level optimization. Advances in heterogeneous integration and packaging-enabled co-design are shaping more efficient, scalable, and resilient systems. Moving forward, system-centric strategies that align architecture, packaging, and collaboration across the ecosystem are paramount to shaping the golden era of AI and semiconductors.

These sessions are open to all conference attendees.

2026 ECTC Student Innovation Challenges

Wednesday, May 27, 2026, 6:45 p.m. - 8:00 p.m.

Chairs: Przemyslaw Gromala, Robert Bosch Kft; Ibrahim Guven, Virginia Commonwealth University



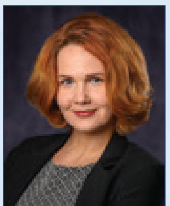
Finalists for the ECTC 2026 Student Innovation Challenges Competition in BSc/MSc and PhD level categories will make their presentations during this session. This competition allows participants to demonstrate their skills, apply their academic knowledge, and collaborate on innovative ideas in the field of electronic/photonic packaging. The winners in each category will be announced during the Friday luncheon.

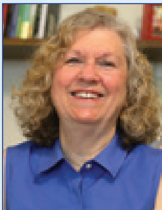
2026 Plenary Session on Data Centers Needs

Efficiency Is Not Enough: Are We Solving the Wrong Problem in Data Center Energy Use?

Thursday, May 28, 2026, 8:00 a.m. – 9:15 a.m.

Chairs: Masha Gorchichko, Applied Materials, Inc.; Jan Vardaman, TechSearch International, Inc.





This session will explore the key challenges and opportunities in improving energy use in data center applications, spanning hardware, system architecture, software, and infrastructure to showcase the complexity of the issue and highlight the necessity to adopt a holistic framework for the energy use conversation. We will discuss the role of cutting-edge packaging technologies influencing the energy consumption of high-performance applications.

David Lo, Google; Ankur Agarwal, Celestia AI; Raja Swaminathan, AMD; John Knickerbocker, IBM; Rich Bonner, Accelsius

2026 ECTC Start-Up Challenges

The Light Age: Strategic Investment in Photonics to Power the Next Computing Era

Thursday, May 28, 2026, 6:00 p.m. - 7:45 p.m.

Chairs: Rozalia Beica, Rapidus; Farhang Yazdani

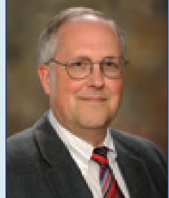
Start-up companies will pitch their innovative ideas to a panel, followed by audience Q&A, jury deliberation, and then awards and a networking event.

2026 IEEE EPS President's Panel

Data Centers in the Age of AI: Challenges and Solutions

Friday, May 29, 2026, 8:00 a.m. – 9:15 a.m.

Chairs: Benson Chan, Binghamton University; David McCann, Amkor Technology; Jeff Suhling, Auburn University



Discussion and Panel Moderated by: Prof Kanad Ghose, Binghamton University

Foundational/Large Language models for AI applications continue to drive the energy and natural resource demands for data centers. Projected energy demands of AI data centers are about to exceed the available energy sources. Hard-pressed utilities providing electricity to data centers have, in many cases, passed the cost of additional generation and distribution on to customers. The cooling needs for the AI data centers are also taxing the water sources. This is a crisis in the making and has to be addressed in a proactive manner to enable society-at-large to capitalize on the benefits of AI without overtaxing natural resources and without financial burdens on the public. This panel features presentations and discussion by area experts on the technology, economic and environmental challenges posed by AI data centers and potential solutions in the systems, microelectronics, and advanced packaging realm to address these challenges.

Luncheons

ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. The QR code on your registration badge is your access to lunch! Please come and enjoy time with other attendees and colleagues in the industry. Lunch times will vary; see below for specifics for each day.

Tuesday: **12:00 Noon – 1:15 p.m.**

Wednesday: **12:45 p.m. – 2:00 p.m.**
Sponsored by: ASE

Thursday: **12:45 p.m. – 2:00 p.m.**
Sponsored by: Amkor
Hosted by: EPS

Friday: **12:45 p.m. – 2:00 p.m**
Sponsored by: IBM
Don't miss out on this lunch! We will be raffling off several prizes, including a hotel stay, free conference registrations, and many other industry gadgets!

ECTC Student Reception

Tuesday, May 26, 2026, 5:00 p.m. – 6:00 p.m.
Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise!

General Chair's Speakers Reception

Tuesday, May 26, 2026, 6:00 p.m. – 7:00 p.m.
(by invitation only)

Exhibitor Reception

Wednesday, May 27, 2026, 5:30 p.m. – 6:30 p.m.

EPS Chapter Officer Meet and Greet

Thursday, May 28, 2026, 2:00 p.m. – 3:00 p.m.

All EPS Chapter Officers are invited in person to meet with other regional Chapter officers and share EPS Chapter activities and best practices.

Chapter Program Director: Andrew Tay
Regions 1–7 & 9 (Americas): Annette Teng
Region 8 (Europe and Africa): Steffen Kroehnert
Region 10 (Asia): Shaw Fong Wong

76th ECTC Gala Reception

Thursday, May 28, 2026 – 7:30 p.m.
Sponsored by Koh Young Technology

(All badged attendees are invited)

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PROFESSIONAL DEVELOPMENT COURSES

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MORNING COURSES
8:00 a.m. – 12:00 Noon

1. HIGH RELIABILITY SOLDERING IN ADVANCED SEMICONDUCTOR PACKAGING

Course Leader(s): Ning-Cheng Lee, ShinePure Hi-Tech

Course Description:
Semiconductor soldering is much more delicate and is very critical for reliability of devices. This course covers the critical parameters governing the reliability of soldering in semiconductor packaging. The reliability discussed includes parameters affecting the intermetallic compounds (IMC), voiding, electromigration, low temperature soldering, high temperature soldering, and electrochemical migration under a variety of material combinations. The failure modes are discussed in detail, with preferred choices of materials and designs recommended.

Course Outline:
1. IMC - Effect of Cu Pad Grain Size on IMC
2. IMC - Interaction of Cu and Ni
3. IMC - Effect of Base Metal Co-P on IMC
4. Voiding - Effect of Solder Form on Voiding
5. Voiding - Effect of Joint Height, Temperature, Electrical, Mechanical on Kirkendall Voiding
6. Voiding - Effect of Cu Structure on Kirkendall Voids
7. Electrochemical Migration (ECM)
8. Electromigration
9. LTS - Bi-Rich Whisker Growth
10. LTS - TCT Reliability of LTS
11. LTS - Collapse of LTS
12. LTS - Deposition, Hot Tear, Bi Stratification of LTS
13. LTS - Hot Tear of Homogeneous LTS BiSn - Effect of Profile
14. LTS - Drop Test of LTS
15. HTS - TLPB (Transient Liquid Phase Bonding)

Who Should Attend:
Anyone who cares about achieving high reliability solder joints for semiconductor packaging and wants to know how to achieve it should take this course.

IMPORTANT NOTICE
Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

2. PHOTONIC COMPONENTS AND PACKAGING TECHNOLOGIES FOR DATA CENTER, COMMUNICATION, SENSING, AND DISPLAYS

Course Leader(s): Torsten Wipiejewski, Huawei Technologies Duesseldorf GmbH

Course Description:
This course will provide an overview of the various photonic components and packaging technologies that enable optical interconnects, communication, sensing, and modern display applications. These applications are key for the information and communication technology of today and pave a way to the future. High speed optical interconnects from board level in data centers to long haul transmission systems require photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of various types including Vertical Cavity Surface Emitting Lasers (VCSELs), high speed optical modulators and photodetectors. AI has become a major driver to increase data throughput in data centers and high-performance computing. Optical interconnects provide a large bandwidth and can help to reduce energy consumption for data transfer. Bringing the optical engine close to the GPU/ASIC core is the target of co-packaged optics (CPO) solutions replacing the electrical signal lines on board level. Packaging technologies play a key role in the implementation of optical solutions, because the cost of the system is typically dominated by the assembly and packaging cost. Integration schemes such as photonic integrated circuits (PICs) have become mainstream technologies for cost and size reduction. Optical waveguides and the coupling of optical waveguides and components to optical fiber will be discussed. This is a key challenge in optical packaging because of the tight alignment tolerances.

Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitate the usage by end-users without specific medical knowledge. Today, displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. Current technologies and new developments such as quantum dots and micro-LEDs as well as some features of 3D displays will be reviewed. In particular, micro-LEDs for large size displays require novel assembly technologies to mount chips of only several micrometers in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

Course Outline:
1. Fundamental Properties of Photonic Components
2. Light Sources: LEDs, Laser Diodes, VCSELs, Others
3. Transmitter and Receiver Components in Optical Data Communication Systems: Lasers, Modulators, Photodetectors, Passive Optical Components, Optical Modules, Co-packaged Optics (CPO)
4. Monolithic and Hybrid Integration, Photonic Integrated Circuits (PICs), Silicon Photonics, Optical Waveguides and Optical Fiber Coupling, Assembly and Packaging.
5. Optical Sensing Elements and Applications: Spectrometers, Light Sources, Photoacoustic Sensors, Frequency Combs
6. Display Technologies: Liquid Crystal Displays (LCD), Organic Light Emitting Diode (OLED) Displays, Quantum Dot Emissive Layers, Micro-LED Arrays and Large Size Displays Using Chiplet Mass Transfer and Bonding, 3D Displays
7. Summary and Outlook

Who Should Attend:
The course addresses engineers, scientists and students who would like to get a general overview of the various photonic components and packaging technologies used in today's products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are, and which new technologies are being developed for further improvements aimed at technological breakthroughs.

3. WAFER-TO-WAFER AND DIE-TO-WAFER HYBRID BONDING FOR HETEROGENEOUS INTEGRATION AND ADVANCED PACKAGING

Course Leader(s): Viorel Dragoi, EV Group

Course Description:
This course addresses fundamental and practical aspects of low temperature fusion and hybrid bonding with the aim of providing a good understanding of the status and the potential of this technology to provide manufacturing solutions for current and future applications. The course starts with a short overview of all wafer bonding processes currently in use. A detailed explanation of the working principles of low temperature fusion and hybrid bonding is presented. Aspects related to materials specifications and surface preparation are reviewed.

Wafer-to-wafer alignment concepts are further introduced, with emphasis on face-to-face alignment. An overlay model is introduced, and the benefits of its use are illustrated with experimental results. Aspects regarding the implementation of advanced process control methods are discussed, with an example on bond wave monitoring and control.

The concept of die-to-wafer bonding is introduced as a heterogeneous integration technology for chiplets-based applications. The different process flows available are reviewed. Some important aspects specific to die-to-wafer bonding are discussed, with an emphasis on die preparation and specific requirements of the various process flows. Experimental results are used for illustration of this technology capabilities. A short overview of the current and future challenges of wafer bonding concludes this course.

Course Outline:
1. Introduction: Wafer Bonding Processes Short Overview (Principles, Basic Conditions)
2. Short Overview of the Wafer Bonding Process Variables
3. Low Temperature Fusion Bonding: Description, Specifications, Surface Preparation and Activation, Bonding Process
4. Low Temperature Hybrid Bonding:

Description, Specifications, Surface Preparation, Bonding Process
5. Wafer-to-wafer Alignment: General Principles (Methods, Errors), SmartView Alignment Introduction, Overlay and Distortion
6. Advanced Process Control: Numerical Simulation, Data Analysis and Modelling as New Tool
7. Advanced Bond Wave Monitoring and Control
8. Wafer Bonding: Process Results Assessment and Specific Metrology
9. Die-to-wafer Bonding: Introduction of the Concept and Process Flows
10. Summary: Short Overview of Current and Future Challenges

Who Should Attend:
The course is addressed to engineers involved in heterogeneous integration technology development who wish to understand the status of wafer bonding technology and its application potential. Basic principles and concepts are presented and explained together with more advanced topics. No prior experience in wafer-to-wafer or die-to-wafer bonding is required.

4. INTRODUCTION TO QUALITY AND RELIABILITY ENGINEERING OF ADVANCED MICROELECTRONICS PACKAGING

Course Leader(s): Shubhada Sahasrabudhe, QuRIuS LLC; Shalabh Tandon, QuRIuS LLC

Course Description:
As AI workloads push the boundaries of performance, advanced semiconductor packaging technologies must evolve to meet demanding quality and reliability expectations. Optimal package design to avoid over-engineering (inflated costs) or under-designing (premature failures) is critical. This balance requires engineering rigor that utilizes numerical simulations and physics-based models backed by empirical validation.

This PDC introduces an engineering methodology to achieve stellar quality and reliability (Q&R) in advanced, heterogeneously integrated packages. It presents a comprehensive physics-aware, data driven approach for estimating reliability metrics that rely on device usage. This includes complete characterization of product survivability using relevant stress tests, numerical simulations, failure analysis tools for characterization of failures, lab-level metrologies for physics of failure calibration as well as statistical methodologies for life prediction. The course also discusses upstream methods that facilitate designing and manufacturing for quality and downstream methods on field monitoring. The course will prepare the audience to tackle Q&R challenges by providing a blueprint that aids in delivering package capabilities that meet the market demands. The course is designed for the participants to get hands-on experience with tailored exercises that reinforce topics.

Course Outline:
1. Advanced Packaging Trends and Q&R Challenges
2. Introduction to Seven Foundational Q&R Tenets
   • Understanding Use Conditions / Mission Profiles
   • Designing and Manufacturing for Q&R
   • Establishing Qualification Infrastructure
   • Modeling Failure Mechanisms Using Physics-of-failure and FEA
   • Planning and Analyzing Accelerated Life Test Data
   • Quantifying Metrics such as DPM and Failure Rates
   • Monitoring Field Performance Through Health Management Systems
3. Discussion on the Seven Tenets with Industry Examples
4. Hands-on Exercises to Reinforce Learning

Who Should Attend:
This course is devised for engineers engaged in design, materials development, process engineering, and the qualification of advanced packaging technologies. It is equally valuable for technical managers responsible for decisions related to process and product quality assurance. Engineers working with PCBs and system-level integration will also find the course beneficial.

5. 2.5D/3D PACKAGE FAILURE ANALYSIS - FAILURE MECHANISMS AND ANALYTICAL TOOLS

Course Leader(s): Deepak Goyal, Carl Zeiss, Inc.

Course Description:
Heterogeneous Integration (HI) of disparate computing and communication functions is a key enabler of performance in micro-electronic systems. HI is enabled by advanced packaging since packages are an optimal HI platform. This technical course will provide an overview of the failure modes and mechanisms observed in 2.5D/3D packages. A brief introduction to the methodology of failure analysis of these packages will be described. The focus of the course will be on package failure mechanisms highlighted by case studies and on analytical tools and techniques currently used and the future direction for the tools and techniques required for successful and timely failure analysis of 3D package technologies. A discussion on the strategies for use of these techniques and a flow chart for failure analysis will be included.

Course Outline:
1. 2.5D/3D Package Technology – Trends, Drivers and Challenge
2. Failure Analysis Challenges Offered by 3D Package Technology Roadmap
3. Introduction to the Methodology of Failure Analysis of 3D Packages
4. Current Analytical Capabilities for Package Fault Isolation and Failure Analysis
5. Strategies to Use these Techniques to Identify Failures and Understand Failure Mechanisms
6. Analytical Capabilities to Support Next Generation 3D Packaging Technologies
7. Typical Failure Analysis Flow Charts for Opens and Shorts.
8. Failure Modes/mechanisms Including Chip/package Interactions, 1st/2nd Level Interconnections and Package/board Substrates.
9. Failure Analysis Case Studies.

Who Should Attend:
Engineers and technical managers who are involved in package technology development, reliability assessment of packages and failure analysis will benefit from this course.

6. AI-APPLICATIONS IN SEMICONDUCTOR PACKAGING

Course Leader(s): Pradeep Lall, Auburn University

Course Description:
This intensive short course provides an essential introduction to the transformative role of Artificial Intelligence (AI) and Machine Learning (ML) in modern semiconductor packaging and advanced integration. Chiplet and heterogeneous integration technologies are driving complexity, and AI is becoming crucial for optimizing design, manufacturing, and reliability. Participants will learn the core concepts, practical applications, with packaging case studies that showcase how AI is solving critical challenges in this high-stakes field. The course is ideal for packaging engineers, process specialists, reliability analysts, and technical managers seeking to leverage AI for faster time-to-market, improved yield, and enhanced product reliability. The course will begin with an introduction to key AI concepts (Machine Learning, Deep Learning, Generative AI) and how they can be used to specifically address challenges in semiconductor packaging. The course will cover selected ML models and how they can be used to analyze process data for anomaly detection, root cause analysis, and real-time process parameter adjustment. Reliability topics will cover the use of sensor data and ML to predict potential failures (e.g., thermal fatigue, delamination) in packaged devices, enabling predictive maintenance and extending component lifespan. By the end of the course, students will be able to: recognize key AI techniques and how they can be applied to packaging processes; identify how machine learning algorithms can be used to predict yield, detect defects, and optimize packaging processes; and critically assess the future trends and challenges of AI in semiconductor packaging.

Course Outline:
1. Advanced Packaging Landscape Challenges
2. AI vs Traditional Approach to Semiconductor Packaging Reliability
3. Categories of Artificial Intelligence
4. AI in Process Control
5. Yield Prediction and Optimization
6. Defect Detection and Classification
7. AI for Material Selection and Testing
8. Electronics Reliability and Leading Indication of Failure
9. Fault Classification in Semiconductor Packaging
10. Remaining Useful Life Assessment
11. Virtual Testing and Simulation

Who Should Attend: Engineers and Managers who are interested in learning artificial intelligence methods for use in electronics packaging manufacturing, design, reliability, and testing. No extensive prior knowledge of AI programming is required, but a basic understanding of semiconductor packaging processes and architectures is highly recommended.

7. FUNDAMENTALS OF FABRICATION PROCESSES AND RF DESIGN OF ADVANCED PACKAGES INCLUDING FAN-OUT, CHIPLETS, GLASS AND POLYMER INTERPOSERS

Course Leader(s): Ivan Ndip, Brandenburg University of Technology/Fraunhofer IZM; Markus Woehrmann, Fraunhofer IZM

Course Description:
Advanced packaging technologies such as fan-out wafer and panel-level packages (FO-WLPs, FO-PLPs), interposers (e.g., glass interposers with TGVs, polymer interposers) and chip-embedding packages (e.g., PCB embedding) play a key role in heterogeneous integration and enable the development of system in package (SiP) modules, antenna-in/on-package (AiP/AoP) and chiplet based systems. The packaging materials, fabrication processes and electrical behavior of these packages contribute significantly to the cost, performance and reliability of the entire system. The main objective of this course is to provide a thorough overview of packaging materials, fundamentals of fabrication processes as well as basic RF and high-speed design of advanced packages (e.g., fan-out wafer/panel level packages, glass and polymer interposers, SiP and AiP/AoP) for a wide range of applications. Furthermore, an introduction to chiplet design and heterogeneous integration, considering interconnects for chiplet communication and UCIe, will be given. The applications driving advanced packages such as 5G, 6G communication, radar sensing, high-performance computing (HPC) and AI in various industries will also be extensively discussed.

Course Outline:
1. Introduction, Basic Definitions and Explanations of Key Terminologies Related to Advanced Packages, RF and High-speed Design, Chiplets and Heterogeneous Integration
2. Applications Driving Advanced Packages such as 5G, 6G Communication, Radar Sensing, HPC and AI in Various Industries
3. Overview of Different Types of Advanced Packages, Current Trends and Future Directions
4. Challenges and Key Requirements of Advanced Packages for RF and High-speed Applications
5. Fundamentals of Packaging Materials and Fabrication Processes of Fan-out Wafer/panel Level Packages, Interposers (Glass, Organic) and AiP/AoP
6. Fundamentals of RF and High-speed Design of Building Blocks of Fan-out Wafer/panel Level Packages, Interposers (Glass, Organic) and AiP/AoP
7. Introduction to Chiplet Design and Heterogeneous Integration, Considering Interconnects for Lateral Chiplet Communication and UCIe
8. Examples of Advanced Packages Fabricated at Fraunhofer IZM

Who Should Attend:
Engineers, scientists, researchers, designers, managers, graduate students and business developers interested in the fundamentals of electronic packages and chiplets as well as those involved in the process of electrical design, layout, fabrication and/or system-integration of electronic packages and chiplets for emerging applications.

AFTERNOON COURSES
1:30 p.m. – 5:30 p.m.

8. ELECTRONICS COOLING AND RELIABILITY FOR DATA CENTERS

Course Leader(s): Patrick McCluskey, University of Maryland, College Park

Course Description:
Data Centers are the backbone of Artificial Intelligence, and as such, they are expected to consume 8% of US power by 2030. It has been estimated that 40% of the total energy consumed by data centers is used for cooling off the servers. This has created a powerful incentive for the development and commercialization of more efficient cooling solutions for data centers. Design of these cooling systems requires more than just a thermal solution. However, it is critically important that the insertion of these new cooling solutions does not adversely impact the availability of the data center, which needs to exceed 99.875% for Tier 3 data centers. This means assessing and ensuring the reliability of data center electronics and their cooling systems is of paramount importance.
This short course will present the challenges in developing reliable and efficient cooling technologies and methods to mitigate those concerns. It will cover thermal modeling, physics-of-failure reliability modeling and approaches for assessing the degradation of cooling system components, and use Markov chain analysis for assessing system reliability, including the impact of redundancy on availability and efficiency. Software tools that can be used to conduct this modeling will be introduced.

Course Outline:
1. State of the Art Data Center Cooling
2. Single Phase Liquid and Hybrid Cooling Approaches
3. Reliability Modeling of the Cooling System
4. Reliability Modeling of the Electronics
5. Markov Chain Analysis and Availability Modeling
6. Software Tools for Thermal, Energy Efficiency and Reliability Modeling

Who Should Attend:
Data Center Designers, HVAC Engineers, Electronic Packaging Engineers and Managers interested in addressing key challenges to the growth of data centers.

9. POLYMERS FOR ADVANCED PACKAGING

Course Leader(s): Jeff Gotro, InnoCentrix, LLC

Course Description:
The professional development course has been updated to include a detailed discussion of the polymers and polymer-related processing for: Fan-Out Wafer Level (FOWLP) Packaging; Fan-Out Panel Level packaging (FOPLP); Advanced Underfills; and Low Dk/Df Polymers for 5G such as Antenna-in-package. The course will provide an overview of the important structure-property-process-performance relationships for polymers used in several advanced packaging applications. The main learning objectives are to:

- Gain Insights Into How Polymers Are Used in Fan-Out Packaging, Specifically Mold Compounds and Polymer Redistribution Layers (RDL)
- Learn About Polymers and Processes Used in Fan-Out Panel Level Packaging Including New Materials for Mold Compounds and a Detailed Description of the Polymers Used for RDL in FOPLP
- Discuss Advanced Underfills for Both Capillary and Pre-applied Underfill Applications
- Cover the Key Polymer Properties for 5G Dielectric Applications (Low Dk and Low Df)

Course Outline:
1. Overview of Polymers Used in Fan-Out Wafer Level Packaging (FOWLP)
2. Wafer Level Process Flows (Chip First Versus Chip Last / RDL First)
3. Epoxy Mold Compounds for Fan-Out Packages
4. Photosensitive Polyimides (PI) and Polybenzoxazoles (PBO) for RDL
5. Polymer Reliability Challenges in Fan-Out Wafer Level Packaging
6. Processes and materials for Fan-Out Panel Level Packaging (FOPLP)
7. Pre-applied Underfills and Wafer-level Underfills, Chemistry and Process
8. Polymer Materials for 5G Applications

Who Should Attend:
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

10. DIAMOND HEAT SPREADERS AND HETEROGENEOUS INTEGRATION

Course Leader(s): Joana-Catarina Mendes, Instituto de Telecomunicaciones

Course Description:
The rise in power density within 3D and 2.5D integrated systems has dramatically increased the complexity of thermal management. Thermal issues are now emerging as a key limitation to both electrical performance and long-term reliability. Ensuring thermal integrity in future heterogeneously integrated architecture requires addressing critical challenges related to material properties and heat-spreading efficiency.

Thanks to its unmatched thermal and mechanical properties, the incorporation of synthetic diamond in advanced system-in-package (SiP) technologies holds tremendous potential to enhance heat dissipation and improve overall reliability. For instance, the replacement of SiC with diamond has enabled Akash Systems to commercialize RF radios and power amplifiers with higher power densities and smaller form factors.

However, as a relatively new technology, diamond still presents technical challenges that potential users must fully understand. This course is designed to equip participants with the essential knowledge to assess whether and how to integrate diamond into specific applications, while recognizing the key technical factors that influence its successful implementation.

The program introduces diamond as a game-changing material for advanced thermal

management in complex in-package systems. Participants will explore the unique properties that make diamond indispensable, review the main fabrication routes for synthetic diamond and their respective advantages and limitations, and learn effective strategies for integration within 2.5D and 3D architectures. The course will also examine critical technical challenges, highlight recent breakthroughs from both industry and academia, and discuss how the current saturation of the gemstone market affects the cost and availability of synthetic diamond.

Course Outline:

1. Potential of Synthetic Diamond – Why Diamond is Redefining Thermal Management in Advanced Electronics
2. Fabrication Methods – Main Synthesis Routes, Advantages, and Current Limitations
3. Integration in SiP Architectures – How to Embed Diamond at Die, Interposer, and Package Levels
4. Diamond–chip Bonding – Interface Strategies to Maximize Reliability
5. Diamond Power Boards – Applications and Benefits for High-power and RF Systems
6. Diamond & Microfluidics – Synergistic Cooling Through Hybrid Solid–liquid Approaches
7. Direct Diamond Deposition – Emerging Techniques for Selective and Low-temperature Growth
8. Challenges & Solutions – Key Technical Hurdles and Practical Integration Guidelines
9. Market Trends – The Evolving Landscape of Synthetic Diamond Supply and Adoption

Who Should Attend:

This course is designed for professionals and researchers involved in the design, development, and deployment of advanced electronic packaging solutions. It will be particularly valuable for: Packaging and thermal engineers working on 2.5D, 3D, and HI technologies who seek to overcome thermal bottlenecks and enhance reliability; Research and Development engineers and materials scientists exploring novel materials, such as synthetic diamond, to improve heat dissipation in high-power and high-density systems; Academics and graduate students conducting research in microelectronics, materials science, or thermal management for next-generation packaging architectures; Program and engineering managers evaluating innovative approaches to boost system performance and ensure long-term reliability in advanced electronics; Industry professionals and technologists from semiconductor and packaging companies aiming to stay ahead of emerging trends in SiP and chiplet-based thermal solutions; and technology strategists and product planners shaping future integration and packaging roadmaps to address escalating thermal challenges.

11. ADVANCED PACKAGING FOR CHIPLET, HETEROGENEOUS INTEGRATION, AND CO-PACKAGED OPTICS

Course Leader(s): John H. Lau, Unimicron Technology Corp.

Course Description:

Chiplet is a chip “design method” and heterogeneous integration (HI) is a chip “packaging method”. HI uses packaging technology to integrate dissimilar chiplets, photonic devices, and/or components with different sizes and functions, and from different fabless design houses and foundries into a system or subsystem on a common package substrate. Co-packaged optics (CPO) are heterogeneous integration of the optical engine which consists of photonic ICs (PIC) and the electrical engine (EE) which consists of the electronic ICs (EIC) as well as the switch ASIC (application specific IC). The advantages of CPO are: (a) to reduce the length of the electrical interface between the OE/EE (or PIC/EIC) and the ASIC, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging and CPO, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the introduction of recent advances, and trends in advanced packaging for chiplet, HI, and CPO will be presented.

Course Outline:

1. Overlapping Between Semiconductor and Advanced Packaging
2. Advanced Packaging (2D, 2.1D, 2.3D, 2.5D, 3D, 3.3D, and 3.5D IC Integration)
3. System on Chip (SOC) and the Origin of Chiplets
4. Chiplet Design and HI Packaging
5. Communication Between Chiplets (EMIB, UCIe, Bridges Embedded in Fan-Out EMC)
6. Hybrid Bonding (More than 13 HVM Products)
7. Glass Packaging
8. Trends in Advanced Packaging for Chiplet Design and HI Packaging
9. Silicon Photonic
10. Data Centers and Optical Transceivers
11. Optical Engine (OE) and Electrical Engine (EE)
12. OBO (On-Board Optics), NBO (Near-Board Optics), and CPO (Co-Packaged Optics)
13. 3D HI of ASIC Switch, PIC and EIC without Bridges
14. 3D HI of GPU, HBM, Switch, PIC, EIC (Driven by AI and Communication)
15. 3D HI of ASIC Switch, PIC and EIC on Glass Substrate
16. Potential R&D Topics and Trends in Co-Packaged Optics

Who Should Attend:

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. Each attendee will receive more than 300 pages of lecture notes.

12. PREVENTING PACKAGING FAILURE - MODELING AND MITIGATION STRATEGIES FOR WARPAGE, FATIGUE, AND THERMAL ISSUES

Course Leader(s): Xuejun Fan, Lamar University

Course Description:

Electronic packaging has evolved rapidly to meet the demands of high-performance computing, miniaturization, and heterogeneous integration. These advancements introduce complex reliability challenges that require a deep understanding of failure mechanisms from a physics-based perspective. This 4-hour professional development course provides a comprehensive overview of electronic packaging technologies and their evolution, followed by an in-depth discussion of major failure mechanisms and their underlying physics. Topics include warpage, die cracking, solder joint fatigue, drop-induced failures, moisture-related degradation, electromigration, and thermal management issues. The course integrates physics-of-failure principles with modeling approaches and design strategies to predict and mitigate reliability risks.

Course Outline:

1. Evolution of Electronic Packaging Technologies
2. Drivers: Miniaturization, High Power, Heterogeneous Integration
3. Reliability Challenges in Advanced Packaging
4. Physics-of-failure Fundamentals
5. Warpage: Causes, Modeling, and Mitigation
6. Die Cracking Mechanisms and Design Considerations
7. Solder Joint Fatigue: Thermal Cycling and Creep Behavior
8. Drop-induced Failures: Mechanical Shock and Impact Modeling
9. Moisture-related Failures: Diffusion, Swelling, and Delamination
10. Electromigration: Physics, Modeling, and Lifetime Prediction
11. Thermal Management: Heat Transfer and Material Selection
12. Multi-scale Modeling Approaches for Reliability Prediction
13. Design for Reliability Principles and Best Practices
14. Case Studies: Advanced Packaging Reliability Issues
15. Emerging Challenges in AI and High-power Applications
16. Summary and Future Directions in Packaging Reliability

Who Should Attend:

Packaging engineers, reliability and quality engineers, design engineers working on advanced electronics, researchers in materials and electronics mechanics, as well as technical managers overseeing product development and reliability will benefit from this course. Attendees will gain practical insights into how these mechanisms impact package integrity and system performance, and how modeling tools can guide design for reliability. This course is ideal for engineers, researchers, and managers seeking to strengthen their understanding of reliability fundamentals and apply physics-based approaches to packaging design and failure prevention.

13. FAILURE ANALYSIS OF ENGINEERING MATERIALS FOR ADVANCED ELECTRONIC PACKAGING

Course Leader(s): Kuan Yew Cheong, Universiti Sains Malaysia

Course Description:

In high-volume manufacturing, failures in advanced electronic packages are inevitable. Effective failure analysis is therefore crucial for improving product quality, reliability, durability, robustness, and safety. This complex task requires a multidisciplinary approach, integration of fundamental and

technological knowledge of materials, processes, and product operation. As more diverse, complex, and conflict engineering materials with complicated geometry and distinctive differences in dimension, interactions of engineering materials within an advanced package are growing more complicated. Hence, a systematic, effective, and data-driven type of approach must be adopted in failure analysis. This lecture outlines the essential strategies for postulating, verifying, and confirming failures to establish root cause. It will connect critical material properties and characterization methods to failure modes and conclude by addressing key challenges in the field. Upon completion of this course, participants will be able to:

- List Challenges Encountered in Advanced Electronic Packaging.
- Explain Concept of Failure from Perspective of Engineering Materials.
- Correlate Engineering Material Failures with Failure of Advanced Electronic Package.
- Discuss how Purity/contamination and Residual/overstress Relate to Failure in Advanced Electronic Package.
- Explain Typical Failure Mechanisms in Advanced Electronic Package.
- Elaborate the Needs of Characterization Strategy in Failure Analysis.
- Select Appropriate Characterization Technique to Acquire Sufficient Information for Failure Analysis.
- List Challenges of Characterization for Advanced Electronic Packaging.

Course Outline:

1. Challenges of Advanced Electronic Packaging
2. Concept of Failure in Advanced Electronic Packaging
   - Octagonal Relationship of Engineering Materials for Advanced Electronic Packaging and Relation to Failure
   - Overview of Integrated Knowledge to Resolve Failure in Advanced Electronic Packaging
3. Typical Failure Mechanisms and Potential Solutions
   - Purity and Contamination Related Failure
   - Residual and Overstress Related Failure
4. Characterization Strategy and Challenges in Advanced Electronic Packaging
   - Sample Preparation Techniques
   - Non-Destructive and Destructive Imaging Techniques
   - Surface Analysis Techniques
   - Bulk Analysis Techniques
   - Systematic Problem-solving Approach
   - Consideration of Failure Analysis Strategy
   - Characterization Approaches and Selection Criteria
   - Challenges of Characterization in Failure Analysis

Who Should Attend:
All engineers, researchers, post-graduate students, decision makers, policy makers, and managers

14. FLIP CHIP TECHNOLOGIES

Course Leader(s): Shengmin Wen, TATA Electronics Private Limited

Course Description:
Advanced packaging, such as CSP, FCBGA, 2.5D/3D, HBM packaging, heterogeneous with multiple-dies and multiple-Si-node packaging, embedded die packaging, certain wafer level package or panel level packaging, is based on flip chip technologies. For high-speed, high-performance applications such as AI targeted design, flip chip technology is a must. Even some traditional packaging types such as QFN begin to use flip chip technology. Industry wise, in terms of total annual revenue, flip chip packaging has grown steadily and already passed wire bond-based packaging.

This course will cover the fundamentals of flip chip assembly technologies, including major assembly processes, wafer bumping technologies, substrate types and critical BOM selection, design rules, and reliability modeling/evaluation. Two major assembly processes, their related equipment, materials, design rules, and design practices are covered in detail. Examples are presented to demonstrate the versatile flip-chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form mixed interconnection that uses both wire bond / flip chip integration. In-depth discussions include chip package interaction (CPI), package warpage control, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, Si die floor plan optimization, design rules, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their future projects.

Various bumping technologies that are used in today's flip chip assembly are also briefly introduced, i.e., lead-free solder bumping and highly customized Cu pillar bumping. The course will also cover various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc. A group exercise at the end of the class is planned to serve as an in-class capstone project, making sure that the students can walk away with an in-depth understanding of the flip chip assembly technologies, and are ready to apply the knowledge to their real-world packaging designs and projects.

Course Outline:

1. Introduction to Flip-Chip Technologies
2. Flip-Chip Technologies: Mass Reflow Process
3. Flip-Chip Technologies: Thermal Compression
4. Flip-Chip Substrate Technologies
5. Underfill, Package Warpage Control, and Yield Detractors
6. Failure Modes, Examples, Modeling and Reliability Life Assessment
7. Flip-Chip Si Package Co-Design on Various Types (BOT, BOP, AI type) and Examples
8. Variations: Wafer Level CSP, Wafer Level Fan-Out, Panel Level Packaging, Hybrid Bonding
9. Bumping Process, Rules, and Introduction
10. Flip-Chip Under-Bump Metallization and Intermetallic
11. Review and Package Selection Exercise – Group Discussions

Who Should Attend:
Anyone who wants to understand the fundamentals of flip-chip packaging technology is encouraged to take this highly condensed and yet knowledgeable course. These include graduate students who are looking for a packaging engineering career, engineers who are to take advanced package projects, project managers who want to have an in-depth technical understanding every step of the way, and managers who want to expand their understanding of key aspects of flip-chip technologies to flawlessly adopt to their company's product roadmap. This course may help materials and equipment vendors to understand the applications.

IMPORTANT NOTICE

Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

15. ADVANCED PACKAGING FOR 5G/6G - RF FOCUS

Course Leader(s): Premjeet Chahal, Michigan State University

Course Description:
The rapid evolution of fifth generation (5G) communication networks and growing interest in 6G (or beyond 5G) are leading to unprecedented demand for advanced packaging technologies. Packaging not only needs to meet the stringent requirements for mechanical support, thermal management and protection, but also needs to meet the design challenges of ultra-broadband electrical performance. Overall, co-design approaches that consider system performance needs are increasingly used to optimize system performance and make them energy-efficient and cost-efficient.

The 5G/6G architectures will cover a wide range of frequency bands, spanning from sub-6 GHz to THz. This has motivated the use of low-loss substrates (e.g., glass, ceramics and advanced polymers), antenna in package (AiP) and package on antenna (PoA) architectures, compact antenna designs, mmWave antenna arrays and reconfigurable antennas, heterogeneous integration (in 2D and 3D space) of different semiconductor technologies at the front-end. Overall, the 5G/6G systems represent a convergence of RF design, materials science, and advanced manufacturing. Future trends indicate even greater integration, utilizing additive manufacturing, inorganic substrates (such as glass and ceramic), and RF-photonics.

This course focuses on the needs and challenges of advanced packaging for 5G/6G communications with major emphasis on RF designs. This includes RF front-end designs for multiple frequency bands, low-loss materials, various semiconductor technologies, compact package designs utilizing additive manufacturing, and antenna and antenna array designs.

Course Outline:

1. Introduction to 5G/6G - Trends, Opportunities and Challenges
2. Wireless Channels - Different Frequency Bands, Free Space Propagation, Fading
3. RF Front-end for 5G/6G - mmWave Circuits, Modulation Techniques, Signal-to-Noise
4. Antenna and Antenna Arrays - AiP, PoA, Small Antennas, Multi-band Antennas, Phased Arrays, Reconfigurable Antennas
5. Filters - Filter Designs, Diplexers, Multiplexers

6. MIMO - Introduction, Multiple Antenna Integration
7. Low-loss Materials - Glass, Ceramics, Advanced Polymers
8. Heterogeneous Integration - Semiconductor Technologies, Additive Manufacturing
9. Next Generation Packaging Challenges in 5G/6G - Heterogeneous Integration, RF-Photonic Technologies, Chiplets

Who Should Attend:
This course gives a holistic view of 5G/6G communication technologies from an RF perspective. It caters to engineers already working in these fields, managers who wish to understand the technical challenges and future opportunities, and newcomers interested in pursuing this field.

16. THERMAL MANAGEMENT IN THE AGE OF AI

Course Leader(s): Jaime Sanchez, Qualcomm

Course Description:
With the advent of Artificial Intelligence, the demand for electrical power is experiencing exponential growth. The iteration between new processor manufacturing, model training and application development, has caused a cycle where new applications require ever increasing power. While this cycle is already putting strain on the electrical grid, it is also driving innovation in the thermal management space as the heat generated by these devices needs to be removed for their continuous operation. This course provides the fundamentals of heat transfer applied to the design of thermal systems used across the semiconductor industry, from consumer electronics to datacenters. We start with defining the problem statement of heat in semiconductors and emphasize the importance of thermal management as a key feature in the design process of new systems. We cover the basic theory of heat transfer and demonstrate simple concepts to calculate the cooling requirements for an electronic package and the impact of various parameters on thermal performance. This course covers in-depth heat transfer theory and analysis to give the student a comprehensive understanding of the key modes of heat transfer, their applications, and the state-of-the-art in cooling technologies used to date. Practical topics such as thermal interface materials, heat sink and cold plate design, and advanced cooling techniques are reviewed. Finally, an introduction is provided to cover the testing challenges of new devices and how those requirements differ from traditional thermal management.

Course Outline:
1. The New Cycle: Artificial Intelligence, Power and Heat
2. Introduction to Heat Transfer and Its Application to Electronics Cooling
3. Governing Principles of Cooling Solutions
4. Techniques to Determine Cooling Requirements for a Package and Impact of Boundary Conditions
5. Simplification of Heat Transfer Equations to Analyze Cooling Solutions
6. Application of Numerical Methods to Calculate the Performance of Cooling Solutions
7. Thermal Interface Materials and Their Applications
8. Techniques to Size Cooling Requirements and Trade-offs
9. Parameters that Impact the Performance of Cooling Solutions
10. Experimental Characterization of Cooling Solutions and Instrumentation
11. Steady-State vs. Transient Heat Transfer: Test Thermal Challenges vs. Traditional Electronics Cooling

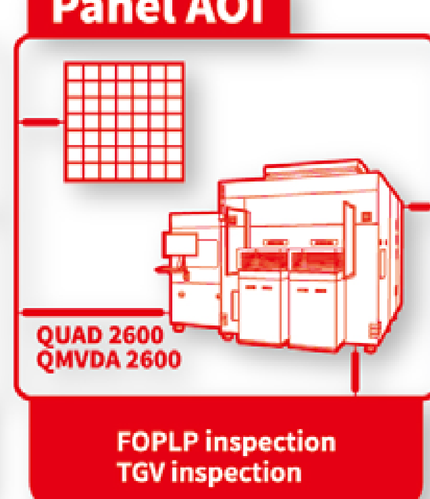
Who Should Attend:
This class is intended for students and engineers working in the field of thermal management.

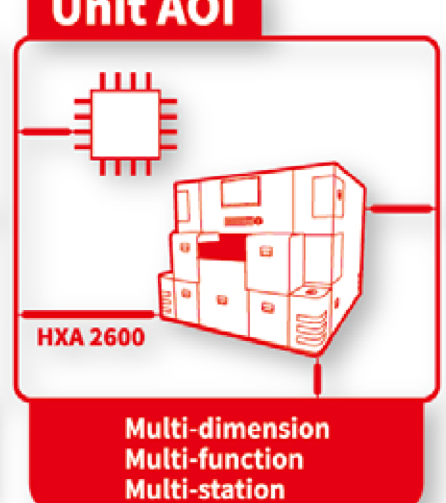
IMPORTANT NOTICE

Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.

See page 32 for registration information

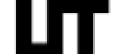
UTECHZONE





Semi AOI for Advanced Packaging

CoWoS — RDL InFO — Bumping — PLP — TGV



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WEBSITE

SEMI DM

Program Sessions: Wednesday, May 27, 9:30 a.m. - 12:35 p.m.

Session 1: Enabling Fan-In and Fan-Out Wafer/Panel Level Packaging Technology	Session 2: Co-Packaged Optics	Session 3: Advances in Low Temperature Hybrid Bonding
Committee: **Packaging Technologies**	**Committee:** **Photonics**	**Committee:** **Materials & Processing**
Session Co-Chairs **Young-Gon Kim** **Renesas Electronics** **Email: young.kim.jg@renesas.com** **Steffen Kroehnert** **ESPAT-Consulting** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs** **Ajey Jacob** **University of Southern California** **Email: ajey@isi.edu** **Soon Jang** **ficonTEC USA** **Email: soon.jang@ficontec.com**	**Session Co-Chairs** **Yoichi Taira** **Keio University** **Email: taira@appi.keio.ac.jp** **Ksenija Varga** **EV Group** **Email: k.varga@evgroup.com**
1. 9:30 AM - A Novel 600mm Panel Interposer with 300mm Panel Assembly Approach for Advanced Packaging Solution in HPC and AI Applications Yung Shun Chang, Teck Chong Lee, Yihsien Wu, Wiwy Wudjud, Lihong Cao, Powei Lu, Ping-Feng Yang – Advanced Semiconductor Engineering, Inc.	***1. 9:30 AM - Proposal of a Novel Opto-Electronic Fan-Out Wafer-Level Packaging Based on Optical RDL and Opto-Chiplets*** Siim Heinsalu, Fumi Nakamura, Satoshi Suda, Akihiro Noriki – National Institute of Advanced Industrial Science and Technology	***1. 9:30 AM - Hybrid Bonding With Ultra-Low Temperature Annealing: Morphological and Electrical Validations*** Margot Faure, Agathe Lerat, Pablo Renaud, Floriane Baudin, Maria-Luisa Calvo-Munoz, Hadi Hijazi, Frank Fournel, Christophe Dubarry – CEA-LETI
2. 9:50 AM - Multi Stacked FOWLP Utilizing Extreme Aspect Ratio Cu Post for Mobile on-Device AI Memory Solution Eun Young Lee, Sangkyu Lee, Woosang Jung, Yieok Kwon, Jongyoun Kim, Haram Park, Jihwang Kim, Choi Dong-Jun, Yongjin Seol, Daewoo Kim, Kyung Don Mun – Samsung Electronics Co., Ltd.	***2. 9:50 AM - High-Density, Energy-Efficient CPO Platform with PIC-in-Mold Interposer Architecture for AI/ML Data Centers*** BG Sajay, JiaQi Wu, Zhonghua Yang, Mihai Rotaru, Lin Ji, Yong Han, Lai Yee Chia, Sharon Lim, Sandra San, Chai Tai Chong, Surya Bhattacharya – Institute of Microelectronics A*STAR	***2. 9:50 AM - Pressure-Less Cu/Polymer Hybrid Bonding at Low-Temperature and Fine Pitch Using a Novel Polymer Adhesive with Precisely Controlled Composition*** Ryo Hayakawa, Yuzo Nakamura, Satoshi Otsuka, Hajime Kato, Shigetaka Hori, Yutaka Hisamune, Satoshi Inada – Mitsui Chemicals, Inc.; Chih-Jing Hsu, Yung-Sheng Lin, Gavin Kao, Chih-Pin Hung, Yung-I Yeh – Advanced Semiconductor Engineering, Inc.
3. 10:10 AM - The Study and Challenges of Ultra-Thin Chip Module for Fan-Out Embedded Bridge Die Package (FO-EB) Kuei-Hsiao Kuo, Jui Teng Hung, Derrick Dai, Chun Sheng Ho, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.	***3. 10:10 AM - Photonic-Electronic Integration on Glass Substrate with Temperature-Stabilized Vertical Optical Coupling by Resin-Encapsulated Collimation Mirror*** Shingo Nakamura, Yasutaka Mizuno, Kunio Kobayashi, Takeru Naito, Tetsuya Nakanishi, Hiroshi Uemura, Keiji Tanaka, Katsumi Uesaka – Sumitomo Electric Industries, Ltd.; Mio Emura, Mami Miyairi, Yoshikatsu Ishizuki – FICT, Ltd.; Yoichiro Kurita – Institute of Science Tokyo	***3. 10:10 AM - Reliable Low-Temperature (≤ 250°C) Cu/Dielectric Hybrid Bonding for High-Bandwidth Memory (HBM) Stack Integration*** Van Nhat Anh Tran, B.S.S. Chandra Rao, Chaeeun Lee, Ser Choong Chong, Norhanani Jaafar, Vempati Srinivasa Rao, Navab Singh – Institute of Microelectronics A*STAR; Prayudi Lianto, Nicholas Boon Leong Chua, Mohammad Faizal Bin Aermie Ang – Applied Materials, Inc.; Rong Ji, Ming Lin – Institute of Materials Research and Engineering A*STAR
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Progress Towards a Fine-Pitch Multi-Layer Organic Substrate Enabled by Fan-Out Technology Georgios (George) Dogiamis, Timothy Takeuchi, Craig Bishop – Deca Technologies, Inc.; Matthew Magnavita, Michael Naujokaitis, Robert Naujokaitis, Gregory Johnson, Stanislau Niauzorau, Leslie Hwang, Binh Duong, Jason Conrad – Arizona State University	***4. 11:15 AM - Thin-Film Lithium Niobate Hybrid Integration for Co-packaged Optics*** Zhixing Lin – University of California; Tam Huynh, Ayed Sayem, K.W. Kim, Yang Liu, Manohar Bongarala, Sarwesh Parbat, Ting-Chen Hu, Rose Kopf, Mark Cappuzzo, Mark Earnshaw – Nokia Bell Labs; Alexander Rylyakov – Nokia Corporation	***4. 11:15 AM - Low-Temperature Chip Scale Cu-Cu Hybrid Bonding by Electroless Ag Passivation*** Cheng-Yan Yang, Ming-Hsuan Hsieh, Po-Shao Shih, Wei Choong Lee, Yu-Hsiang Lu, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.
5. 11:35 AM - A Novel Membrane-Based Adaptive Pressure Curing System for Warpage Suppression in Advanced Packaging HuanPing Su, Minghua Hsu, Hong Auger – Ableprint Technology Co., Ltd.	***5. 11:35 AM - High-Density Integration of III-V Devices and EICs using Vertical Coupled Photonic Packages with Glass-IP and Redistribution Layers*** Kei Masuyama, Mizuki Shirao, Shinji Araki, Kiyotomo Hasegawa, Shinya Okuda, Higashide Seiu, Nobuo Ohata – Mitsubishi Electric Corporation	***5. 11:35 AM - Enabling Low-Temperature Fine-Pitch Hybrid Bonding: Role of Nanocrystalline Copper Microstructures and Pre-Bond Surface Treatments*** Mathieu Loyer, Christelle Rey, Emilie Deloffre – ST Microelectronics; Mathilde Gottardi, Maria-Luisa Calvo-Munoz – CEA-LETI
6. 11:55 AM - Metal-Enhanced Waffle Wafer Design for Thermomechanical Warpage Reduction in Fan-Out Wafer-Level Packaging Bonghak Lee, Sang Won Yoon – Seoul National University	***6. 11:55 AM - A 106Gb/s x 8-Channel 1060nm Single-Mode VCSEL-Based Ultra-Compact CPO Transceiver enabling >2km Parallel-Optical Links*** Wataru Yoshida, Kazuya Nagashima, Hideyuki Nasu – Furukawa Electric Co., Ltd.; Yuto Iwane, Kazutaka Takeda – Fujifilm Business Innovation Corp.; Fumio Koyama – Institute of Science Tokyo	***6. 11:55 AM - A Methodology to Reduce Voiding Along Die Sidewall in Oxide Gap Fill for Die to Wafer Hybrid Bonding*** Alyssa Yaeger, Cristina Camagong – IBM Corporation; Roy Yu, Katsuyuki Sakuma – IBM Research
7. 12:15 PM - Additive Fan-Out Packaging for Discrete Components Arjun Wadhwa, Milan Saalmink, Marieke Burghoorn, Iris Kerkhof, Ruben Pranger, Jeroen van der Brand – Netherlands Organization for Applied Scientific Research (TNO); Edsger Smits, Francesca Chiappini – Chip Integration Technology Center/TNO	***7. 12:15 PM - Thermal-Aware Packaging Techniques for High-Performance DFB Laser Arrays in Co-Packaged Optical Links for Scale-up Applications.*** Nandish Mehta – Nvidia Corporation	***7. 12:15 PM - Scalable Low-Temperature Bonding for Packages with Large-Format Interposers: High Throughput and High Reliability*** Sadaaki Katoh, Keiko Ueno, Takeshi Saito – Resonac Corporation

Program Sessions: Wednesday, May 27, 9:30 a.m. - 12:35 p.m.

Session 4: Breakthrough in Pitch Scaling With Advanced Bonding Technology	Session 5: RF and High-Speed Design for mmWave and Sub-THz	Session 6: Thermo-Mechanical Interactions With Reliability
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Pascale Gagnon** **IBM Canada** **Email: pgagnon@ca.ibm.com** **Cong Zhao** **Meta Platforms, Inc.** **Email: zhaocong@meta.com**	**Session Co-Chairs** **Harrison Chang** **Advanced Semiconductor Engineering, Inc. (US)** **Email: Harrison_Chang@aseglobal.com** **Yong-Kyu Yoon** **University of Florida** **Email: ykyoon@ece.ufl.edu**	**Session Co-Chairs** **Kuo-Ning Chiang** **National Tsing Hua University** **Email: knchiang@pme.nthu.edu.tw** **Ning Ye** **Sandisk** **Email: ning.ye@sandisk.com**
1. 9:30 AM - 100nm-level Post-Bond Accuracy and High-Yield Die-to-Wafer Hybrid Bonding System Using Non-Contact Die Transfer Kentaro Mihara, Takashi Hare, Shimpei Aoki, Sakai Hirofumi – Toray Engineering Co., Ltd.; Fumihiro Inoue – Yokohama National University; Akira Uedono – University of Tsukuba; Hiroyuki Hashimoto, Murugesan Mariappan, Takafumi Fukushima – Tohoku University	***1. 9:30 AM - Developments of Polymer Microwave Fiber Coupler in eWLB Package for Ultra-High-Speed Communication at D- and H-Band*** Maciej Wojnowski, Walter Hartner, Simon Kornprobst, Franz Xaver Engelsberger – Infineon Technologies AG; Parisa Aghdam, Sining An – Ericsson AB; Frida Strömbeck, Herbert Zirath – Chalmers University of Technology	***1. 9:30 AM - Predicting Long-Term Thermal Aging Behavior of Porous Sintered Layers via a Hybrid Potts–Phase Field Model with Thermo-Mechanical Coupling*** Xiao Hu, Zichuan Li, Willem van Driel, G. Q. (Kouchi) Zhang – Delft University of Technology; Chao Gu, Junwei Chen, Jiajie Fan – Fudan University; Jianlin Huang – Ampleon B.V.; Rene Poelma – Nexperia
2. 9:50 AM - A Study of Die Distortion in Die-to-Wafer Hybrid Bonding Yi Shi, Charles El Helou, Haris Khan Niazi, Mohammadreza Yaghoobi, Chytra Pawashe, Tushar Talukdar, Siyan Dong, Sheena Benson, Aleksandar Aleksov, Lance Hibbeler – Intel Corporation	***2. 9:50 AM - A Micro-3D Printed 245GHz Helix Antenna Array for SoP Modules in nextG/6G Applications*** Genaro Soto Valle Angulo, Chenhao Hu, Fernando Pastrana Aguirre, Manos M. Tentzeris – Georgia Institute of Technology	***2. 9:50 AM - Influence of Design and Liner Material on Reliability of Through Glass Vias Under Thermal Cycling: Numerical Modeling and Experimental Validation*** Dalei Yang, Junbo Yang, Karthik Arun Deo, Kewei Shou, Yuhan Gao, Yi Deng, Weichen Zhao, Yangyang Lai, Pengcheng Yin, Seungbae Park – Binghamton University
3. 10:10 AM - INTERCEPT - A Nondestructive, 10µm Pitch, Known Good Die Testing Probe and Reworkable Substrate Enabled by Liquid Metal Patterning Samuel Wang, Hsuan En Lee, Alexis Samoylov, Subramanian Iyer – University of California, Los Angeles	***3. 10:10 AM - Differentially Fed Sub-THz Broadband Antenna Arrays Using Quartz Glass Cavity-Backed Bonding Technology*** Alexander Gäbler, Uwe Maaß, Wojciech Partyka – Fraunhofer IZM; Ivan Ndip – Brandenburg University of Technology/ Fraunhofer IZM; Makoto Iwai – NGK Europe GmbH; Naotake Okada, Jungo Kondo, Shoichiro Yamaguchi, Masato Tokai, Kentaro Tani – NGK INSULATORS, LTD.	***3. 10:10 AM - Fracture Analysis for CoWoS Reliability Improvement*** Ming-Chih (Jason) Yew, Chia-Kuei Hsu, Chien-Yu Wang, Chieh-Ming Chang, Po-Chen Lai, Kuo-Chin Chang, Jia-Ming Yang, Chang-Fu Han, Jyun-Lin Wu, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Assembly Process Optimization to Reduce Particle-Induced and non-Particle-Induced Voids in Chip-to-Wafer Hybrid Bonding Ling Xie, Ser Choong Chong, Hipona Randy Tupaen, Ignatius Lim, Nagendra Sekhar Vasarla, Dileep Kumar Mishra, B.S.S. Chandra Rao, Srinivasa Rao Vempati – Institute of Microelectronics A*STAR; Hegde Nithyananda, Pavel Seroglazov – Besi NL; Ke Zheng, Raymond Hung – Applied Materials, Inc.	***4. 11:15 AM - Advanced Scalable Modeling of High-Q Passives on a 300mm RF Interposer Platform for mmWave and sub-THz Applications*** Come Wallner, Xiao Sun –IMEC; Dimitri Lederer – UCLouvain	***4. 11:15 AM - Thermal Stress Reliability Optimization of TGV Density, Size, and Material Engineering for Glass Based Advanced Substrate Technology*** Jaesung Kim, Geonhee Lee, Yujeong Kim, Eunbi Ko, Jina Lee, Chang Bo Jung, Ken Lee, Mun Sang You, Jun Soo Chang, Soon Gil Lee – SIMMTECH
5. 11:35 AM - Laser Assisted Bonding of InP Power Amplifier Chiplets on a 300mm RF Si Interposer Damien Leech, Siddhartha Sinha, Hamideh Jafarpoorchekab, Angel Uruena, Natalie Roels, Nazia Fathima, Ehsan Shafahian, Punith Kumar Mudiger Krishne Gowda, Koen Kennes, Andy Miller, Eric Beyne, Xiao Sun – IMEC	***5. 11:35 AM - Signal and Power Integrity Co-Analysis of Chiplet(UCIe)-Based GPU-HBM Interconnect for Reduced PHY Area*** Haeseok Suh, Joungho Kim, Hyunjun An, Jiwon Yoon, Junghyun Lee, Junho Park, Byeongmok Kim, Eunji Seo, Keunwoo Kim, Youngsu Yoon – Korea Advanced Institute of Science and Technology	***5. 11:35 AM - Thermal Storage Reliability Evaluation of Non-PFAS Potting Materials Used in Electronic Assemblies*** Pradeep Lall, Yasitha Piyumal – Auburn University
6. 11:55 AM - Impact of Formic Acid Distribution on Panel-Level Reflow: Enhancing Process Uniformity and Performance Xinxuan Tan, Mehmet Kanik, Zulal Ozel, Ashok Das, Saket Chadda, Zia Karim – Yield Engineering Systems	***6. 11:55 AM - Thermally Reconfigurable Split-Substrate Integrated Waveguide for Baseband and Broadband Signal Transmission*** Abdelrahman Omar, Soumitra Joy – University of North Carolina	***6. 11:55 AM - Enhanced Wafer Warpage Prediction in Heterogeneous Integration Wafer Process Through Modelling Thermal Aging Shrinkage of EMC*** Lin Ji – Institute of Microelectronics A*STAR; Alfred Yeo, Yifan Wang, Kai Chong Chan – STATS ChipPAC, Ltd.
7. 12:15 PM - Pillar-Suspended Bridge (PSB): Fabrication Process Verification and Interconnect Design for 25-Micron Pitch Die-to-Die Interface Shinichi Arioka, Tanapun Srichanthamit, Koji Iwabu, Takashi Suzuki, Yoshiaki Aizawa – AOI Electronics Co., Ltd.; Yoichiro Kurita – Institute of Science Tokyo	***7. 12:15 PM - Fully Integrated mmWave MIMO Radar with Compact Antenna-on-Package Design*** Aditya Jogalekar, Mohammad Vatankhah Varnoosfaderani, Marc Dewilde, Zachary Crawford, Cathy Chi, Sunhwan Jang, Venkatesh Srinivasan – Texas Instruments, Inc.	***7. 12:15 PM - High Temperature Board Level Shock Testing of QFN, Flip-Chip and LCR Solder Interconnects*** Max Frank Haeusler, Karsten Meier, Karlheinz Bock – TU Dresden

Program Sessions: Wednesday, May 27, 2:00 p.m. - 5:05 p.m.

Session 7: Heterogeneous Integration: The New Horizons	Session 8: Die-to-Wafer Hybrid Bonding: Current Advancements and Future Directions	Session 9: Advances in Thermal Materials and Encapsulation
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Luu Nguyen** **PsiQuantum** **Email: lnguyen@psiquantum.com** **Subhash Shinde** **Booz Allen Hamilton** **Email: sshinde@nd.edu**	**Session Co-Chairs** **Katsuyuki Sakuma** **IBM Research** **Email: ksakuma@us.ibm.com** **Sunny Ilseok Son** **TEL Technology Center, America, LLC** **Email: Ilseok.Son@us.tel.com**	**Session Co-Chairs** **Dwayne Shirley** **Marvell Semiconductor, Inc.** **Email: shirley@ieee.org** **Ivan Shubin** **Raytheon Technologies** **Email: ishubin@gmail.com**
1. 2:00 PM - Direct Bridge Multi-Die (DBrM) Package: A Novel Silicon Bridge Chiplet Packaging Technology Using Die-Edge Gluing Technique for Chip Reconstitution Akihiro Horibe, Chinami Marushima, Takahito Watanabe, Atom Watanabe, Yasuharu Yamada, Sayuri Kohara, Risa Miyazawa, Hiroyuki Mori – IBM Research; Divya Taneja, Isabel De Sousa – IBM Canada, Ltd.	***1. 2:00 PM - Ultra-Fine 1.4µm Pitch Face-to-Back CoW Cu-Cu Hybrid Bonding for the CoWoW Integration*** Itsuki Imanishi, Takahiro Kamei, Akihiro Urata, Toru Osako, Masanori Chiyozono, Kan Shimizu, Yoshihisa Kagawa – Sony Semiconductor Solutions	***1. 2:00 PM - Enhancement of Thermal Conductivity of the Advanced Packaging Materials by Using BNNT*** Jaewoo Kim, Changho Kim, Junha Hwang, Min Seok Kwak, Ji In Lee, Cheolwoo Kwak – Naieel Technology; Yuka Yamashita, HIkaru Uchida, Hiroki Ito – Denka Innovation Center
2. 2:20 PM - Scaling the EMIB-T Advanced Packaging Technology to Address the Future HPC/AI Demand Tarek Ibrahim, Rahul Manepalli, Kemal Aygun, Kaladhar Radhakrishnan, Zhiguo Qian, Jianyong Xie, Yidnekachew Mekonnen – Intel Corporation	***2. 2:20 PM - Process Optimization for Chip to Wafer Hybrid Bonding Using Inter Die Gap Fill Integration Approach*** Dileep Kumar Mishra, Nagendra Sekhar Vasarla, Ling Xie, Hipona Randy Tupaen, Norhanani Jaafar, B.S.S. Chandra Rao, Ser Choong Chong, Vempati Srinivasa Rao, Sasi Kumar Tippabhotla, Daniel Ismael – Institute of Microelectronics A*STAR	***2. 2:20 PM - AlN-based Chiplet Encapsulation: Enhancing Thermal Performance for High-Density Heterogeneous Integration*** Ashita Victor, Hansol Lee, Muhannad Bakir – Georgia Institute of Technology; Dohyun Go, Andrew Kummel – University of California, San Diego
3. 2:40 PM - Large Reticle Size Advanced Packaging Selection Strategy Based on Warpage: FOCoS and FOCoS-B Wu-Lung Wang, Chung-Hung Lai, Wei-Hong Lai, Wiwy Wudjud, Hsin-Chih Shih, Chin-Li Kao, Chih-Yi Huang, Hung Hsiang Cheng, Kai Jung Su, Lihong Cao, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***3. 2:40 PM - Characterization of Bonding Behavior and Void Formation in Chip-on-Wafer Hybrid Bonding*** ZhaoZe Jiang, Chih-Jing Hsu, Chen-Hung Lee, Yuan-Feng Chiang, Che-Ming Hsu, Gavin Kao, Yung-I Yeh, Alexis Angelo Garcia, Po Hsiang Wang – Advanced Semiconductor Engineering, Inc.; Ruei Yang Chen – National Sun Yat-Sen University	***3. 2:40 PM - Interfacial Reaction of In-Ag Thermal Interface Materials With Ti/Ni/Ag Backside Chip Metallization and its Influence on Thermal Resistance*** Chunen Lin, Chun-Hao Chen, Polina Leger, Thi Minh Anh Dao, Keyen Ma – National Yang Ming Chiao Tung University
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Demonstration of an Optical Packaged Substrate with Embedded Silicon Photonic Transceiver for High Performance Chiplet Packaging Fumi Nakamura, Akihiro Noriki, Kenta Suzuki, Satoshi Suda, Haruhiko Kuwatsuka, Takeru Amano – National Institute of Advanced Industrial Science and Technology; Naoki Matsui, Reona Motoji, Dan Maeda, Tomoya Sugita, Hiroki Yamamoto, Hirotaka Uemura – Kyocera Corporation	***4. 3:45 PM - Inverse Hybrid Bonding at 5µm Pitch for High-Density Heterogeneous Integration*** Madison Manley, Ashita Victor, Danish Baig, Muhannad Bakir – Georgia Institute of Technology; Dipayan Pal, Andrew Kummel – University of California, San Diego	***4. 3:45 PM - Development of High Thermal Conductivity Molding Materials for Automotive Flip Chip Packages*** Masahiro Iwai, Sean Kuo, Koichiro Uchida – Sumitomo Bakelite Co., Ltd.; Hungyuan Li – Siliconware Precision Industries Co., Ltd.; Hsin-Long Chen – MediaTek, Inc.
5. 4:05 PM - Process Integration Challenges in Heterogeneous Integration of XPU, HBM and Photonic Chiplets for AI/HPC Applications Lai Yee Chia, Van Nhat Anh Tran, Sandra San, Chai Tai Chong – Institute of Microelectronics A*STAR	***5. 4:05 PM - Development of Particle Robust Solder-Organic Dielectric Hybrid Bonding Technology Down to 3µm Pitch*** Mitsuru Ooida, Toshihisa Nonaka – Rapidus Corporation	***5. 4:05 PM - In-Situ Cure Monitoring of EMC by Fiber Bragg Grating and Dielectric Sensors with Molecular Dynamics Validation for Accurate Warpage Prediction*** Woo-Jin An, Jeong-Hyeon Baek, Woong-Kyoo Yoo, Jun-Seop Song, Hak-Sung Kim – Hanyang University; Jihye Shim, Gyung-Hwan Oh – Samsung Electronics Co., Ltd.
6. 4:25 PM - Marvell Custom HBM Routing and Signal Integrity Analysis Joshua Dillon, Ting Zheng, Arshiya Vohra, Wolfgang Sauter, Kazin Blacklow, Sid Allman – Marvell Technology, Inc.	***6. 4:25 PM - Sub-10µm Pitch 3-Dimensional Die Level Integration Utilizing Cu-Cu Thermal Compression Bonding (TCB)*** Vineeth Harish, Goutham Ezhilarasu, Jui-Han Liu, Subramanian Iyer – University of California, Los Angeles; Anton Turpault, Adeel Bajwa – Kulicke and Soffa Industries, Inc.	***6. 4:25 PM - Anisotropic 0D–1D Hybrid Molding Compound for Low Warpage and Enhanced Thermal Management in Advanced Packages*** Young-Joon Lee, Woong-Ryeol Yu – Seoul National University
7. 4:45 PM - Package Architectures for Hyper Large Form-Factors for AI and HPC Segment Mohit Khurana, Sujit Sharan, Nisha Ananthakrishnan, Kemal Aygun, Kaladhar Radhakrishnan, Aditya Vaidya, Prasanna Raghavan, Satish Surana, Rajiv Mongia, Chinmay Potdar, Shripad Gokhale, Sashi Kandanur – Intel Corporation	***7. 4:45 PM - Next-Generation Optical-Electrical Co-Design Interconnect Using Low-Temperature Hybrid Bonding Technology*** Lin-Chun Su, Jou-Yun Yeh, Yu-Lun Liu, Chun-Ta Li, Yuan-Chiu Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chien-Kang Hsiung – National Yang Ming Chiao Tung University/Applied Materials, Inc.; Yu-Tao Yang – MediaTek USA, Inc.; Shang-Hsuan Wu – Tokyo Electron America, Inc.	***7. 4:45 PM - Development of Negative Thermal Expansion Fillers for Next-Generation Advanced Semiconductor Encapsulation Materials*** Tetsuharu Yuge, Yutaro Tanaka, Kazuki Tsujikawa, Chie Matsunaga, Akihiro Ohara, Haruki Koshitouge, Masahiro Yokoyama – Mitsubishi Chemical Corporation

Program Sessions: Wednesday, May 27, 2:00 p.m. - 5:05 p.m.

Session 10: Reliability of Large Body High Performance Computing and AI Packaging Solutions	Session 11: Signal Integrity Design for High-Speed Interfaces	Session 12: Characterization and Modeling for Process and Multi-Domain Analyses
Committee: Applied Reliability	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Keith Newman** **AMD** **Email: keith.newman@amd.com** **Paul Tiner** **Texas Instruments, Inc.** **Email: p-tiner@ti.com**	**Session Co-Chairs** **Amit P. Agrawal** **Advanced Micro Devices, Inc.** **Email: ap_agrawal@yahoo.com** **Xiao Sun** **IMEC** **Email: xiao.sun@imec.be**	**Session Co-Chairs** **Rui Chen** **Eastern Michigan University** **Email: rchen7@emich.edu** **Ruiyang Liu** **Tenstorrent Inc.** **Email: ruiyang.liu9@gmail.com**
1. 2:00 PM - Reliability Prediction Model for the Solder Joint Bridging Failure of Large-Body BGA Packages Under System-Level Heatsink Compression Hsueh-Yin Liu, Siao-Yu Chen, Tz-Cheng Chiu – National Cheng Kung University	***1. 2:00 PM - Enabling 12+ Gb/s HBM4e with EMIB-T Advanced Packaging Technology*** Yidnekachew Mekonnen, Jianyong Xie, Xenofon Konstantinou, Zhiguo Qian, Yunpeng Si, Kemal Aygun, Kaladhar Radhakrishnan – Intel Corporation	***1. 2:00 PM - Accelerated Multi-Physics Simulation of Moisture-Induced Stress in Electronic Packages via Sequential Coupling*** Liangbiao Chen, Yong Liu – ON Semiconductor; S M Yeasin Habib, Xuejun Fan – Lamar University
2. 2:20 PM - Systematic Reliability Study of a Large Size 2.5D Package with RDL Interposer for AI Processor Richard (Shiguo) Rao, Ivan Tan, Rich Graf, Tushar Chauhan, Dwayne Shirley, Theo Anemikos, Tim Hayes, Kevin Caffey – Marvell Technology, Inc.	***2. 2:20 PM - Scalable Electroplated Cu/Co Metaconductor for Low-Loss 112–400Gbps Wired Communication Interconnects*** Saeyeong Jeon, Yong-Kyu Yoon, Ariel David Cerpa – University of Florida	***2. 2:20 PM - Micro/Nanostructural Stress Characterization for Advanced 3D Integration Technologies*** Tatsumasa Hiratsuka, Masaki Haneda, Shoji Kobayashi, Yoshiya Hagimoto, Masashi Nakazawa – Sony Semiconductor Solutions; Mario Gonzalez, Peng Zhao, Eric Beyne – imec
3. 2:40 PM -The First Report of Si Bridge Type 2.5D Package Reliability for Automotive Applications Tomoko Takahashi, Ken Imai, Ryota Morimoto, Yasuhiko Maki – Socionext; Shiro Machida, Shuuichi Kariyazaki – Renesas Electronics Corporation; Takuya Nakamura – MIRISE	***3. 2:40 PM - Advanced SI/PI Interposer Design Solution Enabling High-Performance HBM4E at up to 12Gbps*** Taeyun Kim, Kyoungseok Oh, Sungwook Moon, Seungki Nam – Samsung Electronics Co., Ltd.	***3. 2:40 PM - Sequential Fabrication and Mechanics-Based Model of Multilayer RDL Stackup with Embedded Chiplets on Glass Core Package*** Alexander King, Hyunggyu Park, Muhannad Bakir, Suresh K. Sitaraman – Georgia Institute of Technology
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Reliability of Multilayer Glass Core Packages with Organic and Inorganic Through Glass Via (TGV) Liners and Fully Plated TGVs Meghna Narayanan, Pragna Bhaskar, Lakshmi Narasimha Vijay Kumar, Lila Dahal, Durga Gajula, Kyoung-Sik (Jack) Moon, Mark Losego, Mohan Kathaperumal, Suresh K. Sitaraman, Muhannad Bakir – Georgia Institute of Technology	***4. 3:45 PM - Temperature and Yield-Aware Design of UCIe Die-to-Die Interconnects for Advanced Packaging*** Ram Krishna, Xu Chen, Elyse Rosenbaum – University of Illinois; Ashita Victor, Zhonghao Zhang, Muhannad Bakir – Georgia Institute of Technology; Atom Watanabe – IBM Research	***4. 3:45 PM - A Study of Electromigration Failure Criteria and Contributing Damage Factors*** Choong-Un Kim, Harikrishnan Kumarasamy, Dong Seok Lee – University of Texas, Arlington; Sylvester Ankamah-Kusi – Texas Instruments, Inc.; Tae-Kyu Lee – Cisco Systems, Inc.; Yan Li – Samsung Semiconductor, Inc.
5. 4:05 PM - Reliability of SAC PBGA Assemblies Using Constitutive and Failure Models Incorporating Damage Mechanics Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Omma Sumaiya, Jeffrey Suhling, Pradeep Lall – Auburn University	***5. 4:05 PM - Figures of Merit to Characterize the Signal Integrity Performance for High Bandwidth Memory (HBM)*** Taeil Bae, Jinwon Lee, Hyunsik Kim, Hyunggon Bae, Inchul Jeong, Hyungsoo Kim – SK hynix Inc.	***5. 4:05 PM - Experimental Studies Towards Better Understanding of RDL Microstructure and Built-Up Stresses for Reliable Glass-Enabled Advanced Packaging*** Chukwudi Okoro, Rajesh Vaddi – Corning Research and Development Corp.; Mandakini Kanungo, Diego Prado, Robert Schaut – Corning, Inc.
6. 4:25 PM - Chip-Package-Board Interconnects Reliability Challenges and Solutions in Large Die Fine Pitch WLCSP Gaurav Sharma, Greta Terzariol, Michiel van Soestbergen, Varun Thukral, Amar Mavinkurve, Abdullah Fahim, Nishant Lakhera – NXP Semiconductor, Inc.	***6. 4:25 PM - Cross-Topology Transfer Learning Using Bayesian Optimization for Scalable Surrogate Modeling of 3D Packaging Structures*** Md Sultan Mahmud, Madhavan Swaminathan – Pennsylvania State University; Xianbo Yang – IBM Corporation	***6. 4:25 PM - Mechanical Effect of Embedded Capacitors on Processor Module for High Performance Computing Applications*** Robert Darveaux – TMBS LLC; Richard Sheridan, Maryam Rezaie – Saras Micro Devices
7. 4:45 PM - Predictive Reliability Modeling of Hybrid Bonding Through Warpage and Interfacial Defect Correlation Liton Kumar Biswas, Istiaq Firoz Shiam, Pavanbabu Arjunamahnthi, Himanandhan Reddy Kottur, Navid Asadi – University of Florida; Neil Hubble, Paul Handler – Akrometrix LLC; Victor Vilar, Dadi Setiadi, Charles Woychik – NHanced Semiconductors, Inc.	***7. 4:45 PM - Analytical Approach to Statistical Modeling of Power Supply Induced Jitter*** Hyunjun An, Jiwon Yoon, Youngsu Yoon, Haeseok Suh, Junghyun Lee, Junho Park, Jaegeun Bae, Joungho Kim, Byeongmok Kim – Korea Advanced Institute of Science and Technology	***7. 4:45 PM - Experimental and Computational Fracture Strength Characterization at BEOL Structure Sharp Corners for Chip-Package Interaction Reliability Assessment*** Jehun Youn, Jonathan Whitby, Pei-En Chou, Ganesh Subbarayan – Purdue University

Program Sessions: Thursday, May 28, 9:30 a.m. - 12:35 p.m.

Session 13: Advances in Thermal Design and Characterization	Session 14: RDL and Fan-Out Interconnections	Session 15: Optical Interconnects
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: Photonics**
Session Co-Chairs Monita Pau Onto Innovation Email: monita.pau@ontoinnovation.com Eric Tremble Marvell Technology, Inc. Email: etremble@marvell.com	**Session Co-Chairs Takafumi Fukushima Tohoku University Email: fukushima-tak@tohoku.ac.jp Srinivas Pietambaram Intel Corporation Email: srinivas.v.pietambaram@intel.com**	**Session Co-Chairs Richard Pitwon Resolute Photonics, Ltd. Email: rpitwon@resolutephotonics.com Ping Zhou LDX Optronics, Inc. Email: pzhou@ldxoptronics.com**
1. 9:30 AM - Process Development and Thermal Characterization of Micropillar Direct-to-Silicon Liquid Cooling Solution on CoWoS-R Platform Sing-Da Jiang, Chun-Yu Ou, Chi-Shiang Chiou, Chuan-Chang Wu, Yu-Sheng Tsai, Chang-Yi Tsai, Tsunyen Wu, Ying-Ju Chen, Wen-Hsiung Lu, Tzong-Huann Yang, Han-Jong Chia, Kathy Yan – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Low Warpage Double Side RDL Interconnection With Electrical Compensation for Panel Level Package*** Terry Wang, Cheng-Yueh Chang, Chien-Ming Tseng, Yu-Jhen Yang, Pei-Pei Cheng, Wendy Chou – Industrial Technology Research Institute; Yu Chung Chiu – Applied Materials, Inc.; Austin Cheng – FAVITE, Inc.; Hsin-Yi Huang – Everlight Chemical Industrial Corp.; Simon Zhong – TAIWAN TAIYO INK CO., Ltd.; Chi-hua Huang – Alliance Material Co., Ltd.; Kent Chen – CSUN, Ltd.	***1. 9:30 AM - Low-Loss Optical Interconnect Designs in Optimized Glass for Co-Packaged Optics*** Lars Brusberg, Jorge Holguín-Lerma – Corning, Inc.; Matthew Dejneka, Lucas W. Yeary, Betsy Johnson, Chad Terwilliger, Charisse Spier, Jonathan Walter, Katerina Rousseva, Sean Garner – Corning Research and Development Corp.
2. 9:50 AM - Toward Reliable and Thermally Robust BSPDN: A Dual-Path Design based BN–BN Bonding Chi Hsueh, Jia-Rui Lin, Chung-Hsuan Wu, Chun-Che Cheng, Mu-Ping Hsu, Kuan-Neng Chen – National Yang Ming Chiao Tung University	***2. 9:50 AM - Panel CMP Co-Planarization of Heterogeneous Interfaces for Damascene Organic RDL Interposers (L/S = 2/2µm)*** Katsuaki To, Masashi Minami, Sadaaki Katoh – Resonac Corporation	***2. 9:50 AM - Detachable Glass Waveguide Connector for Co-Packaged Optics on Silicon Photonics Platform with < 1.5 dB/Facet Passive Coupling and 280 mW Power Handling*** Arpan Dasgupta, Takako Hirokawa, Zahidur Chodhury, Yarong Lin, Yusheng Bian, Jae Cho, Brian Popielarski, Koushik Ramachandran, Kevin Eaton, Keith Donegan, Geng Ni – GlobalFoundries, Inc.; Sean Garner – Corning Research and Development Corp.
3. 10:10 AM - System-Level Thermal Validation of 2.5D Packages in GPU Servers: Impact of TCB vs HCB HBM Platforms Linus (Woohyun) Park – Samsung Semiconductor, Inc.; Youchang Na, Seongjin Hong, Yeonghyeon Gim, Eduardo Hernandez Pacheco, Jaechoon Kim, Yun Seok Choi – Samsung Electronics Co., Ltd.	***3. 10:10 AM - 3D Integration of an SRAM Chiplet in Fan-Out Embedded Bridge Platform Achieving Low Energy Read/Write*** Dany-Sebastien Ly-Gagnon, Li Chen, Dwight Lee, Max Wu, Jiajing Wang, Ping-Chen Liu, CH Yang, Chung-Ching Peng – Intel Corporation; Steven Lin, Bruce Xu, Chung Kang Cai – Siliconware Precision Industries Co., Ltd.	***3. 10:10 AM - Laser Cleaning of Optical Couplers on Photonic Integrated Circuits*** Jean-Philippe Berube, Alexandre Douaud, Feng Liang, Loic Arias, Simon Duval, Louis-Rafael Robichaud – Femtum; Philippe Lassonde – Femtum/INRS; Francois Legare – National Institute for Scientific Research (INRS)
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - High Performance Direct Liquid Jet Impingement Cooling on Structured Silicon Herman Oprins, Georg Elsinger, Vladimir Cherman, Geert Van der Plas, Zsolt Tokei, Eric Beyne – imec	***4. 11:15 AM - Influence of Metal Surface Characteristics on AF Reference Position and Pattern Fidelity in Fine-Pitch RDL Applications*** Jaehyuk Chang, Seokhun Choi, Zhongchuan Zhang, Jang Fung Chen – Applied Materials, Inc.; Hyunseok Yang, Youmin Chang, Chanjin Park, Mingu Kang – Samsung Electro-Mechanics Co., Ltd.; Kyung Chan Hwang – Applied Materials Korea	***4. 11:15 AM - Development of a High-Efficiency, Wide-Temperature-Range Optical Coupling Structure for CPO Modules*** Shuhei Sudo – Kyocera Corporation
5. 11:35 AM - Process Development of Two-Stacked Chips with a Backside Embedded Two-Phase Cooling Solution Xiaowu Zhang, Boon Long Lau, Huicheng Feng, Gongyue Tang, Ming Chinq Jong, Surya Bhattacharya, Vempati Srinivasa Rao, B.S.S. Chandra Rao, Van Nhat Anh Tran – Institute of Microelectronics A*STAR	***5. 11:35 AM - Study of SeWaRe Failure in Glass Package with 6-12 RDL Layers*** Kaushik Godbole, Nirvan Patel Masini, YongWon Lee, Suresh K. Sitaraman – Georgia Institute of Technology	***5. 11:35 AM - High-Density Polymer Waveguide Integration on Glass Substrate for CPO*** Takuya Kitainui, Yujiro Saito, Naoki Fukuda, Kenichi Ogawa – Dai Nippon Printing Co., Ltd.
6. 11:55 AM - Advances in Direct-to-Chip Liquid Cooling Integration Laura Mirkarimi, Ron Zhang, Gill Fountain, KM Bang, Suhail Sadiq, Arianna Avellan, Bongsub Lee – Adeia	***6. 11:55 AM - Low-Cost Process of Organic RDL-Based Packaging Platform Enabling UCIe 32GT/s Link Speed*** Donggyu Kim, Kwang Il Kim, Jun-Beom Kim, Yong-Gyu Jang, Yeon Ji Shin, Jae-Sung Lim, Sang Gyu Jang, Jin-Wook Jang – HANA Micron, Inc.; Woojin Lee – Swevenz Inc.; Jaeyoung Kim, Sangyong Park, Seungho Lee – Qualitas Semiconductor Co., Ltd.	***6. 11:55 AM - Low-Loss Polymer Waveguide Device for Fiber-to-Chip and Chip-to-Chip Connection*** Takaaki Ishigure, Kai Yokoyama, Haruka Nakajima, Koki Atsumi – Keio University
7. 12:15 PM - Diamond-on-Chip Integration for Enhanced Thermal Management and Warpage Control in 2.5D Chiplets Packaging Zeming Tao, Ningning Xu, Dongchen Fan, Jinbao Zhang, Yixiong Wu, Weiyi Lin, Rongbin Xu, Dongxue Liang, Yi Zhong – Xiamen University; Delong Qiu – Jiashan Fudan Research Institute	***7. 12:15 PM - FOWLP-Enabled 3D Package-Level Heterogeneous Integration with Advanced Heat Spreading Architecture for Next-Generation Mobile Device*** Kyung Don Mun, Jihwang Kim, Sangjin Baek, Daewoo Kim, Se Hoon Jang, Wooyoung Kim, Bongju Cho, Bong-Soo Kim, Dahye Kim, Jaechoon Kim, Suk Won Jang, Eun Young Lee – Samsung Electronics Co., Ltd.	***7. 12:15 PM - Integrated Assembly Process for Pluggable Fiber Connector for Co-Packaged Optics*** Jelena Pesic, Lily Yuan, Joy Zhan, Shuhe Li, Suresh Pothukuchi, Subal Sahni, Ankur Aggarwal – Celestial AI

Program Sessions: Thursday, May 28, 9:30 a.m. - 12:35 p.m.

Session 16: Assembly and Manufacturing: 3D Stacking and Thermal Solutions	Session 17: Digital Twin and AI in Advanced Packaging and Interconnect Security	Session 18: Hybrid Bonding: Advanced Processing and Modeling
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committees: Materials & Processing and Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Wenhao (Eric) Li** **GlobalFoundries** **Email: liwenhao2010@gmail.com** **Jobert Van Eisden** **MKS** **Email: Jobert.van-Eisden@MKS.com**	**Session Co-Chairs** **Masha Gorchichko** **Applied Materials, Inc.** **Email: maria.gorchichko@gmail.com** **Dishit Parekh** **AMD Inc.** **Email: dpparekh@alumni.ncsu.edu**	**Session Co-Chairs** **Ercan (Eric) Dede** **Toyota Research Institute North America** **Email: eric.dede@toyota.com** **Vidya Jayaram** **Chipletz** **Email: vidya.jayaram@chipletz.com**
1. 9:30 AM - Selective Layer Transfer to Enable Fine-Grain Mixed Front-End Devices with Monolithic Interconnects Tushar Talukdar, Paul Nordeen, Thomas Sounart, Mohammadreza Yaghoobi, Abhishek Sharma, Andrey Vyatskikh, Brandon Rawlings, Felipe Bedoya, Siyan Dong, Lei Jiang, Charles El Helou, Myung-Hee Na – Intel Corporation	***1. 9:30 AM - Substrate-Cloak: A MEMS-Enabled Reconfigurable Obfuscation Framework for Secure Substrate Interconnects*** Himanandhan Reddy Kottur, Mohammad Shafkat Khan, Pavanbabu Arjunamahnthi, Pragyna Titty, Liton Kumar Biswas, Katayoon Yahyaei, Istiaq Firoz Shiam, Navid Asadi – University of Florida; Liam Hayes, Bo Liu, Joshua Hihath – Arizona State University; Michael Delany – BuildEmber LLC	***1. 9:30 AM - Multiscale Mechanical Characterization of Hybrid-Bonding Copper: From Instrumented Indentation to AFM*** Nicolas Alderete, Yvonne Gerbig, Gheorghe Stan – National Institute of Standards and Technology; Paresh Daharwal – Intel Corporation; Cristian Ciobanu – Colorado School of Mines/NIST
2. 9:50 AM - First Demonstration of µBump-Based Massive Orthogonal Stacking Assembly IC (MOSAIC) Cube for SoC-DRAM Direct Stacking Hung-Chih Huang, Yuki Mitarai, Masaya Kawano, Mototsugu Hamada, Atsutake Kosuge – University of Tokyo; Takafumi Fukushima – Tohoku University	***2. 9:50 AM - Cryogenic Via-Last TSVs for 2.5D Qubit Chip Implementation Demonstrating DC–20GHz Signal Transmission at Millikelvin Temperatures*** Misato Taguchi, Takuji Miki – Kobe University	***2. 9:50 AM - Nanoindentation-Based Analysis of Wafer-to-Wafer Bond Strength Using Cohesive Zone Modeling and Machine Learning*** Yusuf Ozdemir, Kris Vanstreels, Oguzhan Orkut Okudur, Mario Gonzalez, Clement Merckling, Eric Beyne – imec
3. 10:10 AM - Electroplated Cu-Diamond Composite Thermal Vias for Interposer-Level Heat Management in 2.5D/3D Packages Ye Yang, Tiwei Wei – University of California, Los Angeles; James Chien – Taiwan Foresight Co. Ltd.	***3. 10:10 AM - Novel Via-Last Process for Superconducting-Material-Filled TSV on Cryogenic Packaging Platform*** Hong Yu Li, Ya-Ching Tseng, Norhanani Jaafar, Anh Tran Van Nhat, Yong Chyn Ng – Institute of Microelectronics A*STAR	***3. 10:10 AM - Effects of Chip Geometry and Bonding Initiation Point on Bonding Distortion in Die-to-Wafer Hybrid Bonding*** Takaaki Hirano, Tatsumasa Hiratsuka, Taichi Yamada, Shoji Kobayashi, Yoshiya Hagimoto, Masashi Nakazawa – Sony Semiconductor Solutions
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Optical Engine (OE) Integration Challenges for Next-Generation CPO on Networking and HPC Application Mike Tsai, Ming Zhuang, Shane Lin, Steven Lin, Michael Fu, Bruce Xu, Don Son Jiang – Siliconware Precision Industries Co., Ltd.; Yih Jiang – SPIL	***4. 11:15 AM - Design and Integration of a 3D-Stacked Glass-Packaged Voltage Regulator Module with Embedded Passive Components for 12-to-1 V, 5MHz Operation*** Ramin Rahimzadeh Khorasani, Madhavan Swaminathan – Pennsylvania State University	***4. 11:15 AM - First Demonstration of 450nm Pitch Cu-Cu Hybrid Bonding with 98% Yield Across 20M Interconnects for Ultra-Dense 3D Integration*** Ying Trickett, Roger Quon, Yoocharn Jeon, Amit Prakash, Raghav Sreenivasan, Jing Xu, Pijeng Khor, Prayudi Lianto, Samuel Tackett, Raghuveer Patlolla, Joan Chung, JuSeon Goo – Applied Materials, Inc.
5. 11:35 AM - High Power System Scaling Using Double-Sided Connection in Embedded Substrate Li Sheng – Advanced Semiconductor Engineering, Inc. (US)	***5. 11:35 AM - Hidden in Traffic: Timing Leakage in Heterogeneous Integrated Processors*** Abir Ahsan Akib, Ankur Srivastava – University of Maryland	***5. 11:35 AM - System-Level Thermal Characterization of Hybrid Cu Bonded HBM on 2.5D Advanced Packaging*** Seongjin Hong, Hae Jung Yu, Hyuek Jae Lee, YoungLyong Kim, Jin Hyuk Chang, Mingyu Kang, Sangho Shin, Eunhee Jung, Yeonghyeon Gim, Jaechoon Kim, Yun Seok Choi – Samsung Electronics Co., Ltd.; Linus (Woohyun) Park – Samsung Semiconductor, Inc.
6. 11:55 AM - Top-Side Silicon Capacitor for Co-Optimized Thermal and Power Delivery in FOWLP for Mobile SoCs Kyojin Hwang – Murata Manufacturing Co., Ltd.; Woobin Jung, Youngsang Cho, Heeseok Lee, Daehyun Kim – Samsung Electronics Co., Ltd.; Seung Wook Yoon – Samsung Electronics Co. Ltd.,	***6. 11:55 AM - Conformal Dry-Electrode-Based Impedance Sensor for Inspection of Complex Composite Structures*** Riadh Al-Haidari, Stephen Gonya, Mark Poliks – Binghamton University; Daniel Balder, Veerendra Balchand – SunRay Scientific, Inc.	***6. 11:55 AM - Near-Infrared Activated Upconversion Nanoparticles for Optical Wafer-to-Wafer Bonding*** Aparnaa Iyer, Eren Özmen, Mark Losego, Mohan Kathaperumal, C. P. Wong – Georgia Institute of Technology
7. 12:15 PM - High-Thermal-Conductivity (1.0W/m·K) Dry-Film Solder Resist at 20µm: Compatible with Standard Process Flow and Steady-State Thermal Validation Takumi Suzuki – Taiyo America, Inc; Kohei Kitagawa, Ryohei Nojima, Fumitaka Kato, Daichi Okamoto – Taiyo Ink Mfg. Co., Ltd.; Zihao Lin, Kyoung-Sik (Jack) Moon, Mohan Kathaperumal, C. P. Wong – Georgia Institute of Technology	***7. 12:15 PM - AI-Driven Inverse Design and Vision Fusion Framework for Automated Signal Integrity Optimization of Organic RDL Interposers*** Minsun Cho, Taeheon Lee, Jiho Yu, Dayeong Kim, Sungyeop Jung – Korea University	***7. 12:15 PM - Fine-Pitch Cu-Cu Hybrid Bonding Using Electroless-deposited (111) Nanotwinned Cu*** Wei Choong Lee, Po-Shao Shih, I-En Chen, Cheng-Yan Yang, Yu-Hsiang Lu, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

Program Sessions: Thursday, May 28, 2:00 p.m. - 5:05 p.m.

Session 19: Substrate Core Innovations: Glass, Ceramic, and Silicon	Session 20: Performance Analysis and Metrology of High-Bandwidth Electrical and Optical Interconnects	Session 21: Novel Laser-Based Technologies and Fine-Pitch Interconnects
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Kuldip Johal** **MKS Instruments** **Email: kuldip.johal@mks.com** **Markus Leitgeb** **AT&S AG** **Email: m.leitgeb@ats.net**	**Session Co-Chairs** **Yu-Tao Yang** **MediaTek USA, Inc.** **Email: yu-tao.yang@mediatek.com** **Chaoqi Zhang** **Apple Inc.** **Email: chaoqi.gt.zhang@gmail.com**	**Session Co-Chairs** **Bing Dang** **IBM Corporation** **Email: dangbing@us.ibm.com** **Mark Poliks** **Binghamton University** **Email: mpoliks@binghamton.edu**
1. 2:00 PM - Glass Core Substrates – Next Generation Advanced Packaging Platform for AI and HPC Srinivas Pietambaram, Tarek Ibrahim, Nicholas Psaila, Yonggang Li, Jeff Kaplan, Izabela Murtagh, John Macdonald, Rahul Manepalli, Vinith Bejugam, Dhruba Pattadar, Sreeramagiri Praveen, Jesse Jones – Intel Corporation	***1. 2:00 PM - Hybrid Bonding Surface Roughness Characterization: A RHEED Approach With High Speed and Atomic Scale (sub-nm) Sensitivity at Wafer Level*** Weichang Lin, James Lu, Toh-Ming Lu, Gwo-Ching Wang – Rensselaer Polytechnic Institute; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research	***1. 2:00 PM - Fabrication and Transfer of Fine Pitch RDL Using Si Temporary Carrier Combined With IR Laser Release Approach*** Francois Chancerel, Gilberto Casillas, John Slabbekoorn, Steven Brems, Koen Kennes, Arnita Podpod, Eric Beyne – imec; Peter Urban, Simon Halas, Mario Gram, Thomas Uhrmann, Markus Wimplinger – EV Group
2. 2:20 PM - Optimization of Glass Substrate CTE for Warpage Control and Solder Joint Reliability in Large HPC Packages Pengcheng Yin, Yangyang Lai, Junbo Yang, Karthik Arun Deo, Dalei Yang, Kewei Shou, Seungbae Park – Binghamton University	***2. 2:20 PM - Signal and Power Integrity of Organic, Silicon, Hybrid Interposer in HPC Chiplet-Based System*** Ming-Hung Wu, Yaotsu Chen, Yi-Chin Tsai, Po-Yuan Wei, Liang-Kai Chen, ChungHsuan Wu, Chun-Hong Chen, Sheng-Fan Yang – Global Unichip Corporation	***2. 2:20 PM - IR Laser Debond Process Modeling*** Thomas Sounart, Henning Braunisch, Paul Nordeen – Intel Corporation
3. 2:40 PM - First Demonstration of Low-loss Vertical Interconnects on Multi-Stacked Ceramic-Glass Substrate for 6G Antenna-in-Package Modules Chenhao Hu, Kyoung-Sik (Jack) Moon, Manos M. Tentzeris – Georgia Institute of Technology	***3. 2:40 PM - Experimental Investigation of Cu–Cu Bonding-Induced Stress Coupling with TSV Keep-Out Zones via Raman Spectroscopy*** Jie Li, Keyu Wang, Amaea Tripathi, Shuhang Lyu, Ganesh Subbarayan – Purdue University; Tiwei Wei – University of California, Los Angeles	***3. 2:40 PM - Novel Organic Temporary Bonding Material for High-Temperature Semiconductor Processing Applications*** Taichi Kikkawa, Yuzo Nakamura, Yutaka Hisamune, Satoshi Inada – Mitsui Chemicals, Inc.
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Impact of Glass and Silicon-Bridge on Electrical, Mechanical and Thermal Performance of 2.5D and 2.3D Platforms Heeyoub Kang – Samsung Electronics Co., Ltd.	***4. 3:45 PM - Vertical Interconnects Characterization for 448Gbps/lane Co-Packaged Optics Using Double-Sided Probing Method*** JiaQi Wu, BG Sajay, Teck Guan Lim, Surya Bhattacharya – Institute of Microelectronics A*STAR	***4. 3:45 PM - Study of Sn Damascene Process for Novel Fine Pitch Micro-Bump Formation and Bonding*** Kosuke Yamashita – Fujifilm Electronic Materials Europe; John Slabbekoorn, Jaber Derakhshandeh – imec; Eric Turner, Haiying Zhou – Fujifilm Electronic Materials U.S.A., Inc.; Kazuki Tomota – Fujifilm Business Innovation Corp.
5. 4:05 PM - Development of Long-Term Reliability for Glass Core Substrates with Build-Up Layers Koji Fujimoto, Takahiro Tai, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.	***5. 4:05 PM - Photonic Interconnects in Glass Core for AI Data Center Applications*** Md Rayid Hasan Mojumder, Ziyu Guo, Ning Li, Madhavan Swaminathan – Pennsylvania State University	***5. 4:05 PM - Novel Thin Organic Laser Release Layer With Ultralow Transmittance in UV-A Region for Temporary Bonding and Debonding in Advanced Packaging Application*** Hanlin Chen – Brewer Science, Inc.
6. 4:25 PM - Scaling Interconnect Density with Silicon-Core-Substrate Nano-Integrated Via Technology Seann Ayers, Steven Verhaverbeke, Han-Wen Chen, Suresh Ramalingam – Applied Materials, Inc.	***6. 4:25 PM - Photonic Fabric™ Interconnect for a Scale-Up Network Solution in Accelerated Computing*** Dan Oh, Ankur Aggarwal, Suresh Pothukuchi, Jelena Pesic, Subal Sahni, Parmanand Mishra, Phil Winterbottom, David Lazovsky – Celestial AI	***6. 4:25 PM - Novel Temporary Bonding Film and Debonding Method Adapted for the Fabrication Process of Large Size Panel Packages*** Motohiro Negishi, Yuta Akasu, Koji Yukimatsu, Emi Miyazawa, Tetsuya Enomoto, Tomohiro Ohkubo, Saeko Ogawa, Masanori Natsukawa, Tomohiko Kotake – Resonac Corporation
7. 4:45 PM - InfinityBoard: A Panel-Level Packaging Technology-Platform Roland Rettenmeier, Laurent Nicolet, Michael Kothe, Udo Kirsch, Christian Buchner, Christian Schmid, Thomas Widmann, Dian Zhang – SCHMID Group	***7. 4:45 PM - Advanced 3D Packaging Optics Engine With Integrated Micro-VCSEL Array for Ultra-High Bandwidth Optical Interconnect*** Yuk-Tong Cheng, Murphy Lee, Tzu-Hung Lin, Wang Shi Yu, Jr-Hau He, Chih-Hsiang Ho – Rayleigh Vision Intelligence	***7. 4:45 PM - Electroplated Indium Micro-Bumps: Toward Scalable Low Temperature Ultra-Fine Pitch Interconnects*** Maria-Luisa Calvo-Munoz, Yacoub Sahouane, Mathilde Gottardi, Erwan Mekadem-Belaid, Abdelhak Hassaine, Marie Maubert, Laurence Gabette, Laurence Andreutti, Jean-Marie Quemper, Catherine Pellissier, Chafik Mhamdi, Thierry Mourier – CEA-LETI

Program Sessions: Thursday, May 28, 2:00 p.m. - 5:05 p.m.

Session 22: Reliability of High Current and High Power Packaging Solutions	Session 23: Power Integrity Analysis for High-Performance Computing	Session 24: AI and Machine Learning for Electronics Packaging
Committee: Applied Reliability	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Nokibul Islam** **STATS ChipPAC, Ltd.** **Email: Nokibul.ISLAM@jcetglobal.com** **Yan Li** **Samsung Semiconductor, Inc.** **Email: yanli7274@gmail.com**	**Session Co-Chairs** **Markondeya Raj Pulugurtha** **Florida International University** **Email: mpulugur@fiu.edu** **Atom Watanabe** **IBM Research** **Email: atom@ibm.com**	**Session Co-Chairs** **Pradeep Lall** **Auburn University** **Email: lall@auburn.edu** **Karsten Meier** **TU Dresden** **Email: karsten.meier@tu-dresden.de**
1. 2:00 PM - ENEPES as an Effective Surface Finish for Enhancing Electromigration Reliability in Solder Joints Mai Yokota, Tsuyoshi Maeda, Katsuhisa Tanabe – C. Uyemura & Co., Ltd.	***1. 2:00 PM - Deep Coordination Graph-Based Reinforcement Learning for Multi-Domain PDN Optimization*** Junho Park, Seonguk Choi, Jiwon Yoon, Junghyun Lee, Haeseok Suh, Hyunjun An, Youngsu Yoon, Byeongmok Kim, Jaegeun Bae, Eunji Seo, Inyoung Choi, Joungho Kim – Korea Advanced Institute of Science and Technology	***1. 2:00 PM - Multi-Agent Automation for Design-for-Reliability: From Literature to Auditable Knowledge and Experimental Design*** Jialong Liang, Willem van Driel, G. Q. (Kouchi) Zhang – Delft University of Technology; Jiajie Fan – Fudan University
2. 2:20 PM - Direct-to-Silicon Microfluidic Cooling for Datacenters: Design, Thermal Performance, Reliability, and System-Level Integration Sashikanth Majety, Baris Dogruoz, Venkata Chivukula, Bharath Ramakrishnan, Husam Alissa, Cam Turner, Camille Couturier, Srikant Bharadwaj – Microsoft Corporation; Malik Fahrni, Yann Meier, Remco van Erp, Samuel Higginbotham – Corintis	***2. 2:20 PM - Design Methodology and Power Integrity Analysis of Staggered Current Pattern for Voltage Drop Mitigation in High-Power Multi-Core HPC system*** Hyunwoong Kim, Sungwook Moon, Jungil Son, Chaewon Baek, Seungki Nam – Samsung Electronics Co., Ltd.	***2. 2:20 PM - Physics-Informed Neural Network Approach for Fast Prediction of Temperature Distribution and Hot Spots in Co-Packaged Optics*** Sohrab Sheikh Sofla, Madhavan Swaminathan – Pennsylvania State University
3. 2:40 PM - Enabling Reliability Testing of Solder Interconnects Under Extreme Current Stressing Choong-Un Kim, Dong Seok Lee – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.	***3. 2:40 PM - Dynamic Power Management Methodology for Distributed Vertical Power Delivery in High-Performance Computing Systems*** Sriharini Krishnakumar, Inna Partin-Vaisband – University of Illinois	***3. 2:40 PM - StressScore: Evaluating AI Generated Stress Contours in Advanced Packaging With Contrastive Learning*** Kart Leong Lim – Institute of Microelectronics A*STAR; H S V Thanmaya Bharadwaj Puvvada – Nanyang Technological University (NTU)
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Cu-Core Solder Interconnect Mechanical Shear Strength Under High Current Density Tae-Kyu Lee, Yujin Park, Adnan Mahmud, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.; Young-Woo Lee, Hui-Joong Kim, Jae-Yeol Son, Seul-Gi Lee – MK Electron Co., Ltd.; Choong-Un Kim – University of Texas, Arlington	***4. 3:45 PM - Neural Surrogates for Fast Signal and Power Integrity Co-Simulation and Co-Design of Chiplets Integration*** En-Xiao Liu, Richard Xian-Ke Gao, Wenzu Zhang, Jun Liu, Dingjie Lu, Sridhar Narayanaswamy – Institute of High Performance Computing A*STAR; Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR	***4. 3:45 PM - AI-Driven Surrogate Modeling and Uncertainty Quantification for Active Power Cycling in Power Electronics Packages*** Dharshan Barkur – TU Dresden/Robert Bosch GmbH; Przemyslaw Gromala – Robert Bosch GmbH; Karsten Meier, Karlheinz Bock – TU Dresden
5. 4:05 PM - Evolution and Correlation of Microstructure and Mechanical Properties in Aged SAC/LTS Hybrid Solder Joints Mahbub Alam Maruf, Souvik Chakraborty, Jeffrey Suhling, Pradeep Lall – Auburn University	***5. 4:05 PM - Design Space Exploration of Chiplet and Interposer PDNs for 2.5D AI Systems*** Seungmin Woo, Madison Manley, Muhannad Bakir – Georgia Institute of Technology; Taehoon Kim – Samsung Electronics Co., Ltd.	***5. 4:05 PM - In-Situ Anomaly Detection for Power MOSFET's Degradation Based on Unsupervised LSTM-Autoencoder*** Shaojian Xie, Jiajie Fan – Fudan University; Mesfin Ibrahim, Hiu Hung Lee, Chang Lu – Centre for Advances in Reliability and Safety, New Territories, Hong Kong; Jialong Liang, G. Q. (Kouchi) Zhang – Delft University of Technology
6. 4:25 PM - Real In-situ Imaging of Electromigration of Microbump in 2.5D Package Junbo Yang, Dalei Yang, Karthik Arun Deo, Yuhan Gao – Binghamton University	***6. 4:25 PM - Fast Signal and Power Integrity Analysis Algorithm of UCIe-Based High-Speed Links with Transistor-Level Equalizers*** Yi Zhou, Lewei Tang, Tahsin Shameem, Bobi Shi, Jose Schutt-Aine – University of Illinois	***6. 4:25 PM - Cross-Domain Integrated Digital Twin for HI CPUs*** Mumtahina Islam Sukanya, Aniket Bharamgonda, Abhijit Dasgupta, Ankur Srivastava – University of Maryland
7. 4:45 PM - Effects of Plating Current Density on Electrochemical Reliability of RDL: In-Situ Electrochemical Migration Testing and Time-to-Failure Prediction Hojin Lee, Jeong-Hyeon Baek, Haesu Ahn, Hak-Sung Kim – Hanyang University; Taehoon Kim, Jihye Shim – Samsung Electronics Co., Ltd.	***7. 4:45 PM - PINS: Power-Integrity-Aware Power Delivery Network Synthesis in Interposer-Based Advanced Packaging*** Iris Hui-Ru Jiang, Tzu Han Hsu – National Taiwan University	***7. 4:45 PM - A Physics-Informed AI Platform for SMT Feasibility and Warpage Prediction in Versatile 2.5D Packaging*** Kewei Shou, Junbo Yang, Karthik Arun Deo, Dalei Yang, Pengcheng Yin, Yangyang Lai, Weichen Zhao, Yi Deng, Yuhan Gao, Seungbae Park – Binghamton University

Program Sessions: Friday, May 29, 9:30 a.m. - 12:35 p.m.

Session 25: Optical and Electrical Design for High-Performance Computing	Session 26: Advanced Wafer-to-Wafer Hybrid Bonding	Session 27: Innovation in Glass and Dielectric Materials for Heterogeneous Integration
Committees: Electrical Design and Analysis and Packaging Technologies	**Committee: Interconnections**	**Committee: Materials & Processing**
Session Co-Chairs **Nicolas Boyer, Ciena Corporation** **Email: nboyer@ciena.com** **Mike Gallagher, Qnity** **Email: michael.gallagher@qnityelectronics.com** **Srikrishna Sitaraman, Marvell Technology, Inc.** **Email: srikrishna.sitaraman@gmail.com**	**Session Co-Chairs** **Anne Jourdain** **imec** **Email: anne.jourdain@imec.be** **Tiwei Wei** **University of California, Los Angeles** **Email: tiwei32@ucla.edu**	**Session Co-Chairs** **Jay Cho** **GlobalFoundries, Inc.** **Email: jay.cho@gf.com** **Ziyin Lin** **Intel Corporation** **Email: ziyin.lin@intel.com**
1. 9:30 AM - Advancing Interconnect Performance and Reliability with Innovations in 3D Photonic Integration, Packaging and Fiber Coupling Sufi Ahmed, Darius Bunandar, Sandeep Sane – Lightmatter; Suresh Jayaraman – Amkor Technology, Inc.	***1. 9:30 AM - Novel Process Integration for Highly Reliable and Manufacturable 0.4µm-pitch 50M Cu-Cu connections*** Yukako Ikegami, Ken Arano, Masanori Chiyozono, Kengo Kotoo, Kan Shimizu, Yoshihisa Kagawa – Sony Semiconductor Solutions	***1. 9:30 AM - Non-Destructive Characterization of Laser Modification in Glass for Selective Etching to Fabricate Through-Glass Vias (TGV) in Advanced Packaging*** Mruga Panse, Kyoung-Sik (Jack) Moon, Mohan Kathaperumal, C. P. Wong – Georgia Institute of Technology; Jehhoon Bhang, Stefan Janssen, Youngho Suh – LG Electronics; Myungjoo Park – LG Chem
2. 9:50 AM - Enabling Photonic Fabric™ Chiplets for Co-Packaged Optics in AI Data Centers Suresh Pothukuchi, Ankur Aggarwal, Jared Farr, Sagar Dubey, Dan Oh, Joy Zhan – Celestial AI	***2. 9:50 AM - Reducing Wafer-to-Wafer Bonding Misalignment to Enable 140nm Pitch Hybrid Bonding*** Christopher Netzband, Andrew Tuchman, Joshua Greklek, Sunny Ilseok Son, Sayantan Das, Brittany Hedrick, Hirokazu Aizawa – TEL Technology Center, America, LLC; Yuki Taniguchi, Atsushi Nagata, Shinichi Tan – Tokyo Electron Kyushu, Ltd.; Nathan Ip – Tokyo Electron America, Inc.; Angelique Raley – Tokyo Electron, Ltd.	***2. 9:50 AM - Crack-Free Through-Hole Drilling of 400µm-thick Aluminosilicate Glass by Direct Laser Processing*** Toshio Otsu, Tsubasa Endo, Hiroharu Tamaru, Yohei Kobayashi – University of Tokyo
3. 10:10 AM - V-Groove Based Edge Coupling Enabled by Optical Glass Coupler Attach for Co-Packaged Optics Zhou Yang, Fan Fan, Bohan Shan, Ryan Mcqueen, Jesus Nieto Pescador, Corey Logston, Pratyasha Mohapatra, Anita Dey, Anurag Tripathi, Timothy Gosselin, Shan Zhong, Nicholas Psaila – Intel Corporation	***3. 10:10 AM - Wafer-to-Wafer Hybrid Bonding Technology with 200nm Interconnect Pitch*** Stefaan Van Huylenbroeck, Lieve Bogaerts, Koen D'have, Soon Aik Chew, Hung-Chieh Tsai, Serena Iacovo, Sven Dewilde, Shuo Kang, Joeri De Vos, Zsolt Tokei, Eric Beyne – imec	***3. 10:10 AM - Development of Low-Modulus Primer "Cbla" to Prevent SeWaRe in Glass-Core Substrates*** Daichi Kobayashi, Marie Ohuchi, Kosuke Urashima, Satoshi Takayasu, Yuzuru Kobayashi, Masahiro Miyasaka, Tomohiko Kotake – Resonac Corporation
	Refreshment Break: 10:30 a.m. - 11:15 a.m.	
4. 11:15 AM - Power Distribution Network (PDN) Design and Analysis for Multi-Stack 3D Heterogeneous Integrated High Bandwidth Memory (3D-HI-HBM) Module Jiwon Yoon, Haeseok Suh, Junho Park, Junghyun Lee, Youngsu Yoon, Eunji Seo, Byeongmok Kim, Hyunjun An, Jaegeun Bae, Hyunseo Uhm, Chaemin Yang, Joungho Kim – Korea Advanced Institute of Science and Technology	***4. 11:15 AM - Robust Wafer to Wafer Cu Direct Bonding for Multi Stack CBA Technology in Future 3D Flash Memory*** Masayoshi Tagami, Hiroyuki Ashidate, Mitsuhiko Noda, Ryo Tanaka, Mamoru Watanabe, Ryuta Mizumoto, Genki Sawada, Yoshiharu Ono, Tomoyuki Takeishi, Katsuyuki Sekine – KIOXIA Corporation	***4. 11:15 AM - Novel Photosensitive Material with Low Shrinkage and Low Dielectric Properties for High-Density RDL in Glass Packaging*** Ritsuya Kawasaki, Kazuya Nakashima – Sumitomo Bakelite Co., Ltd.; Yu-Chieh Lin, Hyunggyu Park, Kyoung-Sik (Jack) Moon, Mohan Kathaperumal, C. P. Wong – Georgia Institute of Technology
5. 11:35 AM - Thermal-Aware Power Integrity Analysis of Embedded Integrated Voltage Regulator (IVR) in Interposer for 2.5D High-Power HPC Hyunwoong Kim, Sungwook Moon, Jungil Son, Jinho Kim, Seungki Nam – Samsung Electronics Co., Ltd.	***5. 11:35 AM - Process Integration for 300nm Pitch Hybrid Bonding with SiCN: 50nm Overlay, Fine-Grain Cu Metallurgy, and Reliability Assessment*** Kai Ma, Nikolaos Bekiaris, Jingting Chen, Jing Xu, Huixiong Dai – Applied Materials, Inc.; Jakob Haimberger, David Goldberger, Gernot Probst, Thomas Uhrmann, Markus Wimplinger – EV Group	***5. 11:35 AM - Digital Lithography Patterning of Novel Dry Film Resists for High Aspect Ratio Cu Pillar Applications on 310x310mm² Panel Substrates*** Ksenija Varga, Lisa Berger, Roman Holly, Tobias Zenger – EV Group; Hajime Furutani, Masayuki Kishino – Asahi Kasei Corporation
6. 11:55 AM - Multi-Physics Design Methodology for Enlarged Chiplets Interconnections in Advanced Packaging Chih-Yi Huang, Teck Chong Lee, Po-Chih Pan, Tsung-Tang Tsai, Chung-Hung Lai, Wei-Hong Lai, Chin-Li Kao, Chen-Chao Wang, Chih-Pin Hung, Yung-Sheng Lin – Advanced Semiconductor Engineering, Inc.; Smith Chen, Fu-Chen Chu – Advanced Semiconductor Engineering, Inc. (US)	***6. 11:55 AM - Synchrotron-Based Characterization of Cu/SiCN Pretreatment for Hybrid Bonding via Ozone/Ethylene Radical Activation*** Bungo Tanaka, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Soichiro Motoda, Tetsuya Nishiguchi, Yuma Okadome – MEIDEN NANOPROCESS INNOVATIONS, INC.	***6. 11:55 AM - Low-Warpage Multilayer RDL Technology Using Thin Dry Film Dielectric with Reduced Curing Shrinkage and Dry Etched Ultrafine Via*** Yusuke Naka, Tadahiko Hanada – Taiyo Ink Mfg. Co., Ltd.; Osamu Okada, Yoichiro Kurita – Institute of Science Tokyo; Takafumi Fukushima, Hiroyuki Hashimoto – Tohoku University; Yasuhiro Morikawa, Fumito Ootake – ULVAC, Inc.; Masahiro Sawa, Yasuhiro Ogo – JCU Corporation
7. 12:15 PM - Topology-Driven Organic Interposer Design for RDL Layer Reduction in Automotive UCIe-A 2.5D Chiplet Packages Shuuichi Kariyazaki, Hiroki Shibuya, Tatsuaki Tsukuda – Renesas Electronics Corporation	***7. 12:15 PM - Nanostructured Porous Cu for Ultralow-Temperature Direct Bonding*** Su-Ching Hsiao, Wei-Lan Chiu, Shih-cheng Yu, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo, Shih-Chieh Chang – Industrial Technology Research Institute	***7. 12:15 PM - Inkjet-Printed Photo-Imageable Dielectric for Large-Area Uniform Coating and High-Resolution Patterning in Advanced Packaging.*** Wanhyuk Chang, Youngho Suh, Keejoon Kim, Beomsoo Kim – LG Electronics; Hyunsoon Lim, Wooram Oh, Minyoung Lim, Myungjoo Park – LG Chem

Program Sessions: Friday, May 29, 9:30 a.m. - 12:35 p.m.

Session 28: Beyond Silicon: Innovation in Glass Substrates and Panel Level Packaging	Session 29: Innovation in Metallization, Alignment, Additive Manufacturing, and Low Temperature Interconnection	Session 30: Thermal Management and Cooling Simulation
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Timo Henttonen** **Microsoft Corporation** **Email: timo.henttonen@microsoft.com** **Venkata Mokkapati** **AT&S AG** **Email: v.mokkapati@ats.net**	**Session Co-Chairs** **Jae-Woong Jeong** **Korea Advanced Institute of Science and Technology** **Email: jjeong1@kaist.ac.kr** **Chukwudi Okoro** **Corning Research and Development Corp.** **Email: okoroc@corning.com**	**Session Co-Chairs** **Yong Liu** **ON Semiconductor** **Email: Yong.Liu@onsemi.com** **Patrick McCluskey** **University of Maryland, College Park** **Email: mcclupa@umd.edu**
1. 9:30 AM - RDL Interposer Scheme Optimization for Electrical Performance with Varied RDL and Dielectric Via Thicknesses Chia-Hsiang Lin, Kathy Yan, Chien-Hsun Lee, Eric Chen, Rachel Lu, Yu-Wei Chen – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Game-Changing Nanosolder Technology: Self-Assembling Adhesives for Sub-10µm Ultra-Fine Interconnects*** Jin Woo Huh, Seol Kim, Changhoon Sim, Kyungsub Lee – Nopion Co., Ltd.; Tae-Wan Kim, Hyeong-Bin Park, Hak-Sung Kim – Hanyang University	***1. 9:30 AM - Mitigating the Thermal Bottleneck in Advanced BEOL Interconnects*** Xinyue Chang – imec/KU Leuven; Herman Oprins, Melina Lofrano, Bjorn Vermeersch, Seongho Park, Zsolt Tokei, Ingrid De Wolf – imec
2. 9:50 AM - First Demonstration of Stitching-Free Exposure Over an Ultra-Large 18-Reticle Area with High-Resolution 1.5µm Line/Space on Glass Substrates Naoya Sohara, Toshimitsu Arai, Ryotaro Takahashi, Naoki Gotou, Hirosuke Takamatsu – USHIO	***2. 9:50 AM - Additively Manufactured Foldable Interconnects for 4D/Morphing Origami-Inspired mm-Wave Arrays*** Hani Al Jamal, Manos M. Tentzeris – Georgia Institute of Technology	***2. 9:50 AM - Multiscale Thermal Simulator Development for High Resolution Hot Spot Analysis*** Hiroyuki Ryoson – Dexerials Corporation; Takayuki Ohba, Shinji Sugatani – Institute of Science Tokyo
3. 10:10 AM - First Demonstration of a 200x200 mm² Large Area Glass Substrate Jaewon Lee, Hyunggyu Park, Seungwoo Cha, Muhannad Bakir – Georgia Institute of Technology; Srujan Penta – Georgia Institute of Technology/Marvell	***3. 10:10 AM - Rapid Additive Manufacturing of Multi-Layered RDL and Interconnects Enabled by Hybrid Metal-Polymer*** Natalya K Crawford – University of Texas, Austin	***3. 10:10 AM - Experimental Characterization of Thermal Transport in Cu–Diamond Microbumps*** Keyu Wang, Zhengwei Chen, Noah Opendo, Amy M. Marconnet – Purdue University; Shusmitha Kyatam, Miguel A. Neto – University of Aveiro; Joana-Catarina Mendes – Institute of Telecommunications; Tiwei Wei – University of California, Los Angeles
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Technical Study of RDL in Advanced Package Using Ultra-Low Df Film-Type Photo Imageable Dielectric Keigo Yamaguchi, Yuta Yamakawa, Megumi Tanaka, Masayuki Miura, Daisuke Ando, Naoki Sato, Takuya Komine, Eiichi Hayashi, Takashi Kariya – Samsung (Japan)	***4. 11:15 AM - High-Precision Wafer-Level Bonding in Thin-3D: A Moiré Pattern and Deep-Learning Alignment Approach*** Chen-Chia Chang, Shie-Ping Chang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; TingRay Chung – Horace Greeley High School; Chih-Chao Yang, Po-Jung Sung, Nien-Chih Lin – Taiwan Semiconductor Research Institute	***4. 11:15 AM - Flash Boiling of Methanol/Water Mixture in Silicon Microchannel Thermal Dissipation Unit for High Heat Flux Thermal Management*** Naarendharan Meenakshi Sundaram, Zachary Wong, Priyanth Elango, Subramanian Iyer, Timothy Fisher – University of California, Los Angeles
5. 11:35 AM - Dry-Film-Only Process for Panel-Level 2.xD Packaging Enabling 2/2µm Line/Space RDL and 5µm Microvias Ryo Kikuta, Sachiko Matsushita, Ryosuke Kimura, Katsuaki To, Masashi Minami, Sadaaki Katoh – Resonac Corporation	***5. 11:35 AM - Metallization Challenges: Conformable Deposition for Super High-Aspect Ratio (> 100) Fine TGV and Cu Pillar Embedment for 1mm-Deep Fat TGV*** Chang Liu, Jiayi Shen, Bungo Tanaka, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Kiyoharu Mori – NICHe; Hidenori Miyauchi – Micro Technology Co., Ltd.	***5. 11:35 AM - Advanced Thermal Solutions for Thin 3D: AlN 3D Heat Dissipation Network*** Shang-Lun Pai, Shie-Ping Chang, Chen-Chia Chang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Po-Jung Sung, Nien-Chih Lin, Chih-Chao Yang – Taiwan Semiconductor Research Institute; Kyle Huang, Gary Huang, Jeremy Lin – Skytech
6. 11:55 AM - Tether-Free Micro-Transfer-Printing of Si-Based Micro-Inductors: Demonstration of on-Glass and in-Silicon Integration for PowerSoC Applications Amit Tanwar, Muhammet Genc, Liang Ye, Somnath Pal, Ranajit Sai, Cian O'Mathuna, Brian Corbett – Tyndall National Institute; Sambuddha Khan – Tyndall National Institute/University College Cork	***6. 11:55 AM - Glass-Stacked Interposers with Microdispensed Silver Nanopaste for Low-Temperature 3D Interconnection*** Sam LeBlanc, Jason Benoit – nScrypt; Bryce Gray, Kenneth Church – Sciperio	***6. 11:55 AM - High-Fidelity Package-Level Conjugate Thermal-Flow Simulation for a Memory-on-Logic 3D System with Embedded Liquid-Cooling*** Yujui Lin, Hongchi Liu, Luke Min, Mehdi Asheghi, Kenneth Goodson – Stanford University; Walker Turner, John Wilson, Tahir Cader, C. Thomas Gray – Nvidia Corporation
7. 12:15 PM - Advanced Manufacturing Solutions for Large Form Factor Patch on Interposer (PoINT) Scaling Andrew Carlson, Qichang Wang, Khalid Abdelaziz, Fatemeh Rahimi, Tingting Gao, Xiao Lu – Intel Corporation	***7. 12:15 PM - Advancing Sustainable Die-Attach Technologies with Filled Bio-Sourced Epoxy Resin Systems*** Frederic A. Banville, Saria Berger, Cloe Druillole, David Danovitch, Serge Ecoffey – University of Sherbrooke; Catherine Marsan-Loyer – Centre de Collaboration MiQroInnovation (C2MI); Josée Labrecque, David Gendron – Kemitek; Benjamin Busseniers, Katherine Pilger, Valerie Oberson – IBM Canada, Ltd.	***7. 12:15 PM - Detection of Local Dryout in Two-Phase Microchannel Heat Sinks Using a Multi-Chip Module Thermal Test Vehicle*** Rishav Roy, Yang Liu, Sarwesh Parbat, David J. Apigo, Manohar Bongarala, Syed Faisal, Todd Salamon, Mark Cappuzzo, Ting-Chen Hu, Rose Kopf, Bob Farah, Mark Earnshaw – Nokia Bell Labs

Program Sessions: Friday, May 29, 2:00 p.m. - 5:05 p.m.

Session 31: 3D Integration, TSV, and Hybrid Bonding Innovations	Session 32: Solder and Through Via Interconnections: Material & Process Innovations	Session 33: Emerging Materials and Interconnect Technologies for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs **Lihong Cao** **Advanced Semiconductor Engineering, Inc.** **Email: lihong.cao@aseus.com** **Peng Su** **Hewlett Packard Enterprise** **Email: peng.su1@hpe.com**	**Session Co-Chairs** **Yoshihisa Kagawa** **Sony Semiconductor Solutions** **Email: Yoshihisa.Kagawa@sony.com** **Jean-Charles Souriau** **CEA-LETI** **Email: jcsouriau@cea.fr**	**Session Co-Chairs** **Fumihiro Inoue** **Yokohama National University** **Email: inoue-fumihiro-ty@ynu.ac.jp** **Zhangming Zhou** **IC Packaging Agent Inc.** **Email: zhou.zhming@gmail.com**
1. 2:00 PM - Die-To-Wafer Hybrid Bonding Technology Down to 1µm Pitch for Multi-Die Stacking Integration Melissa Najem, Agathe Lerat, Carine Ladner, Loic Sanchez, Julien Diaz, Renan Bouis, Jérôme Dechamp, Antonio Roman, Stéphane Nicolas – CEA-LETI	***1. 2:00 PM - Fluxless Thermo-Compression Bonding of 4X Reticle Die Stack*** Kartik Srinivasan, Danis Nugroho, Nicholas Cool, Mine Kaya, Niranjan Parab, Karthik Visvanathan, Shan Zhong – Intel Corporation	***1. 2:00 PM - Optical RDL Interposer Technology Using Polymeric Hybrid Bonding and Waveguide for Integrated CPO*** Toshihiko Katayama, Kyohei Hayashi, Kazuki Inoue, Ryota Kinoshita, Yuma Tanaka, Motoya Kaneta – Sumitomo Bakelite Co., Ltd.; Takafumi Fukushima – Tohoku University
2. 2:20 PM - Enabling Scalable Die-to-Wafer Hybrid Bonding Through Die Distortion Correction and Grid Measurement Alex Hsu, Etienne De Poortere – ASML; Anne Jourdain, Andy Miller, Eric Beyne, Imene Jadli, Samuel Suhard, Koen Kennes, Amir-Hossein Tamaddon, Victor Manuel Blanco Carballo – imec	***2. 2:20 PM - Simplified Fluxless Bonding via Ultraviolet Activation: Enabling High-Reliability Fine-Pitch Interconnections*** You-Gwon Kim, Dong-Hoon Yoo, Hyeong-Bin Park, Jong-Whi Park, Seungchul Shin, Hak-Sung Kim – Hanyang University; Dongsuk Kang – Hanwha Semitech Co.	***2. 2:20 PM - Multi-Mode Polymer Waveguides for Co-Packaged Optics*** Ross Johnson, Yaming Jiang, Mike Gallagher – Qnity; Rui Zhang, Zhou Lu – DuPont; James Ryley, Barbara Roeske, Henry Cain, Nancy Tassi, John Allen, Elizabeth Brundage, Masaki Kondoh – DuPont Electronics and Imaging
3. 2:40 PM - Reworkable Die-to-Wafer Hybrid Bonding Process Rajan Gangadharan, Dominik Suwito, Thomas Workman, Laura Mirkarimi, Suhail Sadiq, Arianna Avellan, Gill Fountain, Cyprian Uzoh, Justin Chen, Pawel Mrozek – Adeia	***3. 2:40 PM - Fluxless TCB with Atmospheric Pressure Plasma Surface Treatment Enabling Ultra-Fine Pitch Solder Micro-Bumps for 3D Integration*** Mohammed Alhendi, Katsuyuki Sakuma, Luke Darling, Roy Yu – IBM Research; Neng Liu – IBM Corporation; Ma Zetao, Kai-ming Yeung, Ming Li, Li Cheng – ASM Pacific Technology, Ltd.	***3. 2:40 PM - Layer Transfer of Epitaxial Ru by Metal-Metal Bonding: Towards Single-Crystal Interconnects*** Christoph Adelmann, Francois Chancerel, Jean-Philippe Soulié, Steven Brems, Zsolt Tokei, Seongho Park – imec; Peter Kerepesi, Michael Dornetshumer, Florian Medl, Tobias Wernicke, Christoph Floetgen, Markus Wimplinger – EV Group
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Enabling Beyond-16-Layer 3D Stacking with Ultra-Thin Die Hybrid Bonding with Integrated Bonder Guan Huei See, Shin-Puu Jeng, Arvind Sundarrajan, Loke Yuen Wong, Yin Wei, Patrick Lim, Xiaodong Chen, Santosh Kumar Rath, Xing Zhao – Applied Materials, Inc.	***4. 3:45 PM - Processing and Cold Testing of Superconducting and Thermal Conducting TSVs*** Qian Yang, Jaber Derakhshandeh, Anish Dangol, A. M. Vadiraj, Anne Jourdain, Geraldine Jamieson, Karl Ceulemans, Rami Chukka, Koen Kennes – imec	***4. 3:45 PM - Reflectivity-Tunable Localized Epitaxy for Multi-Tier Monolithic 3D ICs*** Ching-Lin Chen, Yu-Chun Chen, Yu-Ming Pan, Chiao-Yen Wang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chih-Chao Yang – Taiwan Semiconductor Research Institute; Chang-Hong Shen – National Tsing Hua University; Chenming Hu – University of California, Berkeley
5. 4:05 PM - Low distortion fusion bonding evaluation using pneumatically warped wafers Utkarsh Jain, Koen D'have, Damien Leech, Serena Iacovo, Koen Kennes, Steven Brems, Eric Beyne – imec; Philipp Schmidt, Philippe Muller, Dennis Bumueller, Thomas Schmidt – SUSS MicroTec GmbH	***5. 4:05 PM - BBCube 2.5D: A Bumpless 2.5D Integration Technology Enabling High-Density Inter-Chiplet Interconnection Using Waffle-Wafer and Via-Last TSVs*** Norio Chujo, Shinji Sugatani, Koji Sakui, Masao Taguchi, Hiroyuki Ryoson, Takayuki Ohba – Institute of Science Tokyo	***5. 4:05 PM - Siloxane Elastomer Zero-CTE Substrates for Foldable FPCB and Stress-Free Semiconductor Packaging*** Hyungshin Kweon, Seung-Mo Kang, SungHun Park, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology
6. 4:25 PM - Wafer Bonder and Lithography Co-Optimization for Sub-5nm Post-Bonding Overlay in Backside Power Delivery Architectures Andrew Tuchman, Christopher Netzband, Sheldon Meyers, Sayantan Das, Sunny Ilseok Son – TEL Technology Center, America, LLC; Leon van Dijk, Niyam Haque, Manav Tiyagi, Lieneke Kusters – ASML; Nathan Ip – Tokyo Electron America, Inc.; Angelique Raley – Tokyo Electron, Ltd.	***6. 4:25 PM - TSV Stress and Cu Pumping Prediction via Machine Learning on EBSD–Raman and Optical Correlations*** Zhenliang Pan, Tiwei Wei – University of California, Los Angeles; Jie Li, Shuhang Lyu – Purdue University	***6. 4:25 PM - Characterization of Solderless Connection by Laser Welding and Its Application on Power Module*** Ming-Hung Chen, Vik Chou, Chun-Yi Cheng, Yung-I Yeh – Advanced Semiconductor Engineering, Inc.
7. 4:45 PM - Enabling Ultra Low Temperature Hybrid Bonding for D2W Scaling Veronica Strong, Jeff Bielefeld, Richard Vreeland, Haris Khan Niazi, Siyan Dong, Michael Njuki, Brandon Rawlings, William Brezinski, Trianggono Widodo, Saurabh Chauhan,, Pilin Liu, Satyajit Walwadkar – Intel Corporation	***7. 4:45 PM - Chemically-Tailored Cu Electroplating and Contactless Isostatic-Pressure Annealing of 1mm-Thick Full Glass Wafer Cu Through-Glass Vias (Cu-TGVs)*** Murugesan Mariappan, Takamichi Miyazaki, Takafumi Fukushima – Tohoku University; Kiyoharu Mori – T-Micro; Jinta Nampo, Masahiro Sawa – JCU Corporation	***7. 4:45 PM - Extreme High-Temperature Evaluation of Printed Platinum Materials for Aerospace Applications*** Abdullah Obeidat, Waleed Alshaibani, Erik Busse, Olya Noruz Shamsian, Stephen Gonya, Mark Poliks – Binghamton University; Masoud Mahjouri-Samani – NanoPrintek, Inc.; Felippe Pavinatto – GE Aerospace Research

Program Sessions: Friday, May 29, 2:00 p.m. - 5:05 p.m.

Session 34: Optimizing Power Delivery, Thermal Management, and Metrology Solutions for Next-Generation Devices	Session 35: Reliability of Advanced Automotive, AI, and Interconnect Packaging Solutions	Session 36: Flexible Electronics and Thin-Assembly Warpage
Committee: Emerging Technologies	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs **Premachandran Chirayarikathuveedu** **Menlo Microsystems** **Email: 319prem@gmail.com** **Tengfei Jiang** **University of Central Florida** **Email: tengfei.jiang@ucf.edu**	**Session Co-Chairs** **Tz-Cheng Chiu** **National Cheng Kung University** **Email: tcchiu@mail.ncku.edu.tw** **Richard (Shiguo) Rao** **Marvell Technology, Inc.** **Email: richardrao@marvell.com**	**Session Co-Chairs** **Xuejun Fan** **Lamar University** **Email: xuejun.fan@ieee.org** **Suresh K. Sitaraman** **Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 2:00 PM - 3D Analysis of Hybrid Copper Bonding Through X-Ray Photon-Counting Nano-CT Imaging Till Dreier, Julius Hållstedt – Excillum AB; Darius Rückert – Voxray GmbH; Spyridon Gkoumas – DECTRIS Ltd.	***1. 2:00 PM - Understanding the Effect of Bismuth and Surface Finish on Thermo-Mechanical Reliability of Flip-Chip BGA Solder Joints*** Varun Thukral, Eleni Tsepi, Lara Reboucas, Pieter Gommers, Sharan Kishore, Abdullah Fahim, C.S. Foong – NXP Semiconductor, Inc.	***1. 2:00 PM - Printing Path Optimization for Reliability Enhancement in Direct-Writing Flexible Circuits*** Yusen Nie, Luke McGinnis, Rui Chen – Eastern Michigan University
2. 2:20 PM - Microchannel-Embedded 3D-Printed Ceramic Substrates for Liquid-Cooled Power Module Packaging Haksoon Jung, Jimin Kwon – Ulsan National Institute of Science & Technology; Seongju Kim – Hanbat National University	***2. 2:20 PM - A Real-Time Resistance Monitoring Architecture Using Artificial Intelligence for Accelerated Life Testing and PHM of Electronic Assemblies*** Shaheen Pouya, Jeffrey Suhling – Auburn University; Saad Hamasha – Binghamton University	***2. 2:20 PM - Multilayer Additive Circuit Process-Performance-Reliability Interactions in Dynamic Flexing of Wearable Applications*** Pradeep Lall, Avhishek Jha – Auburn University
3. 2:40 PM - 3D Stacked GPU Architecture with Ultra-Thin 3D DRAM Dies and Voltage Regulators Embedded into Glass Substrate Pin-Jun Chen, Janak Sharda, Po-Kai Hsu, Muhannad Bakir, Shimeng Yu – Georgia Institute of Technology; Min Gyu Park, Sung Kyu Lim – University of Southern California	***3. 2:40 PM - Automotive Reliability of Micro–Cu Pillar Bumps for 2.5D Chiplet Integration*** Koichi Ando, Yoshiaki Yamada, Hideaki Tsuchiya, Hiroki Shibuya – Renesas Electronics Corporation	***3. 2:40 PM - Interfacial Fracture Characterization Using Wedge Testing of Electroless Plated Films on Additively Manufactured Conductive Polymers*** Joshua Corbin, Nicholas Ginga – University of Alabama in Huntsville; Sharmin Jahan, Nathan Lazarus – University of Delaware
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Efficiency Meets Fidelity: A Computational Paradigm for 3D X-Ray Imaging of HBM Packages Yang Yu, Jie Wang, Richard Chang, Ramanpreet Pahwa, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong, Leong Ching Wai – Institute of Microelectronics A*STAR	***4. 3:45 PM - Enhanced Fault Localization Approach for Advanced Packaging with RDL Interconnection Nano-Defects*** Yi-Sheng Lin, Yu-Jing Cheng – Advanced Semiconductor Engineering (Taiwan); Wiwy Wudjud, Chen-Chao Wang, Chih-Pin Hung, Lihong Cao – Advanced Semiconductor Engineering, Inc.; Cheng-Hsin Liu – Advanced Semiconductor Engineering, Inc. (US); Yu-Ting Lin – Advanced Semiconductor Engineering, Group, Inc. (Taiwan)	***4. 3:45 PM - Mechanical Simulation of Stretchable Sensors Conforming to Non-Euclidean Surfaces using ANSYS LS-DYNA*** Sara Lieberman, Mark Poliks – Binghamton University; Felippe Pavinatto – GE Aerospace Research
5. 4:05 PM - Double-Sided Chemical Vapor Deposition (CVD) Diamond-filled Through Vias for Enhanced Vertical Heat Transport in 3D Heterogeneous Integration Ye Yang, Tiwei Wei – University of California, Los Angeles; Joana-Catarina Mendes, Gil Cabral – Institute of Telecommunications; Miguel A. Neto – University of Aveiro	***5. 4:05 PM - Dependence of Leakage Current Characteristics on Bonding Dielectrics in Fine-Pitch Hybrid Cu Bonding*** Sohye Cho, Hyeonmin Lee, Young-Chang Joo – Seoul National University; Seokho Kim, Hojin Lee, Seunghun Lee – Samsung Electronics Co., Ltd.	***5. 4:05 PM - Warpage Prediction after Compression Molding Using Cure-Dependent Viscoelastic Properties*** Bongtae Han, Sukrut Prashant Phansalkar – University of Maryland
6. 4:25 PM - Wafer-Level Integrated 1200V SiC MOSFET Package with Room-Temperature Wafer Bonding and Embedded Microfluidic Cooling Pan Liu, Xinyue Wang, Jiuyang Tang, Hao Guan, Jiajing Nie – Fudan University; G. Q. (Kouchi) Zhang – Delft University of Technology	***6. 4:25 PM - Reliability Enhancement of FC-QFN Packages Using Cu Pillar Bump with PSPI and Buffer RDL for ULK*** Daehyun Kim – Samsung Electronics Co., Ltd.	***6. 4:25 PM - Warpage Prediction of PCB in Multi-Laminating Processes Considering Cure Shrinkage and Anisotropic Visco-Elastic Properties of Prepreg Core*** Sanjay Kumar, Woong-Kyoo Yoo, Jaesung Kim, Chae-Young Ahn, Hak-Sung Kim – Hanyang University; Chan Hyuk Park, Jinwoong Kim – Doosan Corporation Electro-Materials BG; Hyung-mo Koo – Shin & Co.
7. 4:45 PM - An Innovative Automated Tracing Method for Sub-Micron Defect Identification in Advanced Packages Cheng-Hsin Liu, Yu-Jen Chang – Advanced Semiconductor Engineering, Inc. (US); Yi-Sheng Lin, Yu-Jing Cheng – Advanced Semiconductor Engineering (Taiwan); Yu-Ting Lin, Fan-Ju Hsiao – Advanced Semiconductor Engineering, Group, Inc. (Taiwan); Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***7. 4:45 PM - Reliability Evaluation of 10-Second Cu/Polymer Hybrid Bonding for Next-Generation 3D Integration*** Tzu-Yu Chen, Yu-Lun Liu, Jia-Rui Lin, Yuan-Chiu Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Kazuaki Ebisawa, Makiko Irie, Ya-Chien Chuang, Hsiaowei Yeh, Satoshi Fujimura – Tokyo Ohka Kogyo Co., Ltd.	***7. 4:45 PM - Coupled Thermo-Mechanical-Chemical Simulation Framework for Warpage and Stress Analysis in PMC*** Kyeong-Bin Kim, Eun-Ho Lee – Sungkyunkwan University

Session 37: Interactive Presentations Thermo-Mechanical Stress and Reliability Analysis for Materials in Future Packaging

Committee: Interactive Presentations

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1. Experimental Studies of Assembly Materials Creep Behaviors and The Impact to Package Warpage
Ziyin Lin, Yanbiao Chu, Mohammad Kabiri, Cih Cheng – Intel Corporation

2. Layout-Driven FEM for Thermal and Thermo-Mechanical Analysis of MPGA and BGA packages
Woongkee Kim, Hyunggyun Noh, Youngbong Kim, Sanggon Lee – Samsung Electronics Co., Ltd.

3. In-Situ Observation and Modeling of Crack Velocity at Wafer-to-Wafer Bonding Interface
Kyeong-Bin Kim, Ju-Yong Shin, Eun-Ho Lee – Sungkyunkwan University; Haeri Kim, Jeong Wonyeop, YoungSu Yun, Jong Han Shin – SK hynix Inc.; Jiho Kang – Absolics Inc.

4. A Novel and Cost-Effective Evaluation Strategy for Solder Joints for HPC and AI Applications
Peng Su, Omar Ahmed – Hewlett Packard Enterprise; Leif Hutchinson, Bernard Glasauer – Juniper Networks

5. Methodology for Root Cause Analysis of 3D Multi-Chip Module Severely Damaged in Data Center Application
Charles Odegard, Alfred Griffin, Kasey Adams, Venkat Kalyanaraman, James McElrath, Anagha Kulkarni – Texas Instruments, Inc.

6. Finite Element Analysis Based Methodology to Predict Electrical Shifts due to Mechanical Stress
Siva Gurrum, Hung-Yun Lin, Alexander Gamez, Li Jen Choi, Benjamin Amey, Ann Concannon – Texas Instruments, Inc.

7. Thermal Behavior of Hybrid Bonding Interfaces in Advanced Packaging Technologies
Bijan Nili, Charles El Helou, Hadi Zandavi, Siyan Dong, Yi Shi, Tushar Talukdar, Je-Young Chang, Aleksandar Aleksov – Intel Corporation

8. FEA-Integrated 3PB and BOR Testing for Fracture Strength Characterization of Ultrathin Dies: Effects of Thickness, Surface Conditions, and Anisotropy
Jun-Seop Song, Sang-Il Kim, Gyu-Won Kim, Woong-Kyoo Yoo, Hak-Sung Kim – Hanyang University; Jong-Woon Yoo, Sang-Hoon Ko – SK hynix Inc.

9. Simulation-Based Corrective Strategies for Warpage Behavior in Automotive Electronic Assemblies
Chih-Yang Weng – WNC Corporation; Shen-Yu Yang, Chao-Chieh Chan – Wistron NeWeb Corporation; Chang-Chun Lee – National Tsing Hua University

10. Stress Analysis of Cu-Cu Hybrid Bonding Interface Under Thermal Loading
Haozhong Wang, Hongtao Chen – Harbin Institute of Technology (Shenzhen); Binxu Ma, Peijiang Liu, Wanchun Tian, Xiaofeng Yang – China Electronic Product Reliability and Environmental Testing Research Institute; Hang Liang – Anhui Polytechnic University; Xincheng Zhang – Xiamen University

11. Thermal Characterization and Power Dissipation Enhancement of Hybrid-Bonded Chip Stack
Yong Han – Institute of Microelectronics A*STAR

12. Orientation-Engineered AlN for Lateral Heat Spreading and Hotspot Management in 2.5D/3.5D ASICs on the Cloud AI Platform
Jun-Nan Liu, Tzu-Tai Chiu, Kuan Chung Fu, Chih Huang Lai – National Tsing Hua University

13. AI Headnodes Socketed Interconnect Yield, Warpage, and Functionality
Steven Klein, Amit Abraham, Alexander Huettis, Taylor Rawlings, Eric Erike, Jacob Schichtel, Sugadh Bakare, Srinivasa Aravamudhan, Renn Chan Ooi, Prasanna Raghavan – Intel Corporation

14. Liquid Metal Cooling for High-Power Electronics Driven by Magnetohydrodynamic Effect
Huicheng Feng, Bin He, Gongyue Tang, Xiaowu Zhang, Javen Tan – Institute of Microelectronics A*STAR

15. A Holistic Study of Board Level Reliability of CoWoS-R Advanced Packaging on Open Accelerator Modules
Sing-Da Jiang, Jing-An Huang, Chi-Shiang Chiou, Shih-Wei Liu, Tsunyen Wu, Ying-Ju Chen, Kathy Yan – Taiwan Semiconductor Manufacturing Company, Ltd.

16. Controlling the Reaction Pathway to Tune Packaging Epoxy Properties
Polette Centellas, Ran Tao, Andrew Korovich, Alexander Landauer, Amanda Forster, Huong Giang Nguyen, Jan Obrzut, Christopher Soles – National Institute of Standards and Technology; Siena Iavarone-Garza – University of Maryland; Dante Ribeiro – Pennsylvania State University; Stian Romberg – University of Tennessee

17. Influence of Pad Surface Finish on Electromigration of High-Reliability SAC-Based Hybrid BGA Solder Joints
Karthik Arun Deo, Junbo Yang, Yangyang Lai, Dalei Yang, Kewei Shou, Weichen Zhao, Yi Deng, Yuhan Gao, Pengcheng Yin, Seungbae Park – Binghamton University

18. Demonstration of Two-Phase Jet Impingement Cooling with Phase Separation Membrane on High-Power NVIDIA V100 GPU
Yunchun Yang, Tiwei Wei – University of California, Los Angeles; Sidharth Rajeev, Harish Kumar Lattupalli, Srikanth Rangarajan – Binghamton University; Ketan Yogi – Purdue University; Bahgat Sammakia – State University of New York at Binghamton

19. Enhancing In-Package Thermal Management of 3D V-NAND Flash Memory Using Under-Periphery Thermal Pins (UPTPs) and Materials-and-Structure Co-Design
Eun Pyo Hong, Jungsu Yoon, Ho Beom Han, Sang Won Yoon – Seoul National University; Suk-Kang Sung – Samsung Electronics Co., Ltd.

20. Comprehensive Transient Thermal Analysis of Laser Assisted Bonding (LAB) Process
Boyu Huang, Lev Tseng, Meng-Hsueh Yang, Wei-Cheng Huang, Tien-Chiang Lu – Advanced Semiconductor Engineering, Inc.; Hui Chung Liu – Advanced Semiconductor Engineering, Inc. (US)

21. Reliability Characteristics of Through Glass Vias with Polymer Liners
Meghna Narayanan, Mark Losego, Mohan Kathaperumal – Georgia Institute of Technology; Loic Constantin, Marvin Brent, Poulomi Mukherjee, Sarah Wozny – Applied Materials, Inc.

22. A Thermodynamic Continuum Framework for Electromagnetic–Mechanical Dissipation in Superconducting Qubit Systems
Sung-Hyun Oh, Jin-Woong Cha – Korea Research Institute of Standards and Science; Yonuk Chong, Eun-Ho Lee – Sungkyunkwan University

23. Experimental and Simulation-Based Assessment of Die Attach and Solder Mask Material Influence on Substrate Trace Cracking in BGA Packages
Stephen Lee, Tu-Anh Tran, Jasmine Lim, Ryan Zhang, Sharan Kishore, Abdullah Fahim, Jetse De Witte, HY Liu – NXP Semiconductor, Inc.; Hannah Samsol Bahri – NXP Semiconductor Malaysia

24. Impact of Microstructure and Current Management on Electromigration Reliability in BGA Solder Joints for High-Performance Computing
Tengfei Jiang, Andrea Molina Moreno, Miftahul Nabila, Kaitlyn Munoz, Junyoung Bang – University of Central Florida; Peng Su, Omar Ahmed – Hewlett Packard Enterprise; Valery Kugel, Bernard Glasauer, Leif Hutchinson – Juniper Networks; Nicholas Rudawski – University of Florida

25. Multiphysics Phase-Field Modeling of IMC Evolution and Reliability in Cu/Sn, Cu/In, and Cu/Co Fine-Pitch Interconnects
Haohan Guo, Shubhra Bansal – Purdue University

26. Assembly and Reliability Characterization of Glass-Cored Substrate Package for AI/HPC Applications
JoonYoung Choi, YoungJoo Choi – STATSChipPAC Korea; Nokibul Islam – STATS ChipPAC, Ltd.

27. Rapid Prediction of Orthotropic Elastic Properties for 2.5D Chiplet Packaging RDL
Dingjie Lu, Jun Liu, Wenzu Zhang, Richard Xian-Ke Gao, En-Xiao Liu, Sridhar Narayanaswamy – Institute of High Performance Computing A*STAR; Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR

28. Fluxless Vacuum Formic Acid Reflow of Indium Solder Thermal Interface Materials in Large Area BGA Packages
Kyle Aserian, Ryan Mayberry, Andy Mackie – Indium Corporation; Fred Tarazi, Xike Zhao, Phil Lehrer, David Heller – Heller Industries

29. Effect of Bi Concentration on the Creep Behavior and Reliability of Mixed SAC-LTS Solder Joints
Souvik Chakraborty, Mahbub Alam Maruf, Golam Rakib Mazumder, Jeffrey Suhling, Pradeep Lall – Auburn University

30. Modeling and Simulation of Se-Wa-Re Failure in Glass Core Substrates
Eduardo Barros De Moraes, Stanislav Sikulskyi, Robert Schaut – Corning, Inc.

Session 38: Interactive Presentations Photonics, mmWave Applications, and Emerging Technologies

Committee: Interactive Presentations

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1. Heterogeneous Integration of Compound Infrared FPAs and Silicon ROICs Through 15μm-Pitch Bonding
Ga-Eun Lee, Jiho Joo, Kwang-Seong Choi, Young-Sung Eom, Gwang-Mun Choi, Jungho Shin, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh – Electronics and Telecommunications Research Institute; Sang Jun Lee, Dayoung Kim – Korea Research Institute of Standards and Science; Jungwon Yoon – IRSpectra Co., Ltd.

2. Segment-Based Impedance Optimization of Vertical Transition Regions in Package for 112Gbps SERDES IF
Jiyoung Park, Hyunwoong Kim, Seungki Nam, Sungwook Moon – Samsung Electronics Co., Ltd.

3. Design and Optimization of 2mm Staggered RDL Interposer Channels for UCIe 3.0 up to 64GT/s
Hong Seok Kim, Youngeun Na, Yeon Ji Shin, Soo Jeong Kim, Jae-Sung Lim, Sang Yeul Yeum, Jayden Donghyun Kim – HANA Micron, Inc.; Woojin Lee – Swevenz Inc.

4. System-Level Framework for Co-Optimizing Electromigration and Voltage Drop in High-Power Packages
Jungil Son, Sungwook Moon, Seungki Nam – Samsung Electronics Co., Ltd.

5. A Fully Printed Electrochemical DNA Sensor with 3D Printed Microfluidics for SoP Lab-on-Chip Applications
Theodore Callis, Manos M. Tentzeris – Georgia Institute of Technology

6. Damascene Fine Pitch RDL Process Development of 1.0μm CD for Line/Space using High-NA i-Line Scanner
Lili Wang, Natalie Roels, Carine Gerets, Denis Dochain, Nancy Heylen, Murat Pak – imec; Kosuke Yamashita – Fujifilm Electronic Materials Europe; Kazuki Tomota, Tomoki Matsuda – Fujifilm Business Innovation Corp.

7. PALTO: Physics-Informed Active Learning for Tri-Gate FinFET Design Optimization for Vertical Power Delivery
Ayoub Sadeghi, Leonid Popryho, Inna Partin-Vaisband – University of Illinois

8. Low Loss Polymer Waveguides Based Architecture for Co-packaged Optics
Aparnaa Iyer, Sai Saravanan Ambi Venkataramanan, Janagama Goud, Mohan Kathaperumal, C. P. Wong, Muhannad Bakir – Georgia Institute of Technology; Yusuke Uraoka, Maki Tanaka, Atsushi Yamaguchi, Hirotaka Akiyama – Panasonic Industry Co., Ltd.; Tomo Mugurma, Tom Shin – Panasonic Industrial Devices Sales Company of America

9. Laser Assisted Transfer (LAT) of Coupon of InP Epitaxial Layer for Silicon Photonics devices.
Takenori Fujiwara, Daichi Miyazaki, Yukari Jo, Jumpei Jumpei Oniki – Toray Industries, Inc.; Peter O'Brien, James O'Callaghan – Tyndall National Institute; Yoshiaki Arai, Tstsuya Okada, Haruka Fujishige, Takumi Ikehara – Toray Engineering Co., Ltd.

10. Real-Time Lock-in Thermography and X-Ray CT for Early Failure Detection in Large-Size Packages
Yuji Inui, Sojiro Isomura, Nao Matsuo, Motoo Aoyama, Masaki Takahashi, Dongchul Kang, Sadaaki Katoh – Resonac Corporation

11. 3D-Printed Coaxial-Fed Patch Antenna-Embedded Substrates for 5G Antenna-In-Package Applications
Kyungsun Kim, Nahyeon Kim, Yongwoo Lee, Haksoon Jung, Jimin Kwon – Ulsan National Institute of Science & Technology

12. High-Bandwidth UCIe 2.0 Routing on Fine-Line Organic RDL with Enhanced Signal and Power Integrity for Scalable 64Bit Multi-Chiplet Integration
Amit Kumar, Jitesh Shah, Nandakumar Ravi – Renesas Electronics Corporation

13. Ultra-High Optical Power ELSFP Modules for CPO SiPh-Based Transceivers
Tetsuya Matsuyama, Kohei Umeta, Yuki Shiroishi, Taketsugu Sawamura, Hideyuki Nasu – Furukawa Electric Co., Ltd.

14. Integrated IR-Drop Analysis Framework for PDNs in 3D Stacked Dies
Taehoon Kim – Samsung Electronics Co., Ltd.; Seungmin Woo, Madison Manley, Muhannad Bakir – Georgia Institute of Technology

15. Monolithic Passive Low-Loss Fiber Coupling to Photonic Glass Core Substrates Using Ion-Exchanged Waveguides and SLE-Fabricated V-Grooves
Maurice Haffner, Julian Schwietering, Ulrike Gasnesh – Fraunhofer IZM; Tom Chojne, Hashem Al-Shami – Technical University Berlin

16. Electrical Design Guidance of Chiplet Interface Channels to Achieve 2634GB/s/mm Die Edge Bandwidth
Jiwoon Moon, Jonghyeon Lee, Yuchul Jung, Youngwoo Kim – Sejong University

17. Multi-Channel and Multi-Scale Optical Analysis Toward a Glass Coupler Based Detachable Edge Coupling Connector for CPO
Zhichao Zhang, Dekang Chen, Yalong Gu, Fan Fan, Nicholas Psaila, Kumar Abhishek Singh, Rahul Jain, Ravi Mahajan, Kemal Aygun – Intel Corporation

18. Interface Enhancement Method for Silver-Sintered Flexible Strain Sensors Toward Improved Reliability and Sensitivity
Pan Liu, Xinyue Wang, Letao Bian, Jiayu Ge – Fudan University; G. Q. (Kouchi) Zhang – Delft University of Technology

19. Multi-Agent Reinforcement Learning Driven Package PDN Design Automation
Haran Manoharan, Chulsoon Hwang – Missouri University of Science and Technology

20. Inverse Design for Ion-Exchanged Waveguides in Photonic Glass Core Substrates
Tom Chojne – Technical University Berlin; Victor Doroshenko, Boris Bergues, Marc Schartmann – OmegaLambdaTec; Maurice Haffner, Julian Schwietering, Ulrike Gasnesh – Fraunhofer IZM

21. 2.5D and Vertical Integration for Real-time Co-Optimization of Voltage Regulation and Power Gating in HPC Systems
Salma Abdelzaher, Inna Partin-Vaisband – University of Illinois

22. A Metrology Development Platform for Digital Image Correlation-Based Measurement of Thermal Expansion and Cure Shrinkage in Epoxies
Alexander Landauer – National Institute of Standards and Technology

23. 3D Heterogenous Integration Packaging of 5G RF Systems Using Additive Electronics
Waleed Alshaibani, Abdullah Obeidat, Riadh Al-Haidari, Zhi Dou, Sara Lieberman, Shiwantha Gunathilake, Yoga Vyas Viswanathan, Stephen Gonya, Mark Poliks – Binghamton University; Jason Case, Joseph Iannotti, Felippe Pavinatto – GE Aerospace Research

24. Optical Multi-Die Interconnect Bridge (OMIB) Interposer Demonstration to Enable High-density Photonic Interconnects for HPC Applications
Suresh Pothukuchi, Ankur Aggarwal, Digvijay Raorane, Lakshmi Kari, Jelena Pesic – Celestial AI

25. High-Density 2D Fiber Interface for Integration into 3D Packaging
Rebecca Schaevitz, Qijun Xiao – Mixx Technologies; Vivek Raghuraman – Broadcom, Inc.

26. Additively Manufactured Interdigitated Capacitors for High Temperature Applications
Erik Busse, Abdullah Obeidat, Mousa Al-Zanina, Stephen Gonya, Mark Poliks, Emuobosan Enakerakpo, Waleed Alshaibani – Binghamton University; Matthew Erdtmann, Adrian Pyke – Micro-Precision Technologies, Inc.

27. A Switchable Longitudinal and Shear BLS Microscope for Comprehensive Modulus Imaging of Semiconductor Packaging Materials
Andrew Gayle, Ran Tao, Andrew Korovich, Polette Centellas, Christopher Soles, Chris Michaels – National Institute of Standards and Technology; Sebastian Engmann – Theiss Research

28. Ultra High Resolution Micro-LED Display Enablement at 300mm Using W2W Hybrid Bonding for AI and AR Applications
Raghav Sreenivasan, Sangwoo Lim, Jason Appell – Applied Materials, Inc.; Gernot Probst – EV Group; Abhishek Bhat – Mojo Vision

29. Low-Temperature Ultrathin Al_2O_3–SiO_2 Direct Bonding: Development and Optimization for Heterogeneous Integration of All-Optical Neuromorphic Chips
Albert Anthony, BG Sajay, Ser Choong Chong, Leong Ching Wai – Institute of Microelectronics A*STAR

30. Piezo-Magnetostrictive Transducer-Powered Wireless Implanted Sensors for Monitoring Hemodynamics
Veeru Jaiswal, Reshmi Banerjee, Ghaleb Al-Duhni, Mohammad Mohtasim Pial, Okeoma Arinze, Angelique Dominguez, Geraldine Pineda Andrade, Markondeya Raj Pulugurtha – Florida International University

31. High-Efficiency 2 by 1 Antipodal Vivaldi Array on Ultra-thin PTFE for sub-6 GHz 5G: Cricut-Based Rapid Prototyping and Measured Beam Steering
Mohamad El Yassine, Mutaz Shannag, Amanpreet Kaur – Oakland University

32. Modeling and Optimization of 2-Stage Power Delivery Systems for High-Performance, Large-Area Packages
Jin Woong Kwak, Juyeop Baek, Muhannad Bakir, Visvesh Sathe – Georgia Institute of Technology

33. BEM-Based Characterization of a D-Band On-Chip Patch Antenna Array
Jonatan Aronsson – CEMWorks, Inc.; Hans Schreckenbach – CEMWorks; Iaroslav Shilinkov, Rob Maaskant – Chalmers University of Technology

34. A Design-Space Exploration of Active Interposer Architectures for Long-Reach Signaling in Large-Area Advanced Packages
Taesoo Kim, Seungmin Woo, Muhannad Bakir – Georgia Institute of Technology; Srujan Penta – Georgia Institute of Technology/Marvell

35. Language-Model Interfaces for SerDes Design Optimization: Comparing Prompt-Based and Agentic Approaches
Nirjhor Rouf, Fin Amin, Sounak Dutta, Paul Franzon – North Carolina State University; Priyank Kashyap, Chris Cheng – Hewlett Packard Enterprise

36. Channel-Adaptive Generative Learning for Diverse Equalizer Design Space Exploration in High-Speed Links
Junghyun Lee, Hyunjun An, Jiwon Yoon, Haeseok Suh, Junho Park, Youngsu Yoon, Byeongmok Kim, Jaegeun Bae, Eunji Seo, Inyoung Choi, Hyunseo Uhm, Joungho Kim – Korea Advanced Institute of Science and Technology

Session 39: Interactive Presentations Bonding Processes and Analysis in Next Generation Interconnects

Committee: Interactive Presentations

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Synopsys, Inc.
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1. Trace-Element Effects in SAC Alloys: Mitigating HIP Defects in 5G/Automotive SoC SMT Assemblies
Tai-Yin Lin, Chien-Min Lin, Zhe-Cheng Xu, Che-Kuan Chu – Advanced Semiconductor Engineering, Inc. (US); Fa-Chuan Chen, Bo-Kuan Yeh, Hsin-Long Chen – MediaTek, Inc.

2. Electromigration Resistance of Fine-Pitch Copper Lines: Comparison of Fine-Grained, Nanotwinned, and Standard Cu Lines
Wei-Lan Chiu, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo, Shih-Chieh Chang – Industrial Technology Research Institute; Tao-Chi Liu, Yun-Yu Chen,, Elie Najjar – MacDermid Alpha

3. Design of UCIe-A x64 Chiplets Integration for 16-36GT/s Using Organic Interposer
Sheng-Fan Yang, Liang-Kai Chen, Wei-Chiao Wang – Global Unichip Corporation

4. Unit Level Die-to-Die Attach with Low Thermal Input TCB for Co-Packaged Optics Applications
Liban Jibril, Anita Dey, Jesus Nieto Pescador, Sungmin Han, Madhu Krishna Murthy, Niranjan Parab, Anurag Tripathi, Timothy Gosselin, Shan Zhong – Intel Corporation

5. Novel Microbump Structure of Direct Solder Bumping on Seed Layer with Barrier Functionality (SoSBF)
Yusuke Tanaka, Keiichiro Hattori, Yuji Ohba, Aya Kurokawa, Toshiki Furutani, Takashi Kariya – Samsung (Japan)

6. Fine-Pitch Cu/Polymer Hybrid Bonding Using Excimer Laser Damascene Process
Rikuo Kajiwara, Taichi Mikami, Yuzo Nakamura, Yutaka Hisamune, Satoshi Inada – Mitsui Chemicals, Inc.

7. High-Density RDL Scaling Using Digital Lithography Technology
Peng Suo, Chi-Ming Tsai, CC Chuang, YingChiao Wang, Jingxuan Wang, Guan Huei See, Arvind Sundarrajan, Jang Fung Chen, Shin-Puu Jeng, Frederick Lnu – Applied Materials, Inc.

8. Simultaneous Surface Reduction and Self-Passivation via Ar-CH_4 Plasma for Cu Hybrid Bonding
Hoogwan Lee, Byeongchan Go, Sarah Kim – Seoul National University of Science and Technology

9. Influences of Bonding Misalignment on Copper Bulge Out in Wafer-to-Wafer Hybrid Bonding
Ryohei Kojima, Yuriko Yamano, Kengo Kotoo, Naoki Komai, Suguru Saito, Yoshiya Hagimoto – Sony Semiconductor Solutions

10. Laser-Assisted Bonding with h-BN Filled Non-Conductive Film for Fine-Pitch Semiconductor Packaging
Seong Cheol Kim, Jiho Joo, Young-Sung Eom, Jungho Shin, Jin-Hyuk Oh, Ki-Seok Jang, Chanmi Lee, Gwang-Mun Choi, Ga-Eun Lee, Mi-Ri Yoon, Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Seung-Yoon Lee – Hanbat National University

11. Overcoming Extreme Warpage: A Study on Ultra-Large 2.xD Molded Interposer Bonding Process
Minseog Myung, Yanggyoo Jung, Seungjae Lee, Sangyong Park, Jaeho Han, Juhong Shin, Byeongjin Lee, Daewoo Kim – Samsung Electronics Co., Ltd.

12. Glass Substrate Bonding via Dry Processing and Inorganic Layers for Heterogeneous Integration
Kuan Chung Fu, Jun-Nan Liu, Ying Li Chen, Chih Huang Lai – National Tsing Hua University; Shih-Lian Cheng, Jin-Sheng Wang – Unimicron Technology Corp.

13. Methodology for Fine Line Strength in Fan-Out Architectures
Yung-Sheng Lin, Min-Yan Tsai, Ting Chun Lin, Chung-Hung Lai, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

14. Contamination-Controlled Pre-Assembly for High-Density Die-to-Wafer Hybrid Bonding
Fabiana Tanaka, Marie Sano, Kenta Hayama, Fumihiro Inoue – Yokohama National University; Jun Maeda, Tomoko Iwatsubo – LINTEC Corporation; Takashi Ouchi, Tsuyoshi Nakayama – JX Metals Trading Co., Ltd.; Shinji Ishitani, Naoya Hirota – Panasonic

15. Hierarchical 3D-Vertically Multi-Layers Stacking by Transferable Cu/Polymer Hybrid Bonding
Ou-Hsiang Lee, Wei-Lan Chiu, Hsiang-Hung Chang, Chia-Wen Chiang, Yu-Ping Chan, Chin-Hung Wang, Wei-Chung Lo, Shih-Chieh Chang, Meng-Hsuan Chen – Industrial Technology Research Institute; Chia-Hsin Lee, Chung-An Tan – Brewer Science, Inc.; Kuan-Neng Chen – National Yang Ming Chiao Tung University

16. Integration and Characterization of Two Connection Schemes for Backside Power Delivery Network
Peng Zhao – Interuniversity Microelectronics Centre; Liesbeth Witters, Michele Stucchi, Vladimir Cherman, Melina Lofrano, Rami Chukka, Kevin Vandersmissen, Joeri De Vos, Gerald Beyer, Zsolt Tokei, Eric Beyne – imec; Jan Willem Maes – ASM

17. Proposal of a Novel Design Method for Inter-Channel Crosstalk in High-Density Optical Interconnects Toward Massively Parallel Co-Packaged Optics
Ryosuke Matsumoto, Yuki Atsumi, Takayuki Kurosu, Fumi Nakamura, Siim Heinsalu, Akihiro Noriki, Satoshi Suda, Takeru Amano – National Institute of Advanced Industrial Science and Technology

18. Bumpless Flip-Chip (BFC) as a Next-Generation Interconnect Technology for the AI Era
Rabindra Das, Daniel Oates, Alex Wynn, David Kim, Ravi Rastogi, Neel Parmar, Leonard Johnson, Steven Weber, Mollie Schwartz – MIT Lincoln Laboratory

19. Thermally Functional Self-Activated Bonding for EUV-Compatible Backside Integration
Hayato Kitagawa, Taisuke Yamamoto, Fumihiro Inoue – Yokohama National University; Jenyu Lee, Shuntaro Machida, Kazuhiro Yuasa – KOKUSAI ELECTRIC; Shunsuke Teranishi – DISCO Corporation; Joichi Nishimura – SCREEN Holdings Co., Ltd.

20. Electrodeposition of Aluminum on Direct Bonded Copper Substrates for Power Module Packaging
Thi Minh Anh Dao, Phuong Thao Hoang, Chun-Hao Chen – National Yang Ming Chiao Tung University; Ming-Si Jian, Peng-Wei Chu – National Tsing Hua University

Interactive Presentations: Thursday, May 28, 10:00 a.m. - 12:00 Noon and 2:30 p.m. - 4:30 p.m.

21. Direct Transfer Bonding of Ultra-Thin Warped Chips for Advanced Heterogeneous 3DIC Integration with Fine-Pitch Direct/Hybrid Bonding
Ichiro Sano – TAZMO Co., Ltd.; Shinya Takyu, Tomoka Kirihata – LINTEC Corporation; Takafumi Fukushima – Tohoku University; Jun Kaneyasu – Tazmo, Inc.; Yoichiro Kurita – Institute of Science Tokyo

22. Through-Glass Via and Substrate Recess Technologies: Enabling Embedded Devices and Co-Packaged Optics in Advanced Glass Packaging
Nils Anspach, Daniel Dunker, Roman Ostholt – LPKF Laser & Electronics SE; Andreas Ostmann, Julian Schwietering – Fraunhofer IZM; Christian Buchner – SCHMID Group

23. Reliable and Cost-Effective Fabrication of Low-Resistive and Void-Free Through-Glass Vias Using a Reduction Gas-Generating Sinterable Cu Paste
Murugesan Mariappan, Hiroyuki Hashimoto, Takafumi Fukushima – Tohoku University; Kiyoharu Mori, Harumi Hosogoe – T-Micro; Hirokatsu Sakamoto, Akihiko Happoya – Daicel Corporation

24. Transient Additive Manufactured Packaging for SoP RF Modules in Harsh Environments Using Biodegradable Materials with Customizable Decomposition Rates
Denitsa Dimitrova, Manos M. Tentzeris – Georgia Institute of Technology

25. Impact of Copper Density on >Via-to-Via Hybrid Bonding: Morphological and Electrical Characterizations
Agathe Lerat, Christophe Dubarry, Pablo Renaud, Margot Faure, Floriane Baudin, Hadi Hijazi, Sebastien Dominguez, Frank Fournel – CEA-LETI

26. A Low-Cost 2.5D Photonic Silicon Interposer Assembly Process for HPC Applications
Digvijay Raorane, Ankur Aggarwal, Suresh Pothukuchi, Sagar Dubey, Dan Oh, Jelena Pesic – Celestial AI

27. Exploring Cu-Cu Hybrid Bonding Failure Mechanisms Under Current Stress via 3D Focused Ion Beam Tomography
Sari Al Zerey – State University of New York at Binghamton; Junghyun Cho – Binghamton University; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research

28. An Evaluation of Hybrid Bonding of Cu/SiO2 Using Vacuum Ultraviolet Light Under Redox Gases
Shinichi Endo, Kejun Wu, Kengo Nishio, Akihiro Shimizu – Ushio, Inc.

29. Novel O_2/H_2 Plasma Treatment for Cu Oxide Removal and Dielectric Activation in Hybrid Bonding
Kazutaka Noda – Tokyo Electron, Ltd.; Atsushi Nagata, Norifumi Kohama, Yoshihiro Kondo – Tokyo Electron Kyushu, Ltd.; Christopher Netzband, Andrew Tuchman, Sunny Ilseok Son – TEL Technology Center, America, LLC

30. Fine-Pitch Thermally Resistive Superconducting 3D Interconnects for Quantum Systems
Pablo Renaud, Candice Thomas, Meriem Guergour, Charles Bon-Mardion, Hadi Hijazi, Laurent Truong, Richard Souil, François Aussenac, Jean Charbonnier – CEA-LETI; Nathan Portatiu-Cambusset – University of Technology of Troyes; Edouard Deschaseaux – CEA-LETI/Grenoble Alps University

31. Comprehensive Characterization of Surface Activation for Chip-to-Wafer Hybrid Bonding in 3D Flash Memory Application
Jingqi Zhang, Bungo Tanaka, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University

32. High-Throughput Metrology of CMP-Treated Surface Topography Using Fizeau Interferometry for Hybrid Bonding
Ryoichi Sato, Hiroyuki Hashimoto, Bungo Tanaka, Kota Sasaki, Murugesan Mariappan, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Kohei Nishiyama, Yuki Fujii – Kobe Steel

33. Interfacial Analysis of Hybrid Bonding Using Water Surface Tension-Driven Self-Assembly for HBM
Kota Sasaki, Bungo Tanaka, Ryoichi Sato, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Hiroshi Kikuchi, Hayato Hishinuma – Yamaha Robotics Co., Ltd.

34. Advanced Metrology for Heterogeneous Chiplet Integration with 100% (Chip-to-Wafer Bond) Overlay Control at High Speed with Four Parameter Modeling
Tan Nguyen, Bhaskar Jyoti Krishnatreya, Siyan Dong – Intel Corporation; Frank Boegelsack, Elisabeth Brandl, Thomas Uhrmann – EV Group

35. Understanding Scaling and Temperature Limits in Cu Bulge-Out Mechanism for Hybrid Wafer-to-Wafer Bonding
Jo De Messemaeker, Boyao Zhang, Aleksandar Radisic, Zaid El-Mekki, Sven Dewilde, Stefaan Van Huylenbroeck, Koen Van Sever, Herbert Struyf, Joeri De Vos, Gerald Beyer, Eric Beyne, Zsolt Tokei – imec

36. Die-Shift of Sub-20µm Thickness Embedded Die in Glass-Core Package Redistribution Layers
Hyunggyu Park, Jaewon Lee, Muhannad Bakir – Georgia Institute of Technology

37. Implanted Nanotwin Boundaries Enable Stable Hybrid-Bondable Copper Metallization
Abdelhamid El-Sawy, Pingping Ye, Jianwen Han, Stephan Braye, Harhsul Khanna, David Doughty, Veronica Lambert, Adam Letize, Kyle Whitten, Thomas Richardson, Elie Najjar – MacDermid Alpha

38. A Compact Optical Engine With Novel 2D Thin Film µ-VCSEL Array Architecture for CPO and LPO Application at 3.2Tbps
Murphy Lee, Yuk-Tong Cheng, Jr-Hau He, Tzu-Hung Lin, Wang Shi Yu – Rayleigh Vision Intelligence

39. High-Speed LVDS Twisted Pair Transmission Across PCB and Chiplet RDL Interfaces
Mayukh Nandy, James Doyle, Siyang Liu, Hongbin Yu – Arizona State University

Session 40: Interactive Presentations Materials, Manufacturing, and Assembly Techniques in Advanced Packaging Solutions

Committee: Interactive Presentations

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1. Heterogeneous Integration on Thin Glass Substrates for RF Applications Using Aerosol Jet Printing
Ethan Kepros, Bhargav Avireni, Premjeet Chahal – Michigan State University

2. Low-Temperature Sintering and Bonding Performance of Gradient Oxidized Copper Nanoparticles
Tetsu Yonezawa, Hiroki Tsukamoto – Hokkaido University

3. Reliability Assessment of Liquid Metal Alloy TIMs in Fan-Out Embedded Bridge Packages
Wen-Yu Teng, Jyun-De Jhan, Don Son Jiang, Andrew Kang, Dai-Fei Li, Shane Lin, Yung-Ta Lin – Siliconware Precision Industries Co., Ltd.

4. Comparative Study of Electroless Noble Metal Layers for Low-Temperature Hybrid Bonding
Byeongchan Go, Hoogwan Lee, Sarah Kim – Seoul National University of Science and Technology

5. Metal–Polymer Hybrid Bonding for Contamination Mitigation in Polymer-Based Semiconductor Packaging
Dong Yun Sung, Seul Ki Hong, Seoyeon Choi, Jiyun Lee – Seoul National University of Science and Technology

6. Challenges and Solutions for Package-Level Encapsulation of Ultra-Large Die Complexes
Yang Guo, Ziyin Lin, John Decker, Eylul Simsek, James Breyfogle, Hsin-yu Li, Yiqun Bai, Chengzi Huang, Wen Yang – Intel Corporation

7. Evaluating Large Body Packaging Performance of Glass Core Substrates for AI and HPC Applications
Jongmin Park – Amkor Technology Korea

8. Current-Assisted Cu–Cu Bonding at Low Temperature: Process Window and Mechanism
Byungkwan Kwak, Jinmyeong Seo, Haneul Han, Sanghwa Yoon, Bongyoung Yoo – Hanyang University

9. Correlation of Copper Pattern Surface Morphology and Insertion Loss for High-Speed Communication
Yasutaka Amitani – MEC Co., Ltd

10. Microstructure for Zero Void by Control of Cu2+ in Metallization for TGV of Glass Core Substrate
Sung-Bin Kim, Jae-Hyung Kim, Myung-Jun Kim, Kyeong-Seop Park – AnyCasting Co., Ltd.; So-Yeon Lee – Inha University

11. Robust LCP Bonding for Medical Implants: Impact of Surface Roughness and Reactive Accelerated Aging
Ladan Jiracek-Sapieha, Ryan Wilkerson, Jack Judy – University of Florida

12. Study of Lithography Process Comparison for Co-Package Optics
Hironobu Fujishima, Koya Mita, Makoto Ogusu, Hiromi Suda, Ken-Ichiro Mori – Canon, Inc.

13. Collective Die-to-Wafer Bonding of Si Dies and 4 Inch Polycrystalline Diamond Wafer with Ultralow Thermal Boundary Resistance and High Bonding Quality
Shuchao Bao, Yi Zhong, Daquan Yu – Xiamen University; Ran He – Huawei Technologies Co., Ltd.

14. Overcoming BEOL Thermal Constraints via Low-Temperature Cu-Cu and Cu-Oxide Bonding of a-Ga2O3 UV-C Photodetectors
Jiyun Lee, Dong Yun Sung, Seoyeon Choi, Seul Ki Hong – Seoul National University of Science and Technology

15. Scalable Construction of 3D Graphene Frameworks via Combined Foaming and Freeze-Drying in High-Performance Epoxy Nanocomposites for Advanced Packaging
Zihao Lin, Jung Yi Chen, Kyoung-Sik (Jack) Moon, C. P. Wong – Georgia Institute of Technology

16. A Low Profile DC-DC Converter on the Inductor-Embedded-Substrate as an Integrated Package Solution (L-type-iPaS) Substrate
Nobuyoshi Adachi, Yoshimitsu Ushimi, Kenji Nishiyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.; Manabu Yano – Murata Electronics North America

17. A Novel Capacitor Embedded Substrate Based on Capacitor-Type Integrated Package Solution (iPaS) in Advanced Semiconductor Packaging
Akitomo Takahashi, Shuhei Yamada, Yuuki Yabuhara, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.; Manabu Yano – Murata Electronics North America

18. Technology for Sequential Integration of HPA and LNA on Stacked GaN Layers for 3D Packaging of Next Gen Miniaturized Power RF Transceiver Front Ends
Kai Zoschke, Hermann Oppermann – Fraunhofer IZM; Antonis Stavrinidis, Nikolaos Makris – Foundation for Research & Technology Hellas; Philomela Komninou, Nikoletta Florini – Aristotle University of Thessaloniki; Paolo Fioravanti, Errikos Lourandakis – Circuits Integrated Hellas; Bruno Heusdens, Adrien Hertay – Taipro Engineering; Mohamad Abo Ras – Nanotest; Afshin Ziaei – Thales Research & Technology

19. RADAR System-in-Package with Integrated Antennas Based on Fan-Out Wafer-Level Packaging RDL-First Integration
Arnaud Garnier, Laetitia Castagne, Rémi Franiatte, Daniel Mermin, Alexandre Siligaris, Mykhailo Zarudniev, Francesco Foglia Manzillo, Maciej Smierzchalski – Grenoble Alps University/CEA-LETI; Jean-Charles Souriau, Perceval Coudrain – CEA-LETI

20. Sub-Millimeter GaN-on-Si Dielet Fabrication in Advanced Packaging Substrates Using Femtosecond Laser for 3D Heterogeneous Integration Applications
Pradyot Yadav, Ulrich Rohde, Ruonan Han, Tomás Palacios – Massachusetts Institute of Technology; Xingchen Li, Danish Baig, Muhannad Bakir – Georgia Institute of Technology; Madhavan Swaminathan – Pennsylvania State University

21. Room-Temperature Reduction of Tungsten Oxide via Vacuum Ultraviolet Irradiation under Reducing Gases
Akihiro Shimizu, Shinichi Endo – Ushio, Inc.

22. High-Performance Low-Temperature PECVD SiCN Stacks for C2W and W2W Hybrid Bonding in Advanced 3D Integration
Guanyu Song, Chunhai Ji, Yuchen Hou, Hu Kang, Ming Li – Lam Research Corporation

23. Silicon Bridges for Chiplets Heterogeneous Integration with Microbump and Cu-Cu Hybrid Bonding
John H. Lau, Ning Liu, TJ Tseng – Unimicron Technology Corp.

24. Enhanced Bonding Strength via Single-Wafer Annealing with Reduced Thermal Budget
Masha Gorchichko, Shashank Sharma, Jacob Yagura, Yoocharn Jeon, Vijay Sukumaran, Evan Iler, Raghav Sreenivasan, Siddarth Krishnan, Michael Chudzik – Applied Materials, Inc.

25. Assembly Process Development for Ultra-Large 88x52mm² Size Fan-Out Interposer with Bridge Chips to Integrate Multi-HPC, HBM, and Photonic OE Chiplets
Sharon Pei Siang Lim, Lai Yee Chia, Pan Manyi, Hipona Randy Tupaen, Ignatius Lim, Mohamed Zakir Hussain Mohamed Ishak, Jerald Soh, Sandra San, Yong Liang Ye, Chai Tai Chong – Institute of Microelectronics A*STAR

26. Fine Pitch and Ultra Low Profile Double-Side Molded LGA Solution
Ming-Hung Chen, Yu-Chang Chen, Ying-Hung Lin, Yung-Li Lu, Gavin Kao, Yung-I Yeh – Advanced Semiconductor Engineering, Inc.

27. Thermo-Pressing Treatment to Enhance Conductivity of Printed Carbon on Flexible Substrates
Babatunde Falola, Riadh Al-Haidari, Olya Noruz Shamsian, Shiwantha Gunathilake, Mark Poliks – Binghamton University

28. Integration of Novel PE-CVD Film as Inter-Die-Gap-Fill (IDGF) and Advanced Thermal Interface Materials (TIM) for Next Generation 3DICs
Vijay Sukumaran, Siddarth Krishnan, Raghav Sreenivasan, Michel Khoury, Yoocharn Jeon, Michael Chudzik, Sean Seutter, Jeremiah Hebding, Ying Trickett, Jinho An, Guan Huei See, Prayudi Lianto – Applied Materials, Inc.

29. Evaluation of Electroless-Plated Copper Circuits on Polyethylene Terephthalate (PET) for Roll-to-Roll Manufacturing of Flexible Hybrid Electronics
Zhi Dou, Riadh Al-Haidari, Mark Schadt, Mark Poliks – Binghamton University; James Honan, Thomas LeBlanc, Emily Rej, Carolyn Ellinger – Eastman Kodak Company; Fabian Schnegg – Nextflex

30. Temperature-Dependent Electrical Characterization of New ABF Type A Material up to 220GHz
Mahin Ahamed, Madhavan Swaminathan – Pennsylvania State University; Lakshmi Narasimha Vijay Kumar – Georgia Institute of Technology; Habib Hichri, Takashi Yamanaka, Yuko Shibata – Ajinomoto Fine-Techno USA; Yoshio Nishimura – Ajinomoto Co., Inc.

31. Modular 3D Heterogeneous Integration with Stacked-Via 3D Stitch-Chips (SV-3DSC)
Shane Oh, Zhonghao Zhang, Paul Jo, Muhannad Bakir – Georgia Institute of Technology

32. 60GHz mmWave Radar in Compact Fan-In Wafer-Level Chip Scale Package (FI-WCSP) Technology
Aditya Jogalekar, Mohammad Vatankhah Varnoosfaderani, Marc Dewilde, Karan Bhatia, Tim Davis, Sangamesh Anandwade, Sunhwan Jang, Arnab Das, Vivek Sridharan, Krishnanshu Dandu, Venkatesh Srinivasan – Texas Instruments, Inc.

Session 41: Student Interactive Presentations

Committee: Interactive Presentations

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1. Organics-Free Porous Nano-Dendritic Cu Films for High-Power Packaging Interconnects
Fatin Battal, Jeroen Maasen, Peter Mulder, Elias Vlieg, John Schermer – Radboud University; Nikhil Gupta – Delft University of Technology; Ruben Pranger – Netherlands Organization for Applied Scientific Research (TNO); Rene Poelma – Nexperia

2. Ground Resonance Suppression on 212.5-Gbps OSFP with FEM and Mixed-Mode dPBTL Circuit
Kewei Song, Shixuan Yuan, Yulin He, Milton Feng – University of Illinois; Joseph Wang – Foxconn Interconnect Technology

3. Study of Moisture Analysis Technology Based on Fan-Out Package
Yang Yang, Meiying Su, Rui Ma, Hualong Fu, Anqi Zhou, Jun Li, Jingyi Zhao, Yunyan Zhou, Qidong Wang, Liqiang Cao – Chinese Academy of Science-Institute of Microelectronics

4. Location-Dependent Microstructure and Mechanical Properties Evolution of TGV-Cu via an EBSD–Nanoindentation Co-Localization Characterization
Junwei Chen, Chao Gu, Xuyang Yan, Jiajie Fan – Fudan University; Xiao Hu, G. Q. (Kouchi) Zhang – Delft University of Technology; Bin Yang, Chengqiang Cui – Guangdong Fozhixin Microelectronics Technology Research Co. Ltd

5. CMP-Free and Low-temperature Cu-PI Hybrid Bonding for Rapid Multi-Chip to Wafer Integration
Jinzhu Li, Wang Xinyao, Qicun Lou, Han Jiang, Xianlong Wang, Mingze Ban, Nanjiang Yuan, Hao Wang, Ziyu Liu – Fudan University; Yabin Sun – East China Normal University

6. Ultrasonic-Assist Thermocompression Al-PI Hybrid Bonding Applied for Chiplet Heterogeneous Bonding
Jinzhu Li, Mingze Ban, Qicun Lou, Wang Xinyao, Han Jiang, Xianlong Wang, Hao Wang, Ziyu Liu, Lin Chen, Qingqing Sun – Fudan University; Wenchao Wang – Jiashan Fudan Research Institute; Yabin Sun – East China Normal University

7. Robust Design of Hybrid Bonding Considering Cu Pad Inelastic Deformation for Reliability
Kim Sang Hoon, Eun-Ho Lee – Sungkyunkwan University; Yeoun-Soo Kim, Haeri Kim, Jong Han Shin – SK hynix Inc.; Jiho Kang – Absolics Inc.

8. Thermal Distribution Analysis of a 2.5D CPO Structure Integrated With a DFB Laser
Thu Huong Bui – National Taiwan University

9. Reliability Evaluation of Intense Pulsed Light Flip Chip Bonding with Various Surface Finishes
Hyeong-Bin Park, Young-Min Ju, Jong-Whi Park, Yun-Joong Kim, Hak-Sung Kim – Hanyang University

10. Enhancing SiO_2 Bond Strength for Cu/SiO_2 Hybrid Bonding via H_2O-Assisted Plasma Treatment
Gyeongyeol Lee, Youngjoon Cha, An Nguyen, Rino Choi – Inha University

11. A Co-Optimization Method for IVR and PDN in Embedded Vertical Power Delivery Substrate
Lihao Ou, Xiangan You, Fang Yang, Zhidan Fang, Yunyan Zhou, Shanjun Ding, Fengze Hou – Chinese Academy of Science-Institute of Microelectronics

12. Low Temperature and Low Pressure Fine-Pitch Cu-Cu Bonding by Electroplated In-Sn-Passivation
Yu-Hsiang Lu, Po-Shao Shih, Wei Choong Lee, Cheng-Yan Yang, C. Robert Kao – National Taiwan University; Yun-Ching Hung, Yung-Sheng Lin, Chen-Chao Wang, Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.

13. A Compact 10GHz Marchand Balun on Glass Using TGV-Based Integrated Passive Devices
Seokyoung Hwang, Sojeong Kim, Gangtae Jin, Young-Joon Kim – Gachon University; Jongmin Yook, Jein Yu – Korea Electronics Technology Institute

14. Next-Generation Scanning Electron Microscope for Advanced Packaging: Coating-Free, Ambient, and Ready-to-Use
Weichen Zhao, Junbo Yang, Yuhan Gao, Dalei Yang, Kewei Shou, Yi Deng, Karthik Arun Deo, Stephen Cain, Seungbae Park – Binghamton University; Donghwa Kwak, Young-Eun Kwon, Junhee Lee – Coxem Co., Ltd.

15. High-Fidelity Reliability Prediction of SAC Solder Under Drop Impact via High Strain Rate and Temperature-Dependent Properties
Dong-Hoon Yoo, You-Gwon Kim, Semin Lee, Hak-Sung Kim – Hanyang University; Jin-Young Bang, Jong-Bum Lee – Samsung Electronics Co., Ltd.

16. 3D Interconnection Using TGVs on Glass Interposer for Vertical 32Gbps High-Speed Transmission
Suin Chae, Jein Yu – Korea Electronics Technology Institute; Jaemyung Lim – Hanyang University

17. Reliability Prediction of Automotive SiC MOSFET Packages Based on Degradation of EMC Viscoelasticity and Interfacial Strength
Semin Lee, Sejun Park, Heeju Han, Hongyun So, Hak-Sung Kim – Hanyang University; Hyun-Woo Jung, Kyung-Woo Lee, Dae-Un Sung – Hyundai Motor Company

18. Towards High-Conductivity Aerosol Jet Printed Copper with Amine Surfactant
Cheng Zheng, Chee Lip Gan – Nanyang Technological University; Alfred Zinn – Kuprion, Inc.

19. Ultra-Low Coefficient of Thermal Expansion Spin-on Polymer for Deep Trench Gap-Filling for 3D-IC Heterogeneous Integration
Pin-Lin Chen, Chih Chen – National Yang Ming Chiao Tung University; Ya-Chien Chuang, Hsiao-Wei Yeh, Satoshi Fujimura – Tokyo Ohka Kogyo Co., Ltd.

20. Design and Signal Integrity Analysis of PCIe 5.0 SFF-8639 (U.2) Connector for AI Data Servers
Byeongmok Kim, Jihun Kim, Junho Park, Eunji Seo, Hyunseo Uhm, Youngsu Yoon, Jaegeun Bae, Jongho Kim, Jiwon Yoon – Korea Advanced Institute of Science and Technology

21. Novel CMP-Free Cu/Polymer Low Temperature Hybrid Bonding with Wide Process Window for Advanced Packaging and 3D Integration
Kai-Yu Chao, Mu-Ping Hsu, Yuan-Chiu Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Yen-An Chen – Feng Chia University; Chung-Hsiang Wang – Lam Research Corporation; Chee Ping Lee, Audrey Charles – Lam Research

22. Room-Temperature Au-Au Bonding of Rough-Surface Ceramics Smoothed by Au Thin Film Transfer and the Plastic Deformation of Intermediate Metal Layer
Shintaro Goto, Kai Takeuchi, Eiji Higurashi – Tohoku University

23. High-Resolution Nanoscale X-Ray Imaging for Non-Destructive Inspection of Copper Grains in Fine-Pitch Pads for Hybrid Bonding
Nimish Nazirkar, James Lu, Edwin Fohtung – Rensselaer Polytechnic Institute; Nicholas Polomoff, Roy Yu, Katsuyuki Sakuma – IBM Research; Dmitry Karpov – European Synchrotron Radiation Facility

24. Advanced Acoustic Emission (AE) Sensing and Analytics Scheme for In-Situ Warpage Characterizations of Flip-Chip Packaging
Yigit Turan, Xinchen Wang – Binghamton University; Sathya Raghavan – IBM Research; Zimo Wang – State University of New York at Binghamton

25. Board-Level Reliability of 100mm x 100mm Large Glass Packages: Die Placement Configuration Based Thermo-Mechanical Reliability for AI/HPC Applications
Kaushik Godbole, YongWon Lee, Muhannad Bakir, Suresh K. Sitaraman – Georgia Institute of Technology

26. Direct Glass-Copper Vias Integrated with Blind-Cavity Embedded Chips Using Nanoscale Liner
Sai Saravanan Ambi Venkataramanan, Mohan Kathaperumal, Aparnaa Iyer, C. P. Wong, Mark Losego – Georgia Institute of Technology; Zhaoxia Yang, Mark Broman – Thin Film Technology Corp.

27. Plasma-Free Wafer-Level Hybrid Bonding Using iCVD Polymer Thin Film for Feasible 3D Multi-Chip Integration
HyungJun Kim, MinJu Kim – Dankook University; Jongkyung Park, Taehun Jeon – Seoul National University of Science and Technology

28. Interfacial Engineering for Cost-Effective Cu-to-Cu Direct Bonding Using an Ultra-Thin Cu-Selective Passivation Coating
Kevin Antony Jesu Durai, Duwage Anushka Perera, Khanh Tuyet Anh Tran, Dinesh Kumar Kumaravel, Shinoj Sridharan Nair, Oliver Chyan – University of North Texas

29. Photonic Chiplet Integration into Electrically Active Flextrate for High Bandwidth Connectors
Alexis Samoylov, Randall Irwin, Subramanian Iyer – University of California, Los Angeles

30. Ultraprecise Additive Printing of Reliable Fine-Pitch Features
Olya Noruz Shamsian, Erik Busse, Abdullah Obeidat, Mark Poliks – Binghamton University

31. Compact 6GHz Microstrip Bandpass Filter with Folded-Arm Resonators and Dual Transmission Zeros: Design, Fabrication and Measurement
Jaehyuk Lee, Alexander Wilcher, Ariel David Cerpa, Hanna Jang, Yong-Kyu Yoon – University of Florida

32. Strain Range Dependent Fatigue Behavior of High Temperature Solder Alloys
Sean Lai, Chung Shuo Lee, Lijia Xie, John Blendell, Carol Handwerker, Ganesh Subbarayan – Purdue University

33. A Novel Hierarchical Global Multi-Scale Network for X-Ray Image Enhancement in Wafer-Level Packaging
Hanwen Li, Nagarajan Raghavan – Singapore University of Technology and Design; Senthilnath Jayavelu – Institute for Infocomm Research A*STAR

34. Rapid Multichip-Level TSV Formation and Heterogeneous 3D Integration from Multi-Project Wafers Using Photosensitive Temporary Adhesives
Jiayi Shen, Akihiro Tominaga, Bungo Tanaka, Chang Liu, Tetsu Tanaka, Takafumi Fukushima – Tohoku University

35. Additively-Deposited Fan-Out Interconnects for Power/RF Co-Packaging with Glass-Laminate Hybrid Panels
Sajith Rathnayaka, Daniel Escobar, Arjuna Madanayaka, Markondeya Raj Pulugurtha – Florida International University; Gilbert Rodriguez, Ronald Olmen – Haiku Tech Inc.

36. Novel Immersion-Sn Passivation Process to Address Nanoporous-Cu Seed Layer Etching Challenge for Scalable, Low-Temperature, Panel-Level Cu-Cu Bonding
Ramón A. Sosa, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology; Jobert Van Eisden – MKS; Kuldip Johal – MKS Instruments

37. Heterogeneous Integration of BEOL 22nm CMOS FDSOI AI to Cu Interposers by Direct Bonding
Kirthika Nahalingam, Mohammad Rezaeifer, Kamran Entesari, Linda Katehi – Texas A&M University

38. Link Quality Aware Pathfinding for Chiplet Interconnects
Aaron Yen, Jooyeon Jeong, Puneet Gupta – University of California, Los Angeles

39. Thermally-Aware System-Technology Co-Optimization for AI Systems
Dedeepyo Ray, George Karfakis, Alexander Graening, Puneet Gupta – University of California, Los Angeles; David Ratchkov – Anemoi Software

2026 ECTC EXHIBITION

The ECTC 2026 Exhibition is pleased to showcase dozens of companies and organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, exhibitors and attendees will enjoy continual interactions with conference attendees. We are also excited to bring back the ECTC Lounge, where attendees and exhibitors can take a few minutes to relax or converse with colleagues. Exhibit hours will be from 9:00 a.m. to 12:30 p.m. and 2:00 p.m. to 6:30 p.m. on Wednesday, May 27, 2026, and 9:00 a.m. to 12:30 p.m. and 2:00 p.m. to 4:00 p.m. on Thursday, May 28, 2026. Exhibit booths for 2026 are currently on a waitlist. Should you desire to be placed on the waitlist or need additional information about ECTC 2026, please contact our Exhibits Chair, Chris Bower, at chris.bower@ectc.net or exhibits@ectc.net.

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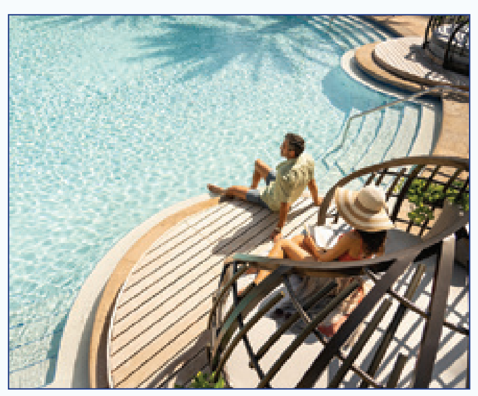

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Hotel reservations for ECTC 2026 can be made in one of the following ways:

1) ECTC Website: **www.ectc.net/locations**

2) By Phone: Reference the ECTC conference to receive discounted rates

- The Ritz-Carlton: +1-888-707-9325 - $290++/night
- JW Marriott: +1-800-433-5402 - $240++/night

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for ECTC. Be advised that you may receive emails about booking a hotel room for ECTC from 3rd party companies. These emails and sites are not to be trusted. **The only formal communication ECTC** will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: **registration@ectc.net**

HOW TO REGISTER FOR ECTC:

By Internet: Submit your registration electronically via **www.ectc.net**. Your registration must be received by the cutoff date, May 8, 2026, to qualify for the early registration discounts.

You may contact our registration staff at **registration@ectc.net** for additional information. Payment can be made by Visa, Mastercard, Discover, or American Express.

2026 ECTC REGISTRATION INFORMATION

Conference Registration		Advance Registration Until May 8	Door Registration Starting May 9
IEEE Member	Attendee (full ECTC conference)	US $1155	US $1330
	Attendee (Joint ECTC + ITHERM conferences)	$1500	$1750
	Attendee One-Day Registration	$875	$875
	Speaker or Chair (full ECTC conference)	$980	$1190
	Speaker or Chair One-Day Registration	$770	$770
Non-IEEE Member	Attendee (full ECTC conference)	$1435	$1605
	Attendee (Joint ECTC + ITHERM conferences)	$1750	$2095
	Attendee One-Day Registration	$875	$875
	Speaker or Chair (full ECTC conference)	$980	$1190
	Speaker or Chair One-Day Registration	$770	$770
Student	Attendee or Speaker (full conference)	$480	$480
Professional Development Courses (PDCs)			
IEEE Member	Full PDC (both a.m. and p.m.)	$625	$625
	Single PDC (a.m. or p.m.)	$440	$440
Non-IEEE Member	Full PDC (both a.m. and p.m.)	$675	$675
	Single PDC (a.m. or p.m.)	$490	$490
Student	Full PDC (both a.m. and p.m.) or Single PDC	$150	$150
Other Registration Options			
Extra Luncheon Tickets		$105	$105
Cancellation Fee		$100	$100

Please note that we are no longer offering the purchase of an extra proceedings.
Additionally, the various exhibit registration types are no longer available for the general public.

Please log onto www.ectc.net/registration to register for 2026 ECTC.

There will be no refunds or cancellations after May 8, 2026. Please note that a $100 cancellation fee will be in effect for all cancellations made on or prior to May 8, 2026. Substitutions can be made at any time.

For additional information about registration or ECTC please email us at: registration@ectc.net .

If you join IEEE **BEFORE you register for the 2026 ECTC you can save on registration fees and get the Electronics Packaging Society (EPS) add-on membership free for the reminder of 2026!*

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At destination, create your IEEE Web Account. Once complete, proceed to the Shopping Cart and enter EPS2026ECTC in the promotion code box. Click "Apply" and the Shopping Cart will be updated to show the discount. Use your new IEEE membership ID number and register for ECTC at the discounted IEEE Member Rate.

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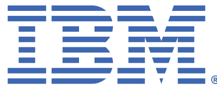
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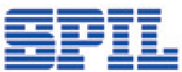
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CONFERENCE OVERVIEW

TUESDAY, MAY 26, 2026

Morning Professional Development Courses
8:00 a.m. - 12:00 Noon

1. High Reliability Soldering in Advanced Semiconductor Packaging
2. Photonic Components and Packaging Technologies for Data Center, Communication, Sensing, and Displays
3. Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Heterogeneous Integration and Advanced Packaging
4. Introduction to Quality and Reliability Engineering of Advanced Microelectronics Packaging
5. 2.5D/3D Package Failure Analysis - Failure Mechanisms and Analytical Tools
6. AI-Applications in Semiconductor Packaging
7. Fundamentals of Fabrication Processes and RF Design of Advanced Packages Including Fan-Out, Chiplets, Glass and Polymer Interposers
8. Electronics Cooling and Reliability for Data Centers

ECTC Special Sessions
8:30 a.m. - 10:00 a.m.

1. Quantum Infrastructure for AI Applications: Packaging Challenges and Roadmap
2. System Integration Challenges of Large-Size and High-Power Components for High-Performance Computing and AI Applications
3. HIR

ECTC Special Sessions
10:30 a.m. - 12:00 Noon

1. New Packaging Technologies for Panel Level Integration
2. Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging
3. HIR

Afternoon Professional Development Courses
1:30 p.m. - 5:30 p.m.

9. Polymers for Advanced Packaging
10. Diamond Heat Spreaders and Heterogeneous Integration
11. Advanced Packaging for Chiplet, Heterogeneous Integration, and Co-Packaged Optics
12. Preventing Packaging Failure - Modeling and Mitigation Strategies for Warpage, Fatigue, and Thermal Issues
13. Failure Analysis of Engineering Materials for Advanced Electronic Packaging
14. Flip Chip Technologies
15. Advanced Packaging for 5G/6G - RF Focus
16. Thermal Management in the Age of AI

Tuesday Luncheon
12:00 Noon – 1:15 p.m.

ECTC Special Sessions
1:30 p.m. - 3:00 p.m.

1. AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging
2. Enabling Next-Generation Advanced Packaging Technology from Wafer to Panel
3. HIR Workshop

ECTC Special Sessions
3:30 p.m. - 5:00 p.m.

1. Photonics-Based Systems for AI and Exascale Computing
2. Innovative Materials for Advanced Packaging – Materials for Packaging, Integration, and Performance
3. HIR Workshop

Young Professionals Networking Panel
7:00 p.m. - 7:45 p.m.

ECTC EPS Seminar
7:45 p.m. - 9:15 p.m.

Redefining System Integration: The Rise of Organic Substrates in the Chiplet Era

WEDNESDAY, MAY 27, 2026

ECTC Keynote
8:00 a.m. - 9:15 a.m.

Advanced Packaging and the Future of System Optimization

Technical Sessions
9:30 a.m. - 12:35 p.m.

1. Enabling Fan-In and Fan-Out Wafer/Panel Level Packaging Technology
2. Co-Packaged Optics
3. Advances in Low Temperature Hybrid Bonding
4. Breakthrough in Pitch Scaling With Advanced Bonding Technology
5. RF and High-Speed Design for mmWave and Sub-THz
6. Thermo-Mechanical Interactions With Reliability

Interactive Presentation Session 37
10:00 a.m. - 12:00 Noon

Wednesday Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

7. Heterogeneous Integration: The New Horizons
8. Die-to-Wafer Hybrid Bonding: Current Advancements and Future Directions
9. Advances in Thermal Materials and Encapsulation
10. Reliability of Large Body High Performance Computing and AI Packaging Solutions
11. Signal Integrity Design for High-Speed Interfaces
12. Characterization and Modeling for Process and Multi-Domain Analyses

Interactive Presentation Session 38
2:30 p.m. - 4:20 p.m.

ECTC Student Competition
6:45 p.m. - 8:00 p.m.

Finalists for the ECTC 2026 Student Innovation Challenges Competition in BSc/MSc and PhD level categories will make their presentations during this session. This competition allows participants to demonstrate their skills, apply their academic knowledge, and collaborate on innovative ideas in the field of electronic/photonic packaging. The winners in each category will be announced during the Friday luncheon.

THURSDAY, MAY 28, 2026

ECTC Plenary Session
8:00 a.m. - 9:15 a.m.

Efficiency Is Not Enough: Are We Solving the Wrong Problem in Data Center Energy Use?

Technical Sessions
9:30 a.m. - 12:35 p.m.

13. Advances in Thermal Design and Characterization
14. RDL and Fan-Out Interconnections
15. Optical Interconnects
16. Assembly and Manufacturing: 3D Stacking and Thermal Solutions
17. Digital Twin and AI in Advanced Packaging and Interconnect Security
18. Hybrid Bonding: Advanced Processing and Modeling

Interactive Presentation Session 39
10:00 a.m. - 12:00 Noon

Thursday EPS Awards Luncheon
12:45 p.m. - 2:00 p.m.

EPS Chapter Officer Meet and Greet
2:00 p.m. - 3:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

19. Substrate Core Innovations: Glass, Ceramic, and Silicon
20. Performance Analysis and Metrology of High-Bandwidth Electrical and Optical Interconnects
21. Novel Laser-Based Technologies and Fine-Pitch Interconnects
22. Reliability of High Current and High Power Packaging Solutions
23. Power Integrity Analysis for High-Performance Computing
24. AI and Machine Learning for Electronics Packaging

Interactive Presentation Session 40
2:30 p.m. - 4:20 p.m.

Start Up Competition

The Light Age: Strategic Investment in Photonics to Power the Next Computing Era

6:00 p.m. - 7:30 p.m.

FRIDAY, MAY 29, 2026

ECTC EPS President's Panel

Data Centers in the Age of AI: Challenges and Solutions

8:00 a.m. - 9:15 a.m.

Technical Sessions
9:30 a.m. - 12:35 p.m.

25. Optical and Electrical Design for High-Performance Computing
26. Advanced Wafer-to-Wafer Hybrid Bonding
27. Innovation in Glass and Dielectric Materials for Heterogeneous Integration
28. Beyond Silicon: Innovation in Glass Substrates and Panel Level Packaging
29. Innovation in Metallization, Alignment, Additive Manufacturing, and Low Temperature Interconnection
30. Thermal Management and Cooling Simulation

Student Interactive Presentations Session 41
10:00 a.m. - 12:00 Noon

Raffle Prize Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

31. 3D Integration, TSV, and Hybrid Bonding Innovations
32. Solder and Through Via Interconnections: Material & Process Innovations
33. Emerging Materials and Interconnect Technologies for Advanced Packaging
34. Optimizing Power Delivery, Thermal Management, and Metrology Solutions for Next-Generation Devices
35. Reliability of Advanced Automotive, AI, and Interconnect Packaging Solutions
36. Flexible Electronics and Thin-Assembly Warpage

Session Summary by Interest Area

Applied Reliability
S10, S22, S35

Assembly & Manufacturing Technology
S4, S16, S28

Emerging Technologies
S17, S29, S34

Electrical Design and Analysis
S5, S11, S23, S25

Interconnections
S8, S14, S20, S26, S32

Materials & Processing
S3, S9, S18, S21, S27, S33

Packaging Technologies
S1, S7, S13, S19, S25, S31

Photonics
S2, S15

Thermal/Mechanical Simulation & Characterization
S6, S12, S18, S24, S30, S36

Interactive Presentations
S37, S38, S39, S40, S41

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