

Welcome to the 73rd Electronic Components and Technology Conference (ECTC)

Special Sessions

Program Chair

Florian Herrault– PseudolithIC, Inc.

ECTC 2023 Special Sessions - Agenda



	Special Session Topics	Chair/co-chair/moderator	Date	Time
1	Advanced Packaging and HIR for Harsh Environment – Current Status and Opportunities	Tanja Braun (Fraunhofer IZM) and Przemyslaw Gromala (Bosch)	Tuesday	8:30 a.m. – 10:00 a.m.
2	Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications	Thomas Gregorich (Infinaera) and Chaoqi Zhang (Qualcomm)	Tuesday	10:30 a.m. – 12:00 p.m.
3	Photonic Integrated Circuit Packaging : challenges, pathfinding and technology adoption	Stéphane Bernabé (CEA Leti) and Hiren Thacker (Cisco)	Tuesday	1:30 p.m. – 3:00 p.m.
4	Advanced Packaging Manufacturing in North America: Building the Ecosystem	Nancy Stoffel (GE Research), Jan Vardaman (TechSearch International), and William Chen (ASE)	Tuesday	3:30 p.m. – 5:00 p.m.
5	Young Professionals Network Panel	Yan Liu (Medtronic)	Tuesday	7:00 p.m. – 7:45 p.m.
6	IEEE EPS Seminar: The Future of High-density Substrates – Towards Submicron Technology	Takashi Hisada (IBM) and Yasumitsu Orii (Rapidus)	Tuesday	7:45 p.m. – 9:15 p.m.
7	ECTC Keynote: Prof. Michael Manfra (Purdue University) - Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging	Ibrahim Guven (ECTC General Chair)	Wednesday	8:00 a.m. – 9:15 a.m.
8	ECTC / iTherm Diversity Panel: Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative	Kim Yess (Brewer Science) and Nancy Stoffel (GE Research) (ECTC) & Cristina Amon (University of Toronto) (iTherm)	Wednesday	6:30 p.m. – 7:30 p.m.
9	ECTC Plenary: Millimeter-Wave Phased Array Frontend Integration and Packaging for Next-Generation Communication and Radar Systems	Kevin Gu (Metawave Corp) and Ivan Ndip (Fraunhofer IZM / Brandenburg University of Technology)	Thursday	8:00 a.m. – 9:15 a.m.
10	IEEE EPS President’s Panel: How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP	Kitty Pearsall (Boss Precision Inc., IEEE EPS President) and David McCann (Lyte)	Friday	8:00 a.m. – 9:15 a.m.

Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging

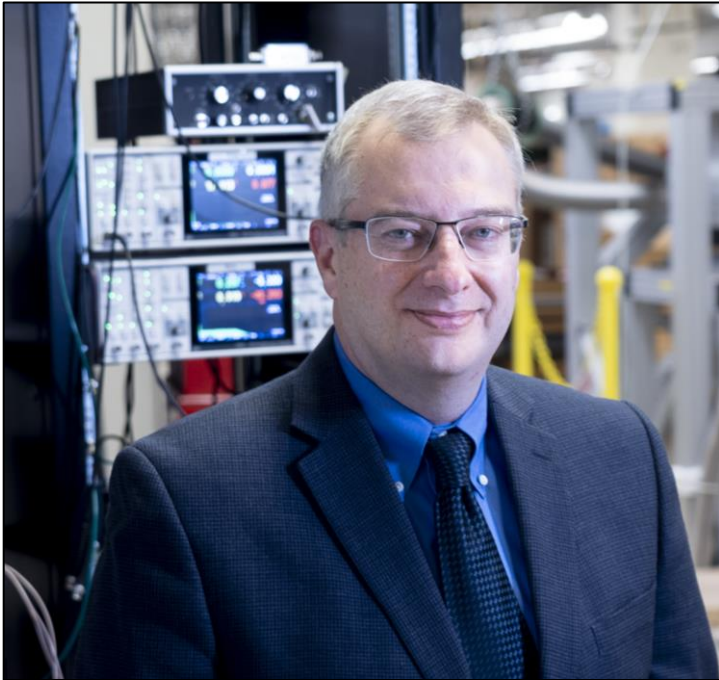
Wednesday, May 31, 2023, 8:00 a.m. – 9:15 a.m.

Chair: Ibrahim Guven, Virginia Commonwealth University, ECTC 2023 General Chair

We cordially thank our Keynote sponsor EMD Electronics



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Keynote Speaker

Prof. Michael J. Manfra

Purdue University

Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging

Quantum computing will revolutionize the way we tackle certain societally relevant but currently intractable problems. To reach this promise, significant advances in quantum hardware on multiple scales are required. This keynote address will explore the challenges and opportunities in quantum computing hardware ranging from basic choice of qubit platform, through scalable control and readout, to system architecture. Technology advancement will require innovations in material science and device physics to tackle challenges on the quantum plane. Progress will also hinge on innovations in interconnect technology and advanced packaging for an integrated quantum-classical hardware system. As in classical digital computing, thermal management and reliability concerns will impact quantum system performance and must be addressed directly. In this presentation, some exemplars that demonstrate the opportunities for contributions to quantum technology from the community focused electron devices, interconnects and advanced packaging will be discussed. Development of a full-stack quantum computer necessitates industrial programs stimulated and informed by innovation generated in government labs and academic research groups.

Advanced Packaging and HIR for Harsh Environment – Current Status and Opportunities

Tuesday, May 30, 2023, 8:30 a.m. – 10:00 a.m.

Chairs: Tanja Braun (Fraunhofer IZM) and Przemyslaw Gromala (Robert Bosch)

We cordially thank our Special Session sponsor Zymet





Chair
Tanja Braun
Fraunhofer IZM



Chair
Przemyslaw Gromala
Robert Bosch GmbH



Panelist
Dae-Woo Kim
Samsung

Panelist
Giuseppe Barone
Robert Bosch GmbH



Panelist
Vikas Gupta
ASE



Panelist
Shin-Puu Jeng
TSMC



Panelist
Ram Trichur
Henkel



Panelist
Vanessa Smet
Georgia Tech



Panelist
G.Q. Zhang
TU Delft

Advanced Packaging and HIR for Harsh Environment – Current Status and Opportunities

Electronic components and systems are a main contributor to most of innovative ideas and products of today's world. In automotive industry, electronic components and systems are accountable for more than 80% of all innovation. When we think about highly automated and autonomous systems, advanced packaging is a must. Nowadays, most advanced electronic components such as CPUs or GPUs they are being introduced into harsh environment such as automotive, avionics or space applications almost at the same time as in consumer products. Therefore, in our special session, we would like to discuss with the top experts from industry and academia what the current status and opportunities are for advanced packaging for harsh environment.

Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications

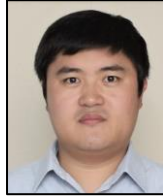
Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.

Chairs: Thomas Gregorich (Infinera) and Chaoqi Zhang (Qualcomm)

Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications



Chair
Thomas Gregorich
Infirera



Chair
Chaoqi Zhang
Qualcomm



Moderator
Jan Vardaman
TechSearch International



Speaker
Eric Beyne
IMEC



Speaker
Kenneth Larsen
Synopsys



Speaker
Raja Swaminathan
AMD



Speaker
Thomas Uhrmann
EVG



Speaker
Chris Scanlan
Besi



Speaker
Xavier Brun
Intel

As one of the primary building-blocks of IC packages, electrical interconnections are evolving rapidly to address increasing ultra-high bandwidth requirements. Copper Hybrid Bonds deliver the highest-density chip-to-chip interconnect and are seen as a key enabling technology for ultra-high bandwidth devices/systems such as vertically-stacked chiplets.

This Special Session will explore the applications, requirements, and challenges of Copper Hybrid Bonds (CHB) for Chip-to-Wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand. While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

Photonic Integrated Circuit Packaging : challenges, pathfinding and technology adoption

Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.

Chairs: Stéphane Bernabé (CEA Leti) and Hiren Thacker (Cisco)



Chair
Stéphane Bernabé
CEA Leti



Chair
Hiren Thacker
Cisco



Speaker
Gianlorenzo Masini
Cisco



Speaker
Thierry Mourier
CEA Leti



Speaker
Colin Dankwart
Ficontec Service GmbH



Speaker
Alexander Janta-Polczynski
IBM



Speaker
Peter O'Brien
Tyndall Institute



Speaker
Hesham Taha
Teramont

Photonic Integrated Circuit Packaging : challenges, pathfinding and technology adoption

Photonic integrated circuit (PIC) technologies are proliferating into many application spaces; from hyperscale data center, High Performance Computing to sensing including LiDAR. Packaging remains the greatest challenge to high volume manufacturing at high throughput and yield. The main challenges are: optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC SC86C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption towards high-volume reality.

Advanced Packaging Manufacturing in North America: Building the Ecosystem

Tuesday, May 30, 2023, 3:30 p.m. – 5:00 p.m.

Chairs: Nancy Stoffel (GE Research), Jan Vardaman (TechSearch International), and
William Chen (ASE)



Chair
Nancy Stoffel
GE Research



Chair
William Chen
ASE



Chair
Jan Vardaman
TechSearch International



Panelist
Frank Gayle
NIST



Panelist
Carl McCants
DARPA



Panelist
Subramanian Iyer
UCLA



Panelist
Dick Otte
Promex Industriks, Inc.



Panelist
Hem P. Takiar
Micron Technology Inc.

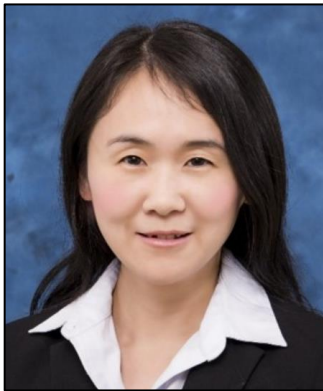
Advanced Packaging Manufacturing in North America: Building the Ecosystem

North America has companies that excel in design for electronics systems, device, and advanced packaging. However less than 2% of the packaging occurs in the US. This session will discuss the ambitious goals being set through the CHIPS ACT to bring Advanced Packaging to North America. We will review the targets and developing plans of the US government, funded through the CHIPS Act. The panelists will overview major initiatives launched in R&D and Manufacturing. We will also discuss the challenges to meeting the goals.

ECTC Young Professionals Network Panel

Tuesday, May 30, 2023, 7:00 p.m. – 7:45 p.m.

Chair: Yan Liu (Medtronic)



Chair
Yan Liu
Medtronic

ECTC Young Professionals Network Panel

Join your peers for a session designed with you in mind. You will network with industry professionals, ECTC leaders, EPS members, and other students as you team up for activities to learn more about packaging-related topics all the while engaging with top professionals. Make this opportunity a priority!

Come and take advantage of meeting face to face with industry leaders and top professionals, ask career questions, and get to know what industry has to offer!

The Future of High-density Substrates – Towards Submicron Technology

Tuesday, May 30, 2023, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada (IBM) and Yasumitsu Orii (Rapidus)

We cordially thank our Special Session sponsor



Chair
Takashi Hisada
IBM



Chair
Yasumitsu Orii
Rapidus



Panelist
Yasushi Araki
Shinko



Panelist
Yu-Hua Chen
Unimicron



Panelist
Satoru Kuramochi
Dai Nippon Printing (DNP)



Panelist
Madhavan Swaminathan
Pennsylvania State University



Panelist
Griselda Bonilla
IBM

The Future of High-density Substrates – Towards Submicron Technology

Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules while Si scaling is slowing down. One of the key attributes of chiplets and HI technologies is the bandwidth of interconnection between chips within the same package. A very short-distance and high-density interconnection from one chip to another enables high-speed data transmission with low energy loss. High-density chip carrier substrate is the core technology driving the evolution of chiplets and HI technologies. In this session, we will discuss ultra-fine-pitch substrate technologies towards submicron ground rule for Chiplets and Heterogeneous Integration.

Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative

Wednesday, May 31, 2023, 6:30 p.m. – 7:30 p.m.

Chairs: Kim Yess (Brewer Science) and Nancy Stoffel (GE Research) (ECTC) & Cristina Amon (University of Toronto) (ITherm)



Chair
Nancy Stoffel
GE Research



Chair
Kim Yess
Brewer Science



Chair
Cristina Amon
University of Toronto



Panelist
Dereje Agonafer
University of Texas Arlington



Panelist
Courtney Power
NextFlex



Panelist
Jennifer Edwards
GE Foundation/NEXT Engineer

Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative

The electronic industry has an urgent need to increase the technical workforce and address challenges related to recruitment, inclusion and retention of diverse talents. The panelists will discuss the development of initiatives, policies and programs to increase and diversify the workforce, along with metrics to assess progress. Discussions will include the benefits of diversity in high-performing workplaces, strategies to build a larger and more diverse workforce, and tools for inclusion and engagement – sharing both successes and challenges associated with achieving these goals.

Millimeter-Wave Phased Array Frontend Integration and Packaging for Next-Generation Communication and Radar Systems

Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.

Chairs: Kevin Gu (Metawave Corp) and Ivan Ndip (Fraunhofer IZM /
Brandenburg University of Technology)



Chair
Kevin Gu
Metawave Corp



Chair
Ivan Ndip
Fraunhofer IZM / Brandenburg
University of Technology (BTU)



Panelist
Madhavan Swaminathan
Pennsylvania State University



Panelist
Hasan Sharifi
HRL Laboratories



Panelist
Augusto Gutierrez-Aitken
Northrop Grumman Space
Systems



Panelist
Shahriar Shahramian
Nokia Bell Labs



Panelist
Alberto Valdes-Garcia
IBM T. J. Watson Research
Center



Panelist
Jonathan Hacker
Teledyne Scientific

Millimeter-Wave Phased Array Frontend Integration and Packaging for Next-Generation Communication and Radar Systems

Phased arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly-emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and latest advancement of packaging and integration technologies for designing and implementing phased array front-end modules including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, and system demos/prototypes.

How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP?

Friday, June 2, 2023, 8:00 a.m. – 9:15 a.m.

Chairs: Kitty Pearsall (Boss Precision Inc., IEEE EPS President) and David McCann (Lyte)



Chair
Kitty Pearsall
IEEE EPS President
Boss Precision Inc.



Chair
**David McCann
Lyte**



Panelist
Amr S. Helmy
University of Toronto



Panelist
Stefano Oggioni
AT&S



Panelist
Ritesh Jain
Lightmatter



Panelist
Ajey Jacob
University of Southern California

How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SiP

This panel will discuss the tools, technologies and approaches that will enable the industry to enhance the bandwidth density of interconnections in SiP enabled by photonics. To be adopted, such capabilities must be provided with energy per bit which meets the roadmaps and standards targets for the interconnection protocols within the package and on chip.