FIRST CALL FOR PAPERS

IEEE 76th Electronic Components and Technology Conference • www.ectc.net
to be held May 26 – May 29, 2026 at the JW Marriott Orlando, Grande Lakes, Orlando, Florida, USA

The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee. Authors are encouraged to review the sessions of the previous ECTC programs to determine which committees to select for their abstracts.

Applied Reliability: Reliability of 2D, 2.5D, Si bridge, 3D, chiplets, WLCSP, FOWLP, FOPLP & heterogeneous integration and co-packaged optics; interconnect reliability in micro-bump, micro-pillar, Cu pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip & wire bonded packages, novel reliability test methods, life models, FA techniques & materials characterization, component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays and memory; reliability and test methods for thermal interface materials and reliability related to liquid cooling and immersion cooling.

Assembly and Manufacturing Technology: Assembly and manufacturing challenges for new markets; die bonding methods and process challenges: D2D, D2W, W2W; wafer level process/ materials technologies; die and package singulation manufacturing; new & next generation substrates; smart factory/ manufacturing; assembly related test/yield hardware development/improvement; integrating advanced thermal solutions in manufacturing: design/performance, integrating solutions, thermal materials, low stress/high thermal; process advancements/yield enhancements; cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/ compression/injection mold; heterogeneous integration and process: flip chip, chiplets, 3D stacking, bridge technology, large body, warpage management; shielding/protection technologies and manufacturing and market requirements.

Emerging Technologies: Packaging for quantum computing and other cryogenic applications; metrology for advanced packaging and emerging technologies; AI in electronics packaging and its applications; challenges in hardware security; AI electronics packaging and its applications; power electronics and energy storage; MEMS & NEMS; emerging, novel and unique flexible/ stretchable/ wearable hybrid electronics, medical devices and bioelectronics; additive, hybrid, nano, and smart manufacturing for electronics packaging; green and sustainable electronics, net zero strategy/ technology; digital twins.

Electrical Design & Analysis: 5G/6G, IoT, cloud computing, autonomous vehicles, AI/ML; antennas, sensors, power transfer, wired/wireless communications, RF to THz; multiphysics/multiscale modeling & characterization of interconnects, modules, components, and systems; chiplet, heterogeneous integration, chip-to-chip, die-to-die, SiP/MCM/system co-design (chip/package/board), UCIe, HBM/ HPC; opto-electronic (OE) hybrid integration, analog packaging, power electronics modeling/ characterization; high-speed/frequency (RF, mm-wave, THz) signal integrity, power integrity, and EMI/ EMC.

Interconnections: Interconnects for chiplets, heterogeneous integration, hybrid bonding, C2W, W2W, fan-out, panel-level, TSV, TGV; interconnects for 2.5D/3D, Si/glass/organic interposers, fine-pitch/multi-layer RDL, SiP, wafer-level system integration; interconnects for thermo-compression/ laser assisted/ transient liquid phase bonding, low temperature solder, flip-chip, micro-bump, Cu pillar, wirebond, Al ribbon bond; printable interconnects, flexible interconnect, quantum interconnects, optical interconnects, interconnects for SiC/GaN or WBG; interconnection materials, chemistries, metrology, characterization and reliability; conductive/non-conductive adhesives, ACF, underfill, molding compounds; chiplet interconnect design and validation, UCIe/BoW/etc. standards; thermal interface materials, thermal/mechanical/electrical tests and reliability.

Materials & Processing: Advanced materials and processes for hybrid bonding, fan-out, Si interposer, 2.5D/3D, chiplets, HI, TSV; advanced materials and processes for thermal and mechanical improvement for packaging; wafer & panel level packaging materials and process advancements; dielectrics and underfills, molding compounds, thermal interface materials; harsh environment resistant materials; temporary wafer bond/debond materials and processes, TCB and hybrid bonding, conductive adhesives; emerging electronic materials and processes; novel solder metallurgies; novel materials and processes for high density interconnect.

Thermal/Mechanical Simulation & Characterization: Thermal/ mechanical simulation and characterization at component, board, and system levels for all packaging technologies; reliability related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); material constitutive relations; chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; novel modeling techniques including multi-scale physics, co-design approaches; quantum computing; measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; application of artificial intelligence on modeling, characterization, and digital twins; credible simulations; CFD simulation.

Packaging Technologies: 2.XD/3D architectures/designs for energy efficient HPC, C2C links, structures, thermal solutions, and methods & processes; heterogeneous (chiplet) integration for 2.5D, 3D-IC for AI, neural nets, HBM, CPU, GPU, ASIC, and CPO; silicon, glass, diamond & organic interposer and advanced package technology; dual-Damascene Cu, Cu TSV, hybrid bonding, and backside power; embedded die, bridge, and passives; flexible, advanced substrates & modules; fanout wafer and panel level packaging, advanced flip-chip, SiP, CSP, PoP; RF, wireless, MEMS, Sensors & IoT, automotive, wireless power and power electronics; SiC, GaN, PMIC, SPS; bio, medical, flexible, wearable & extreme environments packaging.

Photonics: Photonic components packaging for computing, communications, data processing, mobility, healthcare, green energy photonics, agriculture, horticulture, food, environmental, climate and atmosphere monitoring, space, automobile, underwater, industrial, defense, process integration, co-packaging (photonics, electronics, and laser integration), free space optics, microscopy and advanced spectroscopy, 3D printing of micro-optical components for packaging, assembly and manufacturing; packaging for the quantum photonics world; packaging of new photonics materials; optical characterization of packaging components; equipment and tools for photonics packaging; detachable fiber array unit; ultra-low power photonics and materials; heterogeneous materials; quantum dots; meta-surfaces and meta-materials.

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract that describes the novelty, scope, content, and key points of your proposed manuscript via the website at www.ectc.net.

If you have any questions, contact:
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Abstracts cannot contain more than 700 words and must be received by October 6, 2025, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors. The authors are notified about the abstract selection outcome by December 12, 2025.

Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From the proposals received, 16 PDCs are selected for offering at the 76th ECTC on Tuesday, May 26, 2026.

Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 19, 2025. Authors are notified of course acceptance with instructions by December 12, 2025.

If you have any questions, contact:
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The 2026 IEEE 76th Electronic Components and Technology Conference

May 26 – 29, 2026

Mark Your Calendars Now!

JW Marriott Grande Lakes, Orlando, Florida

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