ECTC 2025

75 YEARS

The 2025 IEEE 75th Electronic Components and Technology Conference

May 27 – 30, 2025

2025 Conference Program & Exhibitor Listings

WELCOME TO THE IEEE 75th ECTC FROM THE GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program and Executive Committees, we are delighted to welcome you to the IEEE 75th Electronic Components and Technology Conference (ECTC). This premier event, sponsored by the IEEE Electronics Packaging Society (EPS), takes place May 27–30, 2025, at the Gaylord Texan Resort & Convention Center in Dallas, Texas. ECTC brings together over 2,000 professionals from across the global microelectronics packaging industry, including manufacturers, design houses, foundries, material suppliers, universities, and investors. Join us to connect with key stakeholders and explore cutting-edge advancements in the field.

The 75th ECTC conference introduces several new and exciting program events. First, the number of special sessions on Tuesday has more than doubled – from four to nine – with two sessions running in parallel and some really exciting topics and panelists. To support workforce development, we are launching a new student engagement program. We have partnered with local universities and colleges to invite approximately 20 undergraduate students on Wednesday, introducing them to the fascinating world of microelectronic packaging and technologies. Additionally, this year features a student competition challenge. Three winning teams are invited to the conference to present their projects during Pitch Night, co-organized with the Start-Up Competition Challenge. Lastly, our Thursday ECTC Reception Gala contains a special event to celebrate the conference's 75th anniversary.

At the 75th ECTC, approximately 400 technical papers are planned to be presented in 36 oral sessions and five interactive sessions. Authors from over 20 countries share their latest research on topics including 3D integration, bridge and chiplet integration, hybrid bonding, wafer-to-wafer and chip-to-wafer bonding, novel substrate materials, high-density RDL, next-generation interconnections, and warpage management of large panels. Also, large-package manufacturing, additive manufacturing, wearable and medical applications, AI/ML, and advanced RF and antenna design are on the agenda. Thermal management, interconnect reliability, advanced characterization, and process simulations, eco-friendly packaging, and secure designs are discussed as well. Interactive sessions focus on innovations in bonding, power delivery, optimization algorithms, specialized device packaging, and reliability testing. The 75th ECTC serves as a global platform for exploring cutting-edge advancements in microelectronic packaging, fostering innovation, and addressing industry challenges.

This year, the conference features a total of eleven special sessions with industry experts, including nine on Tuesday, each lasting 90 minutes. On Tuesday, two parallel sets of special sessions take place instead of one as in previous years. Rozalia Beica (Rapidus) and Habib Hichri (Ajinomoto Fine-Techno USA) chair the first session, which explores Ultra High-Density Interconnect Technologies. Mascha Gorchichko (Applied Materials) and Dishit Parekh (AMD) chair the second session, focusing on Hybrid Bonding. Richard Pitwon (Resolute Photonics Ltd.) and Ajey Jacob (University of Southern California) discuss Quantum Advanced Packaging. Simultaneously, Jan Vardaman (TechSearch International), Zia Karim (Yield Engineering Systems), and Thom Gregorich (Zeiss) present on Glass Core vs. RDL Interposers. In the afternoon, Vidya Jayaram (Chipletz) and Karan Bhangaonkar (Google) co-chair a session on Advanced Materials for Co-Packaged Optics. For those interested in Fault and Failure Analysis in Chiplets, Yan Li (Samsung), Tae-Kyu Lee (Cisco), and Zhi Yang (Groq) simultaneously lead a dedicated session. The final two special session blocks include a discussion on Sub-THz Packaging for Communication and Radar, chaired by Maciej Wojnowski (Infineon Technologies AG) and Ivan Ndip (Fraunhofer IZM/Brandenburg University of Technology), as well as a session on Thermal Management for Power Delivery, chaired by Dwayne Shirley (Marvell) and Tiwei Wei (Purdue University).

Parallel to the special sessions, the Heterogeneous Integration Roadmap (HIR) workshop is organized by IEEE EPS, chaired by William Chen (ASE) and Ravi Mahajan (Intel). Four sessions are planned: IoT & AI at the Edge, moderated by Wei Chung Lo (ITRI) and Rockwell Hsu (Cisco); Advancing Heterogeneous Integration Through Metrology & AI, moderated by Chris Bailey (ASU) and Xuejun Fan (Lamar University); Integrating Photonics in HPC & Network Systems, moderated by Kanad Ghose (Binghamton Univ.) and John Shalf (LBL); and Advances in Panels, Substrates and Printed Circuit Boards moderated by William Chen (ASE) and Ravi Mahajan (Intel).

Tuesday evening offers additional opportunities to engage. Aakrati Jain (IBM) leads a Young Professionals Networking Event from 6:45 p.m. to 7:45 p.m., featuring a new fish-bowl discussion format. Following this, Takashi Hisada and Yasumitsu Orii (both with Rapidus) chair the IEEE EPS Seminar on User Perspectives of Chiplet Technology from 7:45 p.m. to 9:15 p.m.

On Wednesday morning, May 28, 2025, ECTC features a keynote presentation on Achieving Efficient Zettascale Compute in the AI Era by Sam Naffziger (AMD), invited by General Chair Florian Herrault (PseudolithIC, Inc.) The Student Engagement Program, chaired by Ibrahim Guven (Virginia Commonwealth University), takes place throughout the day, welcoming undergraduate students from local universities and colleges. On Thursday, May 29, 2025, from 8:00 a.m. to 9:15 a.m., a Plenary Session on Emerging Advanced Power Delivery for the AI Computing Era is planned, chaired by Dongming He (Qualcomm) and Eric Beyne (imec). Additionally, an IEEE EPS President's panel titled ECTC at 75: Celebrating the Past, Innovating for the Future, organized by IEEE EPS President Patrick Thompson (Texas Instruments) is held on Friday morning, May 30, 2025.

The IEEE ITherm Conference is co-located with the 75th Anniversary ECTC and co-organizes 16 CEU-approved Professional Development Courses (PDCs). Organized by Kitty Pearsall and Jeffrey Suhling, these expert-led courses are held on Tuesday, May 27, 2025.

The ECTC Exhibits, running Wednesday, May 28, and Thursday, May 29, showcase cutting-edge technologies and products from over 100 leading companies in electronic components, materials, packaging, and services. Starting daily at 9 a.m., the exhibits provide excellent opportunities for networking during coffee breaks, luncheons, and evening receptions.

Whether you are an engineer, manager, student, or executive, ECTC offers unique experiences for everyone in the microelectronics packaging and components industry. We invite you to join us for the Anniversary 75th ECTC and to be a part of all the exciting technical and professional opportunities.

We want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the Anniversary 75th ECTC a success. We look forward to meeting you at the Gaylord Texan Resort & Convention Center, Dallas, Texas, from May 27 to May 30, 2025.

Przemyslaw Gromala
75th ECTC Program Chair
pgromala@ieee.org

Florian Herrault
75th ECTC General Chair
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WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, I am delighted to welcome you to the 75th Electronic Components and Technology Conference – the world's premier event for electronics packaging. First held 75 years ago, ECTC continues to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging. Building upon the outstanding event held in 2024 and the very positive feedback from attendees and sponsors, we expect attendance at ECTC 2025 to well exceed 2,000 packaging professionals, setting another record. Our conference portfolio continues to find innovative ways to grow and serve our community.

2025 is our 75th anniversary, making this ECTC special. It's worth looking back at some milestone years. The initial gathering of what would become the ECTC was held in Washington, DC, in 1950 and was called "Symposium on Improved Quality Electronic Components." In 1950, only two years after the invention of the transistor, modern electronics were in their infancy. Leaders in the field recognized improvements in methodology and implementation of standards were necessary for the new technology to be successful. This symposium contained five sessions. All electronics at this time were discrete. By 1975, our 25th anniversary, the conference was named the Electronic Components Conference (ECC). The conference ran for two and a half days, with a dozen sessions. The handheld calculator was three years old, the mobile phone had been demonstrated but not released, and the first microprocessor-based PC, the Altair 8800, had just been launched. In 2000, our conference was known by its current name, ECTC, and was a full three-day conference, with 36 oral sessions and two interactive sessions. CDs were at their peak, with MP3 players on the rise, and DVDs had supplanted VHS for video. Cell phones with cameras were newly released. Today, as our 75th ECTC gets underway, we are a four-day conference with nearly 50 special, oral and interactive sessions. Packaging is an equal partner with semiconductors in providing today's leading-edge electronic solutions.

The ECTC, together with the EPS flagship conferences in Europe and Asia-Pacific, ESTC and EPTC, respectively, continues to bring high quality technical content to a growing packaging community. These achievements would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year's exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community. I also thank our authors, presenters, and sponsors for their contributions to this year's event. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members. In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website. Finally, I thank you for attending this year's ECTC. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Patrick Thompson, EPS President 2024 – 2025

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Conference organizers reserve the right to cancel or change this program without prior notice.

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to the conference including to all training courses, sessions, seminars, meals, exhibits and Interactive Presentation areas, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly electronics, cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Please follow hotel policies and signs regarding smoking. Smoking is NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, seminars, meals, exhibits and hallway areas, and all conference social functions. Thank you for your consideration and cooperation.

REGISTRATION AND MISCELLANEOUS INFORMATION

REGISTRATION LOCATION AND HOURS

ECTC registration will be open at the ECTC Registration Desk located in The Gaylord Texan Resort & Convention Center on the lobby level of the Convention Center.

Monday, May 26, 2025: 12:00 Noon – 4:00 p.m.
Tuesday, May 27, 2025: 6:45 a.m. – 7:45 p.m.
Until 8:15 a.m. on Tuesday registration is for morning session PDC and Special Session Attendees*
Wednesday, May 28, 2025: 6:45 a.m. – 4:00 p.m.
Thursday, May 29, 2025: 7:00 a.m. – 4:00 p.m.
Friday, May 30, 2025: 7:00 a.m. – 12:00 Noon

On Tuesday, May 27, light morning refreshments will be provided from 6:45 a.m. – 7:30 a.m. Come pick up your registration materials EARLY and grab a bite to eat before our PDCs and Special Sessions start!

**** The above schedule for Tuesday will be vigorously enforced to prevent attendees from being late for their courses and sessions. Please make sure to take advantage of the 6:45 a.m. start time as registration becomes very congested prior to the start of morning programming.***

DOOR REGISTRATION FEES

Door Registration includes the digital Proceedings. Instructions for downloading the Proceedings will be shared with eligible attendees.

IEEE Members

IEEE Member JOINT Registration (full ECTC + ITHERM conference) $1665
IEEE Member Full Registration $1265
IEEE Member Speaker / Session Chair $1135
IEEE Member One Day $835
IEEE Member Speaker One Day $735

Non-Members

JOINT Registration (full ECTC + ITHERM conference) $1995
Non-Member Full Registration $1530
Non-Member Speaker / Session Chair Full Registration $1135
Non-Member One Day $835
Non-Member Speaker / Session Chair One Day $735

Student $455
Student Speaker $455

Tuesday Professional Development Courses

IEEE Members

Tuesday AM or PM Course with luncheon $440
Tuesday All-Day Courses with luncheon $625

Non-Members

Tuesday AM or PM Course with luncheon $490
Tuesday All-Day Courses with luncheon $675
Tuesday Student All-Day Courses with Luncheon $150

Extra Luncheon Tickets for Each Day $100

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctors Briefing
(Room Location: San Antonio 2–3)

SESSION CHAIRS AND SPEAKERS BREAKFAST

Session chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, speakers and session chairs will get to meet each other and instructions for the day will be provided by the Program Chair.

7:00 a.m. Wednesday – Friday
(Room Location: Texas C)

SPEAKER PREP ROOM

Speakers should prepare and review their digital presentations within the allotted times and at the location below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday
(Room Location: Dallas 4)

MISCELLANEOUS INFORMATION

Hotel Concierge

The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room

Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or +1-845-475-1290.

LUNCHEONS

Main Stage Room: Texas A & B

This year ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Your conference badge will be scanned for entry into lunch. Please come and enjoy time with other attendees and colleagues in the industry!

Lunch times will vary, see below for specific details for each day.

Tuesday's PDC & Special Sessions Luncheon:
12:00 Noon – 1:15 p.m.

Wednesday's General Chair Luncheon:
12:45 p.m. – 2:00 p.m.

Thursday's EPS Luncheon:
12:45 p.m. – 2:00 p.m.

Friday's Program Chair Luncheon:
12:45 p.m. – 2:00 p.m.

Don't miss out on this lunch! We will be raffling off several prizes including a hotel stay, free conference registrations, and many other industry gadgets!

ECTC Student Reception

Tuesday, May 27, 2025
5:00 p.m. – 6:00 p.m.
Mission Plaza, Hotel Atrium

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

General Chair's Speakers Reception

Tuesday, May 27, 2025
6:00 p.m. – 7:00 p.m.
Riverwalk Cantina Restaurant, Hotel Atrium
Invited session chairs and speakers are requested to attend the reception.

Exhibition Reception

Wednesday, May 28, 2025
5:30 p.m. – 6:30 p.m.
Longhorn D
All attendees and guests are invited.

75th ECTC Gala Reception

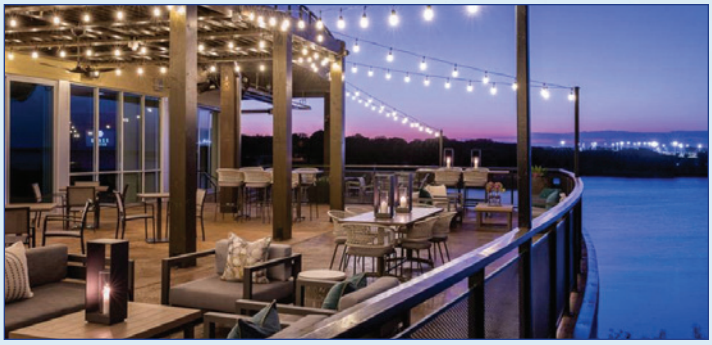
Thursday, May 29, 2025
7:30 p.m.
Glass Cactus Venue

Transportation is available in the hotel lobby at the Tour Bus Lobby, across from Cocoa Bean.

EPS Worldwide Chapter Officer Meet and Greet

Thursday, May 29, 2025
7:00 a.m. – 8:00 a.m.
Dallas 3 (online by invitation)

Please attend if you are an officer of an EPS Chapter (breakfast included).
Chapter Program Director: Andrew Tay
Regions 1–7 and 9: Annette Teng
Region 8: Steffen Kroehnert
Region 10: Shaw Fong Wong



ECTC Mobile App

ECTC is pleased to announce a new free mobile app this year called eConference.io by X-CD Technologies. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and venue maps. The app also features tools to create your personal itinerary by setting your schedule, so you never miss a presentation, social interaction functions, and the ability to vote for the best paper. The app is available for iOS and Android devices from their respective app stores by searching "eConference.io" in stores or scanning the QR code included here. Once downloaded, enter the code **ECTC2025** (not case-sensitive). Log into the app **using the email you registered with** and start browsing the content.

IEEE Transactions on Components, Packaging, and Manufacturing Technology

If you are an author of a 75th ECTC paper, consider submitting an enhanced and extended version of your work to the IEEE Transactions on Components, Packaging, and Manufacturing Technology for peer-reviewed journal publication after the conference. A journal manuscript should go beyond the conference paper by incorporating new results, deeper analysis, additional discussions, and expanded references that were not included in the original submission. For more details on submitting an extended conference paper, see the "Papers Presented at Conferences" section at **https://eps.ieee.org/publications/ieee-transactions-on-cpmt/information-and-resources-for-authors.html**

75th ECTC CONFERENCE OVERVIEW

2025 Special Session on Ultra High Density Interconnect

Ultra High Density Interconnect Technologies and Supply Chain Readiness for AI & HPC

Tuesday, May 27, 2025, 8:30 a.m. – 10:00 a.m. • Texas C

Chairs: Rozalia Beica, Rapidus and Habib Hichri, Ajinomoto Fine-Techno USA Corporation


Heterogeneous integration and chiplets will require fine line and space interconnects, as well as low warpage materials, to achieve the required performance for various applications in the rapidly evolving landscape of Artificial Intelligence (AI) and High-Performance Computing (HPC), which have significantly increased computational and memory needs. One of the critical areas that continues to have challenges in the industry is advancing the interconnects at the organic substrate level, a reason why various different approaches are being considered:

- Ultra-high density organic substrate (2.0D), bringing front-end of the line processes into the substrate/panel infrastructure to meet ultrafine via/line/spacing (2/2/2 µm and below).
- Building the organic substrate at wafer level (SOW)
- Hybrid substrates
- Bringing the well-known redistribution layers (RDLs) to substrates using 2.xD technologies
- Bringing glass substrates to address the needs for advanced interconnects and warpage issues for large size and complex substrates

Each of these approaches have their own limitations and challenges. This session will discuss the different alternative technologies addressing the latest developments and remaining challenges, and supply chain readiness to address the next generation of interconnects.

The session will comprise a panel of industry experts across the supply chain with global participation. Each panelist will provide a short presentation of their view on these technologies and supply chain readiness followed by a panel discussion.

Yu Hua Chen, Unimicron; Niranjan Khasgiwale, Applied Materials; Kuldip Johal, Atotech; Yoshio Nishimura, Ajinomoto; Monita Pau, Onto Innovation; Yoshio Takatsu, ORC Manufacturing Co., Ltd.

2025 Special Session on Hybrid Bonding

Hybrid Bonding (HB): to B, or Not to B? Needs and Challenges for the Next Decade

Tuesday, May 27, 2025, 8:30 a.m. – 10:00 a.m. • Texas 1–3

Chairs: Masha Gorchichko, Applied Materials, Inc. and Dishit Parekh, AMD


Hybrid bonding is the key technology for high-density 3D integration and advanced packaging. In recent years, significant advancements were made in pitch scaling, die-to-die bonding, alternative materials, and low-temperature processes. However, there are still engineering and technological challenges that need to be addressed to expand the application domain, such as defectivity, metrology, design challenges, and costs.

This panel aims to summarize the recent advancements in hybrid bonding, identify the most pressing issues limiting the adoption of this technology for mainstream electronics, and outline the expected development of this technology for the next decade.

Sujin Ahn, Samsung Electronics; Brett Wilkerson, AMD; Chet Lenox, KLA Corporation; Anne Jourdain, imec; Masao Tomikawa, Toray Industries, Inc.; Laura Mirkarimi, Adeia

2025 Special Session on Quantum Packaging

Quantum Photonic Advanced Packaging

Tuesday, May 27, 2025, 10:30 a.m. – 12:00 p.m. • Texas C

Chairs: Richard Pitwon, Resolute Photonics Ltd. and Ajey Jacob, University of Southern California


As quantum technologies advance, the need for robust and scalable systems to support applications like Quantum Key Distribution (QKD) and quantum photonic computation becomes increasingly critical. These emerging technologies demand a sophisticated ecosystem capable of integrating high-fidelity quantum photonic systems into the quantum physical layer, where single or entangled photon qubits are conveyed and processed. Quantum photonic systems, by their nature, require exceptional precision and control at the quantum level, which necessitates the heterogeneous integration of diverse materials and technologies into a cohesive unit that functions seamlessly. This integration is vital for ensuring the accurate transmission and manipulation of quantum information, which is the cornerstone of quantum computing and secure quantum communication. In this session, we will explore the latest advances in the assembly and packaging of quantum photonic systems. The focus will be on how innovative packaging solutions can address the unique challenges posed by quantum technologies, such as minimizing photon loss, ensuring thermal stability, transduction schemes, and maintaining the coherence of quantum states. We will discuss how these packaging techniques are being developed to support the high volume manufacturing of quantum devices, enabling their widespread adoption of data centric industries.

Andre Meek, Senko; Michael Fanto, Air Force Research Lab; Takahiro Kashiwazaki, NTT; Inna Krasnokutska, Xanadu Quantum Technologies Inc.

2025 Special Session on Glass Core vs. RDL Interposers

Glass Core vs. RDL Interposers: Ready for Prime-Time?

Tuesday, May 27, 2025, 10:30 a.m. – 12:00 p.m. • Texas 1–3

Chairs: Jan Vardaman, TechSearch International, Inc., Zia Karim, Yield Engineering Systems, and Thom Gregorich, Zeiss



Given the critical role of high-density substrates in the semiconductor industry, glass-core substrates and RDL interposer advantages have been discussed. With growing demand for higher performance, larger devices, and increased interconnect density, where does each technology fit, and what are the necessary steps to address the critical challenges faced by the entire industry?

This session will address economic and technical perspectives for high volume solutions, including design, materials, process/equipment, and metrology to meet product needs and reliability requirements. The session will include a moderator and six panelists.

Brett Wilkerson, AMD; Kathy Yan, TSMC; Duan Gang, Intel Corp.; Richard Bae, Samsung; Akira Tamura, FICT; Makoto Kouzuma, Toppan

2025 Special Session on Advanced Materials for Co-Packaged Optics

Advanced Materials for Enabling Co-Packaged Optics Integration

Tuesday, May 27, 2025, 1:30 p.m. – 3:00 p.m. • Texas C

Chairs: Vidya Jayaram, Chipletz and Karan Bhangaonkar, Google


Modern computing techniques are pushing the boundaries for high performance requirements. Co-packaged optics emerged as the future of microelectronics packaging, integrating optics and electronics on a single substrate, to meet the computing and communication demands for high bandwidth at low power. Although there are numerous challenges in realizing the optical co-packaging technology, what comes along are great opportunities for foundries, IDMs and OSATs. Materials and processes play a key role in enabling this disruptive technology. Thus, this special session will invite industry leaders to share their insight about the innovations, challenges and future needs in realizing CPO technology.

Christopher Striemer, AIM Photonics; Padraic Morrissey, Tyndall Institute; Mark Gerber, ASE; Kumar Abhishek Singh, Intel; Rena Huang, Rensselaer Polytechnic Institute

2025 Special Session on Fault and Failure Analysis in Chiplets

Advances in Chiplets: Tackling Fault Isolation and Failure Analysis in Heterogeneous Integration

Tuesday, May 27, 2025, 1:30 p.m. – 3:00 p.m. • Texas 1–3

Chairs: Yan Li, Samsung; Tae-Kyu Lee, Cisco Systems, Inc.; and Zhi Yang, Groq



By providing timely feedback data for effective failure root cause investigation, problem solving proposal and validation, process technology improvement, yield enhancement, and reliability risk assessment, fault isolation (FI) and failure analysis (FA) play a crucial role during the technology development of heterogeneous integration, which is the leading advanced packaging technology developed to meet the high-performance computing (HPC) and artificial intelligence (AI) market demands of ever higher performance, lower power consumption, and wider memory bandwidth with reduced latency. During the panel discussion, experts from both industry and academia will discuss the technology gaps and novel methodologies and techniques in FI and FA of heterogeneous integration.

Lihong Cao, ASE; Wenbing Yun, Sigray; Bernice Zee, AMD Singapore; Martin Igarashi, TaraView; Navid Asadi, University of Florida; Thomas Rodgers, Zeiss

2025 Special Session on Sub-THz Packaging

Advancements in mmWave and Sub-THz Packaging for Communication and Radar Applications

Tuesday, May 27, 2025, 3:30 p.m. – 5:00 p.m. • Texas C

Chairs: Maciej Wojnowski, Infineon Technologies AG and Ivan Ndip, Fraunhofer IZM/Brandenburg University of Technology


In this session, experts from industry and academia will present the latest developments in high-frequency packaging and system integration at mmWave and sub-THz frequency bands. The session will begin with presentation of emerging wireless communication and radar sensing applications in these bands, and resulting challenges and opportunities for RF packaging. Advanced system integration platforms using different

high-frequency materials for these applications will be presented. Emphasis will be laid on characterizing the packaging materials and interconnects at these very high frequencies as well as on co-design and co-simulation techniques. The session will conclude with presentation and discussion of concrete examples of latest developments of novel interconnects, components and wireless modules for 6G communication and radar applications at mmWave and sub-THz bands.

Madhavan Swaminathan, Penn State University; Xiao Sun, imec; Parisa Aghdam, Ericsson; Atom Watanabe, IBM T.J. Watson Research Center; CP Hung, ASE Group

2025 Special Session on Thermal Management for Power Delivery

Thermal Management Solutions for Next-Generation Backside Power Delivery

Tuesday, May 27, 2025, 3:30 p.m. – 5:00 p.m. • Texas 1–3

Chairs: Dwayne Shirley, Marvell Semiconductor, Inc. and Tiwei Wei, Purdue University


The increasing power density and thermal challenges in advanced semiconductor packaging have led to the development of backside power delivery (BPD) technology. BPD relocates the power delivery network from the frontside to the backside of a silicon wafer, enhancing power efficiency, performance, and design flexibility. However, this technology also introduces new thermal management challenges, including higher thermal densities and the need for innovative cooling solutions.

This special session aims to bring together experts from academia and industry to discuss the latest advancements and challenges in thermal management solutions for next-generation BPD.

Dureseti Chidambarrao, IBM; Muhannad S Bakir, Georgia Tech; Herman Oprins, imec; Rongmei Chen, Peking University

2025 IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 27, 2025, 8:00 a.m. – 5:00 p.m. • Texas D

Chairs: Ravi Mahajan, Intel Corporation and William Chen, ASE


8:00 a.m. – 8:30 a.m.: HIR Welcome, Introduction & Agenda Review

8:30 a.m. – 10:00 a.m.: IoT & AI at the Edge

10:30 a.m. – 12:00 Noon: Advancing HI Through Metrology & AI

1:30 p.m. – 3:00 p.m.: Integrating Photonics in HPC & Network Systems

3:30 p.m. – 5:00 p.m.: HIR Session With Joint Participation by IPC: Components to System – Integration Needs, Gaps, Challenges, Solutions

2025 ECTC Young Professional Networking Event

Tuesday, May 27, 2025, 6:45 p.m. – 7:45 p.m. • Texas C

Chairs: Aakrati Jain, IBM; Rui Chen, Eastern Michigan University; Zhangming Zhou, Independent Consultant



Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior IEEE EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2025 IEEE EPS Seminar on Chiplet Technology

User Perspective of Chiplet Technology

Tuesday, May 27, 2025, 7:45 p.m. – 9:15 p.m. • Texas A–B

Chairs: Takashi Hisada, Rapidus and Yasumitsu Orii, Rapidus


The EPS Seminar organized by the technical committee TC6 (High-Density Substrate and Board) of IEEE EPS will discuss the current status and future evolution of chiplet technology from the end use perspective. We will have six panelists from various segments such as high-end computing, automotive and network. Each panelist will give a short talk presenting insights on technical trends/challenges including optically integrated chiplet, application requirements, user's expectation of chiplet technology, followed by a panel discussion.

Raja Swaminathan, AMD; Takao Iwaki, ASRA (MIRISE Technologies); Takashi Saida, NTT; Omar Bchir, Qualcomm; Carlos Macian Ruiz, Marvell; Sam Karikalan, Broadcom

2025 ECTC Keynote Talk

Achieving Efficient Zettascale Compute in the AI Era

Wednesday, May 28, 2025, 8:00 a.m. – 9.15 a.m. • Texas A–B

Chair: Florian Herrault, PseudolithIC Inc.

Speaker: Sam Naffziger, AMD


The demand for compute and the energy to power it is increasing faster than ever before in our industry. Meeting the challenge of delivering this processing power in the AI era requires holistic innovation from the device to the datacenter level. It starts with integrating highly optimized, domain-specific accelerators with advanced 2.5D and 3.5D packaging to maximize the amount of compute within the most efficient, local communication domain. These accelerators and other system components must be packed into tightly integrated sleds that minimize losses and power for high-speed communication while taking advantage of workload-aware power management. Scaling to the rack and datacenter level will require many advances in signaling technologies, rack design, and power optimization to enable the training and inference computation required by the most demanding frontier models. This talk will cover these trends and key technologies that will power compute growth at a scale we wouldn't have conceived of just a few short years ago.

2025 ECTC Student & Start-Up Innovation Challenge

Future Forward: The Student & Start-up Innovation Challenge!

Wednesday, May 28, 2025, 6:30 p.m. - 8:30 p.m. • Texas A–B

Chairs: Rozalia Beica, Rapidus, Farhang Yazdani, BroadPak, and Jason Rouse, Taiyo America, Inc.



This session is organized as a competition and will have competing pitches of both student teams and start-ups followed by deliberation of a jury panel, awards announcements, and networking session. We will have three student pitches and six start-up pitches (7 min. each) followed by Q&A from the jury panel. The Q&A will be open to the audience. The jury will deliberate and choose the winning student team and start-up. The session will end with the announcement of the winners and a networking session.

Startup competitors: Adrian Lopez Vasquez, Micro Quasar Tech; Patrick Heissler, Scrona; Sanjive Agarwala, EuQlid; Juniyali Nauriyal, Photonect; David Morris, ICSPI

Jury panel: Yik Yee Tan, Yole Group; Martin Pierik, Kiterocket; Yvonne Lutsch, LAM CVC; John Wei, Applied Ventures; Henry Huang, Micro Ventures; Paul Pickering, Silicon Catalyst

2025 Plenary Session on Advanced Power Delivery for AI

Emerging Advanced Power Delivery for the AI Computing Era

Thursday, May 29, 2025, 8:00 a.m. – 9:15 a.m. • Texas A–B

Chairs: Dongming He, Qualcomm and Eric Beyne, imec


AI computing introduces significant challenges for energy consumption and thermal management. Optimal power delivery network (PDN) is crucial for CPU, GPU and NPU power and performance. Advanced PDN solutions such as silicon deep trench capacitor (DTC) and integrated stacked capacitor (ISC), integrated voltage regulator (IVR), silicon metal-insulator-metal (MIM) capacitor and thin film inductor, backside power rail, etc., have been explored, developed, and adopted. Industry leaders and experts will share their views on benefit and tradeoff for these building blocks, integration challenges, and opportunities at silicon device, package, and board levels plus system technology co-optimization (STCO).

Kaladhar Radhakrishnan, Intel Corp.; Harrison Chang, ASE Global; PR. Chidi Chidambaram, Qualcomm; Raja Swaminathan, AMD; Chuei-Tang Wang, TSMC

2025 IEEE EPS President's Panel

ECTC at 75: Celebrating the Past, Innovating for the Future

Friday, May 30, 2025, 8:00 a.m. – 9:15 a.m. • Texas A–B

Chair: Patrick Thompson, Texas Instruments

Join EPS/ECTC luminaries as they share:

- Early memories of ECTC and key innovations that revolutionized the industry
- What's happening now that is exciting to them
- Their thoughts on what we'll be reviewing at the 100th ECTC

Rao Tummala, Emeritus Professor, Georgia Institute of Technology; John Lau, Unimicron; William Chen, ASE; Kitty Pearsall, Capstan Technologies

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 27, 2025

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Dallas 7 **1. High Reliability Soldering in Semiconductor Packaging** *Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech*	Texas 6 **9. 3D Packaging Failure Analysis – Failure Mechanisms and Analytical Tools** *Course Leader: Deepak Goyal – Independent Consultant*
Texas 5 **2. Photonic Technologies for Communication, Sensing, and Displays** *Course Leader: Torsten Wipiejewski – Huawei Technologies*	Texas 5 **10. Diamond for Heterogeneous Integration** *Course Leader: Joana Mendes – University of Aveiro*
Texas 6 **3. From Wafer to Panel Level Packaging** *Course Leaders: Tanja Braun and Piotr Mackowiak – Fraunhofer IZM*	Texas 4 **11. Chiplet, Heterogeneous Integration, and Co-Packaged Optics** *Course Leader: John Lau – Unimicron*
Dallas 5 **4. Eliminating Failure Mechanisms in Advanced Packages** *Course Leader: Darvin Edwards – Edwards Enterprises*	Dallas 5 **12. Analysis of Fracture and Delamination in Microelectronic Packages** *Course Leader: Andrew Tay – National University of Singapore*
Dallas 6 **5. Introduction to and Advances in 2.3D Fan-Out Wafer Level Packaging (FO-WLP)** *Course Leader: Beth Keser – Zero Asic*	Dallas 6 **13. Advanced Fan-Out Developments and Applications** *Course Leaders: John Hunt and Jan Vardaman – TechSearch International*
Texas 4 **6. Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Advanced Interconnects** *Course Leader: Viorel Dragoi – EV Group E. Thallner GmbH*	Dallas 7 **14. Flip Chip Technologies** *Course Leader: Shengmin Wen – TATA Electronics*
San Antonio 5 & 6 **7. Fundamentals of Fabrication Processes and RF Design of Advanced Packages Including Fan-Out, Chiplets, Glass and Polymer Interposers** *Course Leaders: Ivan Ndip – Brandenburg University of Technology & Fraunhofer IZM and Markus Wöhrmann – Fraunhofer IZM*	San Antonio 5 & 6 **15. Design-on-Simulation for Advanced Packaging: Warpage Management, Reliability and Life Prediction** *Course Leaders: Kuo-Ning Chiang – National Tsing Hua University and Xuejun Fan – Lamar University*
San Antonio 4 **8. Design of Reliable Data Center Cooling Systems** *Course Leaders: Patrick McCluskey – University of Maryland and Damena Agonafer – University of Maryland*	San Antonio 4 **16. Current and Future Challenges and Solutions in AI & HPC System and Thermal Management** *Course Leader: Gamal Refai-Ahmed – AMD*

Refreshment Breaks
10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Texas 4-6 Foyer

COMMITTEE MEETINGS

ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 27, 2025

7:00 a.m – 8:00 a.m.
EPS Reliability TC
Dallas 3

7:00 a.m – 8:00 a.m.
EPS Power TC
San Antonio 1

8:00 a.m. – 5:30 p.m.
EPS HIR Workshop
Texas D

9:00 p.m. – 10:30 p.m.
ECTC Photonics Committee
San Antonio 3

9:00 p.m. – 10:30 p.m.
ECTC Interconnections Committee
Dallas 3

Wednesday, May 28, 2025

7:00 a.m. – 8:00 a.m.
EPS EDMS TC
Dallas 3

7:00 a.m. – 8:00 a.m.
EPS High Density Substrate Boards TC
San Antonio 1

7:00 a.m. – 8:00 a.m.
EPS Materials & Processes TC
San Antonio 2

7:00 a.m. – 8:00 a.m.
EPS Photonics TC
San Antonio 3

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
Dallas 3

Thursday, May 29, 2025

7:00 a.m. – 8:00 a.m.
EPS Chapter Chairs Meeting
Dallas 3

7:00 a.m. – 8:00 a.m.
EPS Emerging Technology TC
San Antonio 1

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
San Antonio 2

7:00 a.m. – 8:00 a.m.
EPS Nanotech TC
San Antonio 3

8:30 a.m. – 10:00 a.m.
EPS Conference Organizers
San Antonio 3

4:30 p.m. – 6:00 p.m.
EPS BoG Information Session
San Antonio 2–3

5:30 p.m. – 6:30 p.m.
ECTC 2025 Program Committee Meeting
Texas 4–6

6:30 p.m. – 7:30 p.m.
ECTC Program Subcommittee Chairs & Assistant Chairs Reception (by invitation only)

9:30 p.m.
75th ECTC Governing/ Executive Committee Reception (by invitation only)

Friday, May 30, 2025

7:00 a.m. – 8:00 a.m.
EPS RF & THz Technology TC
Dallas 3

7:00 a.m. – 8:00 a.m.
EPS 3D/TSV TC
San Antonio 3

9:00 a.m. – 10:00 a.m.
EPS T-CPMT SAEs/AEs
San Antonio 3

2:15 p.m. – 4:45 p.m.
ECTC Executive Committee
San Antonio 2 & 3

5:00 p.m. – 6:00 p.m.
ECTC / EPS Steering Committee
San Antonio 2 & 3

ECTC 2024 BEST PAPER AWARDS

BEST SESSION PAPER

Advanced Thermocompression Bonding on High Density Fan-Out Embedded Bridge Technology for HPC/AI/ML Applications

Wiwy Wudjud, Lihong Cao – ASE Austin; ShuYu Lin, Yungshun Chang, Jean Yen, Reno Liao, LeoHS Cheng, Yihsien Wu, Simon YL Huang, Jui Tzu Chen, ChengYu Lee, JoeyCl Huang – ASE Kaohsiung

BEST INTERACTIVE PRESENTATION PAPER

A Novel Plasma Etching Technology of RIE-Lag Free TSV and Dicing Processes for 3D Chiplets Interconnect

Taichi Suzuki, Kenta Doi, Toshiyuki Nakamura, Yasuhiro Morikawa – ULVAC Susono

OUTSTANDING SESSION PAPER

3-Layer Fine Pitch Cu-Cu Hybrid Bonding Demonstrator With High-Density TSV for Advanced CMOS Image Sensor Applications

Stéphane Nicolas, Jerzy-Javier Suarez-Berru, Nicolas Bresson, Carole Socquet-Clerc, Myriam Assous, Stéphan Borel, Rémi Vélard, Jérôme Dechamp, Renan Bouis, Antonio Roman, Karine Abadie, Damien Hebras – CEA-Leti, Grenoble Alpes University

OUTSTANDING INTERACTIVE PRESENTATION PAPER

Optimization of Core Material Properties for Large Flip-Chip Ball Grid Array Substrate to Manage Both Warpage and Board Level Reliability

Hirokazu Noma, Masaki Takahashi, Nene Hatakeyama, Yuichi Yanaka, Akito Fukui, Keita Johno, Hitoshi Onozeki – Resonac Corporation

INTEL BEST STUDENT PAPER

In Situ Analysis of Copper Microstructures in Electromigration Using SEM-EBSD Techniques

Yaqian Zhang, Yixin Yan, Sten Vollebregt, Guoqi Zhang – Delft University of Technology

INTEL OUTSTANDING STUDENT PAPER AWARD

Performance Evaluation of UCIe-based Die-to-Die Interface on Low-Cost 2D Packaging Technology

Srujan Penta – Georgia Institute of Technology; Marvell Burlington; Ting Zheng, Marvell Santa Clara; Eric Tremble, Aatreya Chakravarti, Anthony Sigler, Carl Benes, Wolfgang Sauter – Marvell; Zhonghao Zhang, Muhannad S. Bakir – Georgia Institute of Technology

TI BEST IP STUDENT PAPER

Deep Reinforcement Learning-Based Power Distribution Network Design Optimization for Multi-Chiplet System

*Weiyang Miao, Zhen Xie, Chuan Seng Tan – Nanyang Technological University; Mihai Dragos Rotaru – IME A*STAR*

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PROGRAM SESSIONS: WEDNESDAY, MAY 28, 9:30 A.M. - 12:35 P.M.

Session 1: Processing and Packaging Articles for 3D Integration	Session 2: Co-Packaged Optics	Session 3: Hybrid Bonding Materials and Processing for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Photonics**	**Committee:** **Materials & Processing**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Subhash L. Shinde - Notre Dame University** **Email: sshinde@nd.edu** **Peng Su - Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs** **Soon Jang – ficonTEC USA** **Email: soon.jang@ficontec.com** **Hiren Thacker – Cisco Systems, Inc.** **Email: hithacke@cisco.com**	**Session Co-Chairs** **Vidya Jayaram – Chipletz** **Email: vidya.jayaram@chipletz.com** **Hongbin Yu – Arizona State University** **Email: Hongbin.Yu@asu.edu**
1. 9:30 AM - SoW-X: A Novel System-on-Wafer Technology for Next Generation AI Server Application *Po-Chang Shih, An-Jhih Su, Tze-Chiang Huang, King-Ho Tam – Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 9:30 AM - Heterogeneous Integration of Fiber-Based Co-Packaged Optics With EMIB Technology: Assembly, Performance, and Reliability*** *Kumar Abhishek Singh, Ziyin Lin, Peter Williams, Darren Vance, Joel Wright, Bilas Chowdhury, Todd Coon, Shahin Mani – Intel Corporation*	***1. 9:30 AM - Morphological Microstructure Characterization and Optimization of Nanocrystalline Copper Deposition for Fine-Pitch Hybrid Bonding Cu/SiO2 at Low Temperature.*** *Mathieu Loyer, Emilie Deloffre – ST Microelectronics; Maria-Luisa Calvo-Munoz, Marie Maubert, Mathilde Gottardi, Pierre-Emile Philip, Gilles Romero – CEA-LETI*
2. 9:50 AM - Face-Down Bonding and Heterogeneous Chiplet Integration by Using Bumpless Chip-on-Wafer (COW) With Waffle Wafer Technology *Yoshiaki Satake, Tatsuya Funaki, Takayuki Ohba – Institute of Science Tokyo; Wataru Doi – Murata Manufacturing Co., Ltd.; Shogo Okita, Hajime Kato – Panasonic Connect Co., Ltd.*	***2. 9:50 AM - 6.4Tbps, 224Gbps/Lane Co-Packaged Optical Engines With Fine Pitch Through-Package Interconnects: Powering AI/ML and Next-Gen Data Centers*** *BG Sajay, Jia Qi Wu, Rathin Mandal, Sandra San, Surya Bhattacharya – Institute of Microelectronics A*STAR; Li Xin, Jason Tsung-Yang Liow – Rain Tree Photonics Pte. Ltd.*	***2. 9:50 AM - Wafer-to-Wafer Bonding With Ultralow Thermal Resistance and High Bonding Energy*** *Wenhao (Eric) Li, Feras Eid, Andrey Vyatskikh, Richard Vreeland, William Brezinski, Michael Njuki, Christopher Jezewski, Rajiv Mongia, Krishna Vasanth Valavala, Hao Mei, Chaitanya Bakre – Intel Corporation*
3. 10:10 AM - Electrical Properties and Reliability of Back-Side Redistribution Layers Based on Inorganic Dielectrics in 3D Stacked Memory Packages *Jongyeon Kim, Jaecheol Shim, Sungkyu Kim, Seungchul Han, Hoyoung Son, Kangwook Lee – SK hynix Inc.*	***3. 10:10 AM - Flip-Chip Photonic-Electronic Integration Platform for Co-Packaged Optics Using a Glass Substrate With Vertically-Coupled Beam Expanding Lens*** *Yasutaka Mizuno, Kunio Kobayashi, Shingo Nakamura, Masaki Migita, Hajime Arao, Tetsuya Nakanishi, Hiroshi Uemura, Keiji Tanaka, Katsumi Uesaka – Sumitomo Electric Industries, Ltd.; Mami Miyairi, Yoshikatsu Ishizuki – FICT LIMITED; Yoichiro Kurita – Institute of Science Tokyo*	***3. 10:10 AM - Novel Polymer for Hybrid Bonding With Precise Tunable Crosslink Density*** *Shintaro Nagayama, Ryo Sugano, Tetsuya Ogawa, Hiroyoshi Deguchi, Eisaku Ishikawa, Hiroshi Nakagawa – Resonac Corporation*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Longhorn D		
4. 11:15 AM - A Novel 3D Heterogeneous Integration Using 2 µm Bond Pitch Die-to-Wafer Hybrid Cu Bonding and Wafer Reconstruction Process *Pilkyu Kang, Jaejin Lee, Moonkeun Kim, Eunmi Kim, Kyu-Ha Lee, Chanmi Lee, Jaehwa Park, Minwoo Rhee – Samsung Electronics Co., Ltd.*	***4. 11:15 AM - Optical and Electrical Characterization of a Compact Universal Photonic Engine*** *Ming-Fa Chen, Hao-Tien Cheng, Chia-Han Tsou, Shang-Yun Hou, Ryan Lu, Kuo-Chin Hsu, T. H. Yu, Scott Liu – Taiwan Semiconductor Manufacturing Company, Ltd.*	***4. 11:15 AM - Hybrid Bonding With Particle Accommodation Using Polymer Dielectric: Design, Process and Yield Study*** *Ling Xie, Ser Choong Chong, Nagendra Sekhar Vasarla – Institute of Microelectronics A*STAR; Yu Shoji, Masaya Jukei, Kota Nomura, Takenori Fujiwara, Hitoshi Araki – Toray Industries, Inc.*
5. 11:35 AM - Enabling Chip-to-Wafer Hybrid Bonding Scaling to 1 µm Pitch With Optimal Power Delivery Using New Bond Via Architectures *Golsa Naderi, Adel A Elsherbini, Brandon Rawlings, Saurabh Chauhan, Qiang Yu, Arian Rahimi, Shawna Liff, Cynthia Cooper, Theodros Bejitual, Phanindhar Shivapooja, Matthew Stolt, Md Imran Hossain, Cemil M. Atay – Intel Corporation*	***5. 11:35 AM - Large-Scale Glass Waveguide Circuit for Board-Level Optical Interconnects Between Faceplate and Co-Packaged Optical Transceivers*** *Lars Brusberg – Corning, Inc.; Betsy Johnson, Jason Grenier, Matthew Dejneka, Chad Terwilliger – Corning Research and Development Corp.; Julian Schwietering, Christian Herbst, Henning Schroeder – Fraunhofer IZM*	***5. 11:35 AM - Characterization of Self-Nanoparticulated Cu-Cu Interconnection for Low-temperature Hybrid Bonding*** *Ryotaro Kawashima, Bungo Tanaka, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Hirokatsu Sakamoto – Daicel Corporation*
6. 11:55 AM - Fluxless Thermocompression Bonding: Adapting to the Future *Jonathan Abdilla, Martin Kainz, Benedikt Pressl, Mario Fraubaum – Besi NL; Jaber Derakhshandeh – imec; Chris Scanlan – Besi Switzerland*	***6. 11:55 AM - All-SMF Arrays for Co-Packaged Optics: Optimizing Cost, Complexity, and Performance*** *Nandish Mehta – Nvidia Corporation*	***6. 11:55 AM - AlN Gap-Fill Process by Aerosol Deposition Method for Application in 3D-IC Packaging*** *Takeki Ninomiya, Takeshi Takagi, Tadahiro Kuroda – University of Tokyo; Masakazu Mori – Ryukoku University; Masaaki NIWA – The University of Tokyo*
7. 12:15 PM - Integration Solution for Thin D2W Hybrid Bonding for Yield and Reliability *Xiaodong Chen, Guan Huei See, Patrick Lim, Prayudi Lianto, Peng Suo, Andy Yong, Santosh Kumar Rath, Xing Zhao – Applied Materials, Inc.*	***7. 12:15 PM - A +21-dBm per Channel Operation of a 16-Channel CWDM ELSFP Module in Practical Air-Cooling Conditions*** *Kohei Umeta, Taketsugu Sawamura, Yuki Shiroishi, Maaya Tsukamoto, Hideyuki Nasu – Furukawa Electric Co., Ltd.*	***7. 12:15 PM - Effect of Grain Size on Cu-Cu Bonding Quality for Fine-Pitch Hybrid Bonding Application*** *Chen-Ning Li, Chih Chen – National Yang Ming Chiao Tung University*

PROGRAM SESSIONS: WEDNESDAY, MAY 28, 9:30 A.M. - 12:35 P.M.

Session 4: Large Package Manufacturing and Panel Level Processing	Session 5: Advanced Design for Heterogeneous Integration	Session 6: AI - ML and Emerging Modeling Methods
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Zia Karim – Yield Engineering Systems** **Email: zkarim@yes.tech** **Jason Rouse – Taiyo America, Inc.** **Email: jhrouse@taiyo-america.com**	**Session Co-Chairs** **Ivan Ndip – Brandenburg University of Technology/ Fraunhofer IZM / Email: Ivan.Ndip@izm.fraunhofer.de** **Li-Cheng Shen – Miniaturization Competence Center (MCC), USI / Email: li-cheng_shen@usiglobal.com**	**Session Co-Chairs** **Pradeep Lall – Auburn University** **Email: lall@auburn.edu** **Guangxu Li – Texas Instruments, Inc.** **Email: guangxu3559@gmail.com**
1. 9:30 AM - Package Warpage Reduction for Large CoWoS-R Packages *Yu-Hsiang Hu, Chien-Hsun Lee, Jyun-Siang Peng, Hsin-Yu Chen, Pei-Hsuan Lee, Jowett Li, Cheng-Chi Hsieh, Eric Chen, Ming-Chih Yew, Kathy Yan, Jun He, Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 9:30 AM - Enabling 20 Tb/s/mm Die-to-Die Bandwidth Density With Advanced Packaging Technologies*** *Zhiguo Qian, Kemal Aygun – Intel Corporation*	***1. 9:30 AM - NAND Package Warpage Prediction and Design With Tolerance Through Machine Learning*** *Min Lin, Chaolun Zheng, Yuhang Yang, Ning Ye, Bo Yang – Western Digital Corporation*
2. 9:50 AM - Process Development and Reliability Investigation of 120 mm x 120 mm Large 2.5D Package With Low Melting Temperature Solder *Kazue Hirano, Dongchul Kang, Masaki Takahashi, Motoo Aoyama, Yuji Inui, Sadaaki Katoh – Resonac Corporation*	***2. 9:50 AM - Quantifying Signal Return Path Imperfections on Eye Aperture in Die-to-Die Communication*** *Nicolas Izquierdo, Jiawei Zhang, Manoj Rafalia, Eric Foronda, Chan Qian, Gerardo Romo – Qualcomm Technologies, Inc.; Jaimeen Shah – Qualcomm India Pvt. Ltd.*	***2. 9:50 AM - Compact Models for Nonlinear Thermo-Mechanical Simulations of Chiplets in Automotive*** *Mike Manuel Feuchter, Hanna Baumgartl, Martin Hanke – CADFEM GmbH; Bragadesh Srivatsan, Przemyslaw Gromala – Robert Bosch GmbH; Ghanshyam Gadhiya, Sven Rzepka – Fraunhofer ENAS*
3. 10:10 AM - New Silicon Capacitor Solutions With Over 1mm -Thick Core Based Embedded Substrate for Extremely Large Package Platform *Kyojin Hwang, Woobin Jung, Sunghawn Bae, Kisu Joo, Junso Pak, Heeseok Lee – Samsung Electronics Co., Ltd.*	***3. 10:10 AM - Design and Optimization of High-Speed Packages for the Chiplet Era*** *Meenakshi Upadhyaya, Srikrishna Sitaraman, Chander Ravva, Arshiya Vohra, Roxana Vladuta, Luciana Chitu, Ting Zheng – Marvell Technology, Inc.*	***3. 10:10 AM - Peridynamics Enabled Digital Image Correlation for Small Scale Defect Detection*** *Amin Yaghoobi – Global Engineering Research and Technologies; Erdogan Madenci – University of Arizona; Qi Tang, Mostafa Hassani – Cornell University*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Longhorn D		
4. 11:15 AM - Board-Level Assembly Challenges and TIM Selections for the Large-Size FCBGA Packages *Chengjian Wang, Yangfan Zhong, Xianfeng Chen, Yangyang Xu, Chunjia Sun – Alibaba Group; Wenchao Wang – Fudan Research Institute in Jiashan; Chuan Chen – Chinese Academy of Science-Institute of Microelectronics; Delong Qiu – Jiashan Fudan Research Institute*	***4. 11:15 AM - Power Integrity and Circuit Characteristics of Integrated Voltage Regulator (IVR) in CoWoS® Advanced Packaging Technology*** *Chuei-Tang Wang, Yen-Ming Chen, Yuhuan Chen, Shu-An Shang, Yu-Ming Hsiao, Kai-Yi Tang, Kuo-Ching Hsu, Ching-Hui Chen, Mirng-Ji Lii, Kam Heng Lee, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.*	***4. 11:15 AM - DiffChip: Fast Chiplets Design by Automatic Differentiation*** *Giuseppe Romano – Massachusetts Institute of Technology; Nima Dehmam, Xin Zhang, Arvind Kumar, Cheng Chi, Aakrati Jain – IBM Corporation*
5. 11:35 AM - Yield Prediction Technology: A Game Changer for Cutting Costs and Reducing Ramp Time in FOPLP Lithography *John Chang, Keith Best, Jian Lu, Timothy Chang – Onto Innovation*	***5. 11:35 AM - Multi-Chiplet Power Delivery Network Co-Optimization Considering Current Spectrum by Deep Reinforcement Learning-Based Decoupling Capacitor Placement*** *Haeseok Suh, Taesoo Kim, Hyunjun An, Haeyeon Kim, Seonguk Choi, Keeyoung Son, Keunwoo Kim, Jiwon Yoon, Byeongmok Kim, Youngsu Yoon, Jaegeun Bae, Joungho Kim – Korea Advanced Institute of Science and Technology*	***5. 11:35 AM - Support Vector Algorithm-Driven Simulation for Predicting Mechanical Performance in High-Power Modules*** *Chang-Chun Lee, Jui-Chang Chuang, Wei-Cheng Tsai, Yan-Yu Liou – National Tsing Hua University*
6. 11:55 AM - Glass-Core Advanced Packaging Substrate Post-Dicing Die Strengths Comprehensive Comparisons for Different Singulation Methods - Dicing Induced SeWaRe Failures Re-Visited Ten Years Later *Frank Wei, Andrew Frederick – DISCO Corporation*	***6. 11:55 AM - RF Si Interposer Platform for Advanced Chiplet-Based Heterogeneous Systems*** *Xiao Sun, Siddhartha Sinha, Hamideh Jafarpoorchekab, Melina Lofrano, Vladimir Cherman, Damien Leech, Angel Uruena – imec; Martijn Huynen – Ghent University*	***6. 11:55 AM - Advanced Numerical Modeling of Microstructure Effect on Fine Cu Redistribution Lines Under Electric Current Stressing*** *Tai-Yu Pan, Wen-Dung Hsu – National Cheng Kung University; Min-Yan Tsai, Yung-Sheng Lin, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)*
7. 12:15 PM - Fundamental Transmission Performance Evaluation of Sub-2 Micron Fine-Wiring on Glass Core Substrate *Masaya Tanaka, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.*	***7. 12:15 PM - A Heterogeneous Integrated Low Noise Amplifier With High-Q Si-Interposer Inductor for Dual (Ka/V)-Band Millimeter Wave Applications*** *Mei Sun – Institute of Microelectronics (IME), Dan Lei Yan, Jun Wei Ong, Pei Siang Lim, Binte Kuyob Nur, Jia Qi Wu, Yong Liang Ye, Teck Guan Lim, T.C. Chai – Institute of Microelectronics A*STAR*	***7. 12:15 PM - Deep Clustering Based Boundary-Decoder Net for Inter and Intra Layer Stress Prediction of Heterogeneous Integrated IC Chip*** *Kart Leong Lim, Ji Lin – Institute of Microelectronics A*STAR*

PROGRAM SESSIONS: WEDNESDAY, MAY 28, 2:00 P.M. - 5:05 P.M.

Session 7: High Performance Computing and Design Challenges and Solutions	Session 8: Novel Structures and Processes for Chip-to-Wafer Hybrid Bonding	Session 9: Co-Packaged Optics and Hybrid Bonding Innovations for HI
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Monita Pau – Onto Innovation** **Email: monita.pau@ontoinnovation.com** **Eric Tremble – Marvell Technology, Inc.** **Email: etremble@marvell.com**	**Session Co-Chairs** **Katsuyuki Sakuma – IBM Research** **Email: ksakuma@us.ibm.com** **Dingyou Zhang – Broadcom, Inc.** **Email: dingyouzhang.brcm@gmail.com**	**Session Co-Chairs** **Jae Kyu Cho – GlobalFoundries, Inc.** **Email: jaekyu.cho@globalfoundries.com** **Mark Poliks – Binghamton University** **Email: mpoliks@binghamton.edu**
1. 2:00 PM - Fine Pitch High Density CoWoS-R Package With 1.4/1.4 µm RDL Lines and 3 µm via CD *Kathy Yan, Yu-Hsiang Hu, Chien-Hsun Lee, Hsin-Yu Chen, Monsen Liu, Eric Chen, Ming-Chih Yew, Chia-Kuei Hsu, Jun He, Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 2:00 PM - 2 µm Pitch Direct Die-to-Wafer Hybrid Bonding Using Surface Protection During Wafer Thinning and Die Singluation*** *Ye Lin, Pieter Bex, Samuel Suhard, Boyao Zhang, Fulya Ulu Okudur, Amaia Diaz De Zerio, Naveen Reddy, Efrain Altamirano Sanchez – imec*	***1. 2:00 PM - Demonstration of Co-Packaged Optics Assembly for Fiber-Based Optical Interconnect*** *Michael Baker, Jesus Nieto Pescador, Edidiong Udofia, Gustavo Beltran, Albert Lopez, Wei Gong, Abid Ameen, Jason Yao, Sunny Situ, Han Wang, Feifei Cheng, Feifei Cheng Vidya Jayaram– Intel Corporation*
2. 2:20 PM - Development of Embedded Multi Si Bridge Package in Panel Level Process for HPC/AI Applications *Hyeji Han, Jieun Park, Mijin Park, Jeongho Lee, Wonkyung Choi, Daewoo Kim – Samsung Electronics Co., Ltd.*	***2. 2:20 PM - Innovative SoIC® Cool-Stacking Technology to Overcome the Thermal Wall of Future High Performance Compute*** *Shih-Chang Ku, C.H. Tsai, Cheng-Chieh Hsieh, J.C. Twu, R.F. Tsui, S.W. Lu, C.S. Liu, Douglas C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.*	***2. 2:20 PM - Optical Multi-Chip Interconnect Bridge (OMIB™) Interposer Assembly Process to Enable High-Density Photonic Interconnects for High-Performance Computing Applications*** *Ankur Aggarwal, Suresh Pothukuchi, Subal Sahni – Celestial AI; Anmol Rathi, Phil Winterbottom, David Lazovsky – Celestial AI Inc.*
3. 2:40 PM - Self-Alignment of Active Si Bridge Using Solder Joint Capillary Forces *Thomas Lesueur, David Danovitch, Dominique Drouin – University of Sherbrooke; Isabel De Sousa, Divya Taneja – IBM Canada, Ltd.; Akihiro Horibe, Sayuri Kohara – IBM Research, Tokyo*	***3. 2:40 PM - Influences of Chip Shape on Scaling in Chip-on-Wafer Hybrid Bonding*** *Koki Onishi, Sotetsu Saito, Toru Osako, Takaaki Hirano, Takahiro Kamei, Naoki Ogawa, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation*	***3. 2:40 PM - Advanced Glass Substrate Fabrication and Metallization Process Technology for Co-Packaged Optics*** *Seong-Ho Seok, Bo-Kyung Kong, Kyeong-Gon Choi, Han-Yeom Lee, Jung-Hyun Noh – Corning Technology Center Korea; Lars Brusberg – Corning, Inc.*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Longhorn D		
4. 3:45 PM - BBCube 3D: Fully Vertical Heterogeneous Integration of DRAMs and xPUs Using a New Power Distribution Highway *Norio Chujo, Hiroyuki Ryoson, Koji Sakui, Shinji Sugatani, Masao Taguchi, Takayuki Ohba – Institute of Science Tokyo*	***4. 3:45 PM - Warpage Engineering in C2W Hybrid Bonding Using Inter-Die Gap Fill Dielectrics for 2.5D/3D Integration*** *Mishra Dileep, Nagendra Sekhar Vasarla, Hemanth Kumar Cheemalamarri, Jun Wei Javier Ong, Chandra Rao B. S. S., Ser Choong Chong, Vempati Srinivasa Rao, Sasi Kumar Tippabhotla – Institute of Microelectronics, A*STAR*	***4. 3:45 PM - Self-Formed Barrier Using Cu-Mn Alloy Seed Applied to a 400 nm Pitch Wafer-to-Wafer Hybrid Bonding Technology*** *Stefaan Van Huylenbroeck, Soon Aik Chew, Boyao Zhang, Emmanuel Chery, Joke de Messemaeker, Prafulla Gupta, Nicolas Jourdan, Sven Dewilde – imec*
5. 4:05 PM - EMIB-TSV Advanced Packaging Technology - EMIB™s Next Evolution *Gang Duan, Sid Alur, Jesse Jones, Mohammad Rahman, Yingying Zhang, Amey Anant Apte, Anil Chandolu, Robin McRee, Tarek Ibrahim, Sai Agraharam, Andrey Gunawan, Numair Ahmed, Xinyu Li, Rungmai Limvorapitux, Ravi Eluri, Rahul Manepalli, Yuxin Fang, Shruti Sharma, Manni Mo, Chandra Subramani, Sid Kumar – Intel Corporation; Johan Mousavi – Development, Intel Foundry*	***5. 4:05 PM - Direct Transfer Bonding Technology Enabling 50 nm Scale Accuracy for Die-to-Wafer 3D/Heterogeneous Integration*** *Ichiro Sano – TAZMO Co., Ltd.; Masanori Yamagishi, Shinya Takyu, Tomoka Kirihata – LINTEC Corporation; Ryoya Kitazawa – ULVAC, Inc.; Takafumi Fukushima – Tohoku University; Yoichiro Kurita – Tokyo Institute of Technology*	***5. 4:05 PM - SiCN CMP Integration for Hybrid Bonding Application*** *Prayudi Lianto, Rachel Emmanuelle Raphael, Avery Tan, Ching Keat Chia, Xiaobo Li, Hui Min Lee, Xiaodong Chen – Applied Materials, Inc.*
6. 4:25 PM - Co-Packaged Optics (CPO) Technology Full Module Test Vehicle Demonstrations *John Knickerbocker, Jean Benoit Heroux, Adrian Paz Ramos, Hsianghan Hsu, Neng Liu, Yoichi Taira, Mark Schultz – IBM Corporation; Chinami Marushima, Sayuri Kohara, Hidetoshi Numata – IBM Research; Hiroyuki Mori, Akihiro Horibe – IBM Research, Tokyo*	***6. 4:25 PM - Hierarchical Multi-layer and Stacking Vias With Novel Structure by Transferable Cu/Polymer Hybrid Bonding for High Speed Digital Applications*** *Ou-Hsiang Lee, Wei-Lan Chiu, Hsiang-Hung Chang, Shih-cheng Yu, Wei-Chung Lo, Chin-Hung Wang – Industrial Technology Research Institute; Chung-An Tan – Brewer Science, Inc.*	***6. 4:25 PM - Inter-Die Hybrid Cu/Diamond Microbump Bonding for 3D Heterogeneous Integration*** *Zhengwei Chen, Keyu Wang, Noah Opendo, Jie Li, Tiwei Wei – Purdue University; Shusmitha Kyatam, Joana Catarina Mendes, Miguel A. Neto, Ricardo Oliveira – University of Aveiro*
7. 4:45 PM - Signal, Power, and Thermal Integrity Co-Design for AI Accelerator ASIC and HBM3 on Silicon Interposer 2.5D-IC Chiplet Integration *Ming-Hung Wu, Chun-Hong Chen, Chi-Lou Yeh, Chi-Ming Yang, Eric Lin, Sheng-Fan Yang – Global Unichip Corporation*	***7. 4:45 PM - Scalable Chip-to-Wafer Hybrid Bonding Processes for Fine-pitch (3 µm and 6 µm) Interconnections*** *Chandra Rao B. S. S., Arvind Sundaram, Mishra Dileep, Yong Liang Ye, Ratan Bhimrao Umralkar, Nagendra Sekhar Vasarla – Institute of Microelectronics A*STAR; Patrick Lim, Santosh Kumar Rath – Applied Materials, Inc.*	***7. 4:45 PM - First Demonstration of Superior Characteristics of Co-Co Bonding With Passivation Structure at Low Thermal Budget for Advanced Packaging and Ultra-Fine Pitch Applications*** *Li Hsin Cheng, Chiao-Yen Wang, Kai-Fang Lai, Mu-Ping Hsu Kuan-Neng Chen – National Yang Ming Chiao Tung University*

PROGRAM SESSIONS: WEDNESDAY, MAY 28, 2:00 P.M. - 5:05 P.M.

Session 10: High Reliability Applications	Session 11: Emerging Trends: Towards High Speed, Secure, Reliable, and Sustainable Packaging	Session 12: Advanced Thermal Management Modeling Committee:
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Nokibul Islam – STATS ChipPAC, Ltd.** **Email: nokibul.islam@statschippac.com** **Paul Tiner – Texas Instruments, Inc.** **Email: p-tiner@ti.com**	**Session Co-Chairs** **Maria Gorchichko – Applied Materials, Inc.** **Email: maria_gorchichko@amat.com** **Hongqing Zhang – IBM Corporation** **Email: zhangh@us.ibm.com**	**Session Co-Chairs** **Kuo-Ning Chiang – National Tsing Hua University** **Email: knchiang@pme.nthu.edu.tw** **Xuejun Fan – Lamar University** **Email: xuejun.fan@lamar.edu**
1. 2:00 PM - Automotive Application-Driven Vibration Test Approach: Bridging the Gap Between Module and Board Level Reliability Test Methods *Varun Thukral, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc.; C. Chou – NXP Semiconductors, Inc/Delft University of Technology; Ovidiu Vermesan – SINTEF Digital; Willem Driel – Delft University of Technology*	***1. 2:00 PM - Lumped Element Multiplexer Design and Calibration in Cryogenic Environment for Quantum Reflectometry Applications*** *Vignesh Shanmugam Bhaskar, Mihai Rotaru – Institute of Microelectronics A*STAR*	***1. 2:00 PM - Development of an Embedded 2-Phase Cooling Technology for Two Stacked High-Power Chips in Future HPC & AI Applications*** *Xiaowu Zhang, Huicheng Feng, Gongyue Tang, Boon Long Lau, Ming Chinq Jong, Surya Bhattacharya, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR*
2. 2:20 PM - Chip Package Interaction Challenges and Solutions for FOWLP Product Reliability for Automotive Applications *Gaurav Sharma, Amar Mavinkurve, Michiel Soestbergen, Greta Terzariol, Taki Fang, Nishant Lakhera – NXP Semiconductor, Inc.*	***2. 2:20 PM - Embedded Silicon Chip Capacitors in Glass Package for Vertical Power Delivery*** *Ramin Rahimzadeh Khorasani – CHIMES, SRC, Penn State; Xingchen Li – Georgia Institute of Technology; Mohammad Al-Juwhari, Madhavan Swaminathan – Pennsylvania State University*	***2. 2:20 PM - Graphite Sheet Embedded in an Organic Flip-Chip Package for Heat Spreading*** *Keiji Matsumoto, Daisuke Oshima, Hiroyuki Mori, Toyohiro Aoki, Akihiro Horibe – IBM Research, Tokyo; Atom Watanabe, Russell Budd – IBM Research; Daniel Edelstein – IBM Corporation*
3. 2:40 PM - Higher Reliability Cu Pillar Bump on ENEPIG Substrate With Suppressed Ni3P for Automotive Applications *Hideaki Tsuchiya, Teruhiro Kuwajima, Yoshiaki Yamada, Nobuhiro Kinoshita, Koichi Ando – Renesas Electronics Corporation*	***3. 2:40 PM - SiPMeter: Active Hardware Metering for Heterogeneously Integrated System-in-Packages (SiPs)*** *Md Latifur Rahman, Amit Mazumder Shuvo, Jingbo Zhou, Mark Tehranipoor, Farimah Farahmandi – University of Florida*	***3. 2:40 PM - Enhanced Thermal Management of a 1.2 kV SiC MOSFET Half-Bridge Fan-Out Panel-Level Packaging With Nanocopper Sintering Die-Attachment*** *Wei Chen, Junwei Chen, Chao Gu, Tiancheng Tian, Jiajie Fan – Fudan University; Xuejun Fan – Lamar University; G. Q. (Kouchi) Zhang – Delft University of Technology*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Longhorn D		
4. 3:45 PM - Reliability and Microstructure Characterization of Through-Silicon Vias (TSV) at Different Aspect Ratios Using EBSD-Raman Spectroscopy *Shuhang Lyu, Thomas Beechem, Tiwei Wei – Purdue University*	***4. 3:45 PM - Advanced Metrology Suite for Linking Residual Stress to Fundamental Properties of Thermoset Packaging Materials*** *Polette Centellas, Stian Romberg, Ran Tao, Gery Stafford, Alexander Landauer, Christopher Soles – National Institute of Standards and Technology*	***4. 3:45 PM - Integrated Package-to-System Thermal Solution Evolution for High-Performance 2.5D CoWoS-R Advanced Packaging Technology Development*** *Tsunyen Wu, Kuo-Chin Chang, Chien-Chang Wang, Bang-Li Wu, Ching Wang, Kathy Yan, Chien-Hsun Lee, Cheng-Chi Hsieh, Jun He, Jing-Ruei Lu, Ruei-Wun Song, Sing-Da Jiang – Taiwan Semiconductor Manufacturing Company, Ltd.*
5. 4:05 PM - Cryogenic and Wide Temperature Thermal Cycling Reliability Study of QFN and CQFJ Packages for Lunar Missions *Harshil Goyal, Wayne Johnson, Michael Hamilton – Auburn University; Bhargav Yelamanchili – ANSYS, Inc.*	***5. 4:05 PM - Predictive Modeling of IMC Growth in BGA Component Solder Joints Using Artificial Neural Networks Under Rework and Temperature Cycling Conditions*** *Adlil Aizat Ismail – National University of Malaysia/Sandisk; Maria Abu Bakar, Azman Jalar, Mohd Ridzwan Yaakub, Muhammad Iqbal Abu Latiffi – National University of Malaysia; Erwan Basiron – Western Digital Corporation; Muhammad Nizam Ilias – National University of Malaysia/Western Digital Corporation*	***5. 4:05 PM - Microfluidic Cooling of Heterogeneously Integrated HBM-GPU Module With Step Height Difference*** *Euichul Chung, Muhannad Bakir – Georgia Institute of Technology*
6. 4:25 PM - The Role of Polymer Shrinkage and Oxidation in Thermal Aging Induced Crack Formation in Glass Fiber Reinforced Printed Circuit Boards *Mandy Krott, Thomas Ewald – Robert Bosch GmbH; Holger Ruckdaeschel – University of Bayreuth*	***6. 4:25 PM - Parameter Degradation Monitoring and Controller Adaptation Using Digital Twin*** *Lidya Mussie Weldehawaryat, Shuofeng Zhao – National Renewable Energy Laboratory; Wajiha Shireen – University of Houston*	***6. 4:25 PM - Real-Time and Scalable Thermal Management Strategy for Power-Sensitive Applications With AI-Enabled Global Optimization*** *Zhi Yang, Yong Pei – Groq; Anni Zheng – Visualization Solution*
7. 4:45 PM - Enhanced AEC Qualification of 5 nm AI Processor With Liquid Cooling for Level 4 Autonomous Driving *Fen Chen – Nvidia; Qing Yang, Jie Liu, Daniel Dsouza, Howard Davidson, Daniel Beckmeier, Elliott Wu, Phong Tran, Anthony Hong, Luqman Mohammed – Cruise LLC*	***7. 4:45 PM - Bio-Sourced Unfilled Epoxy for Die-Attach Applications*** *Saria Berger, Frederic A. Banville, David Danovitch – University of Sherbrooke; Catherine Marsan-Loyer – Centre de Collaboration MiQroInnovation (C2MI); David Gendron – Kemitek; Serge Ecoffey – Universite de Sherbrooke*	***7. 4:45 PM - First Demonstration of Metal-Lidded Integral Microjet Impingement On-Chip Cooling Structures With Alternating Feeding and Draining Nozzles for High-Performance Interposer Packages*** *Gopinath Sahu, Duc Hoang, Ruoyi Li, Akshat Patel, Ketan Yogi, Tiwei Wei – Purdue University*

PROGRAM SESSIONS: THURSDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 13: Large Panel FO for High Density Integration	Session 14: New Materials and Processes in Wafer-to-Wafer Hybrid Bonding	Session 15: Photonics Integration and Subsystems
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Photonics**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Lihong Cao – Advanced Semiconductor Engineering, Inc. (US)** **Email: lihong.cao@aseus.com** **Steffen Kroehnert – ESPAT-Consulting** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs** **Wei-Chung Lo – Industrial Technology Research Institute** **Email: lo@itri.org.tw** **Chih-Hang Tung – Taiwan Semiconductor Manufacturing Company, Ltd. / Email: chtungc@tsmc.com**	**Session Co-Chairs** **Takaaki Ishigure – Keio University** **Email: ishigure@appi.keio.ac.jp** **Richard Pitwon – Resolute Photonics, Ltd.** **Email: rpitwon@resolutephotonics.com**
1. 9:30 AM - Carrier Warpage Improvement Using Non-Photosensitive Dielectric Material for High I/O Density Organic RDL Application in Future Advanced Packaging *Guillermo Fernandez Zapico, Pondchanok Chinapang, Junya Miyake, Susumu Baba – Taiwan Semiconductor Manufacturing Company, Japan; Chih-Kai Cheng, Tsung-Yu Chen, Tsung-Shu Lin, Shimpei Yamaguchi – Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 9:30 AM - Integration, Materials and Equipment Innovations to Enable 100 nm Pitch W2W Bonding for Memory-to-Logic and Logic-to-Logic 3D Stacking*** *Raghav Sreenivasan, Kevin Ryan, Jeremiah Hebding, Tyler Sherwood, Siddarth Krishnan, Ying Trickett, Michael Chudzik – Applied Materials, Inc.; Barbara Weis – EV Group*	***1. 9:30 AM - Functional Demonstrator of a 256 Channels Beam Steering Device of a LIDAR for Autonomous Driving Including Silicon Photonics, 3D and Advanced Packaging Features: TSV and Fine Pitch Flip Chip*** *Thierry Mourier, Nadia Miloud-Ali, Laura Boutafa, Selimen Benahmed, Vincent Moulin, Yacoub Sahouane – CEA-LETI*
2. 9:50 AM - Next Generation Panel Level RDL Interposer Package for High Density Interconnection *Da-Hee Kim, Youngchan Ko, Wooseok Park – Samsung Electronics Co., Ltd.*	***2. 9:50 AM - Advanced Memory Wafer-to-Wafer Bonding With Support of Recyclable Carrier Systems*** *Wei Zhou, Kyle Kirby, Mota Liou, Kunal Parekh, Andrew Bayless, Vladimir Noveski, Akshay Singh – Micron Technology, Inc.*	***2. 9:50 AM - An Ultra-Compact 8-Channel Linear-Drive VCSEL-Based CPO Transceiver for Networks and AI/ML Applications in a Data Center*** *Wataru Yoshida, Kazuya Nagashima, Kensho Nishizaki, Sho Yoneyama, Hideyuki Nasu – Furukawa Electric Co., Ltd.*
3. 10:10 AM - M-Series Fan-Out Interposer Technology (M-FIT) - Scaling up for HPC & AI *Craig Bishop – Deca Technologies; Robin Davis, Liberty Perez, Ryan Sanden, Andrew Hoetker – Deca Technologies, Inc.*	***3. 10:10 AM - Development of Wafer-Level Wet Atomic Layer Etching Process Platform for Cu Surface Topography Control in Hybrid Bonding Applications*** *Seung Ho Hahn, Wooyoung Kim, Seongmin Son, Kyu-Ha Lee, Jung Shin Lee, Joohee Jang, Kyeongbin Lim, Bumki Moon – Samsung Electronics Co., Ltd.*	***3. 10:10 AM - InP/Si Integrated Laser With High-Tolerance-Multi-Step-Long-Period Diffraction Grating*** *Junichi Suzuki, Masahiro Matsuura, Masakazu Takabahashi, Yosuke Suzuki, Nobuo Ohata – Mitsubishi Electric Corporation*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Longhorn D		
4. 11:15 AM - Enhancement of the Adhesion in Multilayered Redistribution Layers of Fan-Out Wafer Level Packages for Memory Application *Kyoungtae Eun, Ki-Jun Sung, Jae-Min Kim, Se-Hyun Jang, Seowon Lee, Sungwon Yoon, Won Hae Kim, Seungchul Han – SK hynix Inc.*	***4. 11:15 AM - Development of a Novel WoWoW Process for 1/1.3-inch 50 Megapixel Three-Wafer-Stacked CMOS Image Sensor With DNN Circuits*** *Kan Shimizu, Ryoichi Nakamura, Wataru Otsuka, Hayato Iwamoto, Takumi Kamibayashi, Nobutatsu Araki, Kenichi Saitou – Sony Semiconductor Solutions Corporation; Yoshihisa Kagawa – Sony*	***4. 11:15 AM - Development of Transfer-Printed III-V C-Band Lasers on Silicon Photonic Integrated Circuits for Multi-Project Wafer Offering*** *George Nelson, Colin McDonough, Christopher Striemer, David Harame – AIM Photonics; James O'Callaghan, Padraic Morrissey, Peter O'Brien – Tyndall National Institute; Stefan Preble – Rochester Institute of Technology*
5. 11:35 AM - Die-to-Die Parallel Interface Optimization Utilizing Deca™s Novel M-Series Gen-2 Fan-Out Technology *Ting Zheng, Joshua Dillon, Eric Tremble, Wolfgang Sauter – Marvell Technology, Inc.; Craig Bishop – Deca Technologies*	***5. 11:35 AM - Wafer-to-Wafer Hybrid Bonding Technology With 300 nm Interconnect Pitch*** *Stefaan Van Huylenbroeck, Soon Aik Chew, Boyao Zhang, Lieve Bogaerts, Cindy Heyvaert, Sven Dewilde, Serena Iacovo, Michele Stucchi – imec*	***5. 11:35 AM - Low-Cost Transceiver Integration for Next Generation Passive Optical Network*** *Tam Huynh, Cuong Tran, Tzu-Yung Huang, Yang Liu, K.W. Kim, Ting-Chen Hu, Rose Kopf, Mark Cappuzzo – Nokia Bell Labs*
6. 11:55 AM - SiO2-Based Chiplet Reconstitution Technology for Multi-Height Chiplet Integration *Ashita Victor, Madison Manley, Muhannad Bakir – Georgia Institute of Technology*	***6. 11:55 AM - Electrical Performance of Hybrid Bonding With Sub-Micron Cu-Cu Bonding Contacts: Effects of Scaling, Microstructure, and Surface Morphology*** *Sari Al Zerey, Alina Bennett-Dubin, Morlidhar Patel, Junghyun Cho – State University of New York at Binghamton; Roy Yu, Nicholas Polomoff, Luke Darling, Katsuyuki Sakuma – IBM Research*	***6. 11:55 AM - Stress, Thermal and Optical Performance (STOP) Analysis of Co-Packaged Optical Processor With FPGA-Memory-Optics-Power Integration*** *Venkata Ramana Pamidighantam, Jugal Kishore Bhandari, Ubed Mohammad, Mayuri Adepu, Vamsi Rekapally, Tanisha Jain, Raghuveer M C – LightSpeed Photonics Pte Ltd; Mihai Rotaru – Institute of Microelectronics A*STAR*
7. 12:15 PM - Advanced Packaging From FOWLP to FOPLP: Development of Fanout Chip Last in 300 mm Panel *Smith Chen, Yung Shun Chang, Lihong Cao – Advanced Semiconductor Engineering, Inc. (US)*	***7. 12:15 PM - Selective Ru Deposition on Cu Bond Pads to Enable Low Thermal Budget Hybrid Bonding for HBM Applications.*** *Hemanth Kumar Cheemalamarri, Nithin Poonkottil, Masahisa Fujino, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR*	***7. 12:15 PM - Direct Flip Chip-on-Board Assembly (FCOB) for Optical Transceivers*** *Hiren Thacker, Tong Wang – Cisco Systems, Inc.*

PROGRAM SESSIONS: THURSDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 16: Manufacturing and Thermal Management Reliability	Session 17: Signal Integrity / Power Integrity for Advanced Packaging Technologies	Session 18: Simulations and Validation on Reliability Challenges of High Performance Packages
Committees: Applied Reliability and Assembly & Manufacturing Technology	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Varughese Mathew – NXP Semiconductor, Inc.** **Email: varughese.mathew@nxp.com** **Venkata Mokkapati – AT&S AG** **Email: v.mokkapati@ats.net**	**Session Co-Chairs** **Amit P. Agrawal – Advanced Micro Devices, Inc.** **Email: amit.agrawal@amd.com** **Xiao Sun – imec** **Email: xiao.sun@imec.be**	**Session Co-Chairs** **Ruiyang Liu – TeraDAR Inc.** **Email: ruiyang.liu9@gmail.com** **Karsten Meier – TU Dresden** **Email: karsten.meier@tu-dresden.de**
1. 9:30 AM - Influence of Sn-Bi Solder Joints Microstructure on the Electrical and Joule Heat Properties *Nathaniel Power, Choong-Un Kim, Pushkar Gothe – University of Texas, Arlington; Tae-Kyu Lee, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.*	***1. 9:30 AM - Simulation and Optimization of 32 Gbps On-Interposer Interconnects With Novel Deep Trench Based Equalizer*** *Changming Song, Xiuyu Shi, Qian Wang, Jian Ca, Shengjuan Zhou – Tsinghua University*	***1. 9:30 AM - Simulation and Experimental Validation of Microstructure Evolution of Sintered Ag Layer During Thermal Aging Using a Hybrid Potts-Phase Field Model*** *Xiao Hu, Qilin Xing, Marcel Hermans, Willem van Driel – Delft University of Technology; Chao Gu, Jiajie Fan – Fudan University; Rene Poelma – Nexperia; Jianlin Huang, Hans van Rijckevorsel, Huib Scholten – Ampleon B.V.*
2. 9:50 AM - A Study on the Improvement of Solder Joint Reliability of Module Products by IPL Soldering Method *Myeong-Hyeon Yu, Jaeseon Hwang, Taegyu Kang, Jongho Lee – Samsung Electronics Co., Ltd.*	***2. 9:50 AM - Mixed-Mode Distributed Physical-Based Transmission Line Model for Fast Signal Integrity Analysis on the S-Parameter Resonances and PAM4 Transmission of 5G Connectors*** *Yulin He, Kewei Song, Haonan Wu, Milton Feng – University of Illinois*	***2. 9:50 AM - Enabling Comprehensive Study of Electromigration and Diffusion Induced Failure Mechanisms in Lead-Free Solder Joint by Frame of Phase Field Modeling*** *Harikrishnan Kumarasamy, Choong-Un Kim, Hariram Mohanram – University of Texas at Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.*
3. 10:10 AM - Improving the Quality and Yield Performance of Vacuum Fluxless Reflow Soldering for High-Density AI Chips *Lei Jing, Anderson Chen, Vladimir Kudriavtsev, Wayne Chen, Hans Lin, Zia Karim, Saket Chadda, Xinxuan Tan – Yield Engineering Systems, Inc.*	***3. 10:10 AM - Signal Integrity Analysis of Differential Through-Silicon Via (TSV) With Silicon Dioxide Well (SDW) for Impedance Compensation in the Serdes Interface*** *Hyunwoong Kim, Sungwook Moon, Jiyoung Park, Seungki Nam – Samsung Electronics Co., Ltd.*	***3. 10:10 AM - In-Situ Confocal Raman Spectroscopy Assisted Interfacial Residual Stress Characterization in SiC Chip Sintered on AMB Substrate With Nanocopper Paste*** *Xuyang Yan, Zhoudong Yang, Chao Gu, Tiancheng Tian, Jiajie Fan – Fudan University; Xuejun Fan – Lamar University; G. Q. (Kouchi) Zhang – Delft University of Technology*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Longhorn D		
4. 11:15 AM - Additive Low-Temperature Assembly on Sustainable Substrates Circuit Reliability Performance and Stability Interactions *Pradeep Lall, Shriram Kulkarni, Md Golam Sarwar, Aditya Harsha – Auburn University; Scott Miller – NextFlex*	***4. 11:15 AM - Software-Defined Power Integrity (PI) Analysis for 2.5D/3D Packages*** *Wei Zhang, Chander Ravva, Moutasem Eltawil, Meenakshi Upadhyaya, Srikrishna Sitaraman, Arshiya Vohra, Ellie Baghernia, Narayan Agnihotri – Marvell Technology, Inc.*	***4. 11:15 AM - Additively Manufactured In-Mold Electronics Reliability Under Thermal Cycling and Sustained High Temperature*** *Shriram Kulkarni, Aditya Harsha, Md Golam Sarwar, Pradeep Lall – Auburn University; Scott Miller – NextFlex*
5. 11:35 AM - Investigation on Joule Heating of Plated Through Hole (PTH) Via *Howard Gan, Antai Xu, Jeffrey Zhang – Advanced Micro Devices, Inc.*	***5. 11:35 AM - Power Integrity Design of a 56 Gb/s Si-Photonic Optical Link for Memory Applications*** *Sagar Dubey, Dan Oh, Sam Khalili, Suresh Pothukuchi, Ankur Aggarwal, Saurabh Vats, Parmanand Mishra, Matteo Staffaroni, Romanas Narevich, Subal Sahni, Phil Winterbottom – Celestial AI*	***5. 11:35 AM - Thermal-Mechanical Modeling of Package Reflow for Cooling of Future CPU and GPU Devices*** *Ercan (Eric) Dede, Shailesh Joshi – Toyota Research Institute North America; Paul Paret, Gilbert Moreno, Sreekant Narumanchi – National Renewable Energy Laboratory; Suhas Tamvada, Saeed Moghaddam – University of Florida; Patrick McCluskey – University of Maryland*
6. 11:55 AM - Thermo-Mechanical Stability of High-Performance Chip Integration: Structure-Induced Stress in Complex System Structures *Yujin Park, Tae-Kyu Lee, Yawei Li, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.*	***6. 11:55 AM - Signal Integrity Design of a High-Performance, High-Frequency (10 MHz to 11 GHz), 3 dB Bandwidth High-Speed ADC Driver Amplifier*** *Rajen Murugan, Li Jiang – Texas Instruments, Inc.; Tony Tang – IEEE*	***6. 11:55 AM - Development and Optimization of a Flexible Printed Coplanar Capacitive Sensor for Accurate Twisting Motion Detection*** *Colleen Stover, Rui Chen, Yuxuan Hou – Eastern Michigan University*
7. 12:15 PM - Enhanced Electromigration Reliability of Cu/SiO2 Hybrid Joints Fabricated by (111)-Oriented Nanotwinned Cu *Shih-Chi Yang, You-Yi Lin, Chih Chen – National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang – Industrial Technology Research Institute*	***7. 12:15 PM - Compact Tri-Band Stub Filter Using Advanced Bridged-CRLH Transmission Line for 5G Applications*** *Junhyuk Yang, Hanna Jang, Yong-Kyu Yoon – University of Florida*	***7. 12:15 PM - Isothermal Shock Testing and Failure State Analysis on Flip-Chip Interconnects*** *Max Frank Haeusler, Karsten Meier, Shengxiang Lyu, Karlheinz Bock – TU Dresden*

PROGRAM SESSIONS: THURSDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 19: Chiplet Integration and Advanced Thermal Solutions	Session 20: Novel Technologies for High Density RDL Interposers	Session 21: Meeting AI Challenges: Large Package Solution and Warpage Management for Advanced Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Young-Gon Kim – Renesas** **Email: young.kim.jg@renesas.com** **Luu Nguyen – PsiQuantum** **Email: lnguyen@psiquantum.com**	**Session Co-Chairs** **Nathan Lower – Consultant** **Email: nplower@hotmail.com** **Tiwei Wei – Purdue University** **Email: wei427@purdue.edu**	**Session Co-Chairs** **Bing Dang – IBM Corporation** **Email: dangbing@us.ibm.com** **Frank Wei – DISCO Corporation** **Email: frank_w@discousa.com**
1. 2:00 PM - Direct-to-Silicon Liquid Cooling Integrated on CoWoS® Platform *Yu-Jen Lien, Sing-Da Jiang, Cheng-Chieh Hsieh, Han-Jong Chia, Tsunyen Wu, S.W. Lu, Kathy Yan, Kuo-Chung Yee, Douglas C.H. Yu, Chien-Chih Lin, Ke-Han Shen – Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 2:00 PM - Pillar-Suspended Bridge (PSB); Transmission Simulation and Fabrication Process of 2 Micron Diameter / 5 Micron Pitch Dry Etched Stacked Via in Low-k Polymer for High Performance RDL Bridge*** *Shinichi Arioka, Tanapun Srichanthamit – AOI Electronics Co. Ltd.; Yusuke Naka, Koh Meiten – Taiyo Ink Mfg. Co., Ltd.; Fumito Ootake, Yasuhiro Morikawa – ULVAC, Inc; Osamu Okada – Institute of Science Tokyo; Yoichiro Kurita – Tokyo Institute of Technology*	***1. 2:00 PM - Containment Solution for Liquid Metal-Based Second-Level Interconnect Technology*** *Ziyin Lin, Karumbu Meyyappan, Taylor Rawlings, Dingying Xu – Intel Corporation*
2. 2:20 PM - A Novel Approach of Multi-Chip FOPKG Chiplet Interconnection Using a Land-Side Si Bridge *Sungoh Ahn, Eunkyeong Park, Seokbeom Yong, Junghoo Yun, Dongsuk Kim, Heeyoub Kang, Sangkyu Lee, Jongyoun Kim – Samsung Electronics Co., Ltd.*	***2. 2:20 PM - Panel Level Interposer by Using Glass Carrier for 2.5D Advance IC Package Application*** *Terry Wang, Cheng-Yueh Chang, William Yang, Yu-Jhen Yang, Pei-Pei Cheng, Chien-Ming Tseng – Industrial Technology Research Institute; Hungyu Wu – Applied Materials, Inc.; Austin Cheng – FAVITE, Inc.*	***2. 2:20 PM - Ultra High Aspect Ratio Photo Resist for Cu Pillar Based Multi-Stack Fan-out Package With Wide I/O LPDDR*** *Seon Ho Lee, Jinyoung Kim, Jeongseok Mun, JunHyeong Park, Jihye Shim, YoungGwan Ko – Samsung Electronics Co., Ltd.*
3. 2:40 PM - Mid-BEOL Heterogeneous Integration Through Sub-1 µm Pitch Hybrid Bonding & Advanced Silicon Carrier Technologies for AI & Compute Applications *Adel A Elsherbini, Tushar Talukdar, Thomas Sounart, Saurabh Chauhan, Yi Shi, Haris Khan Niazi, Paul Nordeen, Andrey Vyatskikh, Brandon Rawlings, William Brezinski, Richard Vreeland, Sou-Chi Chang, Feras Eid, Shawna Liff, Johanna Swan, Kaladhar Radhakrishnan – Intel Corporation*	***3. 2:40 PM - Fine Pitch Semi-Additive RDL-Process Development*** *Nelson Pinho, Lili Wang, Murat Pak, Punith Kumar Mudiger Krishne Gowda, Amaia Diaz De Zerio, Jeonho Kim, Andy Miller, Eric Beyne – imec*	***3. 2:40 PM - Advanced FO PLP Digital Lithography Patterning Development for AI Devices*** *Ksenija Varga, Roman Holly, Boris Povazay, Tobias Tobias, Thomas Uhrmann – EV Group; Marieke Vandevyvere, Niels Van Herck – Fujifilm Electronic Materials*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Longhorn D		
4. 3:45 PM - The Study and Challenges of Backside Metal Interface Material to Enhance Fan-Out Embedded Bridge Die Package (FO-EB) Thermal Performance *Kuei-Hsiao Kuo, Jui Teng Hung, Ting En Lin, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.*	***4. 3:45 PM - Wafer Backside Fine Pitch Copper Interconnects and Low-Profile Micro-Bumps Pad Process for Multiple Chip-on-Wafer Stacking Structure*** *Syuto Tamura, Junichiro Fujimagari, Yuji Uesugi, Kenta Fukushima, Kota Maruyama, Takuji Matsumoto, Kentaro Akiyama – Sony Semiconductor Solutions*	***4. 3:45 PM - Effective Build-Up Substrate Design for Warpage Reduction and Reliability Enhancement in Advanced Semiconductor Packages*** *Daichi Okazaki, Eiji Baba, Yuto Inoue, Ikumi Sawa, Daisuke Hironiwa, Ryo Miyamoto – Ajinomoto Fine-Techno Co., Inc.; YoungGun Han, Taka Kanayama – Fukuoka University*
5. 4:05 PM - Thermal Impact of BSPDN for 3D Memory and Logic Integration *Melina Lofrano, Herman Oprins, Geert Van der Plas, Eric Beyne – imec*	***5. 4:05 PM - Reliability Assessment of a Hybrid Wiring Layer Assembly for Low-Cost Sub 10 µm Pitch Integration*** *Vineeth Harish, Krutikesh Sahoo, Subramanian Iyer – University of California, Los Angeles; Kai Zheng, Gilbert Park, Han-Wen Chen, Steven Verhaverbeke – Applied Materials, Inc.*	***5. 4:05 PM - Development of Negative Thermal Expansion Zeolite Fillers for Next-Generation Low CTE Encapsulation Materials*** *Ryo Nishida, Yutaro Tanaka, Syu Hikima, Ryoji Onishi, Kazuki Tsujikawa, Tetsuharu Yuge, Masahiro Yokoyama – Mitsubishi Chemical Corporation*
6. 4:25 PM - Inter-Die Gap-Filling With Varying Aspect Ratio (AR) Using PECVD Oxide for 3D Packaging: Model Prediction and Experimental Validation *Md Mahbubul Hasan, Taiwo Ajayi, Yuting Wang, Pilin Liu, Rajesh Surapaneni, Xavier Brun – Intel Corporation*	***6. 4:25 PM - A Novel Architecture for On-Device AI in Mobile Application With Enhanced Heat Dissipation*** *Kyung Don Mun, Jihwang Kim, Sangjin Baek, Jaechoon Kim, Suk Won Jang, Kang Joon Lee, DongWoon Park, Daewoo Kim – Samsung Electronics Co., Ltd.*	***6. 4:25 PM - Development of Novel Photosensitive Polyimide With 170 °C Curing Process to Enable Low Warpage and sub-2 µm Patterning for RDLs in Next Generation Interposer*** *Yusuke Murata, Shuhei Horikawa, Mitsuka Inoue, Ryoji Tatara, Hirokazu Ito – JSR Corporation*
7. 4:45 PM - Modeling and Validation of an Integrated Package Solution (iPaS) for Next Generation Power Supply Systems *Akitomo Takahashi, Shuhei Yamada, Yuuki Yabuhara, Masafumi Tanaka, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.*	***7. 4:45 PM - High-Density RDL Fan-Out With L/S 2/2 µm Dry-Etched Micro Vias for Agile Prototyping/Low-Volume Production and TAT/NRE Cost Modeling*** *Yuichi Sukegawa, Kenji Miyake – Maxell, Ltd.; Osamu Okada – Institute of Science Tokyo; Takafumi Fukushima, Hiroyuki Hashimoto – Tohoku University; Yusuke Naka – Taiyo Ink Mfg. Co., Ltd.; Yasuhiro Morikawa – ULVAC, Inc.; Akira Shimada – Toray Industries, Inc.; Yoichiro Kurita – Tokyo Institute of Technology*	***7. 4:45 PM - Innovative Silicon Die Thinning and Edge Protection of Chip-to-Wafer Hybrid Bonded Wafer for High-Density Multi-Chip Stacking*** *Nagendra Sekhar Vasarla, Mishra Dileep, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR; Roman Ivanov – Entegris, Inc.; Subhash Guddati – Entegris Asia Pte. Ltd.*

PROGRAM SESSIONS: THURSDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 22: Heterogeneous Integration Using Bridge and 3D Stacking	Session 23: AI Enabled Innovations in Advanced Packaging Technologies	Session 24: Advanced Characterization and Modeling of Next Generation Packaging Materials
Committee: Assembly & Manufacturing Technology	**Committees: Electrical Design and Analysis and Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Pascale Gagnon – IBM Canada, Ltd.** **Email: pgagnon@ca.ibm.com** **Omkar Gupte – Advanced Micro Devices, Inc.** **Email: Omkar.Gupte@amd.com**	**Session Co-Chairs** **Xinpei Cao – Henkel Corporation** **Email: xinpei.cao@henkel.com** **Hideki Sasaki – Rapidus Corporation** **Email: hideki.sasaki@rapidus.co.jp**	**Session Co-Chairs** **Rui Chen – Eastern Michigan University** **Email: rchen7@emich.edu** **Ning Ye – Western Digital Corporation** **Email: ning.ye@wdc.com**
1. 2:00 PM - Hybrid Bonding With Fluidic Self Alignment: Process Optimization and Electrical Test Vehicle Fabrication *Feras Eid, Charles El Helou, Shashi Bhushan Sinha, Golsa Naderi, Forough Mahmoudabadi, Brandon Rawlings, Brian Barley, Tayseer Mahdi, Sheena Benson, Siyan Dong, Yi Shi, William Brezinski, Felipe Bedoya, Wenhao (Eric) Li, Francesca Bard – Intel Corporation*	***1. 2:00 PM - AI-Based Decision-Tree Concept to Fabricate Active Waferscale Fabric for Heterogeneous Chiplet Integration*** *Rabindra Das, Albert Reuther, Vitaliy Gleyzer, Ryan Touzjian, Alex Wynn, Ravi Rastogi, Brian Tyrrell, Paul Monticciolo – MIT Lincoln Laboratory*	***1. 2:00 PM - Characterization of Moisture Diffusion Properties of ABF and Mold Compounds in Molded Package With High Copper Density Substrate*** *S M Yeasin Habib, Xuejun Fan – Lamar University; Guangxu Li, Yutaka Suzuki, Jonathan Noquil, Mak Kulkarni, Rajen Murugan – Texas Instruments, Inc.*
2. 2:20 PM - Optimization of Alignment Model and Metrology During Backside EUV Lithography Patterning for CFET Technology *Sujan Kumar Sarkar – IMEC; Andrea Mingardi, Rajendra Kumar Saroj, Sandip Halder – imec*	***2. 2:20 PM - AI Trustworthiness in the Era of Advanced Packaging: Challenges and Opportunities*** *Katayoon Yahyaei, Mohammad Shafkat Khan, Nitin Varshney, Anirban Bhattacharya, Baibhab Chatterjee, Navid Asadizanjani – University of Florida; Stephan Larmann – InfraTec; Parth Sandeepbhai Shah – Intel Corporation*	***2. 2:20 PM - Thermal-Mechanical Behavior of Highly (111)-Oriented Nano Twinned Electroplated Copper for Advanced Electronic Packaging*** *Abdellah Salahouelhadj, Kris Vanstreels, Joke de Messemaeker, Aleksandar Radisic, Zaid El-Mekki, Carine Gerets – imec; Iris Chang – BASF Taiwan; Sung-Ho Park – BASF Korea*
3. 2:40 PM - Assessing Queue Time in D2W Hybrid Bonding Through Precise Bond Strength Measurements *Yuki Yoshihara, Junya Fuse, Fumihiro Inoue – Yokohama National University; Shimpei Aoki, Takashi Hare, Kentaro Mihara, Takayuki Miyoshi – Toray Engineering Co., Ltd.; Naoko Yamamoto, Shunsuke Teranishi – DISCO Corporation; Takafumi Fukushima – Tohoku University; Akira Uedono – University of Tsukuba*	***3. 2:40 PM - Efficient Visual Inspection Framework of High-Bandwidth Memory Bumps With Generative and Deep Learning AI*** *Richard Chang, Ramanpreet Pahwa, Jie Wang, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong – Institute of Microelectronics A*STAR*	***3. 2:40 PM - Nanoindentation Based Methodology to Characterize the Adhesion Strength of Dielectric Bond Interfaces*** *Kris Vanstreels, Oguzhan O. Okudur, Yusuf Ozdemir, Mario Gonzalez, Eric Beyne – imec*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Longhorn D		
4. 3:45 PM - Thin 3D: An Innovative Approach to Ultra-Thin Wafer-Level Active Device Transfer Technology With Optimized Material and Thermal Solution for 3D IC *Ting-Yu Chen, Shie-Ping Chang, Bo-Jheng Shih, Zih-Yang Chen, Yu-Lun Liu, Po-Tsang Huang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Po-Jung Sung, Nien-Chih Lin, Chih-Chao Yang – Taiwan Semiconductor Research Institute; Ming-Yang Li, Iuliana P. Radu – Taiwan Semiconductor Manufacturing Company*	***4. 3:45 PM - Generative Model Based Multi-Layer PDN Impedance Estimation With Multi-Power Domain*** *Hyunjun An, Keeyoung Son, Haeyeon Kim, Keunwoo Kim, Junghyun Lee, Taein Shin, Seonguk Choi, Junho Park, Inyoung Choi, Joungho Kim, Haeseok Suh, Taesoo Kim – Korea Advanced Institute of Science and Technology*	***4. 3:45 PM - Non-PFAS Semiconductor Packaging Material Performance and Stability in Comparison With PFAS Materials*** *Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Madhu Kasturi – Auburn University*
5. 4:05 PM - Ultra-Thin Wafer Handling Process for Advanced Packaging Using Novel Temporary Bonding Film and De-Bonding Method *Motohiro Negishi, Yuta Akasu, Emi Miyazawa, Tetsuya Enomoto, Kohei Taniguchi, Takashi Kawamori – Resonac Corporation*	***5. 4:05 PM - RAICEx: a Rapid and Accurate AI-Based Framework for Crosstalk Prediction in IC Packages With a Case Study on High-Speed DDR Systems*** *Katayoon Yahyaei – University of Florida; Tapobrata Bandyopadhyay, Snehamay Sinha – Texas Instruments, Inc.*	***5. 4:05 PM - Predictive Modeling of Thin Films Properties Using an Experimental and Simulation-Based Approach*** *Dao Kun Lim – National University of Singapore/Micron Technology; Derik Rudd, Venkata Rama Satya Pradeep Vempaty, Wen How Sim, Harjashan Veer Singh – Micron Technology, Inc.; Faxing Che – Micron Semiconductor Asia Operations Pte. Ltd; Wentao Yan, Yeow Kheng Lim – National University of Singapore*
6. 4:25 PM - A Novel Thermal Isolation Method With Embedded 'Glass Bridge' Structures in Silicon-Based 2.5D Heterogeneous Integration Systems *Zhengwei Chen, Zixin Xiong, Keyu Wang, Amy M. Marconnet, Tiwei Wei – Purdue University*	***6. 4:25 PM - TDR Optimization Method of 112G Serdes Interface in PKG Using Deep Reinforcement Learning*** *Hyunwoong Kim, Sungwook Moon, Jiyoung Park, Taeyun Kim, Jinho Kim, Haemin Lee, Seungki Nam – Samsung Electronics Co., Ltd.*	***6. 4:25 PM - Physics-Based Modeling With Nanoindentation on the Mechanical Reliability of TGV Substrates Under Annealing Effects*** *Jui-Chang Chuang, Wei-Cheng Tsai, Hao-Zhou Lin, Chen-Tsai Yang, Chung-I Li – Industrial Technology Research Institute; Chang-Chun Lee – National Tsing Hua University; Shih-Hsien Lee, Shih-Hao Kuo – Applied Materials, Inc.*
7. 4:45 PM - FOCoS-Bridge for Emerging Trends in High-Performance Computing (HPC) and Artificial Intelligence (AI) *Teck Chong Lee, Smith Chen, Lihong Cao, Hung-Chun Kuo – Advanced Semiconductor Engineering, Inc. (US); Yuh Shan Su, Chun Jun Zhuang, Po-Chih Pan, C. P. Hung – Advanced Semiconductor Engineering, Inc.*	***7. 4:45 PM - AI-Assisted Electro-Thermal Co-Design for Hybrid Bonded Packages*** *Juhitha Konduru, Jose Schutt-Aine – University of Illinois; Srikanth Rangarajan – Binghamton University*	***7. 4:45 PM - Validated Methodology for Accurate Simultaneous Measurement of Elastic Modulus and CTE of BEOL Materials for Improved Advanced Package Performance Prediction*** *Chukwudi Okoro – Corning Research and Development Corporation; James Price, Diego Prado, Alex Longacre, Nicholas Walker, Shandon Hart – Corning, Inc.*

PROGRAM SESSIONS: FRIDAY, MAY 30, 9:30 A.M. - 12:35 P.M.

Session 25: Advanced Substrate Technologies- Organic, Embedding and Glass	Session 26: Process Innovation in Through-Via and Solder Interconnections	Session 27: Thermal Management and Material Solutions for High Performance 2.5D and 3D Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Kuldip Johal – MKS Instruments** **Email: kuldip.johal@mks.com** **Markus Leitgeb – AT&S AG** **Email: m.leitgeb@ats.net**	**Session Co-Chairs** **Vempati Srinivasa Rao – Institute of Microelectronics A*STAR / Email: vempati@ime.a-star.edu.sg** **Wei Zhou – Micron Technology, Inc.** **Email: zhouwei@micron.com**	**Session Co-Chairs** **Dwayne Shirley – Marvell Semiconductor, Inc.** **Email: shirley@ieee.org** **Ivan Shubin – Raytheon Technologies** **Email: ishubin@gmail.com**
1. 9:30 AM - Development of Glass Core Substrates for Long-Term Reliability Under Thermal Stress *Koji Fujimoto, Takahiro Tai, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.*	***1. 9:30 AM - Deep Via and Trench Etching of Low CTE Glass Package Substrate Using SF6, NF3 and H2O Based NLD Plasma Process*** *Yasuhiro Morikawa – ULVAC, Inc.; Srinivas Tadigadapa – Northeastern University*	***1. 9:30 AM - Optimized TIM1 Solution for Large 2.5D HPC Packages Using Silicone Matrix Containing Liquid Metal Materials*** *Po-Yao Lin, Kevin Lai, Yanling Huang, Han-wen Lin, JS Paek, Max Wu – Intel Corporation*
2. 9:50 AM - Fully Encapsulated Fine Pitch Dual Damascene Organic RDL With Low Dk Df Photosensitive Polyimide and Its Reliability *Minhua Lu – IBM Corporation; Joyce Liu, Peter Sorce, Andrew Giannetta, Michael Lofaro, Adele Pacquette, Michelle Hofman, David Rath – IBM Research; Elizabeth Duch, Stephan Cohen, Curtis Calamari, Evan Colgan – IBM T. J. Watson Research Center*	***2. 9:50 AM - Development of Straight, Small-Diameter, High-Aspect Ratio Copper-Filled Through-Glass Vias (TGV) for High-Density 3D Interconnections*** *Ye Yang, Shuhang Lyu, Tiwei Wei – Purdue University; James Chien – Taiwan Foresight Co. Ltd.*	***2. 9:50 AM - Novel Fabrication of Alumina Nanowires and Their Integration Into Alumina Nanowire, Membranes and Aerogels-Epoxy Composites for Enhanced Thermal Management in 2.5D/3D Semiconductor Packaging*** *Zihao Lin, Wenbin Fu, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology*
3. 10:10 AM - A Comparative Study on Power Delivery Network (PDN) Using Several Capacitor-Embedded Substrates for Next Generation Power Supply Applications *Shuhei Yamada, Yuuki Yabuhara, Akitomo Takahashi, Kazuki Itoyama, Koshi Himeda, Atsushi Yamamoto – Murata Manufacturing Co., Ltd.*	***3. 10:10 AM - Metallization of Helium Tight and Thermo-Mechanically Reliable Through Glass Vias (TGV) by Conformal Pinched Via (CPV) Approach*** *Mandakini Kanungo – Corning, Inc.; Rajesh Vaddi, Scott Pollard, Prantik Mazumder, Chukwudi Okoro – Corning Research and Development Corporation*	***3. 10:10 AM - Characterization of PVD Backside Metal Adhesion for Improved Thermal Management in Heterogeneous Integration*** *Carl Drechsel, Patrik Carazzetti, Eleftherios Stampolis, Ewald Strolz – Evatec AG; Marius Adler, Ole Holck, Marcus Voitel, Friedrich Muller, Karl-Friedrich Becker, Tanja Braun – Fraunhofer IZM*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Texas Foyer		
4. 11:15 AM - Embedded Vertical Power Delivery Network Including Voltage Regulator for Over-1kW FC-BGA Based on 1.4 mm Thick-Core Organic Substrate *Heeseok Lee – Samsung Electronics Co., Ltd.*	***4. 11:15 AM - A Novel Approach to Ultra-Low Temperature Interconnection: Double-Sided SLID Process Using SAC BGAs and Off-Eutectic SnBiIn Paste*** *Hafiz Waqas Ali, David Danovitch, Dominique Drouin – University of Sherbrooke; Divya Taneja – IBM Canada, Ltd.*	***4. 11:15 AM - Novel Low Df and Low CTE Material with High Thermal Stability for Organic Integration Board*** *Shunsuke Tonouchi, Yuji Sakurazawa, Ayaka Takeguchi, Keiichi Kasuga, Yusuke Sera, Hiroshi Shimizu, Shuji Gozu, Yukio Nakamura, Tatsuro Kodama, Yuichi Yanaka, Rimpei Kindaichi – Resonac Corporation*
5. 11:35 AM - Glass Core Substrate versus Organic Core Substrate *John H. Lau, Ning Liu, Mike Ma, TJ Tseng – Unimicron Technology Corp.*	***5. 11:35 AM - Growth of Nanovoids in Electroless Cu Layer of Micro-Via After Thermal Reliability Test*** *Masahiko Nishijima, Ming-Chun Hsieh, Zhang Zheng, Rieko Okumura, Aiji Suetake, Hiroyoshi Yoshida, Chuantong Chen, Katsuaki Suganuma – Osaka University; Hiroki Seto – Okuno Chemical Industries Co., Ltd.*	***5. 11:35 AM - Thermal Management of Nano-TSVs in Advanced BS-PDN: A Comparative Study of AlN and Oxide Dielectrics for Heat Dissipation Efficiency*** *Ya-Ching Tseng, Huicheng Feng, Gongyue Tang, Hong Yu Li – Institute of Microelectronics A*STAR*
6. 11:55 AM - Development of Glass Core Build-Up Substate With TGV *Masahiro Sunohara, Jun Yoshiike, Hiroshi Taneda, Yoko Nakabayashi, Noriyoshi Shimizu – Shinko Electric Industries Co., Ltd.*	***6. 11:55 AM - Formic Acid Vapor Assisted Fluxless TCB for Advanced Packaging- a Key Enabler for Ultra-Fine Pitch and High-Density Interconnects*** *Adeel Bajwa, Suleman Ayub, Tom Colosimo, Matt Wasserman, Bob Chyla – Kulicke and Soffa Industries, Inc.*	***6. 11:55 AM - Mold Underfill Process With Sheet Molding Compound for Full-Reticle Size Dies With Single-Digit Micrometer Gaps*** *Yuki Sugiura, Daisuke Mori, Katsushi Kan – Nagase ChemteX Corporation*
7. 12:15 PM - High-Aspect-Ratio, 6 µm-Diameter Through-Glass-Via Fabrication Into 100 µm-Thick ENA1 by Dry Laser Micro-Drilling Process *Toshio Otsu, Tsubasa Endo, Hiroharu Tamaru, Yohei Kobayashi – University of Tokyo; Yoichiro Sato, Akihiro Shibata – AGC, Inc.*	***7. 12:15 PM - Enhancing Wafer-Level Cu-Solder Bonding: A Fluxless Approach With Cu-Selective Passivation Coating*** *Kevin Antony Jesu Durai, Dinesh Kumar Kumaravel, Khanh Tuyet Anh Tran, Oliver Chyan – University of North Texas*	***7. 12:15 PM - Low Dk/Df Siloxane Hybrid Laminates for Advanced Packaging Substrate*** *Seung-Mo Kang, Hyungshin Kweon, SungHun Park, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology*

PROGRAM SESSIONS: FRIDAY, MAY 30, 9:30 A.M. - 12:35 P.M.

Session 28: Reliability of Heterogeneous Integrated (HI) Packages	Session 29: Advances in Additive Manufacturing, Wearable and Medical Technologies	Session 30: Simulations on Advanced Package Processing - Hybrid Bonding, Chip Stacking and Wafer-to-Wafer
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Keith Newman – Advanced Micro Devices, Inc.** **Email: keith.newman@amd.com** **Scott Savage – Medtronic, Inc.** **Email: scott.savage@medtronic.com**	**Session Co-Chairs** **Tengfei Jiang – University of Central Florida** **Email: tengfei.jiang@ucf.edu** **Chukwudi Okoro – Corning Research and Development Corporation / Email: okoroc@corning.com**	**Session Co-Chairs** **Chang-Chun Lee – National Tsing Hua University** **Email: cclee@pme.nthu.edu.tw** **Yong Liu – ON Semiconductor** **Email: Yong.Liu@onsemi.com**
1. 9:30 AM - A Procedure for Evaluating the Chiplet-Module-System Interaction of a 2.5-D Package Under Board-Level Reliability Test Condition *Jing-An Huang, Tz-Cheng Chiu, Zhi-Yin Huang – National Cheng Kung University*	***1. 9:30 AM - Rapid Prototyping of Advanced Packaging Using 3D-Printed Fanout Interposer Substrates With Diagonal Through-Holes*** *Haksoon Jung, Yurim Choi, Jimin Kwon, Nahyeon Kim – Ulsan National Institute of Science and Technology; Hyunjin Park – Korea Research Institute of Chemical Technology*	***1. 9:30 AM - Atomistic Modeling of Interfacial Cracking in Copper-to-Copper Direct Bonding*** *Shengfeng Yang, Jiali Lu – Purdue University*
2. 9:50 AM - Influence of Passivation Layer on Electromigration Lifetime of Fine-Pitch Cu RDL *Adrija Chaudhuri, Johannes Jaeschke, Astrid Gollhardt, Hermann Oppermann – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin*	***2. 9:50 AM - Fully Printed Pressure Sensor Array for Soft Robotics*** *Sara Lieberman, Riadh Al-Haidari, Babatunde Falola, Mark Poliks – Binghamton University; Deepak Trivedi, Pei-Hsin Kuo – GE Global; Felippe Pavinatto – GE Aerospace Research; Jack Ly – BlueHalo*	***2. 9:50 AM - Crystal Plasticity-Based Modeling and Experimental Validation of the Influence of Microstructures and Grain Boundary Junction Types on the Cu-Cu Bonding Interface.*** *Jae-Uk Lee, Hyun-Dong Lee, Sung-Hyun Oh, Hoo-Jeong Lee, Eun-Ho Lee – Sungkyunkwan University; Sung-Ho Park, Won-Seob Cho, Yong-Jin Park – BASF Korea; Alexandra Haag, Soichi Watanabe – BASF; Marco Arnold – BASF SE*
3. 10:10 AM - Fabrication Optimization and Reliability Study of Hyper RDL (HRDL) Interposer for Advanced Packaging and Heterogeneous Integration *Chun-Ta Li, Yu-Lun Liu, Tzu-Han Sun, Wen-Tzu Tsai, Mu-Ping Hsu, Yuan-Chiu Huang, Kuan-Neng Chen, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Chien-Kang Hsiung – National Yang Ming Chiao Tung University / Applied Materials Inc.; Yu-Tao Yang – MediaTek USA, Inc.*	***3. 10:10 AM - Direct Digital Manufacturing for Laser-Drilled Vias in Multilayer Glass Additively Manufactured Electronics*** *Sam LeBlanc, Jason Benoit – nScrypt; Kenneth Church – Sciperio*	***3. 10:10 AM - Thermal Modeling of IR Laser Debond With Inorganic Thin Film Release Layers*** *Thomas Sounart, Henning Braunisch, Paul Nordeen, Georgios Dogiamis – Intel Corporation*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Texas Foyer		
4. 11:15 AM - Influence of Cycling Induced Damage on the Anand Model Parameters of SAC305 Lead-Free Solder *Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Omma Sumaiya, Jeffrey Suhling, Pradeep Lall – Auburn University*	***4. 11:15 AM - Point of Care Device for Early Detection of Polycystic Ovary Syndrome (PCOS)*** *Musafargani Sikkandhar, Musafargani Sikkandhar, Karen Yanping Wang, Ramona Damalerio, Norhanani Jaafar, Ming-Yuan Cheng – Institute of Microelectronics A*STAR*	***4. 11:15 AM - Tailoring Sintering Pressure to Optimize Nanoparticle Connectivity and Mechanical Strength in Cu-Based Interconnects*** *Leiming Du, Weiping Jiao, G. Q. (Kouchi) Zhang – Delft University of Technology; Jiajie Fan – Fudan University*
5. 11:35 AM - The Influence of Full IMC Structure on Micro-Bump EM Performance *Chung-Yu Chiu, Jui-Shen Chang, Tzuan-Horng Liu, Chen-Nan Chiu, Yao-Chun Chuang, Ryan Lu, An-Jhih Su, Jyun-Lin Wu, John Yeh – Taiwan Semiconductor Manufacturing Company, Ltd.*	***5. 11:35 AM - Design and Fabrication of Bendable Double-Layer RDL Metallization Based on FOWLP for In-Mold Flexible Hybrid Electronics (iFHE)*** *Chang Liu, Jiayi Shen, Atsushi Shinoda, Han Zhang, Tetsu Tanaka, Takafumi Fukushima – Tohoku University*	***5. 11:35 AM - Wafer Substrate Impact on Direct Wafer-to-Wafer Bonding Process*** *Nathan Ip, Yuhai Xiang, Xuemei Chen – Tokyo Electron America, Inc.; Andrew Tuchman, Ilseok Son – TEL Technology Center, America, LLC; Norifumi Kohama, Kimio Motoda – Tokyo Electron Kyushu, Ltd.*
6. 11:55 AM - First Proof of 3D-IC Power Plane Defect Localisation via Frequency Domain Spatial Heat Mapping *Zhansen Shi, Lucas Lum, Yeow Kheng Lim – National University of Singapore; Bernice Zee, J.M. Chin – Advanced Micro Devices (Singapore) Pte Ltd.*	***6. 11:55 AM - FlexPower II : Integration of Flexible Battlet Interdigitated Battery and FlexTrateTM for Wearables*** *Mansi Sunil Sheth,Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)*	***6. 11:55 AM - Advanced Packaging Techniques: Hybrid Numerical and Experimental Analysis of Underfill Flow in Fine Pitch Multi-Chip Modules*** *Srikar Vallury, Leo Shen – Moldex3D Northern America, Inc.; Kazuki Noguchi – Sanyu Rec Co., Ltd.; Ching-Kai Chou, Zi-Hsuan Wei Wei, Wei-Yu Lin, Yu-En Liang – CoreTech System (Moldex3D)*
7. 12:15 PM - Advanced Thermal Management for High Power HPC, AI *Nokibul Islam, JoonYoung Choi – STATS ChipPAC, Ltd.; Choong Kooi Chee – Marvell Technology, Inc.*	***7. 12:15 PM - Design, Materials Selection, and Assembly Process for a CMUT-Based Handheld Ultrasound Probe Head: Overcoming Development Challenges*** *KM Rafidh Hassan, Gaurav Mehrotra, Hazel Caballero, Steven Lee – Renesas Electronics America Inc.; Karim Allidina, Tommy Tsang, Mohannad Elsayed, Hani Tawfik – MEMS Vision International, Inc.*	***7. 12:15 PM - Simulation Analysis of Edge Dot-Void Formation and Edge Roll-Off Effects in Wafer-to-Wafer Bonding*** *Sunghwan Kim, Youngsoo Kim, Geun-Myeong Kim, Minyeong Je, Yoon-Suk Kim, Cheolmin Shin, Kyu-Ha Lee, Dongchan Lim – Samsung Electronics Co., Ltd.*

PROGRAM SESSIONS: FRIDAY, MAY 30, 2:00 P.M. - 5:05 P.M.

Session 31: Automotive Power	Session 32: Design, Materials, Metrology & Standards for Next Generation Interconnections	Session 33: Innovative Interconnects and Through Via Technology for 3D Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Texas D	**Texas C**	**Texas 4-6**
Session Co-Chairs **Mike Gallagher – DuPont Electronic Materials** **Email: michael.gallagher@dupont.com** **Albert Lan – Applied Materials, Inc.** **Email: Albert_Lan@amat.com**	**Session Co-Chairs** **Bernd Ebersberger – Infineon Technologies AG** **Email: bernd.ebersberger@infineon.com** **Yoshihisa Kagawa – Sony** **Email: Yoshihisa.Kagawa@sony.com**	**Session Co-Chairs** **Qianwen (Wendy) Chen – Broadcom, Inc.** **Email: wendy.chen@broadcom.com** **Bo Song – HP Inc.** **Email: bo.song@hp.com**
1. 2:00 PM - Development of a Low Temperature Sinterable Cu Paste Based On Micro Scale Flake *Rocky Kumar Saha, Hamza Bin Aqeel, Gordon Elger – Technical University of Applied Science Ingolstadt; Thomas Rubenbauer – Schlenk; Jens Heilmann, Bernhard Wunderle – Chemnitz University of Technology*	***1. 2:00 PM - Process Development and Characteristics of Small-Diameter (<3 µm), Cobalt-Filled Through Silicon Vias (TSVs) For High-Density 3D Chip Stacking*** *Xinyi Zhang, Shuhang Lyu, Thomas Beechem, Tiwei Wei – Purdue University*	***1. 2:00 PM - Direct Bonding of Porous Cu Bumps Fabricated Using Gas Treatment of Cu-Sn Bumps*** *Zilin Wang, Wenjie Zhao, Ziqing Wang, Zheyao Wang, Xiuyu Shi – Tsinghua University*
2. 2:20 PM - Novel Metal Based Thermal Interface Materials for Flip Chip Ball Grid Array Packages *Karthik Visvanathan, Arifur Chowdhury, Sachin Deshmukh, Sergio A Chan Arguedas, Krishna Vasanth Valavala, Luisa Cabrera Maynez – Intel Corporation*	***2. 2:20 PM - Are Voids Restricted to Cu-Cu bonding Interface? Truth Revealed by CEY-Scanning Transmission X-Ray Microscopy*** *Murugesan Mariappan – NICHe; Shohei Yamashita – High Energy Accelerator Research Organization (KEK); Takafumi Fukushima – Tohoku University*	***2. 2:20 PM - Enabling 10 µm Die-to-Die Pad Pitch in Flexible Fan-Out With TrueAdaptTM*** *Golam Sabbir, Subu Iyer, Jui-Han Liu – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS); Henry Sun – University of California, Los Angeles*
3. 2:40 PM - Chiplet Package for Automotive and Edge Processors *Trent Uehling, Eli Tiffin, Stan Cejka, Nikhita Baladari, Gaurav Sharma – NXP Semiconductor, Inc.*	***3. 2:40 PM - Ultra-Fast Cu/Polymer Hybrid Bonding With Electroless Passivation Layer for Cost-Effective High I/O Interconnection Stacking*** *Yu-Lun Liu, Tzu-Yu Chen, Chun-Ta Li, Jia-Rui Lin, Yi-Hsuan Chen, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Kazuaki Ebisawa, Makiko Irie, Ya-Chien Chuang, Hsiao-Wei Yeh, Satoshi Fujimura – Tokyo Ohka Kogyo Co., Ltd.*	***3. 2:40 PM - Novel Thick Dry Film Photoresist and Process Optimization for High-Aspect Cu Pillar Patterning*** *Hajime Furutani, Junya Kosaka, Masatoshi Ikemi, Masayuki Kishino, Masaya Toba – Asahi Kasei Corporation*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Texas Foyer		
4. 3:45 PM - Study of the Optimal Cu Core Size Based on Surface Evolver for Solder Bridge and HiP Free of Large PBGA Package *Hojin Seo, Junho Lee, Insik Han – Samsung Electronics Co., Ltd.*	***4. 3:45 PM - X64 UCIe Chiplet Interconnection at 32 GT/s on a Silicon Core Substrate*** *Steven Verhaverbeke, Han-Wen Chen, Seann Ayers – Applied Materials, Inc.; Farhang Yazdani – BroadPak Corporation*	***4. 3:45 PM - Study of 2 x 4 µm Pitch Capsule Shaped TSVs and 2 µm Pitch TSVs in WoWoW Integration*** *Masaki Haneda, Takuhiro Miyawaki, Yukari Fukumizu, Kosei Kubota, Kan Shimizu, Hayato Iwamoto, Yoshihisa Kagawa – Sony Semiconductor Solutions Corporation*
5. 4:05 PM - Localized Formation of Laser Non-Conductive Paste (NCP) on 10 µm Diameter Bumps, Applied to 20 µm Pitch Chiplet Chip-on-Wafer (CoW) Bonding *Jungho Shin, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ji-Eun Jung, Ga-Eun Lee – Electronics and Telecommunications Research Institute*	***5. 4:05 PM - Study of High-Density Optical Redistribution Layer Enabling Advanced Chiplet Edge Bandwidth Density on Active Optical Package Substrate*** *Akihiro Noriki – AIST; Fumi Nakamura, Satoshi Suda, Tadashi Murao, Haruhiko Kuwatsuka, Takeru Amano – National Institute of Advanced Industrial Science and Technology*	***5. 4:05 PM - Bottom-Up Electrodeposition of Small Diameter, High Aspect Ratio Nanotwinned Copper-Filled Through-Silicon Vias for Ultra High-Density 3D Integration*** *Yuchen Bao, Shuhang Lyu, Tiwei Wei – Purdue University*
6. 4:25 PM - Mechanical and Electrical Evaluation of Materials for High Temperature Applications On Low CTE AlN Ceramic Substrates *Mousa Al-Zanina, Erik Busse, Emuobosan Enakerakpo, Stephen Gonya, Mohammed Alhendi, Mark Poliks – Binghamton University; David Lin, Cathleen Hoel, David Shaddock, Linda Boyd, Sreya Paladugu – General Electric Global Research*	***6. 4:25 PM - A Study About Bonding Properties With Multilayer Porous Structures for Fine Pitch Interconnection*** *Takuma Nakagawa, Daiki Furuyama, Takuma Katase, Sho Nakagawa – Mitsubishi Materials Corporation*	***6. 4:25 PM - Dry Film Photo-Imageable Dielectric Enabling Glass Core Substrate TGV Filling and Build-Up*** *Yaming Jiang, Patrick Huang, Jason Chuang, George Yen, Zhou Lu, Colin Hayes, Chris Gilmore, LiYen Lin – DuPont*
7. 4:45 PM - Analysis And Optimization Of Multi-Channel E-Mode AlGaN/GaN Trigate FinFET - Design Space Exploration and Optimization for Vertical Power Delivery With Embedded Power Converters *Ayoub Sadeghi, Inna Partin-Vaisband – University of Illinois*	***7. 4:45 PM - Massive Orthogonal Stacking Assembly of IC (MOSAIC) Cube With Inductive Coupling for Exascale Memory Applications*** *Masaya Kawano, Yuki Mitarai, Mototsugu Hamada, Tadahiro Kuroda, Atsutake Kosuge – University of Tokyo; Hiroyuki Hashimoto, Takafumi Fukushima – Tohoku University; Hiroshi Hosokawa, Jumpei Fujikata – EBARA Corporation; Hiroshi Kikuchi – Yamaha Robotics Holdings Co., Ltd.*	***7. 4:45 PM - Development of Via-First TSV and Backside Interconnect Process for Large-Scale Superconducting Quantum Annealing Circuits*** *Naoya Watanabe, Yuuki Araga, Katsuya Kikuchi – National Institute of Advanced Industrial Science and Technology; Ayuka Morioka, Kunihiko Ishihara, Tomohiro Nishiyama – NEC Corporation*

PROGRAM SESSIONS: FRIDAY, MAY 30, 2:00 P.M. - 5:05 P.M.

Session 34: Reliability of Interconnects in Advanced Packaging	Session 35: High-Performance Antenna and RF Design	Session 36: Modeling Driven Packaging and Process Advancements
Committee: Applied Reliability	**Committee: Electrical Design and Analysis**	**Committee: Thermal/Mechanical Simulation & Characterization**
Texas 1-3	**Dallas 5-7**	**San Antonio 4-6**
Session Co-Chairs **Seung-Hyun Chae – SK hynix Inc.** **Email: seunghyun1.chae@sk.com** **Yan Li – Samsung Semiconductor, Inc.** **Email: yanli7274@gmail.com**	**Session Co-Chairs** **Harrison Chang – Advanced Semiconductor Engineering, Inc. (US) / Email: Harrison_Chang@aseglobal.com** **Sungwook Moon – Samsung Electronics Co., Ltd.** **Email: sw2013.moon@samsung.com**	**Session Co-Chairs** **Christopher Bailey – Arizona State University** **Email: christopher.j.bailey@asu.edu** **Suresh K. Sitaraman – Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 2:00 PM - Impact of Current stressed SAC305 and Sn-Bi Interconnect Anode and Cathode Side Thermo-Mechanical Stability *Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna – Cisco Systems, Inc.; Young-Woo Lee, Hui-Joong Kim, Seul-Gi Lee – MK Electron Co., Ltd.; Choong-Un Kim – University of Texas, Arlington*	***1. 2:00 PM - 3D Vertical Glass Stacking for 6G Communications - Interconnect Fabrication and Broadband Characterization*** *Xingchen Li, Lakshmi Narasimha Vijay Kumar – Georgia Institute of Technology; Madhavan Swaminathan – Pennsylvania State University*	***1. 2:00 PM - Warpage Simulation and Experimental Validation of The X-Dimension Fan-Out Integration-Bridge (XDFOI-B) Wafer Level Packaging Process*** *Jian Cheng, Liping Zhu, Cheng Yang, Haijie Chen, Boping Wu – JCET Group Co. Ltd.*
2. 2:20 PM - Toward a Comprehensive Understanding of Electromigration Under AC Loads Impacting Microstructure and Reliability of SAC Solder Interconnects *Hariram Mohanram – University of Texas at Arlington; Yiram Kim – United Test and Assembly Center, Ltd.; Choong-Un Kim – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.*	***2. 2:20 PM - Multi-Disciplinary Design Optimization of High-Speed Ceramic LCCC Package Through Automated Simulation*** *Li Jiang, Guangxu Li, Jie Chen, Rajen Murugan, Muhammad Khan – Texas Instruments, Inc.*	***2. 2:20 PM - Multi-Layer Sequential Fabrication and Mechanics-Based Model of Glass-Core Packages With Embedded Dies*** *Alexander King, Kyoung-Sik Moon, Mohan Kathaperumal, Muhannad Bakir, Suresh K. Sitaraman – Georgia Institute of Technology*
3. 2:40 PM - Deterioration of Electromigration Reliability in Microbumps due to Severe Side Wall Wetting *Yifan Yao, Yuanxing Duan, Yuxuan An, K. N. Tu, Yingxia Liu – City University of Hong Kong; Songpeng Zhao, Yuzheng Guo – Wuhan University*	***3. 2:40 PM - On-Chip Shoelace Fully Integrated Inductor*** *Yushu Zhao, Yousef Safari – McGill University; Boris Vaisband – University of California, Irvine*	***3. 2:40 PM - A Novel Fracture Mechanics Technique on Studying Passivation Crack Behavior for Advanced Si Package With Aluminum Redistribution Layer (Al-RDL) Routing*** *Kuo-Chin Chang, Shao-Chen Tseng, Chieh-Hao Hsu, Wei-Hsiang Tu, Chang-Fu Han, Jyun-Lin Wu, Mirng-Ji Lii, Cheng-Sian Chen, Kathy Yan, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Texas Foyer		
4. 3:45 PM - Prediction of Effect of Bi-Addition in SnAgCu Solders on High Strain Rate Properties *Vishal Mehta, Pradeep Lall, Jeffrey Suhling – Auburn University; David Locker – US Army*	***4. 3:45 PM - Terahertz 300 GHz Antenna in Package for 6G Applications*** *Mei Sun – Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR); Teck Guan Lim – Institute of Microelectronics A*STAR*	***4. 3:45 PM - Interface Reliability of Advanced Packaging Under Sequential Stresses of High-Temperature and Temperature-Humidity in Automotive Environments*** *Pradeep Lall, Padmanava Choudhury, Aathi Pandurangan, Madhu Kasturi, Jeffrey Suhling – Auburn University*
5. 4:05 PM - Low Temperature Solder Reliability Study for Photonics Packages *Nokibul Islam – STATS ChipPAC, Ltd.; Wallace Zhong, Cheng Yang – JCET Group Co. Ltd.*	***5. 4:05 PM - Integration of D-Band 140 GHz III-V Components Transceiver in Embedding PCB-Based Technology*** *Tekfouy Lim, Stefan Kosmider, Kavin Senthil Murugesan, Thi Huyen Le, Marius Van Dijk, Johannes Jaeschke, Ulrike Gasnesh – Fraunhofer IZM; Ivan Ndip – Brandenburg University of Technology/Fraunhofer IZM*	***5. 4:05 PM - Design and Manufacture of Integrated Passive Devices in Coreless Package Substrates for Power Applications.*** *Sylvester Ankamah-Kusi, Guangxu Li, Jonathan Noquil, Ayi Calma, Rajen Murugan, Jason Colte – Texas Instruments, Inc.*
6. 4:25 PM - Challenges and Solutions for Measuring Copper-Polymer Interfacial Adhesion Strength in RDL of Advanced Packaging *Wu-Lung Wang, Hsin-Chih Shih, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chin-Li Kao, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)*	***6. 4:25 PM - Designing Antennas and RF Components at 110-330 GHz Using IPD Technology*** *Muhammad Ibrahim, Kimmo Rasilainen, Aarno Paerssinen, Marko E. Leinonen – University of Oulu; Jan Saijets, Pekka Rantakari – VTT Technical Research Centre of Finland*	***6. 4:25 PM - Simulation of Mechanical Cu Pad Expansion Mechanism and Measures to Increase Expansion*** *Takaaki Hirano, Taichi Yamada, Yuriko Yamano, Naoki Komai, Takumi Onodera, Yukako Ikegami, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation*
7. 4:45 PM - Influence of Doping on the Electromigration Performance of SAC Solder Alloys on BGA Components *Karthik Arun Deo, Junbo Yang, Yangyang Lai, Dalei Yang, Seungbae Park – Binghamton University*	***7. 4:45 PM - G-Band Micromachined 4x1 & 8x1 Crossed Linear Array Antennas*** *Alexander Wilcher, Shreya Sahai, Payman Pahlavan, David Arnold, Yong-Kyu Yoon – University of Florida; Alex Phipps, Jia Chieh – Naval Information Warfare Center*	***7. 4:45 PM - Assessing Solder Joint Reliability Under Multi-Shock Loading by a Cohesive Zone Approach With Irreversible Damage Progression*** *Krishna Kiran Talamadupula, Ning Ye – Sandisk Technologies, Inc.; Bo Yang – Western Digital Corporation*

INTERACTIVE PRESENTATIONS: WEDNESDAY, MAY 28, 10:00 A.M. - 12:00 P.M. AND 2:30 P.M. - 4:30 P.M.

Wednesday, May 28
10:00 AM - 12:00 PM

Session 37: Interactive Presentations 1

Committee: Interactive Presentations

Texas Pre-Function

Session Co-Chairs
Joshua Dillon
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1. Temperature Experiments for a 3D-Printed Encapsulated Thermal MEMS Wind Sensors Under Low Pressure
Sicun Duan, Zongyuan Cao, Zhenxiang Yi, Ming Qin, Qing-An Huang – Southeast University

2. Deep Learning Enhanced Thermal Simulation for Efficient Semiconductor Layout Design Using Thermal Twin
Bin He, Gongyue Tang – Institute of Microelectronics A*STAR; Weiyang Miao– Nanyang Technological University

3. Architecting the Thermal Dissipation and Power Delivery for Large-Scale Systems and Experimental Demonstration of the Segmented Cooling for Silicon Thermal Dielets With a Power Density of 1 W/mm2
Haoxiang Ren, Ben Yang, Naarendharan Sundaram, Timothy Fisher, Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS); Dongkai Shangguan – Thermal Engineering Associates, Inc.

4. Corrosion Analysis of the Electrode Coating in Film Capacitors for Power Electronics Applications
Sandy Klengel, Robert Klengel, Carola Klute, Bolko Muhs-Portius – Fraunhofer IMWS

5. Electromigration Lifetime Improvement of Ball Grid Array Solder Joints for High Performance Computing Applications
Cameron Drewes, Andrea Molina Moreno, Miftahul Nabila, Kaitlyn Munoz, Tengfei Jiang – University of Central Florida; Jeng Hau Huang – National Taiwan University; Omar Ahmed – Juniper Networks

6. Interconnect Reliability for Single-Step Sintered Die Stack
Nikhil Gupta, G. Q. (Kouchi) Zhang – Delft University of Technology; Sebastian Quednau – Nanowired GmbH; Sandy Klengel, Robert Klengel – Fraunhofer IMWS; Robin Simpson, Rene Poelma, Nick Liu – Nexperia

7. Comparison of Mechanical Response and Failure Characteristics of Selected SnAgCu-Based High-Temperature Solder Alloys
Sean Lai, Lijia Xie, David Halbrooks, John Blendell, Carol Handwerker, Ganesh Subbarayan – Purdue University; Morgana Ribas – MacDermid Alpha

8. Rapid Estimation of Anisotropic Thermal Conductivity in RDL for 2.5D Chiplet Designs
Sridhar Narayanaswamy, Dingjie Lu, Wenzu Zhang, Richard Xian-Ke Gao, Mihai Rotaru, Dutta Rahul – Institute of Microelectronics A*STAR; Jun Liu, En-Xiao Liu – Institute of High Performance Computing A*STAR

9. A Novel Methodology for Characterizing and Validating Viscoelastic and Thermal Expansion Properties of Polymer Films
Hung-Yun Lin, Alexander Gamez – Texas Instruments, Inc.

10. Enhancing Reliability of Multi-Chip Modules by Using the Reinforcement Mechanisms of Side-Fill Technology
Chang-Chun Lee, Kai-Cheng Lin – National Tsing Hua University; Shen-Yu Yang, Chao-Chieh Chan, Chun-Wei Wang, Yu-Ju Chen – Wistron NeWeb Corporation

11. Characterization of Coupled Mechanical and Electrical Behavior of Porous Conductive PDMS-CNT/Graphene Based Foams Under Multidirectional Strain for Flexible/Stretchable Electronics
Nicholas Ginga, Nathan Morgan – University of Alabama in Huntsville

12. Leveraging AI to Enable High-Fidelity Modeling of Substrate Thermo-Mechanical Behavior
Mitchell Page, Raquel de Souza Borges Ferreira, Edvin Cetegen, Doruk Aksoy, Nicholas Haehn – Intel Corporation

13. Artificial Intelligence-Based Warpage Prediction Model for Accelerating Thermo-Mechanical Simulation in Advanced Packaging
Jungeon Lee, Daeil Kwon – Sungkyunkwan University; Sun-Woo Lee, Taek-Soo Kim – Korea Advanced Institute of Science and Technology

14. Fast and Accurate Machine Learning Prediction of Back-End-Of-Line Thermal Resistances in Backside Power Delivery and Chiplet Architectures
Prabudhya Roy Chowdhury, Dureseti Chidambarrao – IBM Research; Aakrati Jain – IBM; Atsushi Ogino, Kartik Acharya – IBM Corporation

15. A Flexible and Scalable Thermal Test Vehicle Design for Electronics Cooling Solutions
Logan Horowitz, S. Tahmid Mahbub, Jiarui Zou, Robert Pilawa-Podgurski – University of California, Berkeley

16. An Effective 3D Thermal Network Integrated With Deep Learning for Improved Prediction of the 3D Thermal Properties of Complex Packaging Patterns
Jeong-Hyeon Park, Eun-Ho Lee – Sungkyunkwan University; Jaechoon Kim, Suk Won Jang, Sungho Mun – Samsung Electronics Co., Ltd.

17. Thermal Analysis and Design Guideline of Massive Orthogonal Stacking Assembly of IC (MOSAIC) Cube With Bump Connection Enabling SoC-DRAM Direct Stacking
Hung-Chih Huang, Yuki Mitarai, Masaya Kawano, Mototsugu Hamada, Atsutake Kosuge – University of Tokyo

18. Raman and X-ray Imaging Based Thermo-Mechanical Characterization of Metal-Embedded Chip Assembly
Faharia Hasan Bhuiyan, Haohan Guo, Shubhra Bansal – Purdue University; Christina Seeholzer, Clayton Tu, John Carlson, Christopher Roper – HRL Laboratories, LLC

19. Applying GA-NN and Explainable AI for IC Packaging Warpage Optimization: A Case Study on Product Feature
Yan-Cheng Lin, I-An Shou, Hung-Kai Wang – National Cheng Kung University; Tang-Yuan Chen, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung – Advanced Semiconductor Engineering, Inc.

20. A Computational Framework to Predict the Maximum Possible Warpage Due to Package-to-Package Variations
Sharan Kishore – NXP Semiconductor, Inc.; Sandeep Shantaram – Independent Researcher; Bernd Buettner, Rene Kallmeyer – ANSYS, Inc.

21. Thermal Characterization of HBMs Integrated via Hybrid Bonding
Huicheng Feng, Yong Han, Gongyue Tang, Ling Xie, Nagendra Sekhar Vasarla – Institute of Microelectronics A*STAR

22. An Efficient Data Augmentation and Semantic Segmentation Framework for 3D Defect Detection of HBMs
Yang Yu, Jie Wang, Richard Chang, Ramanpreet Pahwa, Xulei Yang – Institute for Infocomm Research A*STAR; Ser Choong Chong – Institute of Microelectronics A*STAR

23. Warpage Control Mechanism Study of Stiffener on Al Chip IC Packaging
Wei Gong, Shaoyin Guo, Shaojuan Yu, Cih Cheng, Berkan Alanbay, Babak Ashourirad, Taylor Gaines, Hailan Gong – Intel Corporation

24. Digital Design of Inter-Die Gap Fill Dielectric Film Processing for C2W Hybrid Bonding Using Finite Element Modelling
Sasi Kumar Tippabhotla, Mishra Dileep, Nagendra Sekhar Vasarla, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR

25. Mitigation of Wafer-to-Wafer Bonding Distortions Through Accelerated Simulations and Measurements
Oguzhan Orkut Okudur, Serena Iacovo, Shuo Kang, Deewakar Sharma, Mario Gonzalez, Eric Beyne – imec

Wednesday, May 28
2:30 PM - 4:30 PM

Session 38: Interactive Presentations 2

Committee: Interactive Presentations

Texas Pre-Function

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1. Flexible Glass Electrical Characterization Using Aerosol Jet Printing
Ethan Kepros, Bhargav Avireni, Sambit Kumar Ghosh, Premjeet Chahal – Michigan State University

2. Bio-Packaging Development of a Wearable Fluidic Monitoring System for Improved Blood Glucose Management in Critically Ill Diabetic Patients
Ruiqi Lim, James Ven Wee Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

3. Parasitic Extraction and Signal Integrity Analysis of Memristor-Based Crossbar Arrays for Neuromorphic Computing
Tahsin Shameem, Zohreh Salehi, Jose Schutt-Aine – University of Illinois at Urbana-Champaign; Hanzhi Ma – Zhejiang University; Yi Zhou – University of Illinois at Urbana-Champaign

4. Broadband Optical Engine (BOE) System Integration by Wafer Level Process in HPC/AI Era
K.H. Lo, Y.R. Liang, T.W. Chen, Edward Lin, S.W. Liang, J.Y. Gene Wu, C.J. Wang, S.W. Lu – Taiwan Semiconductor Manufacturing Company, Ltd.

5. Cost-Effective Package Design for a Chiplet Interfaces on Organic Substrates Using Low Cost Design Rules
Chungju Kim, Taisik Yang, Yongseok Kang – LG Electronics

6. Signal and Power Integrity Optimization in 2.XD Packaging Using Novel RDL Bridge Die and Copper Pillar Interconnects for Wide I/O Applications
Youngeun Na, Soo Jeong Kim, Yeon Ji Shin, Hong Seok Kim, Sang Yeul Yeum, Jae-Sung Lim – HANA Micron, Inc.; SangYul Ha – Myongji University; Woojin Lee – Swevenz Inc.

7. Systematic Crosstalk Reduction Method for PAM4 Transmission on PCIe Lopro FPIO Connectors
Kewei Song, Yulin He, Haonan Wu, Milton Feng – University of Illinois

Wednesday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Texas Pre-Function

INTERACTIVE PRESENTATIONS: WEDNESDAY, MAY 28, 2:30 P.M. - 4:30 P.M. AND THURSDAY, MAY 29, 10:00 A.M. - 12:00 NOON

8. A Dual Mode BLS/LFR Microscope for Local Mechanical Property Imaging for Semiconductor Packaging Materials
Sebastian Engmann – Theiss Research; Andrew Gayle, Christopher Soles, Chris Michaels – National Institute of Standards and Technology

9. Packaging and Integration of Multifunctional Brain Computer Interface
Ziqi Jia, Yong-Kyu Yoon – University of Florida

10. A K-Band Circularly Polarized Antenna for Short Range Communication Applications
Mohd Rasoul Masadeh, Amanpreet Kaur – Oakland University

11. Design Enablement Methodology for 3D Stacked RF Systems
Raju Mani, Dutta Rahul, Tengiz Svimonishvili, Mihai Rotaru – Institute of Microelectronics A*STAR

12. Leveraging Advanced Packaging for IP Protection in Heterogeneous AI Hardware

Md Saad Ul Haque, Jingbo Zhou, Farimah Farahmandi, Mark Tehranipoor – University of Florida

13. A Compact Dual Band (28/39 GHz) 1x4 Antenna Array Design With Frequency Selective Surface-base (FSS) for 5G AiP Applications
Sheng-Chi Hsieh – Advanced Semiconductor Engineering (ASE Group), Inc. Kaohsiung

14. Large-Scale Spaceborne Deployable Active Phased Array Antenna Design Using Rigid Flexible Board for LEO Satellite Constellation
Hiroki Hayashi, Yasuto Narukiyo, Delburg Mitchao, Sena Kato, Takeshi Ota, Keito Yuasa, Wang Xiaolin, Jil Mayeda – Institute of Science Tokyo

15. A 6G Terahertz 256-Element Dual-Polarized MIMO Antenna Array With Low-Profile and Broadband
Xin Zhang, Qidong Wang, Yuxiang Zheng – Institute of Microelectronics of the Chinese Academy of Sciences

16. Time-Efficient Eye-Opening Estimation Method for High-Bandwidth Memory Interface Design With Equalizers
Joonhyun Kim, Sungwook Moon – Samsung Electronics Co., Ltd.; Yongho Lee – Samsung Foundry

17. Machine Learning-Optimized Metasurface Matching Layer for Enhanced Deep Fat Sensing Using PDMS and FEP
Alfredo Bayu Satriya, James Overmeyer, Yong-Kyu Yoon, Myles Joshua Tan – University of Florida

18. Prediction of Cross Section Images and Optimization of Processes With Neural Network
Kohei Motojima, Hayato Sugiyama, Kaede Ameyama, Chiho Ueta – Taiyo Holdings Co., Ltd.

19. AI-Driven Automatic Routing for UCIe Bridge With Heterogeneous Configurations in Advanced System-in-Package
WEIYANG MIAO, Chuan Seng Tan – Nanyang Technological University; Wang Ling Goh – Nanyang Technological University; Raju Mani, Mihai Rotaru – Institute of Microelectronics A*STAR

20. Additive Manufacturing of Passive Electronic Components Using Aerosol Jet Printing and Reliability Tests for Spaceborne Applications
Abdullah Obeidat, Emuobosan Enakerakpo, Erik Busse, Ashraf Umar, Riadh Al-Haidari, Mohammed Alhendi, Mark Poliks – Binghamton University; Matthew Erdtmann, Adrian Pyke – Micro-Precision Technologies, Inc.

21. Novel Wireless PVDF-PEDOT:PSS/LIG Based Wearable Multimodal Sensing Platform
Reshmi Banerjee, Ghaleb Al-Duhni, Raj Pulugurtha – Florida International University

22. Micro-3D-Printed Antenna-in-Package Substrates With Quasi-Coaxial Through Vias
Nahyeon Kim, Haksoon Jung, Yurim Choi, Yongwoo Lee, Jimin Kwon – Ulsan National Institute of Science & Technology; Yunsik Park – Korea Electronics Technology Institute; Seungyeon Koh, Hyeok Kim – University of Seoul

23. Advanced Characterization of the Cure Kinetics of a Liquid Encapsulant
Anthony Kotula, Ran Tao, Jianwei Tu, Young Jong Lee, Gale Holmes – National Institute of Standards and Technology

24. Surface Smoothing Based on Au Thin Film Transfer on Rough-Surface AlN Ceramic Substrates for Low-Temperature Bonding
Shintaro Goto, Kai Takeuchi, Shogo Koseki, Eiji Higurashi – Tohoku University

25. Capping Layers for Enhanced Crystallinity of Single-Crystal Germanium on Insulator in Monolithic 3D ICs
Yu-Ming Pan, Ching-Lin Chen, Hao-Tung Chung, Chiao-Yen Wang, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Nien-Chih Lin, Chih-Chao Yang, Chang-Hong Shen – Taiwan Semiconductor Research Institute

26. Novel Optical Chiplet Structure Based on MCeP®
Yuji Furuta, Motoyuki Fukuhara, Tatsuaki Denda, Hisashi Kaneda, Tomoharu Fuji – Shinko Electric Industries Co., Ltd.

27. Enabling Heterogeneous Integration of Optoelectronic Circuits via Die-to-Die Low-Temperature Bonding With Ultrathin dielectrics.
Yi Xuan Yeo, BG Sajay, Leong Ching Wai, Ser Choong Chong, Andrew Whye Keong Fong, Hemanth Kumar Cheemalamarri – Institute of Microelectronics A*STAR

Thursday, May 29
10:00 AM - 12:00 Noon

Session 39: Interactive Presentations 3

Committee: Interactive Presentations

Texas Pre-Function

Session Co-Chairs
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Kristina Young
Synopsys, Inc.
Email: kristina.youngfisher@gmail.com

1. An Innovative Flux-Less Solder Ball Attachment Technology (FLAT) for Advanced BGA Assembly
Dongjin Kim, Seonghui Han, Sang Eun Han, Donggyu Choi, Sehoon Yoo – Korea Institute of Industrial Technology; Eunchae Kim, Kwansik Chung – Prinsol Co., Ltd

2. Technology for Forming Micro Vias Smaller Than 20 µm With Low Surface Roughness on Build-Up Films Using UV Nanosecond Laser Drilling and Plasma Desmearing
Nam Son Park, Tae-Young Lee, Sung Yong Kim, Sung Yoon Lee, Sang-a Yoon – Tech University of Korea; Mun Sang You, Geonhee Lee – SIMMTECH; Sehoon Yoo – Korea Institute of Industrial Technology

3. Fabrication of D-band (140 GHz) Broadband Antenna Using Quartz Glass on Silicon Hybrid Bonded Wafer With Cavity
Kentaro Tani, Naotake Okada, Masato Tokai, Shoichiro Yamaguchi, Jungo Kondo, Makoto Iwai – NGK Insulators, LTD./NGK Europe GmbH; Uwe Maaß, Alexander Gäbler, Wojciech Partyka – Fraunhofer IZM; Ivan Ndip – Brandenburg University of Technology/Fraunhofer IZM

4. The Role of Surface Preparation and Bonding Parameters in Improving Hybrid Bonding Quality
Injoo Kim, Siye Lee, Jinho Jang, Minji Kang, Hyein Jin, Sungdong Kim – Seoul National University of Science and Technology

5. High Precision Large Reticle Thermo-Compression Bonding for Advanced Packaging for AI Era
Shripad Gokhale, Kartik Srinivasan, Shan Zhong, Anurag Tripathi – Intel Corporation

6. Electrical Performance of 2-Platen CMP Process for Hybrid Bonding Application With Conventional / nt-Cu and Low Temperature of SixNy / SixOy Dielectrics
Trianggono Widodo, Karan Prabhakar, Xavier Brun – Intel Corporation; Prayudi Lianto, Jing Xu, Avery Tan, Patrick Lim, Guan Huei See – Applied Materials, Inc.

7. IR Laser Debonding for Silicon Based Temporary Carrier Systems Enabling 2.5D and 3D Chiplet Integration Processes
Peter Urban, Simon Halas, Julian Bravin, Thomas Uhrmann, Markus Wimplinger – EV Group; Francois Chancerel, John Slabbekoorn, Steven Brems – imec

8. Hydrophobic Barrier for Controlled Epoxy Keep-Out-Zone in Flip Chip Assembly
Paul Kim, John C. Decker, Xiying Chen, Ziyin Lin, Ifeanyi Okafor, Ke Geng, Yiqun Bai, Hsin-yu Li – Intel Corporation

9. Accelerating Root Cause Identification of Subtle Bonding Failures With Microwave Induced Plasma
Charles Odegard, Liv Bonin, Daniel Scott – Texas Instruments, Inc.; Yashan Peng, Jiaqi Tang, Mark McKinnon – JIACO Instruments; Kees Beenakker – Delft University of Technology

10. Wet-Chemical Cu Cleaning for Fine-Pitch Hybrid Bonding
Kohei Nakayama – YOKOHAMA National University; Kenta Hayama, Fabiana Tanaka, Fumihiro Inoue – Yokohama National University; Sven Dewilde, Steven Deckers, Nancy Heylen, Harold Philipsen – imec; Yoichi Tanaka, Yusuke Okazaki, Nobuko Gan, Hideaki Iino – Kurita Water Industries Ltd.

11. Evaluation of Printed Materials for Flexible Hybrid Electronic (FHE) Interconnections and Packaging
Babatunde Falola, Riadh Al-Haidari, Udara Somarathna, Olya Noruz Shamsian, Bryan Cabrera, Mohammed Alhendi, Mark Poliks – Binghamton University; Gurvinder Singh Khinda – GE HealthCare

12. Rigid-to-Flex Interconnection for Flexible Hybrid Electronics Integration Using Anisotropic Conductive Adhesive
Riadh Al-Haidari, Babatunde Falola, Zhi Dou, Mark Schadt, Mohammed Alhendi, Mark Poliks – Binghamton University; Ekaterina Dvoretskaya, Andrew Stemmermann – SunRay Scientific, Inc.

13. A Mild Surface Activation Under Redox Gases Using Vacuum Ultraviolet Irradiation for Interconnection of Semiconductor Packaging
Shinichi Endo – Ushio, Inc.

14. Demonstration of a Fully Integrated, High Bandwidth, Active Flexible Connector for Large Area Computational Systems
Randall Irwin, Joanna Fang, Subramanian Iyer – University of California, Los Angeles

15. A High Throughput Low-Temperature Copper-Copper Thermal Compression Bonding Scheme Using Tin Passivation
Tanmay Konnur, Krutikesh Sahoo, Randall Irwin, Vineeth Harish, Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

16. Advanced Face-To-Back CoW 2.0 µm Pitch Cu-Cu Hybrid Bonding Process for Three Layer-Stacked 3D Heterogeneous Integration.
Akihiro Urata, Takahiro Kamei, Itsuki Imanishi, Masanori Chiyozono, Toru Osako, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation; Yoshihisa Kagawa – Sony

Wednesday & Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Texas Pre-Function

INTERACTIVE PRESENTATIONS: THURSDAY, MAY 29, 10:00 A.M. - 12:00 NOON AND 2:30 P.M. - 4:30 P.M.

17. Process Approaches to Enable 200 °C Hybrid Bonding With SiCN Bond Layer and 0.5 µm Pitch
Kai Ma, Nikolaos Bekiaris, Eric J Bergman, Santosh Kumar Rath, Lei Xue – Applied Materials, Inc.; Taotao Ding, Barbara Weis, Gernot Probst – EV Group

18. High-Quality Cu µ-Joints by High-Throughput Contactless Hot-Isostatic-Pressure (HIP) Annealing for Chip-to-Wafer and Wafer-to-Wafer Hybrid Bonding
Murugesan Mariappan – NICHe; Mototaka Ochi – Kobe Steel; Takafumi Fukushima – Tohoku University

19. Fabrication of Panel-Level Redistribution Interposer With 1.5/1.5 µm Multilayer Fine Wiring and Solutions to Issues of Miniaturization
Masashi Minami, Sachiko Matsushita, Sasakura Yuuna, Sadaaki Katoh – Resonac Corporation

20. Polyimide Fine Via and Trench Formation Based on Plasma Etching Technology for RDL Interposer
Fumito Ootake, Kenta Doi, Yasuhiro Morikawa – ULVAC, Inc.

21. Development and Characterization of Electrodeposited Tin-Indium Alloy Microbumps for Low Temperature Assembly
Tsvetina Dobrovolska, Martin Mack, Klaus Leyendecker – Umicore Galvanotechnik GmbH; Kevin Martin – Umicore EP USA; Aleksandar Radisic, Ehsan Shafahian, Zaid El-Mekki, Punith Kumar Mudiger Krishne Gowda, Jaber Derakhshandeh, Herbert Struyf – imec

22. Effect of Dimension on Thermal Expansion of Cu Pads in SiO2 Vias for 3D IC Fine-Pitch Hybrid Bonding
Pin-Lin Chen, Chih Chen – National Yang Ming Chiao Tung University

23. Impact of Temporary Substrates and Adhesives on Die-to-Wafer Overlay
Koen Kennes, Pieter Bex, Ye Lin, Samuel Suhard, Dieter H. Cuypers, Alain Phommahaxay, Gerald Beyer, Eric Beyne – imec

24. Patterning of Sub 1 µm Critical Dimension TSV for 2.5 µm pitch 2.5D/3D hybrid bonding Applications
Arvind Sundaram, Chandra Rao B. S. S. – Institute of Microelectronics A*STAR

25. Process Development, Challenges, and Strategies for Void-Free Multi-Chip Stacking in Hybrid Bonding Applications
Ser Choong Chong, Ling Xie, Nagendra Sekhar Vasarla, Mishra Dileep, Chandra Rao B. S. S., Vempati Srinivasa Rao – Institute of Microelectronics A*STAR

26. Ozone-Ethylene Radical Activation of SiCN/Cu Without Water Rinsing for Hybrid Bonding
Bungo Tanaka, Tetsu Tanaka, Takafumi Fukushima – Tohoku University; Murugesan Mariappan – NICHe; Soichiro Motoda, Tetsuya Nishiguchi – Meiden Nanoprocess Innovations, INC.

27. Environmentally Friendly Cu Post Technology, Based on Laser-Assisted Bonding With Compression (LABC) and Fume-Free Laser Solder Paste for Advanced 3D Interconnections
Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Jungho Shin, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ho-Gyeong Yun – Electronics and Telecommunications Research Institute

28. Through GaN Via for 3D Heterogeneous Strata Integration
Jui-Han Liu, Haoxiang Ren, Cheng-Ting Yang, Boris Vaisband, Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

29. Microbump Interconnections Using Vertical Wire Technology for the Power Connections between SoC and Substrate in Bridge Die-Based Packaging Platform
Ye-Jin Jang, Jin-Ho Lee, Yong-Gyu Jang, Sangkyu Jang, Na-Hyun Cho, Jin-Wook Jang – HANA Micron, Inc.

30. Novel Fault Isolation Methodology Applied on Nano-Scale Defect in Fine Line RDL for Advanced Fan-Out Package
Yi-Sheng Lin – Advanced Semiconductor Engineering, Inc. (Taiwan); Cheng-Hsin Liu, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung, Chun-Liang Kuo, Chia-Wen Hung – Advanced Semiconductor Engineering, Inc.

Thursday, May 29
2:30 PM - 4:30 PM

Session 40: Interactive Presentations 4

Committee: Interactive Presentations

Texas Pre-Function

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Ting Zheng
Marvell Technology, Inc.
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1. Improving the Uniformity of Cu Deposition in Fan-Out Panel Level Package With FEM Simulation Model
Yi-Lun Hung, Yung-Sheng Lin, Min-Yan Tsai, Mingtzung Kuo, Ling-yuan Chang, Ping-Feng Yang, C. P. Hung – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US)

2. Lithography-Free Anisotropic Magnetoresistance Sensor-Based Rotational Speed Measurement System on PEEK With Integrated Electronics
Tim Nils Bierwirth, Marc Wurz – Leibniz University Hannover/ Institute of Micro Production Technology; Sebastian Bengsch, Michael Werner – Ensinger GmbH; Eike Christian Fischer – Freelancer

3. Effect of Plasma Etching and Color Difference of the Molding Compound Surface on Adhesion in Electromagnetic Shielding
Soichi Homma, Daichi Okada, Akihito Sawanobori, Susumu Yamamoto – KIOXIA Corporation; Hiroshi Nishikawa – Osaka University

4. Integrated Passive Devices in the Silicon Interconnect Fabric
Haoxiang Ren, Zoe Chen, Cheng-Ting Yang, Jui-Han Liu, Boris Vaisband, Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

5. Parametric Analysis of Thermo-mechanical Behavior for HBM in System-In-Package Configurations
Hyunggyun Noh, Wonhong Choi, Woongkee Kim, Gunhee Bae, Yumi Sim, Seungyeon Kim, Yuchul Hwang – Samsung Electronics Co., Ltd.; Yunsung Lee – Samsung Foundry

6. A Highly Reliable Filling Method for Package-on-Package Utilizing Epoxy Flux
Kisu Joo, Kyojin Hwang, Heeseok Lee – Samsung Electronics Co., Ltd.

7. Holistic Insight Into the Effects of Diverse Surface Modification Methods on Difficult-to-Bond Resin Materials
Akihiro Shimizu – Ushio, Inc.

8. A Novel Disaggregated Approach of Assembling Integrated Heat Spreader for Advanced Packages
Arifur Chowdhury, Jaclyn Avallone, Bamidele Falola, Taylor Gaines, Haowen Liu, Peng Li, Sergio A Chan Arguedas, Aravindha R Antoniswamy – Intel Corporation

9. Characterization of FOWLP Process Using Temporary Bonding Material on Carrier With Very Low Die Shift
Tiffany Tang, Dieter H. Cuypers, Aldrin Vaquilar, Pieter Bex, Koen Kennes, Alain Phommahaxay, Eric Beyne – imec; Alice Guerrero – Brewer Science, Inc.

10. Wafer-to-Wafer Bonding With Saddle-Shaped Wafers
Shuo Kang, Serena Iacovo, Koen D´have, Oguzhan Orkut Okudur – imec; Anton Alexeev, Thomas Plach, Taotao Ding, Markus Wimplinger – EV Group

11. Novel Packaging Platform Based on Bridge Dies With Top and Bottom I/O Connections on Standard Substrates
Jae-Sung Lim, Sangkyu Jang, Yong-Gyu Jang, Yong-Nam Koh, Jin-Wook Jang, Jayden Donghyun Kim – HANA Micron, Inc.

12. Advanced Resin Material Enabling Room-Temperature Bonding for WoW and CoW 3DI Applications
Naoko Araki – Daicel Corporation; Tadashi Fukuda, Takayuki Ohba – Institute of Science Tokyo

13. Bond Wave Analysis of SiCN for Fine Pitch Hybrid Bonding
Ryosuke Sato, Hayato Kitagawa, Fumihiro Inoue – Yokohama National University; Atsushi Nagata, Yoshihiro Kondo – Tokyo Electron Kyushu, Ltd.; Kenichi Saito – Tokyo Electron, Ltd.; Jung Hwan Park, Chiwoo Ahn, Yeoun-Soo Kim, Jiho Kang – SK hynix Inc.

14. Characterization of Interfacial Fracture Strength in Hybrid Bonded Wafers: A Novel Approach for High-Resolution Spatial Profiling
Sathya Raghavan, Nicholas Polomoff, Katsuyuki Sakuma – IBM Research; Ben Yang – UCLA CHIPS

15. Laminate Materials With Excellent Co-Planarity and Dimensional Stability for Advanced 2.xD Package
Norihiko Sakamoto, Keita Johno, Kyousuke Sutou, Takayo Kitajima, Keitaro Iguchi, Yuji Mato – Resonac Corporation

16. Rapid Dendritic Amplification of Amino Groups on BN Surfaces for Enhanced Thermal Conductivity in Polymer Composites
Zihao Lin, Juwon Lim, Yu-Chieh Lin, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology

17. A New Wafer Level Package With Vertical Cu Post Stack for on-Device AI Solution
Woosang Jung, Sangkyu Lee, Haram Park, Eun Young Lee, Yieok Kwon, Myeonghan Bae, Jongyoun Kim, Wonkyung Choi – Samsung Electronics Co., Ltd.

18. Experimental Demonstration of High-Power Thermal Test Vehicle for Two-Phase Cooling for AI Datacenters, 5G RAN, and EDGE Compute Nodes
Yang Liu, Rishav Roy, David J. Apigo, Manohar Bongarala, Syed Faisal, Sarwesh Parbat, Todd Salamon, Mark Cappuzzo – Nokia Bell Labs

19. Addressing Key Process Challenges in Developing High Aspect Ratio TSVs up to 15 With 1 µm Critical Dimension
Van Nhat Anh Tran, Arvind Sundaram, Ya-Ching Tseng, Nandini Venkataraman, Zeng Wei Heng, Binni Varghese, B.S.S. Chandra Rao – Institute of Microelectronics A*STAR

20. Development of High Thermal Conductance Wafer Bonding Interface With PVD Aluminum Nitride
Andrew Tuchman, Ayuta Suzuki, Christopher Netzband, Joshua Greklek, Rinus Lee, Ilseok Son – TEL Technology Center, America, LLC

21. Electrolytic Copper Plating Process for Glass Substrates
Raihei Ikumoto, Hisamitsu Yamamoto, Shinji Tachibana, Yudai Kuramochi, Miho Kawanishi – C. Uyemura & Co., Ltd

Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Texas Pre-Function

INTERACTIVE PRESENTATIONS: THURSDAY, MAY 29, 2:30 P.M. - 4:30 P.M AND FRIDAY, MAY 30, 10:00 A.M. - 12:00 P.M.

22. The Formation of Microvia With a Diameter of 3.5 µm and an Aspect Ratio of 3 in Ajinomoto Build-up Film® (ABF) Using KrF Excimer Laser Ablation
Kanta Wataji, Akira Suwa, Yasufumi Kawasuji – Gigaphoton Inc.; Daisuke Hironiwa, Eiji Baba, Ryo Miyamoto – Ajinomoto Fine-Techno Co., Inc.

23. Efficient Utilization of Different Kinds of Superelements for Thermo-Mechanical Reliability FE-Analysis of Chiplets
Mike Manuel Feuchter, Hanna Baumgartl, Martin Hanke – CADFEM GmbH

24. Mechanical Strength and Pad Cratering Risk Determination of High-Speed PCBs via Physical Testing and Numerical Simulation
Peng Su, Zheming Gou, Omar Ahmed, Aliasghar Dormohammadi, Babak Arfaei, Kai Brown, Leif Hutchinson, Bernard Glasauer – Juniper Networks

Friday, May 30
10:00 AM - 12:00 Noon

Session 41: Student Interactive Presentations

Committee: Interactive Presentations

Texas Pre-Function

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Wenhao (Eric) Li
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Jobert Van Eisden
MKS Instruments
Email: Jobert.van-Eisden@atotech.com

1. Characterization of the Mechanical and Thermal Properties of SAC+Bi Phases in Hybrid SAC/LTS Solder Joints
Souvik Chakraborty, Mahbub Alam Maruf, Golam Rakib Mazumder, Jeffrey Suhling, Pradeep Lall – Auburn University

2. Pick-and-Release: A Novel Contactless Bonding Method for Die Attachment
Ahmed Abdelwahab, Henk van Zeijl, Massimo Mastrangeli – Delft University of Technology; Remco van Hoorn, Hans Kuipers – ITEC Equipment

3. Assessment of Electromagnetic Board Level Shielding Using Continuous Carbon Fiber
Victor Mahaut, Wilson Maia – Thales Research & Technology, IMS Laboratory; Tristan Dubois, Alexandrine Gracia – University of Bordeaux

4. 3D Coupled Line Inductors With Through-Glass Vias for Compact Passive Circuit Integration in Glass Packages
Sojeong Kim, Young-Joon Kim – Gachon University; Jein Yu – Korea Electronics Technology Institute

5. Design, Fabrication and Characterization of a 3D-Printed Radix-Based Array Antenna for 5G mmWave Applications
Waleed Alshaibani, Abdullah Obeidat, Riadh Al-Haidari, Erik Busse, Stephen Gonya – Binghamton University; Jason Case, Joseph Iannotti, Felippe Pavinatto – GE Aerospace Research

6. Enhancing Runtime Security in Heterogeneous System-in-Package Through a Chiplet-Based Root-of-Trust
Amit Mazumder Shuvo, Md Sami Ul Islam Sami, Jingbo Zhou, Farimah Farahmandi, Mark Tehranipoor – University of Florida

7. Physics-Informed Neural Networks for SAM Image Enhancement With a Novel Physics-Constrained Metric for Advanced Semiconductor Packaging Inspection
Shajib Ghosh, Nitin Varshney, Antika Roy, Patrick Craig, Md Mahfuz Al Hasan, Sanjeev J. Koppal, Navid Asadi – University of Florida; Nelly Elsayed – University of Cincinnati

8. Thermo-Seal: A Multi-Layered Watermarking Scheme for On-Field IC Provenance Verification Using Camouflaged Thermal Signatures
Mohammad Shafkat Khan, Himanandhan Reddy Kottur, Nitin Varshney, Liton Kumar Biswas, Navid Asadizanjani – University of Florida; Stephan Larmann – InfraTec

9. Facile Fabrication for Flexible Pressure Sensor Using FDM-Type 3D Printing Technology
Junyoung Park, Hongyun So – Hanyang University

10. Electrospray Deposited Silver Films for Electromagnetic Interference (EMI) Protection on Insulating Targets
Emma Pawliczak, Paul Chiarot – Binghamton University

11. Scalable Metamaterial Antenna Arrays With Reduced Mutual Coupling for SWaP-Constrained Applications
Alexander Wilcher, Ariel David Cerpa, Yong-Kyu Yoon – University of Florida; Shelby Nelson – Mosaic Microsystems

12. Heterogeneous Integration of Memristor Emulator for Low-Power Computing
Zohreh Salehi, Tahsin Shameem, Jose Schutt-Aine – University of Illinois; Hanzhi Ma – Zhejiang University; Yi Zhou – University of Illinois at Urbana-Champaign

13. Design and Verification of a UCIe-A Mimic Channel for Early-Stage Development of UCIe-Based Systems
Taesoo Kim, Haeseok Suh, Taein Shin, Keunwoo Kim, Hyunjun An, Joungho Kim – Korea Advanced Institute of Science and Technology

14. Organic and Hybrid Nanoscale Films for Low Loss Direct Glass-Copper Metallization
Sai Saravanan Ambi Venkataramanan, Hyunggyu Park, Lakshmi Narasimha Vijay Kumar, Lila Dahal, Mohan Kathaperumal, Mark Losego – Georgia Institute of Technology

15. Optimization of Reflow Profile for Solder Thermal Interface Materials With an Inline Vacuum Oven
Piyush Kulkarni, Scott Schiffres – Binghamton University; Ali Davoodabadi – Universal Instruments Corp.

16. Characterization of Dielectric Materials Beyond Room Temperature Using the Lab-Developed Temperature Split Cavity (TSC) Method
Arafat Hossain, Michael Marakovits, Steven Perini, Michael Lanagan – Pennsylvania State University

17. Chiplet Embedding in Glass-Core Package RDL
Hyunggyu Park, Muhannad Bakir – Georgia Institute of Technology

18. High-Frequency Multi-Chip RF Module Enabled by Fused-Silica Stitch-Chip Technology: RF and Interconnect Characterization
Zhonghao Zhang, Ting Zheng, Muhannad Bakir – Georgia Institute of Technology

19. Novel Technique of Universal Micropatterning for High Density Die Packaging
Alice Mo, Zachary Nelson, Luke Theogarajan – University of California, Santa Barbara

20. Void Formation Elimination in Ultra-Thin Au-Sn Solid-Liquid Interdiffusion Bonding Using Rapid Cooling Process for Advanced Packaging and MEMS Applications
Pei-Ru Lee – National Yang Ming Chiao Tung University; Mu-Ping Hsu,, An-Yuan Hou, Wen-Wei Wu, Kuan-Neng Chen – National Yang Ming Chiao Tung University; Yi-Chieh Tsai – TXC Corporation

21. Integration of Packaged Dies for Flexible FOWLP Using Low Temperature Solder Bonding On FlexTrateTM
Henry Sun, Guangqi Ouyang, Mansi Sheth, Subu Iyer – UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS)

22. Enhancing Reliability of 30 µm-Pitch Interconnections by Optimizing Material Properties of Laser Non-Conductive Paste (LNCP) for Room Temperature Laser-Assisted Bonding With Compression (LABC)
Ga-Eun Lee, Young-Sung Eom, Gwang-Mun Choi, Ki-Seok Jang, Jungho Shin, Chanmi Lee, Jin-Hyuk Oh, Ji-Eun Jung – Electronics and Telecommunications Research Institute

23. Innovative High-Permeability Substrate Integrated Ferrite Inductors for Integrated Voltage Regulators
Rui Huang, Haowen Li, Xiaoling Shi, Nian-Xiang Sun – Northeastern University; Hwaider Lin, Hui Lu – Winchester Technology

24. Intermetallic Compounds (IMC) Growth Investigation, Kinetic Parameter Analysis and Reliability Evaluation of Indium Solder Metal for 3D Integration Packaging
Tassawar Hussain – KU Leuven; Jaber Derakhshandeh, Tom Cochet, Ehsan Shafahian, Prathamesh Dhakrasa, Eric Beyne, Ingrid De Wolf – imec; Aksel Goehnermeier – Carl Zeiss

25. High Aspect Ratio Spiral Inductor With Progressive Turn Widths for Embedded Power Converters
Rami Rasheedi, Inna Partin-Vaisband – University of Illinois

26. Efficient Scalable Thermoelectric Modeling of High-Frequency Cylindrical Interconnects for Heterogeneous Package Arrays
Mohamed Gharib – University of Illinois Chicago; Inna Partin-Vaisband – University of Illinois

27. Hybrid Voltage Regulators for High Performance Computing: Analytical Models and Design Methodology
Salma Abdelzaher, Mohamed Gharib, Inna Partin-Vaisband – University of Illinois

28. Imaging Assisted Dual Sided Light Coupling Technique for Propagation Loss Estimation of Waveguide Interconnects
Abhinandan Hazarika – University College Cork - Tyndall National Institute; Brendan Roycroft, Muhammet Genc, Brian Corbett, Zhi Li – Tyndall National Institute

29. Direct-on-Chip Two-Phase Microjet Cooling With Surface-Enhanced Electrodeposited Microporous Structures
Keyu Wang, Ketan Yogi, Gopinath Sahu, Aaron Du, Tiwei Wei – Purdue University

30. Thermal Characterization and Benchmarking of Aluminum Ribbon Ceramic (ARC) Substrates in mmWave/RF Packaging Applications
Chenhao Hu, Kyoung-Sik Moon, Manos M. Tentzeris – Georgia Institute of Technology

31. Reliable Bonding Strength Measurement of SiCN/SiCN Films by Four-point Bending Methodology
Yun-Hsuan Chen, Pin-Syuan He, Yi-Chen Chung, Rou-Jun Lee, Chien-Yu Liu, Chih Chen – National Yang Ming Chiao Tung University; Guan-Zhe You, Chang-Chun Lee – National Tsing Hua University

32. High-Power Vapor Chambers With Hierarchical Dendritic Wick Structures for High-Performance Computing Systems
Chao-Yang Chiang, Po-Hsun He, Chien-Neng Liao – National Tsing Hua University; Yu-Hsiang Chang, Hung-Hsien Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc. (US); C. P. Hung – Advanced Semiconductor Engineering, Inc.

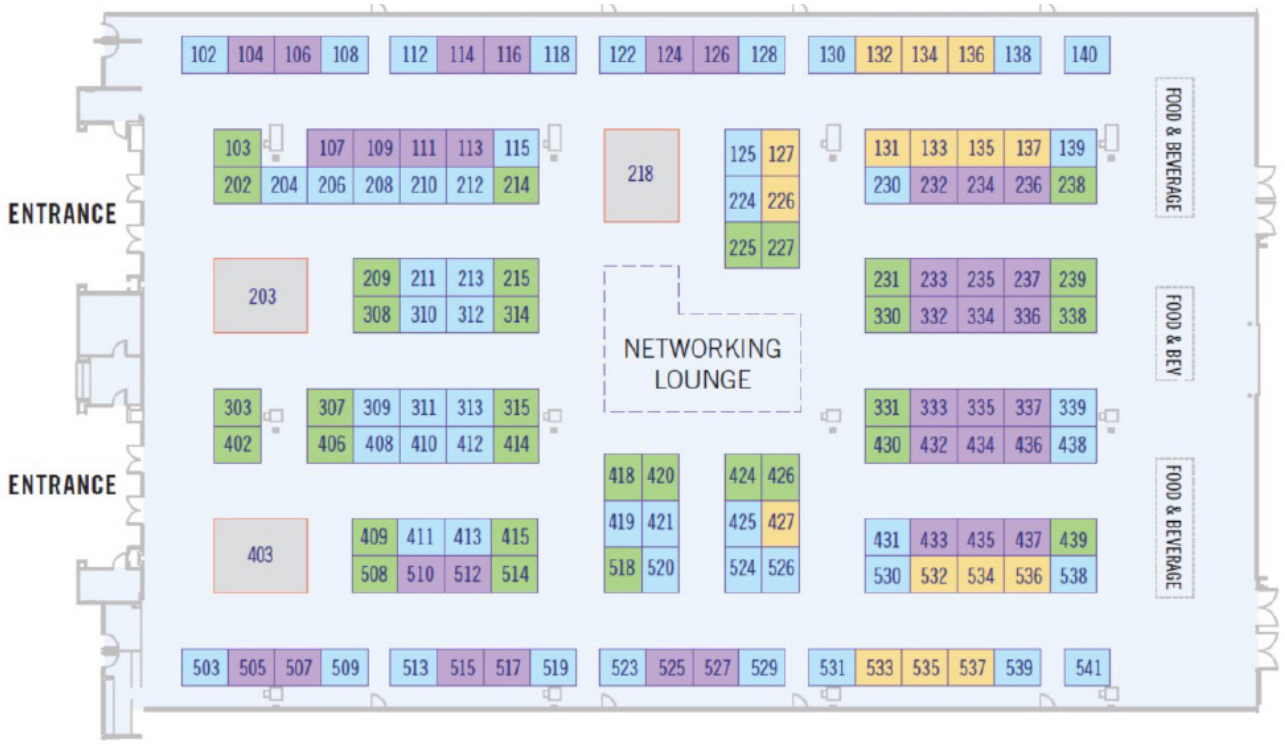
33. Measurement of Thermal, Humidity, Solder and Aging Effects of Mechanical Stress and Silicon Circuit Electrical Performance in Quad Flat Packages
Carl Philipp Riehm, Tobias Chlan, Szabolcs Molnar, Vartika Verma, Ralf Brederlow – Technical University of Munich

Friday Refreshment Break: 10:30 a.m. - 11:15 a.m. – Texas 1-6 Foyer

Exhibit Hall Hours

Wednesday, May 28
9:00 a.m. – 12:30 p.m. & 2:00 p.m. – 6:30 p.m.

Thursday, May 29
9:00 a.m. – 12:30 p.m. & 2:00 p.m. – 4:00 p.m.



2025 ECTC EXHIBITORS

406
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The 3D Systems Packaging Research Center(PRC) at Georgia Tech is a graduated NSF Engineering Research Center focusing on advanced packaging and system integration leading to System on Package (SoP) technologies. The center conducts research and education in all aspects of packaging that includes design, materials, process, assembly, thermal management, and integration driven by applications including areas such as high-performance computing, artificial intelligence, automotive, broadband wireless and space. The team consists of 29 faculty from five schools, 11 research & administrative staff, 50+ graduate & undergraduate students, and several visiting engineers enabled through collaboration with over 40 industry & government organizations and 14 universities.

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Microelectronics Agenda was created as part of the mobilizing agendas of the Portuguese Recovery and Resilience Plan. Involves 17 partners led by Amkor Technology Portugal and seeks to position Portugal at the forefront of the semiconductor management, production, distribution and recycling market, capable of supplying Europe and other countries on a global scale. Main areas of investment: Increased production capacity, Advanced Packaging, High-speed access networks, Industrialisation of products based on integrated optical circuits, The factories of the future and human resources training. Micro.electronics is a structural project that spans the complete value chain from chip design to electronics manufacturing service, engineering, repair and recycling, the consortium will drive technological innovation and productivity while embracing an ecological transition. The Agenda is aligned with the EU's semiconductor initiatives: ICPEI ME and the EU Chips Act., and benefits from a total eligible budget of €67,493,749.13, funded through the NextGenerationEU initiative in €30,048,411,91, with the project's completion scheduled for June 30, 2025.

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The Company was established in July 2019 as a holding company, with Yamaha Motor Co., Ltd. as the parent company and three operating subsidiaries: SHINKAWA LTD, APIC YAMADA CORPORATION, and PFA Corporation. We aim to provide a total solution that exceeds our customers' expectation as the "Turn-Key provider in the field of semiconductors back-end processing" by integrating the technologies of Yamaha Motor's surface mounters (equipment which mounts electronic components and semiconductors on the surface of printed circuit boards) and Industrial Robots, Shinkawa's bonders, and Apic Yamada's molds (package encapsulation equipment).

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The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee. Authors are encouraged to review the sessions of the previous ECTC programs to determine which committees to select for their abstracts.

Applied Reliability: Reliability of 2D, 2.5D, Si bridge, 3D, chiplets, WLCSP, FOWLP, FOPLP & heterogeneous integration and co-packaged optics; interconnect reliability in micro-bump, micro-pillar, Cu pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip & wire bonded packages, novel reliability test methods, life models, FA techniques & materials characterization, component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays and memory; reliability and test methods for thermal interface materials and reliability related to liquid cooling and immersion cooling.

Assembly and Manufacturing Technology: Assembly and manufacturing challenges for new markets; die bonding methods and process challenges: D2D, D2W, W2W; wafer level process/ materials technologies; die and package singulation manufacturing; new & next generation substrates; smart factory/ manufacturing; assembly related test/yield hardware development/improvement; integrating advanced thermal solutions in manufacturing: design/performance, integrating solutions, thermal materials, low stress/high thermal; process advancements/yield enhancements; cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/ compression/injection mold; heterogeneous integration and process: flip chip, chiplets, 3D stacking, bridge technology, large body, warpage management; shielding/protection technologies and manufacturing and market requirements.

Emerging Technologies: Packaging for quantum computing and other cryogenic applications; metrology for advanced packaging and emerging technologies; AI in electronics packaging and its applications; challenges in hardware security; AI electronics packaging and its applications; power electronics and energy storage; MEMS & NEMS; emerging, novel and unique flexible/ stretchable/ wearable hybrid electronics, medical devices and bioelectronics; additive, hybrid, nano, and smart manufacturing for electronics packaging; green and sustainable electronics, net zero strategy/ technology; digital twins.

Electrical Design & Analysis: 5G/6G, IoT, cloud computing, autonomous vehicles, AI/ML; antennas, sensors, power transfer, wired/wireless communications, RF to THz; multiphysics/multiscale modeling & characterization of interconnects, modules, components, and systems; chiplet, heterogeneous integration, chip-to-chip, die-to-die, SiP/MCM/system co-design (chip/package/board), UCIe, HBM/ HPC; opto-electronic (OE) hybrid integration, analog packaging, power electronics modeling/ characterization; high-speed/frequency (RF, mm-wave, THz) signal integrity, power integrity, and EMI/ EMC.

Interconnections: Interconnects for chiplets, heterogeneous integration, hybrid bonding, C2W, W2W, fan-out, panel-level, TSV, TGV; interconnects for 2.5D/3D, Si/glass/organic interposers, fine-pitch/multi-layer RDL, SiP, wafer-level system integration; interconnects for thermo-compression/ laser assisted/ transient liquid phase bonding, low temperature solder, flip-chip, micro-bump, Cu pillar, wirebond, Al ribbon bond; printable interconnects, flexible interconnect, quantum interconnects, optical interconnects, interconnects for SiC/GaN or WBG; interconnection materials, chemistries, metrology, characterization and reliability; conductive/non-conductive adhesives, ACF, underfill, molding compounds; chiplet interconnect design and validation, UCIe/BoW/etc. standards; thermal interface materials, thermal/mechanical/electrical tests and reliability.

Materials & Processing: Advanced materials and processes for hybrid bonding, fan-out, Si interposer, 2.5D/3D, chiplets, HI, TSV; advanced materials and processes for thermal and mechanical improvement for packaging; wafer & panel level packaging materials and process advancements; dielectrics and underfills, molding compounds, thermal interface materials; harsh environment resistant materials; temporary wafer bond/debond materials and processes, TCB and hybrid bonding, conductive adhesives; emerging electronic materials and processes; novel solder metallurgies; novel materials and processes for high density interconnect.

Thermal/Mechanical Simulation & Characterization: Thermal/ mechanical simulation and characterization at component, board, and system levels for all packaging technologies; reliability related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); material constitutive relations; chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; novel modeling techniques including multi-scale physics, co-design approaches; quantum computing; measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; application of artificial intelligence on modeling, characterization, and digital twins; credible simulations; CFD simulation.

Packaging Technologies: 2.XD/3D architectures/designs for energy efficient HPC, C2C links, structures, thermal solutions, and methods & processes; heterogeneous (chiplet) integration for 2.5D, 3D-IC for AI, neural nets, HBM, CPU, GPU, ASIC, and CPO; silicon, glass, diamond & organic interposer and advanced package technology; dual-Damascene Cu, Cu TSV, hybrid bonding, and backside power; embedded die, bridge, and passives; flexible, advanced substrates & modules; fanout wafer and panel level packaging, advanced flip-chip, SiP, CSP, PoP; RF, wireless, MEMS, Sensors & IoT, automotive, wireless power and power electronics; SiC, GaN, PMIC, SPS; bio, medical, flexible, wearable & extreme environments packaging.

Photonics: Photonic components packaging for computing, communications, data processing, mobility, healthcare, green energy photonics, agriculture, horticulture, food, environmental, climate and atmosphere monitoring, space, automobile, underwater, industrial, defense, process integration, co-packaging (photonics, electronics, and laser integration), free space optics, microscopy and advanced spectroscopy, 3D printing of micro-optical components for packaging, assembly and manufacturing; packaging for the quantum photonics world; packaging of new photonics materials; optical characterization of packaging components; equipment and tools for photonics packaging; detachable fiber array unit; ultra-low power photonics and materials; heterogeneous materials; quantum dots; meta-surfaces and meta-materials.

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract that describes the novelty, scope, content, and key points of your proposed manuscript via the website at www.ectc.net.

If you have any questions, contact:
Bora Baloglu, 76th ECTC Program Chair
Intel Corporation
borabal@ieee.org

Abstracts cannot contain more than 700 words and must be received by October 6, 2025, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors. The authors are notified about the abstract selection outcome by December 12, 2025.

Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From the proposals received, 16 PDCs are selected for offering at the 76th ECTC on Tuesday, May 26, 2026.

Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 19, 2025. Authors are notified of course acceptance with instructions by December 12, 2025.

If you have any questions, contact:
Kitty Pearsall, 76th ECTC Professional Development Courses Chair
Capstan Technologies, Inc.
Phone: +1-512-845-3287 • E-mail: kitty.pearsall@gmail.com

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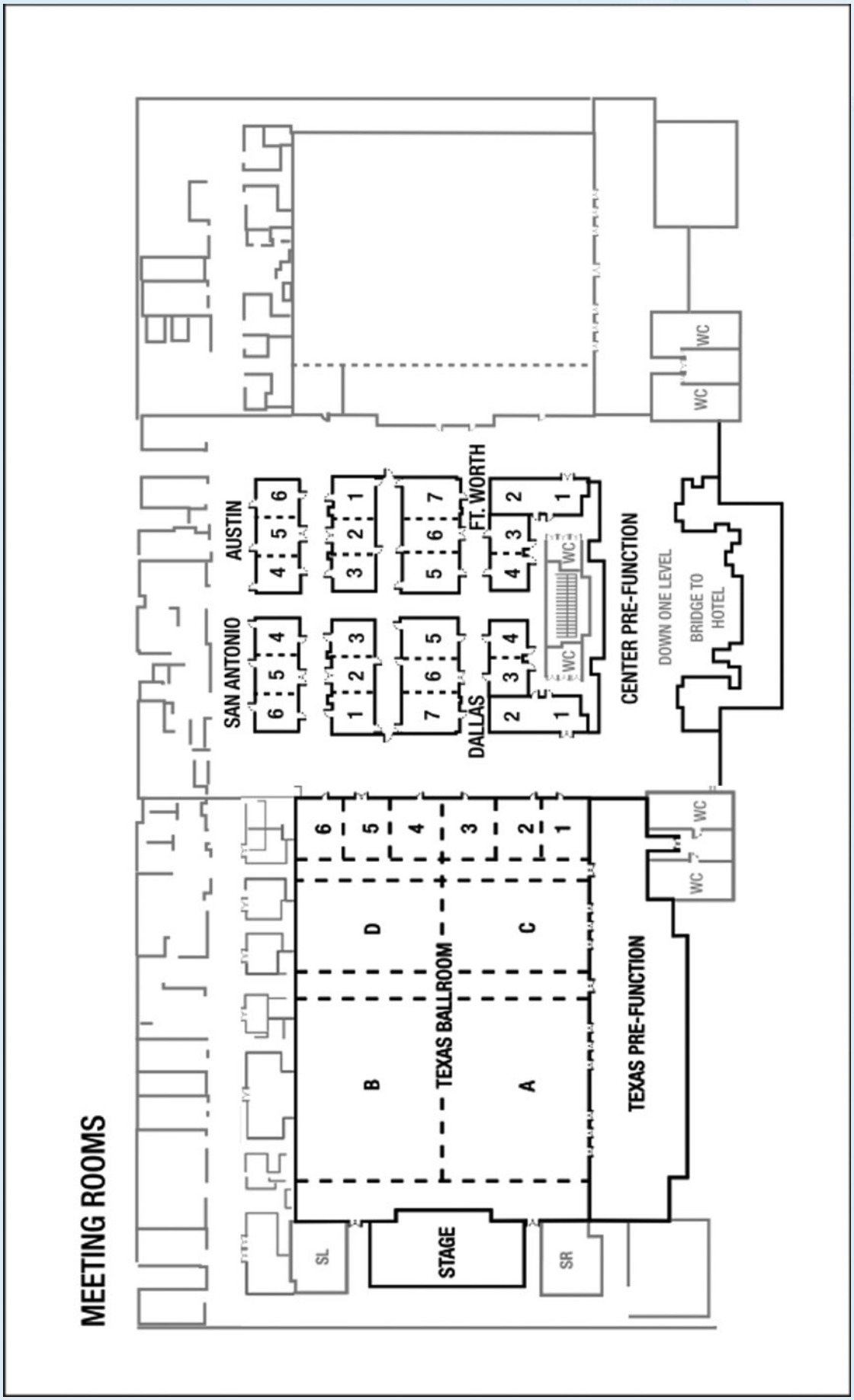
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76TH ELECTRONIC COMPONENTS & TECHNOLOGY CONFERENCE

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CONFERENCE AT A GLANCE

REGISTRATION

Monday, May 26, 2025
12:00 Noon – 4:00 p.m.

Tuesday, May 27, 2025
6:45 a.m. – 7:45 p.m.
Until 8:15 a.m. registration reserved for morning session PDC and Special Session attendees

Wednesday, May 28, 2025
6:45 a.m. – 4:00 p.m.

Thursday, May 29, 2025
7:00 a.m. – 4:00 p.m.

Friday, May 30, 2025
7:00 a.m. – 12:00 Noon

Lobby level of the Convention Center

EXHIBITION HALL

Wednesday
9:00 a.m. – 12:30 p.m.
2:00 p.m. – 6:30 p.m.
Reception: 5:30 p.m. – 6:30 p.m.

Thursday
9:00 a.m. – 12:30 p.m.
2:00 p.m. – 4:00 p.m.
Longhorn D

SPEAKER PREPARATION ROOM

Tuesday – Friday
7:00 a.m. – 5:00 p.m.
Dallas 4

MAIN STAGE MORNING SESSIONS

Wednesday: ECTC Keynote

Thursday: EPS Plenary Session

Friday: IEEE EPS President Panel
8:00 a.m. – 9:15 a.m.
Texas A & B

MAIN STAGE EVENING SESSIONS

Tuesday: IEEE EPS Seminar
7:45 p.m. – 9:15 p.m.

Wednesday: ECTC Student & Start Up Innovation Challenge
6:30 p.m. – 8:30 p.m.
Texas A & B

GALA RECEPTION

Thursday: 7:30 p.m.
Glass Cactus Venue

TUESDAY

PDC Instructors and Proctors Briefing & Breakfast

7:00 a.m. – 8:30 a.m.
San Antonio 2–3

Professional Development Courses (PDCs)

8:00 a.m. – 12:00 Noon
1:30 p.m. – 5:30 p.m.
See page 8 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop

8:00 a.m. – 4:30 p.m.
Texas D

Special Sessions

No. 1: 8:30 a.m. – 10:00 a.m.
No. 3: 10:30 a.m. – 12:00 Noon
No. 5: 1:30 p.m. – 3:00 p.m.
No. 7: 3:30 p.m. – 5:00 p.m.
Texas C

No. 2: 8:30 a.m. – 10:00 a.m.
No. 4: 10:30 a.m. – 12:00 Noon
No. 6: 1:30 p.m. – 3:00 p.m.
No. 8: 3:30 p.m. – 5:00 p.m.
Texas 1–3

Refreshment Breaks

10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Texas 4–6 Foyer

Tuesday Lunch

12:00 Noon – 1:15 p.m.
Texas A & B

ECTC Exhibition Setup

1:00 p.m. – 5:00 p.m.
Longhorn D

ECTC Student Reception

5:00 p.m. – 6:00 p.m.
Mission Plaza, Hotel Atrium

General Chair's Speakers Reception

6:00 p.m. – 7:00 p.m.
Riverwalk Cantina Restaurant, Hotel Atrium
By invitation only

Young Professionals Networking Panel

6:45 p.m. – 7:45 p.m.
Texas C

WEDNESDAY – FRIDAY

Speakers Breakfast

7:00 a.m. – 7:45 a.m.
Texas C

Sessions

9:30 a.m. – 12:35 p.m. or
2:00 p.m. – 5:05 p.m.
see pages 10-21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Texas D

Sessions 2, 8, 14, 20, 26, 32
Texas C

Sessions 3, 9, 15, 21, 27, 33
Texas 4–6

Sessions 4, 10, 16, 22, 28, 34
Texas 1–3

Sessions 5, 11, 17, 23, 29, 35
Dallas 5–7

Sessions 6, 12, 18, 24, 30, 36
San Antonio 4–6

Interactive Presentations

Sessions 37 – 41
10:00 a.m. - 12:00 p.m. and
2:30 p.m. - 4:30 p.m.
(Wednesday & Thursday)
Texas Pre-Function
see pages 22–23 for specifics

Lunch

12:45 p.m. - 1:45 p.m.
Texas A & B

Refreshment Breaks

10:30 a.m. – 11:15 a.m.
3:00 p.m. – 3:45 p.m.
Wednesday & Thursday
Exhibition Hall – Longhorn D

Friday
Texas Pre-Function

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