The 2023 IEEE 73rd Electronic Components and Technology Conference
May 30 — June 2, 2023

2023 Conference Program & Exhibitor Listings

JW Marriott Orlando, Grande Lakes
Orlando, Florida USA

Sponsored by
IEEE ELECTRONICS PACKAGING SOCIETY  IEEE

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On behalf of the Program and Executive Committee, it is my pleasure to invite you to IEEE’s 73rd Electronic Components and Technology Conference (ECTC), which will be held at JW Marriott Orlando, Grande Lakes, Orlando, Florida from May 30 to June 2, 2023. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1500 people attended ECTC 2022 in what was our first in-person event in three years.

At the 73rd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, chiplets, advanced substrates, assembly, materials and thermal modeling, reliability, packaging for harsh conditions, packaging for quantum and AI applications, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 73rd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature seven special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, five special sessions, 90 minutes each, are scheduled. On Tuesday morning, May 30th at 8:30 a.m. Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH, will chair the session on Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment, followed by Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm chairing a special session at 10:30 a.m. on Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications. On Tuesday afternoon at 1:30 p.m. Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco, will host a special session on the topic of Photonic Integrated Circuit Packaging, followed by a special session on the CHIPS Act, organized by Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE.

As in previous years, HIR will host a parallel track throughout the day, with four exciting and complementary sessions on AI/ML in Package Co-Design for Chiplets Perspective, Heterogeneous Integration of MEMS & Sensors: Challenges and Opportunities; The CHIPS and Science Act; Additively Manufactured Electronics for Heterogeneous Integration.

On Tuesday evening, the Young Professionals reception will be organized by Yan Liu, Medtronic. Next, Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus, will co-chair the IEEE EPS Seminar on High-Density Substrates.

New this year, the following days (Wednesday-Friday) will kick off with a single-room special session from 8:00 a.m. to 9:15 a.m., which will then be followed by our traditional technical sessions with six parallel tracks. On Wednesday May 31st at 8 a.m., join us early to receive our Welcome message from our General Chair Ibrahim Guven, followed by a captivating presentation and Q&A session by our Keynote speaker Prof. Michael Manfra from Purdue University; the title of the Keynote is “Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging”.

At the end of the day, at 6:30 p.m., a special session/reception, co-hosted by ECTC and ITherm, will discuss workforce development for semiconductors and packaging. The panel will be chaired by Kim Yess, Brewer Science, Nancy Stoffel, GE Research, and Christina Amon, University of Toronto. This reception/panel event should not be missed.

On Thursday June 1st at 8 a.m., we will have the pleasure of starting the day with our ECTC Plenary Session, featuring an extensive panel of experts focused on next-generation millimeter-wave packaging. The 75-min session will be chaired by Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg Technical University. Kitty Pearshall, Boss Precision, Inc., IEEE EPS President, and David McCann, Lyte, will chair the EPS President’s ECTC panel session on Friday morning at 8 a.m. The session will focus on how photonics can enable the bandwidth densities with lower energy per bit in emerging SIP.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the ECTC Exhibition. Co-located with the IEEE ITherm Conference, the 73rd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearshall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 30th and are taught by distinguished experts in their respective fields. The ECTC Exhibition will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than 120 exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 73rd ECTC and to be a part of all the exciting technical and professional opportunities. I also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 73rd ECTC a success. I look forward to meeting you at the JW Marriott Orlando, Grande Lakes, Orlando, Florida, May 30 – June 2, 2023.
On behalf of the IEEE Electronics Packaging Society, I am delighted to welcome you to the 73rd Electronic Components and Technology Conference – the world’s premier event for electronics packaging. Starting 73 years ago, ECTC continues to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging. Building upon the outstanding event from last in-person years and the very positive feedback to our virtual conferences, we expect attendance at ECTC 2023 to well exceed 1400 packaging professionals. This is a fantastic achievement. Our conference portfolio continues to find innovative ways to grow and serve our community. Together with ECTC and our Asia-Pacific flagship conference EPTC, to be held in December, EPS expects to reach similar well attended in-person conferences world-wide in 2023. These achievements would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year’s exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community. May I also thank our authors, presenters, and sponsors for their contributions to this year’s event. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members. In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website. Finally, may I thank you for attending this year’s ECTC. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Kitty Pearsall
EPS President 2022-2023
REGISTRATION LOCATION AND HOURS
ECTC registration is located at the Grande Registration Desk in the JW Marriott Grande Lakes, across from Mediterranean 3 (lobby level).

Monday, May 29, 2023 – 3:00 p.m. - 6:00 p.m.
Tuesday, May 30, 2023 – 6:45 a.m. - 7:45 p.m.*
(From 6:45 a.m. – 8:15 a.m. registration is for morning session PDC and Special Session Attendees)*
Wednesday, May 31, 2023 – 6:45 a.m. - 4:00 p.m.
Thursday, June 1, 2023 – 7:00 a.m. - 4:00 p.m.
Friday, June 2, 2023 – 7:00 a.m. - 12:00 p.m.

On Tuesday, May 30th light morning refreshments will be provided from 6:45am – 7:30am. Come pick up your registration materials EARLY and grab a bite to eat before our PDC’s and Special Sessions start!

*The above schedule for Tuesday will be vigorously enforced to prevent attendees from being late for their courses and sessions. Please make sure to take advantage of the 6:45am start time as registration becomes very congested prior to the start of morning programming.

DOOR REGISTRATION FEES
Door Registration with Proceedings Download
IEEE Member Pricing
JOINT (full ECTC + IThERM conference) .................. $1250
IEEE Member Full Registration ......................... $950
IEEE Member Speaker / Session Chair .................. $850
IEEE Member One Day ................................ $625
IEEE Member Speaker One Day ...................... $550

Non-Member Pricing
JOINT (full ECTC + IThERM conference) .................. $1500
Non-Member Full Registration ......................... $1150
Non-Member Speaker / Session Chair .................. $850
Non-Member One Day ................................ $625
Non-Member Speaker One Day ...................... $550

Student ................................................. $340
Student Speaker ....................................... $340

Tuesday Professional Development Courses
IEEE Members
Tuesday AM or PM Course with luncheon ................ $440
Tuesday All-Day Courses with luncheon ................ $625

Non-Members
Tuesday AM or PM Course with luncheon ................ $490
Tuesday All-Day Courses with luncheon ................ $675
Tuesday Student All-Day Courses with luncheon .......... $150

Extra Luncheon Tickets for Each Day .................. $75

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST
7:00 a.m. Tuesday
Room Location: Cordova 5 – 6; lower level
PDC Instructors and Proctors are required to attend a briefing breakfast.

SESSION CHAIRS AND SPEAKERS BREAKFAST
7:00 a.m. Wednesday thru Friday
Room Location: Palazzo E
Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC.

SPEAKER PREP ROOM
7:00 a.m. – 5:00 p.m., Tuesday – Friday
Room Location: Brava, lower level
Speakers should prepare and review their digital presentations within the allotted times above.

GENERAL INFORMATION
Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

LUNCHEONS
(Room Location: Mediterranean 4 & 5)
This year ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $75 to replace. Please come and enjoy time with other attendees and colleagues in the industry!

Lunch times will vary, see below for specific details for each day.

Tuesday: 12:00 Noon – 1:15 p.m.
Wednesday: 12:45 p.m. – 1:45 p.m.
Thursday: 12:45 p.m. – 1:45 p.m.
Friday: 12:45 p.m. – 1:45 p.m.

Don't miss out on this lunch! We will be raffling off several prizes including a hotel stay, free conference registrations, and many other industry gadgets!
ECTC Mobile App

ECTC is pleased to announce that a free mobile app “Whova” is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and venue maps. The app also features tools to set your schedule, so you don’t miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching “Whova”. After downloading the Whova app please log in using the email address you used to register for ECTC, and the ECTC content will appear automatically. Alternatively, a generic app invitation code will be made available onsite at the conference for attendees.

New This Year

We are proud to announce that a selection of papers will be invited to be published as journal publications in the IEEE Transactions on Components, Packaging, and Manufacturing Technology after the conference. The journal manuscript will have to follow the Transaction guidelines.
Electronic components and systems are among the main contributors to the most innovative ideas and products of today's world. In the automotive industry, electronic components and systems are accountable for more than 80% of all innovation. When we think about highly automated and autonomous systems, advanced packaging is a must. Nowadays, most advanced electronic components such as CPUs or GPUs are being introduced into harsh environments such as automotive, avionics or space applications almost at the same time as in consumer products. Therefore, in our special session, we would like to discuss with the top experts from industry and academia what the current status and opportunities are for advanced packaging for harsh environments.

Ramesh S., General Motors; Giuseppe Barone, Robert Bosch GmbH; Vikas Gupta, ASE US, Inc.; Dae-Woo Kim, Samsung; Shin-Puu Jeng, TSMC; Ram Trichur, Henkel; Kaichi Zhang, TU Delft; Vanessa Smet, Georgia Tech

Dr. Rami Choufan, University of Calgary; Francois Bilodeau, University of Calgary; Przemyslaw Gromala, Robert Bosch GmbH

2023 ECTC Special Session on Advanced Packaging for Harsh Environments

Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities

Tuesday, May 30, 2023, 8:30 a.m. – 10:00 a.m.

Chairs: Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH

This special session will cover the latest advances in advanced packaging for harsh environments, including challenges and opportunities in copper hybrid bonding, photonics packaging, and 3D packaging technologies. The session will include a panel discussion with leading experts from industry and academia.

Dr. Rami Choufan, University of Calgary; Francois Bilodeau, University of Calgary; Przemyslaw Gromala, Robert Bosch GmbH

2023 ECTC Special Session on Hybrid Bonding

Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications

Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.

Chairs: Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm

This special session will explore the applications, requirements, and challenges of copper hybrid bonding (CHB) for chip-to-wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand. While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

The session will include a moderator and speakers, each with a 10-minute presentation followed by a 20-minute Q&A session.

Junior Vardaman, TechSearch International; Eric Beyne, IMEC; Xavier Brun, Intel; Kenneth Larsen, Synopsys; Raja Swaminathan, AMD; Thomas Uhrmann, EVG; Chris Scanlan, Besi

2023 ECTC Special Session on Photonics Packaging

Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption

Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.

Chairs: Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco

Photonic integrated circuit (PIC) technologies are proliferating into many application spaces, from hyperscale data center, high-performance computing to sensing including LiDAR. packaging remains the greatest challenge to high-volume manufacturing at high throughput and yield. The main challenges are: Optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability, and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC 65566C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption toward high-volume reality.

Gianlorenzo Masini, Cisco; Thierry Mounier, CEA-Leti; Hesham Taha, Teramount; Alexander Jants-Polczynski, IBM; Peter O’Brien, Tyndall Institute; Colin Dankwart, Ficontec Service GmbH

2023 ECTC Special Session on CHIPS Act

Advanced Packaging Manufacturing in North America: Building the Ecosystem

Tuesday, May 30, 2023, 3:30 p.m. – 5:00 p.m.

Chairs: Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE

North America has companies that excel in design for electronics systems, device, and advanced packaging. However less than 2% of the packaging occurs in the US. This session will discuss the ambitious goals being set through the CHIPS ACT to bring Advanced Packaging to North America. We will review the targets and developing plans of the US government, funded through the CHIPS Act. The panelists will overview major initiatives launched in R&D and Manufacturing. We will also discuss the challenges to meeting the goals.

Joshua Dillon, Marvell Technology Inc.; Frank Gayle NIST, Office of Advanced Manufacturing; Subramanian Iyer, University of California Los Angeles; Carl McCloud, DARPA; Dick Otte, Promex Industries, Inc.; Henn P. Takiar, Micron Technology Inc.

2023 ECTC Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 30, 2023, 8:00 a.m. – 4:30 p.m.


Heterogeneous Integration uses packaging technology to integrate dissimilar chips, devices or components with different materials and functions, and from different fabless design houses, foundries, wafer materials, feature sizes and companies into a system or subsystem. 23 Technical working groups will present on their areas of expertise. This workshop is a full-day event with the following schedule.

8:00 a.m. – 8:30 a.m. Welcome & Agenda Review

8:30 a.m. – 10:00 a.m. AI/ML in Package Co-Design for Chiplets Perspective

10:15 a.m. – 11:45 a.m. Heterogeneous Integration of MEMS & Sensors: Challenges and Opportunities

Lunch Break

1:15 p.m. – 2:45 p.m. The CHIPS and Science Act

1:45 p.m. – 3:00 p.m. Additively Manufactured Electronics for Heterogeneous Integration
2023 Young Professionals Networking Panel
Tuesday, May 30, 2023, 7:00 p.m. – 7:45 p.m.
Chair: Yan Liu, Medtronic
Palazzo D

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2023 IEEE EPS Seminar on High-Density Substrates
The Future of High-density Substrates – Towards Submicron Technology
Tuesday, May 30, 2023, 7:45 p.m. – 9:15 p.m.
Chairs: Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus
Palazzo E

Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules where Si scaling is slowing down. One of the key attributes of chiplets and HI technologies is the bandwidth of interconnection between chips within the same package. A very short-distance and high-density interconnection from one chip to another enables high-speed data transmission with low energy loss. High-density chip carrier substrate is the core technology driving the evolution of chiplets and HI technologies.

The EPS Seminar organized by TC6 (High-Density Substrate and Board) will discuss ultra-fine-pitch substrate technologies towards submicron ground rule for Chiplets and Heterogeneous Integration. We will have 5 panelists, and each panelist will give a short talk presenting insights on technology trends, technical challenges, application requirements, recent technical updates, and more covering advanced interposer technologies, followed by a panel discussion.

Yasushi Araki, Shinka; Yu-Hua Chen, Unimicron; Satoru Kuramochi, Dai Nippon Printing (DNP); Madhavan Swaminathan, Penn State University; Giuseppe Bonilla, IBM

2023 Keynote Speaker
Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging
Wednesday, May 31, 2023, 8:00 a.m. – 9:15 a.m.
Prof. Michael J. Manfra, Purdue University
Mediterranean 4 & 5

Quantum computing will revolutionize the way we tackle certain societally relevant but currently intractable problems. To reach this promise, significant advances in quantum hardware on multiple scales are required. This keynote address will explore the challenges and opportunities in quantum computing hardware ranging from basic choice of qubit platform, through scalable control and readout, to system architecture. Technology advancement will require innovations in material science and device physics to tackle challenges on the quantum plane. Progress will also hinge on innovations in interconnect technology and advanced packaging for an integrated quantum-classical hardware system. As in classical digital computing, thermal management and reliability concerns will impact quantum system performance and must be addressed directly. In this presentation, some exemplars that demonstrate the opportunities for contributions to quantum technology from the community focused electron devices, interconnects and advanced packaging will be discussed. Development of a full-stack quantum computer necessitates industrial programs stimulated and informed by innovation generated in government labs and academic research groups.

2023 ECTC Plenary Session on mm-Wave Phased Array Packaging
Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems
Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.
Chairs: Kevin Gu, Metawave Corporation, and Ivan Ndjip, Fraunhofer IZM / Brandenburg University of Technology
Mediterranean 4 & 5

Project arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and the latest advancements in packaging and integration technologies for designing and implementing phased array front-end modules, including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, system demos/prototypes, and so on.

Jonathan Hacker, Teledyne Scientific; Augusto Gutierrez-Aitken, Northrop Grumman Space Systems; Hasan Shanfi, HRL Laboratories, LLC; Madhavan Swaminathan, Pennsylvania State University; Shiva Sharamian, Nokia Bell Labs; Alberto Valdes-Garcia, IBM Research

2023 IEEE EPS President Panel on Photonics
How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP
Friday, June 2, 2023, 8:00 a.m. – 9:15 a.m.
Chairs: Kitty Pearsall, Boss Precision, Inc., and David McCann, Lyte
Mediterranean 4 & 5

This panel will discuss the tools, technologies, and approaches that will enable the industry to enhance the bandwidth density of interconnections in SIP enabled by photonics. To be adopted, such capabilities must be provided with energy per bit that meets the roadmaps and standards targets for the interconnection protocols within the package and on the chip.

Amr S. Helmy, University of Toronto; Ritesh Jain, Lightmatter; Ajey Jacob, University of Southern California; Stefano Oggiioni, ATS
## Professional Development Courses

**TUESDAY, MAY 30, 2023**

### Morning Courses: 8:00 a.m. – 12:00 Noon

**Palazzo B**
- **1. High Reliability of Lead-Free Solder Joints – Materials Considerations**
  - Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech

**Palazzo A**
- **2. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals**
  - Course Leader: Patrick Thompson – Texas Instruments, Inc.

### Afternoon Courses: 1:30 p.m. – 5:30 p.m.

**Palazzo B**
- **9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability**
  - Course Leader: Pradeep Lall – Auburn University

**Palazzo A**
- **10. Fan-Out Packaging and Chiplet Heterogeneous Integration**
  - Course Leader: John Lau - Unimicron

### Mediterranean 3

- **3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Level and Advanced RF Packages**
  - Course Leaders: Ivan Ndjio – Fraunhofer IZM/Brandenburg University of Technology and Markus Wöhrmann – Fraunhofer IZM

**Mediterranean 6**
- **11. Photonic Technologies for Communication, Sensing, and Displays**
  - Course Leader: Torsten Wipiejewski – Huawei Technologies

### Mediterranean 2

- **4. Eliminating Failure Mechanisms in Advanced Packages**
  - Course Leader: Darvin Edwards – Edwards Enterprises

- **12. Flip Chip Technologies**
  - Course Leaders: Shengmin Wen – HaiSemi and Eric Perfecto – IBM Research

### Mediterranean 7

- **6. Reliability Physics and Failure Mechanisms in Electronics Packaging**
  - Course Leader: Xuejun Fan – Lamar University

- **7. Reliable Integrated Thermal Packaging for Power Electronics**
  - Course Leader: Patrick McCluskey – University of Maryland

**Mediterranean 8**
- **8. Introduction to PWB Thermal Analyses**
  - Course Leader: Patrick Loney - Northrop Grumman

### Mediterranean 7

- **15. Polymers in Wafer Level Packaging**
  - Course Leader: Jeffrey Goto – InnoCentrix, LLC

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**Committee Meetings**

#### Tuesday, May 30, 2023

- **8:00 a.m. – 4:30 p.m.**
  - EPS HIR Workshop
  - **Palazzo E**

- **9:00 a.m. – 10:30 p.m.**
  - ECTC OPTO Committee
  - **Cordova 1 (lower level)**

- **9:00 a.m. – 10:30 p.m.**
  - ECTC Interconnect Committee
  - **Cordova 2 (lower level)**

#### Wednesday, May 31, 2023

- **7:00 a.m. – 8:00 a.m.**
  - EPS Power & Energy TC
  - **Cordova 6 (lower level)**

- **7:00 a.m. – 8:00 a.m.**
  - EPS Reliability TC
  - **Cordova 1 (lower level)**

- **7:00 a.m. – 8:00 a.m.**
  - EPS 3D / TSV TC
  - **Cordova 4 (lower level)**

- **4:30 p.m. – 5:30 p.m.**
  - EPS Technical Committee Chairs
  - **Cordova 6 (lower level)**

- **5:30 p.m. – 6:30 p.m.**
  - ECTC 2024 Program Committee Meeting
  - Mediterranean 2-3

#### Thursday, June 1, 2023

- **7:00 a.m. – 8:00 a.m.**
  - EPS RF & THz Tech. TC
  - **Cordova 6 (lower level)**

- **7:00 a.m. – 8:00 a.m.**
  - EPS Materials & Process TC
  - **Cordova 2 (lower level)**

- **7:00 a.m. – 8:00 a.m.**
  - EPS Photonics TC
  - **Cordova 1 (lower level)**

- **7:00 a.m. – 8:00 a.m.**
  - EPS Emerging Tech TC
  - **Cordova 4 (lower level)**

- **9:00 a.m. – 10:00 a.m.**
  - EPS T-CPMT SAE / AE’s
  - **Cordova 5 (lower level)**

- **2:15 p.m. – 5:15 p.m.**
  - ECTC Executive Committee
  - **Cordova 5-6 (lower level)**

#### Friday, June 2, 2023

- **7:00 a.m. – 8:00 a.m.**
  - EPS High Density Substrates & Boards TC
  - **Cordova 1 (lower level)**

#### Refreshment Breaks

- **10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.**
  - Mediterranean & Palazzo Foyers
ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2022
The Electronic Components and Technology Conference is proud to announce the “Best of Conference” papers selected from the 72nd ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper
Advanced Fan-Out Packaging Technology for Hybrid Substrate Integration
Lihong Cao, Teck Chong Lee, Rick Chen, Yung-Shun Chang, Hsingfu Lu, Nicholas Chao, Yen-Liang Huang, Chen-Chao Wang, and Chih-Yi Huang – ASE Group

Best Interactive Presentation Paper
Novel Zero Side-Etch Process for <1μm Package Redistribution Layers
Pratik Nimbalkar, Pragna Bhaskar, Christopher Blancher, Mohanalingam Kathaperumal, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

INTEL BEST STUDENT PAPER – 2022
The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 72nd ECTC.

Co-Design of Thermal Management with System Architecture and Power Management for 3D ICs
Rishav Roy – Purdue University; Shidhartha Das, Benoit Labbe, Rahul Mathur, and Supreet Jeloka – ARM

OUTSTANDING PAPERS – 2022
The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 72nd ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper
Organic Interposer CoWoS-R+ (plus) Technology

Outstanding Interactive Presentation Paper
Scalable through Mold Interconnection Realization for Advanced Fan Out Wafer Level Packaging Applications
Aurélia Plihon, Edouard Deschaseaux, Rémi Franiait, Jérome Dechamp, Simon Vaudaine, Jennifer Guillaume, Catherine Brunet-Manquat, Stéphane Moreau, and Perceval Coudrain – CEA-LETI

ECTC SPONSORS
With 73 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company’s interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under “Sponsors.”

To sign-up for sponsorship or to get more details, please contact Alan Huffman at alan.huffman@ieee.org or +1-336-380-5124.
Program Sessions: Wednesday, May 31, 9:30 A.M. - 12:35 P.M.

Session 1: Heterogeneous Chiplet Integration
Committee: Packaging Technologies
Palazzo D

Session 2: High-Performance Packaging Materials
Committee: Materials & Processing
Palazzo A & B

Session 3: Advancements in Copper/Silicon-Oxide Hybrid Bonding
Committee: Interconnections
Mediterranean 2 & 3

Session Co-Chairs:
Andrew Kim – Apple, Inc.
Email: akim4@apple.com
Mike Gallagher – Dupont Electronics and Imaging
Email: michael.gallagher@dupont.com

1. 9:30 AM – Ultra High Density Low Temperature SoC with Sub-0.5 µm Bond Pitch

2. 9:50 AM – Lithographic Performance and Insulation Reliability of a Novel i-Line Photosensitive Dielectric Material
Go Inoue, Daki Yukiomori, Kaho Shibasaki, Ayano Okuda, Nobuhito Ishikawa, Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.; Young-Gun Han, Taka Kanyayama, Tadasu Suetugyu – Fukuoka University

3. 10:10 AM – Aggressive Pitch Scaling (sub-0.5 µm) of W2W Hybrid Bonding Through Process Innovations
Tyler Sherwood, Raghav Sreenivasan, Jason Appell, Raghuram Patil, Lon Li, Kevin Hao, Joel Selfelder, Ryan Ley – Applied Materials, Inc.; Thomas Kasbauer, Raghuveer Patlolla, Kun Li, Joe Salfelder, Tyler Sherwood, Raghav Sreenivasan, Jason Appell, Ryan Ley – Applied Materials, Inc.; Thomas Kasbauer, Raghuveer Patlolla, Kun Li, Joe Salfelder, Tyler Sherwood, Raghav Sreenivasan, Jason Appell, Ryan Ley – Applied Materials, Inc.

4. 11:15 AM – Design Space Exploration (DSE) for over-136 GB/s IO Bandwidth with LPDDR5X SDRAM Packages on SOCo Package in 200 mm²
Heeseok Lee, Jun So Pak, James Jung, Jisoo Hwang – Samsung Electronics Co., Ltd.

5. 11:35 AM – 3D Stacking of Heterogeneous Chiplets on Modified FOWLP Platform with Thru-Silicon Redistribution Layer

6. 11:55 AM – Same Size Mold Chase Technology for Effective Stack Die Architectures
Nabankur Deb, Xavier Brun, Yoshihiro Tomita – Intel Corporation; Chris Masuyama, Naoki Hamada, Yoshikazu Hirano – Towa Corporation

7. 12:15 PM – A Novel Chiplet Integration Architecture Employing Pillar-Suspended Bridge with Polymer Fine-Via Interconnect

Session Co-Chairs:

1. 9:30 AM – High Modulus Photosensitive Permanent Film Utilizing Novel Polymerization System for Advanced MEMS Structure Fabrication
Ken-ichi Yamagata, Shiori Yuge, Ryosuke Nakamura, Hirofumi Imai – Tokyo Ohka Kogyo Co., Ltd.

2. 9:50 AM – Fine Pitch Die-to-Wafer Hybrid Bonding
Thomas Workman, Jeremy Thell, Gill Fountain, Dominik Suwito, Cyprian Uzoh, Guilian Gao, K. M. Bang, Bongsub Lee, Laura Mirkarimi – Adeia

3. 10:10 AM – Effect of Surface Roughness of Polymer Dielectric Materials on Resolution of Fine Line Features
Pragna Bhaskar, Mohanalagam Kathaperumal, Christopher Blancher, Mark Losego, Madhavan Swaminathan – Georgia Institute of Technology

4. 11:15 AM – Novel High Reliability and Low Dk/Df Dielectric RDL Material for High Frequency 5G Applications
Koai Hamada, Hiroshi Ozaki, Toshiyuki Sato, Shin Teraki, Fumikazu Komatsu, Masaki Yoshida, Hirotatsu Ikarashi – NAMICS Corporation

Okuno Takahisa, Shino Tetsuya, Usui Yuki, Fukuda Takuya, Tani Masaki, Yagyu Masafumi – Nissan Chemical Industries

6. 11:55 AM – Novel Photosensitive Polymides Compositions with Low Dielectric Property and Good Flexibility Corresponding to Redistribution Layers for High Speed Transmission Applications
Takeaki Tazaki, Takeaki Yamaguchi, Taya Nakamura, Madoka Yamasita – Arakawa Chemical Industries, Ltd.

7. 12:15 PM – High Frequency Characteristics of Fine Copper Lines on High Rigidity Dielectrics
Masataka Nishida, Hirokazu Noma, Tetsuro Iwakura, Masaki Yamaguchi, Kazuyuki Matsukura – Resonac Corporation

8. 12:15 PM – Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding with Low Density TSV for 3D Integration Applications
Josy Javier Suarez Bernu, Stephane Nicolas, Nicolas Bresson, Myriam Assous, Stephan Borel – CEA-LETI

9. 12:45 PM – A Study on the Surface Activation of Cu and Oxide for Hybrid Bonding Joint Interface
Bohe Hwang, Soohwan Lee, Youngkun Jeon, Sangcheon Park, Gyeongae Jo, Kwangbok Kim, Sunjin Han, Ilhwan Kim, Jumyong Park, Hyunchul Jung, Dongwoo Kang, Un-Byoung Kang – Samsung Electronics Co., Ltd.-Test and System Package

10. 12:45 PM – New Cu “Bulge-Out” Mechanism Supporting Sub-Micron Scaling of Hybrid Wafer-to-Wafer Bonding
Jo De Mesmaeker, Liesbeth Witters, Boyso Zhang, Ferenc Pogor, Joeri De Vos, Gerald Beyer, Kristof Croes, Eric Beyne – imec; Yan Wen Tsau – KU Leuven
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<th>Session 6: Co-packaged Optical Assembly</th>
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<td>Mediterranean 6</td>
<td>Mediterranean 7 &amp; 8</td>
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<tr>
<td><strong>Session Co-Chairs:</strong> Ramonee Hadiyadi – Cirrus</td>
<td><strong>Session Co-Chairs:</strong> Xuejun Fan – Lamar University</td>
<td><strong>Session Co-Chairs:</strong> Ajay Jacob – University of Southern California</td>
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<td>Email: <a href="mailto:xuejun.fan@lamar.edu">xuejun.fan@lamar.edu</a></td>
<td>Email: <a href="mailto:ajay@ih.edu">ajay@ih.edu</a></td>
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<tr>
<td>Christo Bajkov – Qorvo, Inc.</td>
<td>Yong Liu – ON Semiconductor</td>
<td>Takaaki Ishigure – Keio University</td>
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<tr>
<td>Email: <a href="mailto:cbbajkov.ectc@gmail.com">cbbajkov.ectc@gmail.com</a></td>
<td>Email: <a href="mailto:Yong.Liu@onsemi.com">Yong.Liu@onsemi.com</a></td>
<td>Email: <a href="mailto:ishigure@app.keio.ac.jp">ishigure@app.keio.ac.jp</a></td>
</tr>
</tbody>
</table>

1. 9:30 AM – Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application
   Henry Antony Martin – Chip Integration Technology Center/Delft University of Technology; Marcia Rantapa, Xiao Tang – Minns BV;Dave Raji, Sander Dorrestijn, Martien Kenger, Sebastian Libon, Edgar Smits, Marco Koolik – Chip Integration Technology Center; Rene Pospelov, Willem Van Driel, GuoQi Zhang – Delft University of Technology

2. 9:50 AM – Optimum Rc Control and Productivity Boost in Wafer-Level Packaging Enabled by High-Throughput UBM/RDL Technology
   Carl Drechsel, Patrik Carazzetti, Juergen Weichart, Ewald Strolz – Evatec AG; Carl Wang – Evatec AG, Taiwan; Kay Vehweger – Fraunhofer IZM

3. 10:10 AM – Assembly Challenges and Approaches for 2.5D Chiplet Based System
   Sharon Pei Siang Lim, Mihai Dragos Rotaru, Wen Wei Sei, Hsiao Hsiang Yao – Institute of Microelectronics A*STAR

4. 11:15 AM – A Methodology to Optimize Laser Dicing Parameters to Maximize Dicing Quality Through Machine Learning
   Sathya Raghavan, Asrakati Jain, Prabudyika Roy Chowdhury, Katsuyuki Saluma – IBM Research; Roman Doll, Kees Biesheuvel, Faysal Bougborhel, Jeroen Van Borkulo, Mark Mueller – ASMPt ALSI B.V.

5. 11:35 AM – Maskless Lithography for High-Density Package Redistribution Layers
   Prahalad Murali, Pratik Nimballkar, Mohanalingam Kathaperumal, Mark D. Losego, Rao Tummala, Madhavan Swaminathan – Georgia Institute of Technology

6. 11:55 AM – An Additive Approach to Embed Chips in a Metalized Matrix Infused PCB
   Roberto Aga, Fahina Ouchen – KBR, Inc.;U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL

7. 12:15 PM – Micro Transfer Printing Various Thickness Components Directly from Dicing Tape
   Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd.

**PROGRAM SESSIONS: WEDNESDAY, MAY 31, 9:30 A.M. -12:35 P.M.**

**Mediterranean 1**

1. 9:30 AM – A Heterogeneously Integrated Wafer-Level Processed Co-Packaged Optical Engine for Hyper-Scale Data Centres
   Sajay Bhavanendran Nair Gourikutty, Boon Long Lau, Wen Wei Sei, Ming Ching Jong, David Ho Soon Lee, Jiaqiu Wu, Tiek Guan Lim, Ratini Mandal, Ser Cheong Chong, Lai Yee Chia, Surya Bhattacharya – Institute of Microelectronics A*STAR; Li Xin, Tsu-Yung Law – Rainbow Photonics Pte. Ltd.

2. 9:50 AM – High Density Integration Technologies for SiPs Based Optical I/Os
   Karlheinz Muth, Hari Poturi, Sukesh Kannan – Broadcom, Inc.

3. 10:10 AM – Photonics System Integration by Applying Microelectronic Packaging Approaches Using Glass Substrates
   Henning Schroeder, Oliver Kirsch – Fraunhofer IZM; Daniel Weber – Technical University Berlin; Hendrick Thiem – TQPTICA eagleyard

4. 11:15 AM – Strain-Relief Patterns for Flexible Substrate-Supported Optimized Serpentine Configurations
   Rui Chen, Chong Ye, Colin Stewart, Suresh Sittaraman – Georgia Institute of Technology

5. 11:35 AM – Filler Particle Distribution Impact for Interfacial Delamination of Underfill
   Yutaka Suzuki, Jaimal Williamson, Li Jiang, Rajen Murugan – Texas Instruments, Inc.

6. 11:55 AM – AIM Photonics Demonstration of a 300 mm Si Photonics Interposer
   Colin McDonough, Seth Kruger, Tat Ngii, Sarah Baranowski, David L. Harame – SUNY Research Foundation/SUNY Polytechnic Institute/AIM Photonics; Hào Yang, Skylar Deckoff-Jones, Christopher V. Poulton, Michael R. Watts – Analog Photonics

7. 12:15 PM – Advanced 3D Integration TSV and Flip Chip Technologies Evaluation for the Packaging of a Mobile LiDAR 256 Channels Beam Steering Device Designed for Autonomous Driving Application
   Thierry Pominier, Nadia Miloud-Ali, Natacha Raphoz, Yacoub Sahouane, Patrick Peray, Damien Saint-Patrice, Edouard Deschaseaux – CEA-LETI; Francois Simoens – Steerlight
Program Sessions: Wednesday, May 31, 2:00 p.m. - 5:05 p.m.

Session 7: Large Formfactor Dense System Integration by Fan-Out

Committee: Packaging Technologies

Palazzo D

Session Co-Chairs: Stefan Kroeheer - ESPAT Consulting, Germany
Email: stefan.kroeheer@espat-consulting.com
Bora Baloglu - Intel Corporation
Email: bora.baloglu@intel.com

1. 2:00 PM – 3D Freeform Antenna-in-Package Approach for FOWLP
   Tanja Braun, Tina Thomas, Karl-Friedrich Becker, Thi Huyen Le, Christian Tschoban, Rolf Aschenbrenner – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin

2. 2:20 PM – Comparable Study for Redistribution Layers in FO POP RDL First and Last (Fan-Out Package on Package)
   Kuei-Hsiao Kuo, Derrick Tai, Sam Peng, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.

3. 2:40 PM – Extremely Large Area Integrated Circuit (ELAIC): An Advanced Packaging Solution for Chiplets
   Rabindra Das, Jason Plant, Alex Wynn, Matthew Ricci, Ryan Johnson, Matthew Stamplis, Brian Tyrrell, Kenneth Schulz, Paul Jodawlkis – MIT Lincoln Laboratory

4. 3:45 PM – Advanced Fan-Out Panel Level Package (FO-PLP) Development for High-End Mobile Application
   Hyungmin Kim, Jeoboon Choi, Seok-Won Lee, Eun Seok Cho, Hwasub Oh, Junho Lee, Seungsu Ha, Wonkyung Choi, Dong Wook Kim – Samsung Electronics Co., Ltd.

5. 4:05 PM – Incorporating Chiplets Using Chips First Ultra-High-Density Fan-Out with Maskless Laser Direct Imaging and Adaptive Patterning for High Performance Computing
   Benedict San Jose, Cliff Sandstrom, Erick Talain, Jan Kellar, Tim Olson – Deca Technologies, Inc.; Mary Maye Melgo, Rui Gacho, Byung Cheol Kim – Napes Hayyim Corporation

6. 4:25 PM – Reliability Challenges of Large Organic Substrate with High-Density Fan-Out Package
   Rosa Lin, Laurence Yip, Charles Lai, Cooper Peng – Mediatek, Inc.

7. 4:45 PM – Flip Chip Process Enablement in IC Memory Stack Die Package

Session 8: Novel Reliability Test Methods

Committee: Applied Reliability

Palazzo A & B

Session Co-Chairs: S. B. Park – Binghamton University
Email: spark@binghamton.edu
Sandy Klengel – Fraunhofer IMWS
Email: sandy.klengel@imws.fraunhofer.de

1. 1:20 PM – A New Vibration Test Method for Automotive and Consumer Electronic Devices: Calibration and Fatigue Test

2. 2:20 PM – Magnetic Force-Based Measurement Technique to Investigate the Effect of Lead-Free Solder Intermetallic Compounds (IMC) on Interconnect Reliability
   Rui Chen, Suresh Sarataram – Georgia Institute of Technology; Nicholas Ginge – University of Alabama in Huntsville

3. 3:40 PM – Residual Stress Measurement of Build-Up Layer in Silicon Wafers
   Junbo Yang, Chongyang Cai, Yangyang Dai, Jing Huan Hu, Seungbae Park – Binghamton University; Huyan Wang, Suresh Ramallangam, Gamal Refai-Ahmed – Advanced Micro Devices, Inc.

4. 4:25 PM – In-Situ Observation of Microscale Crack-Tip Strain Field Evolution in Underfill with Different Toughening Agents via SEM-DIC Coupled Method
   Xuecheng Yu, Gang Li, Yixuan Fan, Rong Sun – University of Technology; Zachary Deveraux, Nyi Myat Khine Madin, Manley, Muhannad Bakir – Georgia Institute of Technology

5. 5:05 PM – A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration
   Krunitkesh Saooh, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

Session 9: Innovations in Copper Chip-to-Wafer Bonding

Committee: Interconnections

Mediterranean 2 & 3

Session Co-Chairs: Wei-Chung Liau – Industrial Technology Research Institute
Email: liau@itri.org.tw
Gu Li – Advanced Semiconductor Engineering, Inc.
Email: gu.li@asees.com

1. 1:20 PM – Critical Challenges with Copper Hybrid Bonding for Chip-to-Wafer Memory Stacking
   Wei Zhou, Michael Kwon, Yingta Chi, Huimin Guo, Bharat Bhusan, Brett Street, Kunal Parekh, Akshay Singh – Micron Technology, Inc.

2. 2:20 PM – Development of Copper Thermal Coefficient for Low Temperature Hybrid Bonding

3. 3:40 PM – Impact of Plasma Activation on Copper Surface Layer for Low Temperature Hybrid Bonding
   Christopher Netzband, Kandabara Tapily, Dylan Burns, Iseeok Son, Cory Wajda – TEL Technology Center, America, LLC

Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom

4. 3:45 PM – Advanced Fan-Out Panel Level Package (FO-PLP) Development for High-End Mobile Application
   Hyungmin Kim, Jeoboon Choi, Seok-Won Lee, Eun Seok Cho, Hwasub Oh, Junho Lee, Seungsu Ha, Wonkyung Choi, Dong Wook Kim – Samsung Electronics Co., Ltd.

5. 4:05 PM – In-Situ Observation of Microscale Crack-Tip Strain Field Evolution in Underfill with Different Toughening Agents via SEM-DIC Coupled Method
   Xuecheng Yu, Gang Li, Yixuan Fan, Rong Sun – University of Technology; Zachary Deveraux, Nyi Myat Khine Madin, Manley, Muhannad Bakir – Georgia Institute of Technology

6. 4:25 PM – Optimization of Cu Interconnects – SiCN Interfacial Adhesion by Surface Treatments
   Dong Jun Kim, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sumin Kang – Korea Institute of Machinery and Materials; Sun Woo Lee, Inwha Lee, Seungpu Park, Jihyun Lee, Joong Jung Kim – Samsung Electronics Co., Ltd.

7. 4:45 PM – Towards Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration
   Madison Manley, Muhammad Bakir – Georgia Institute of Technology; Zachary Deveraux, Niyi Myat Khine Linn, Charles Winter – Wayne State University; Victor Wang, Chenthsuan Kuo, Andrew Kummel – University of California, San Diego
PROGRAM SESSIONS: WEDNESDAY, MAY 31, 2:00 P.M. - 5:05 P.M.

Session 10: Packaging Interconnects
Committee: Thermal/Mechanical Simulation & Characterization

Session 11: Additive Manufacturing and Packaging for Flexible Electronics
Committee: Emerging Technologies

Session 12: mm Wave Antenna-in-Package and Arrays
Committee: RF, High-Speed Components & Systems

**Mediterranean 1**

1. 2:00 PM – Finite Element Analysis of Shock & Vibration of a Printed Circuit Board Assembly Using the Beam Elements to Model the Solder Joints

2. 2:20 PM – Modeling and Optimization of Mechanical Performance for Cu Wire Bonding Process
   Liangbiao Chen, Yong Liu – ON Semiconductor

3. 2:40 PM – High-Temperature Creep Properties of a Novel Solder Material and Its Thermal Fatigue Properties Under Potting Material
   Leiming Du, Guoqi Zhang – Delft University of Technology; Xijuan Zhao, Willem Van Driel – Signify; Rene Poelma – Nexperia

**Mediterranean 6**

1. 2:00 PM – Electromechanical and Thermal Characterization of Printed Liquid Metal Ink on Stretchable Substrate for Soft Robotics Multi-Sensing Applications
   El Mehdi Abbara, Mohammed Ahendi, Riadh Al-haidari, Nathaniel Gee, Mark Poliks – Binghamton University; Emily Bogs, Tan Yevteck, Deepak Trivedi – GE Research; Zachary Farrell, Christopher Tabor – AFRL

2. 2:20 PM – Electrochemical Additive Manufacturing: A Novel Approach to Thermal Management of Electronics
   Madeline Frank, Michael Matthews, Joseph Madril, Ian Winfield – FabricBlabs

3. 2:40 PM – Additively Manufactured Flexible Material Characterization and On-Demand “Smart” Packaging Topologies for 5G/mmWave Wearable Applications
   Kexin Hu, Yi Zhou, Suresh Sitaraman, Manos Tentzeris – Georgia Institute of Technology

**Mediterranean 7 & 8**

1. 2:00 PM – A Scalable Heterogeneous AIP Module for a 256-Element 5G Phased Array

2. 2:20 PM – Metamaterial Based Compact Patch Antenna Array for Antenna-in-Package Solutions in Frequency Handover Applications
   PaymanPahlavan, SukI-Choi, AlexanderWilcher, Hae-inKim, HannaJang, Yong-KyuYoon – University of Florida

**Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom**

4. 3:45 PM – A Novel Stacked-Via Cu/ELK Interconnection Design Configuration to Enhance Advanced Si Packages Performance
   Kuo-ChinChang, Ming-JiLii, Chieh-HaoHsu, Wei-HsiangTu, Tai-ShenYang – Taiwan Semiconductor Manufacturing Company, Ltd.

5. 4:05 PM – Advanced Packaging Methods Used for Storage from Interdependent Renewable Sources
   TakafumiFukushima, JiayiShen, ChangLiu – Tohoku University; TianyuXiang, HarshitRanjan, NiharikaTripathi, RandallIrwin, SubramanianS. Iyer – University of California, Los Angeles

6. 4:25 PM – Additive Methodology Assessment of Copper Trace and Solder Joint Fatigue Failures in Board-Level Random Vibrations for Automotive Applications

7. 4:45 PM – Physics-Driven Regression Algorithm on Solder Joint Fatigue Life Prediction for Mobile SIP Packages
   FuxingChe, YeowChinOng, HongWanNg, LingPan – Micron Semiconductor Asia Operations Pte. Ltd; KoustavSinha, ChristopherGlancey, GokulKumar – Micron Technology, Inc.
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<th>Session 14: Advances in Heterogeneous Integration Bonding Technology</th>
<th>Session 15: Innovative Interposer and Through-Via Technologies</th>
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<td>Mediterranean 2 &amp; 3</td>
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</tbody>
</table>

**Session Co-Chairs:**
- Markus Leitgeb – AT&S AG
- Email: m.leitgeb@ats.net
- Dean Malta – Micross Advanced Interconnect Technology
- Email: Dean.Malta@micross.com
- Markus Leitgeb – AT&S AG
- Email: m.leitgeb@ats.net
- Dean Malta – Micross Advanced Interconnect Technology
- Email: Dean.Malta@micross.com

### 1. 9:30 AM – Supercarrier Redistribution Layers to Realize Ultra Large 2.5D Wafer Scale Packaging by CoWoS

### 2. 9:50 AM – Development of Fine Pitch Backside Redistribution Layer (BRDL) Process in Fan-Out Panel Level Packaging (FOPLP)

### 3. 10:10 AM – Fabrication of Two-Types Panel-Level Interposers with Fine Cu W wirings and Outstanding Electrical Reliability
Masashi Minami, Daiuke Yananaka, Masaya Toba, Shan Ho Tsai, Sadaaki Katoh, Kazuyuki Mitsukura – Resonac Corporation

### 4. 11:15 AM – Warpage Modulation Study on Panel-Level Compression Molding Technology for Heterogeneous Integration Applications
Liang He, Jason Xie, Shishir Deshpande, Andrew Jimenez, Jung Kyu Han, Gang Duan, Rahul Maneppali – Intel Corporation

### 5. 11:35 AM – Signal Integrity of 2-µm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System
Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, Takeshi Tsai, Sadaaki Katoh, Kazuyuki Mitsukura – Resonac Corporation

### 6. 11:55 AM – Thermal and Mechanical Characterization of Embedded PTCQ Packaging Test Chip Die
Gerald Wels, Timo Schwarz, Johannes Stahr, Andreas Zloc – AT&S AG; Vladimir Cherman, Geert Van der Plas – imec

### 7. 12:15 PM – Reliability of Heterogeneous Integration on Hybrid Substrate With Ajinomoto Build-Up Film
Channing Yang, John Lau, Gary Chen, Jones Huang, YH Chen, T. J. Tseng – Unimicron Technology Corp.; Ming Li – ASM Pacific Technology, Ltd.

**Refreshment Break: 10:30 a.m.-11:15 a.m. – Coquina Ballroom**

### 4. 11:15 AM – Low-Stress TSVs for High-Density 3D Integration

### 5. 11:35 AM – Low-Temperature and Pressureless Cu-to-Cu Bonding by Electroless Pd Plating Using Microfluidic System
Po-Shao Shih, Jing-Hsiang Huang, Ching-Hsien Shen, Yu-Chun Lin, Simon Johannes Graefner, Vengudusamy Renganathan, C. Robert Kao—National Taiwan University; Chi-Li Kao, Yung-Sheng Lin, Yun-Ching Hung, Chun-Wei Chiang—Advanced Semiconductor Engineering, Inc.

### 6. 11:55 AM – Volume-Controllable Solder Bumping Technology to Package Substrate Using Injection Molded Solder for Fine-Pitch Flip Chip Application
Toshiyuki Aoki, Hiroaki Mori, Koki Nakamura, Takashi Hisada – IBM Research, Tokyo; Katsuaki Sakuma – IBM Research

### 7. 12:15 PM – Micro-Structure Analysis of Solder Joint Using Room Temperature Laser-Assisted Bonding (LAB) Process
Yoon Hwan Moon, Jiho Joo, Gwang-Mun Choi, Chunmi Lee, Ki-Seok Jung, Ji-Hyuk Oh, In-Seok Kye, Yong-Sung Eom, Kwang-Seong Choi – Electronics Telecommunications Research Institute; Yong-Jun Oh—Hanbat National University

**Session 14: Advances in Heterogeneous Integration Bonding Technology**

### 1. 9:30 AM – Assembly-Based Through-X Via (TXV) Integration Technology by Advanced Fan-Out Wafer-Level Packaging
Atsushi Shinoda, Chang Liu, Tadaaki Hoshi, Jiayi Shen, Yuki Susumago, Hitoshi Kino, Tetsu Tanaka, Takanumi Fukushima—Tohoku University

### 2. 9:50 AM – Development of Fine Pitch Inorganic Temporary Direct Bonding for Collective Die to Wafer Hybrid Bonding
Fumihiro Inoue, Tomoya Iwata, Koki Onishi – Yokohama National University; Shunsuke Terasnishi, Naoko Yamamoto, Akito Kawai—DISCO Corporation; Shintei Aoki, Takashi Hara—Toray Engineering Co., Ltd.; Akira Uedono—University of Tsukuba

### 3. 10:10 AM – Cu Damascene Process on Temporary Bonded Wafers for Thin Chip Stacking Using Cu-Cu Hybrid Bonding
Nagendra Sekhar Vasavara, Dilip Kumar Mishra, S. Choong Chong, Srinivasa Rao Vempati—Institute of Microelectronics A*STAR; Prayudi Lianto—Advanced Materials Singapore

### 4. 11:15 AM – Integrated Optical Interconnect Systems (iOIS) for Silicon Photonics Applications in HPC
C. Key Chung, Han Ryun, Jaehyuk Byun, Jin-Hyun Yoo, Yih-Hung Chen, Min-Suk Lim, Chih-Hung Tung, C. S. Liu, Yutong Wu, K. C. Yee, Douglas C. H. Yu—Taiwan Semiconductor Manufacturing Company, Ltd.

### 5. 11:35 AM – Demonstration of a CMOS-Compatible Superconducting Cryogenic Interposer for Advanced Quantum Processors
King Jien Chui, Yong Chyn Ng, Ya-Ching Tseng, Hongyu Li—Institute of Microelectronics A*STAR
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<td>10:10 AM</td>
<td>High Reliability Design of Ag Sinter Joining on a Softened Crack -Less Ni-P / Pt/Ag Metallization AMB Substrate during Aging and Elastomeric Thermal Cycling</td>
<td>Chuanqin Chen, Yang Liu, Huaping Huo, Katsuki Suganuma – Osaka University; Minoru Ueshima, Takashi Sakamoto – Daicel Corporation; Kazushi Nishida – Osaka University</td>
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<tr>
<td>11:55 AM</td>
<td>Planar SiC Power Module Packaging and Interconnections Using Direct Ink Writing</td>
<td>Radh Ahlaidi, Mohamad Ahlendi, Dylan Richmond, El Mehdi Abbara, Abdullah Oleidat, Mark Polsik, Mark Schadt – Binghamton University; Arun Gowda, Jeffrey Erbbaum, Han Xiong, Collin Hitchcock – GE Research</td>
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<tr>
<td>12:15 PM</td>
<td>Influence of Microscale Tin Particles on Mechanical Properties of Silver Sintering Joints with Reduced Processing Parameters</td>
<td>Steffen Haderle, Yanggang Long, Rico Ottermann, Folke Dencker, Jens Twiefel, Marc Christopher Wurz – Leibniz University</td>
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<tr>
<td>1:30 PM</td>
<td>- Full Coupled Electromigration Modeling Using Peridynamics</td>
<td>Yanan Zhang, Sundaram Vinod Anicole, Erdogan Madenci – University of Arizona; Xuejun Fan – Lamar University</td>
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<tr>
<td>3:30 PM</td>
<td>Scalable Fiber-Array-to-Chip Interconnections with Sub-Micron Alignment Accuracy</td>
<td>Shengtao Yu, Muhammad S. Bakir, Thomas Gaylord – Georgia Institute of Technology</td>
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<tr>
<td>Session 19: Advances in 3D Integration and Hybrid Bonding</td>
<td>Session 20: Automotive/Board-Level Reliability</td>
<td>Session 21: Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections</td>
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**Session Co-Chairs:**
- Peng Su – Juniper Networks
- Email: pensu@juniper.net
- Jaisik Lee – Meta Platforms, Inc.
- Email: jaisiklee@fb.com

1. **2:00 PM – Thermal Improvement of HBM with Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond**
   - Taehwan Kim, Youngdeuk Kim, Heejung Hwang, Hwanjoop Park, Jaechoon Kim, Dan (Kung Suk) Oh – Samsung Electronics Co., Ltd.

2. **2:20 PM – Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing**

3. **3:40 PM – 2.5D MCM (Multi-Chip Module) Technology Development for Advanced Package**
   - Laurene Yip, James Tsai, Rosa Lir, Ian Hsu – MediaTek, Inc.

4. **3:45 PM – Reliability Performance on Fine-Pitch SoIC™ Bond**

5. **4:05 PM – Development of 4 Die Stack Module Using Hybrid Bonding Approach**

6. **4:25 PM – Impact of Dielectric and Copper Via Design on Wafer-to-Wafer Hybrid Bonding**
   - Vikas Dubey, Dirk Wuerisch, Knut Gottfried, Tobias Fischer, Mak Wiemer, Harald Kuhn – Fraunhofer ENAS

7. **4:45 PM – Voids-Free Die-Level Cu/ILD Hybrid Bonding**
   - Katsuyuki Sakuma – IBM Research; Roy Yu, John Knickerbocker, Dale McHerron, Ming Li, Siu Cheung So, So Ying Kwok, Chun Ho Fan, Siu Wing Lau – ASM Pacific Technology, Ltd.

**Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom**

4. **3:45 PM – System-Level Reliability Case Studies of High-Performance Automotive and Medical IC Packages**
   - Li Jiang, Guangue Li, Kejun Zeng, Jaimal Williamson, Rajen Murugan – Texas Instruments, Inc.

5. **4:05 PM – Reliability Challenges and Mitigation Measures of Small Body-Sized Components on Complex and High-Layer Count PCBs**
   - Peng Su, Omar Ahmed, Arman Ahari, Leif Hutchinson, Bernard Glasauer – Juniper Networks

6. **4:25 PM – Investigation on Fatigue Life of Non-Symmetric Solder Joints in Chip Resistors**
   - Jonghwan Ha, Junbo Yang, Pengcheng Yin, Karthic Arun Deo, Chongyang Cai, Seungbae Park – Binghamton University

7. **4:45 PM – Investigation of Acceleration Factors for SnAgCu-Bi Solder Joints Under Various Temperature Cycling Test Conditions**
   - Choongyo Jeon, Youngsun Choi, Kwangwon Seo, Keunho Rhee, Jinsoo Bae, Yuchul Hwang – Samsung Electronics Co., Ltd.; Hyunsik Jeong – Hanyang University

8. **4:05 PM – Impact of Temperature Cycling Conditions on Board Level Vibration for Automotive Applications**
   - Varun Thukral, Irene Bacteur, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc.; Willem Driel, G.Q. Zhang – Delft University of Technology


    - Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Jeffrey Suhling – Auburn University

11. **2:20 PM – Solder Joint Reliability of Fully Homogenised SAC-SnBi Low Temperature BGA Interconnections Using Solid Liquid Inter-Diffusion (SLID)**
    - Haliz Wiaaqib Ali, David Dav immedi, Dominique Drouin – University of Sherborne; Richard Langlois, Robert Martel – IBM Corporation

12. **3:40 PM – Intermetallic Growth Study of Ultra-Thin Copper and Tin Bilayer for Hybrid Bonding Applications**
    - Gaurav Khurana – TU Dresden; Iuliana Panchenko – TU Dresden/Fraunhofer IZM

13. **5:05 PM – A Study on the Advanced Chip to Wafer Stack for Better Thermal Dissipation of High Bandwidth Memory**
    - Sangyoung Lee, Jinwoo Park, Jong-Kyu Moon, Minsuk Kim, Gyujei Lee, Kangwook Lee – SK hynix, Inc.

14. **6:25 PM – Seed Layer Etching, Thermal Reflow and Bonding of Cu-Sn Micro Bumps with 5 µm Diameters**
    - Yufan Shi, Zilin Wang, Zheyao Wang – Tsinghua University

15. **7:45 PM – Development of Fluxless Micro-Bonding and Narrow Gap Filling Process**
    - Sadasuki Katao, Dungchul Kain, Keiko Ueno, Kazuyuki Mitsuka – Resonac Corporation
### PROGRAM SESSIONS: THURSDAY, JUNE 1, 2:00 P.M. - 5:05 P.M.

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<td>Committee: RF, High-Speed Components &amp; Systems</td>
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<td>Mediterranean 6</td>
<td>Mediterranean 7 &amp; 8</td>
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<tr>
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<td>Email: <a href="mailto:voberson@ca.ibm.com">voberson@ca.ibm.com</a></td>
<td>Email: <a href="mailto:rohit@ibtrpr.ac.in">rohit@ibtrpr.ac.in</a></td>
<td>Email: <a href="mailto:rohui@cisco.com">rohui@cisco.com</a></td>
</tr>
<tr>
<td>Jobert Van Eiden – MKS Instruments, Inc.</td>
<td>Email: <a href="mailto:santosh.kudtarkar@analog.com">santosh.kudtarkar@analog.com</a></td>
<td>Chuan-Tiang Wang – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
</tr>
<tr>
<td>Email: <a href="mailto:jobert.van-eiden@istotech.com">jobert.van-eiden@istotech.com</a></td>
<td>Email: <a href="mailto:santosh.kudtarkar@analog.com">santosh.kudtarkar@analog.com</a></td>
<td>Email: <a href="mailto:ctwang10492@hotmail.com">ctwang10492@hotmail.com</a></td>
</tr>
<tr>
<td>1. 2:00 PM – Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology</td>
<td>1. 2:00 PM – Thermal-Aware SoC Macro Placement and Multi-Chip Module Design Optimization with Bayesian Optimization</td>
<td>1. 2:00 PM – Comprehensive PDN/PSIJ Analysis of Silicon Capacitor Use for 8.533 GT/s LPDDR5X Application</td>
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<tr>
<td>2. 2:20 PM – Study of Fabrication and Reliability for the Extremely Large 2.5D Advanced Package</td>
<td>2. 2:20 PM – 3D Defect Detection and Metrology of HBMx Using Semi-Supervised Deep Learning</td>
<td>2. 2:20 PM – Design Considerations for Power Delivery Network and Metal-Insulator-Metal Capacitor Integration in Bridge-Chips for 2.5-D Heterogeneous Integration</td>
</tr>
<tr>
<td>Karthik Arun Deo, Yangxian Lai, Junbo Yang, Jong Hwan Ha, Pengcheng Yin, Seungbae Park – Binghampton University</td>
<td>Takuya Wadatsumi, Riku Hasegawa, Kazuki Manta, Takuji Miki, Makoto Nagata – Kobe University, Takaaki Okidono – SCU Co., Ltd.</td>
<td>Sodam Han, Sungwook Moon, Jungil Son, Seungki Nam – Samsung Electronics Co., Ltd-Foundry Business</td>
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<tr>
<td>4. 3:45 PM – Lead Frame vs. Mold Via</td>
<td>4. 3:45 PM – Physical Authentication of Electronic Devices Using Synthetically Generated 3D Material Signatures</td>
<td>4. 3:45 PM – HBM3 Modules on Latest High Density Organic Laminate—Signal Integrity Design and Analysis with Interconnect Budget Results</td>
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<td>Rathin Mandal – Institute of Microelectronics A*STAR</td>
<td>Tejas Ravindra Kulkarni, Nikhilesh Chawla, Ganesh Subbarayan – Purdue University</td>
<td>Frank Libsch – IBM Research; Hiroyuki Mori – IBM Research, Tokyo</td>
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<tr>
<td>5. 4:05 PM – A Novel Low-Temperature Connection and High-Temperature Curing Process for Reducing the Warpage of Bonding Pair in Fan-Out Wafer Level Packaging</td>
<td>5. 4:05 PM – Modeling and Analysis of CMOS-Based Folded Memristive Crossbar Array for 3D Neuromorphic Integrated Circuits</td>
<td>5. 4:05 PM – Signal and Power Integrity Design and Analysis for Bunch-of-Wires (BoW) Interface for Chiplet Integration on Advanced Packaging</td>
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<tr>
<td>Yun Bai, Kang Li, Cheng Zhong, Qiang Liu, Jinhui Li, Guoping Zhang, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology</td>
<td>Sherin A. Thomas, Sahibia Kaur Vohra, Suyash Kushwaha, Rohit Sharma, Devashi Mrinal Das – Indian Institute of Technology Ropar</td>
<td>Ram Krishna, Elsey Rosenbaum – University of Illinois; Atomi Watanabe, John Golz, Ravi Bonam, Frank Libsch, Arvind Kumar – IBM Corporation</td>
</tr>
<tr>
<td>7. 4:45 PM – Thermal Solutions for Large Die and Package</td>
<td>7. 4:45 PM – Characterizations of Indium Interconnects for 3D Quantum Assemblies</td>
<td>7. 4:45 PM – Signal Integrity Co-Design of a High-Speed (20 Gbps) Analog Passive CMOS Switch</td>
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Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom
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<th>Session 25: Next Generation High-Performance Computing Architectures</th>
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<th>Session 27: Next Generation Wafer-to-Wafer Copper Bonding</th>
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<td><strong>Committee:</strong> Applied Reliability</td>
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<tbody>
<tr>
<td>Eric Tromble – Marvell</td>
<td>Nandish Sharma – Texas Instruments, Inc.</td>
<td>Li Li – Infinera Corporation</td>
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<tr>
<td>Email: <a href="mailto:etremble@marvell.com">etremble@marvell.com</a></td>
<td>Email: <a href="mailto:nandish.sharma@ti.com">nandish.sharma@ti.com</a></td>
<td>Email: <a href="mailto:packaging@yahoo.com">packaging@yahoo.com</a></td>
</tr>
<tr>
<td>Subhash L. Shinde – Notre Dame University</td>
<td>Email: <a href="mailto:eunice.davis@ti.com">eunice.davis@ti.com</a></td>
<td>Email: <a href="mailto:dingyouzhang.brcm@gmail.com">dingyouzhang.brcm@gmail.com</a></td>
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<tr>
<td>Email: <a href="mailto:sshinde@nd.edu">sshinde@nd.edu</a></td>
<td>Email: <a href="mailto:packaging@yahoo.com">packaging@yahoo.com</a></td>
<td>Email: <a href="mailto:dingyouzhang.brcm@gmail.com">dingyouzhang.brcm@gmail.com</a></td>
</tr>
</tbody>
</table>

1. **9:30 AM – CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package**

2. **9:50 AM – Reliability Performance of S-Connect Module (Bridge Technology) for Heterogeneous Integration Packaging**
   Heejun Jung, Kyun Ahn, Gamhan Yong, Won-Ho Choi, Ji-Hyun Kim, Dave Hiner, Taekyeong Hwang, Mike Kelly, WonChul Do, JinYoung Kim – Amkor Technology, Inc.

3. **10:10 AM – Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration**
   Lihong Cao – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang, Chih-Yi Huang – ASE Corporate R&D Center

   Po Yuan (James) Su, David Ho, Jacy Pu, Yu Po Wang – Siliconware Precision Industries Co., Ltd.

5. **11:35 AM – Die to Wafer Hybrid Cu Bonding for Fine Pitch 3D-IC Applications**
   Yeongseon Kim, Juhyeon Kim, Hyeokun Kim, Dohyun Kim, Seokkyung Seo, Chajea Jo, Dae-Woo Kim – Samsung Electronics Co., Ltd.

6. **11:55 AM – C2W Hybrid Bonding Interconnect Technology for Higher Density and Better Thermal Dissipation of High Bandwidth Memory**
   Kibum Kim – SK hynix, Inc.

7. **12:15 PM – Direct Bonded Heterogeneous Integration (DBHi): Surface Bridge Approach for Die Tiling**
   Claudia Cristina Barrera Pulido, Divya Taneja, Philip McIntyre, Isabel De Sousa – IBM Canada, Ltd.; Sayuri Kohara, Akihiro Horibe – IBM Japan, Ltd.; Aakrati Jain, Thomas Wasick – IBM Corporation

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**PROGRAM SESSIONS: FRIDAY, JUNE 2, 9:30 A.M. -12:35 P.M.**

**Refreshment Break: 10:30 a.m.-11:15 a.m. – Mediterranean & Palazzo Foyers**

4. **11:15 AM – Fine-Pitch 30 µm Cu-Cu Bonding Using Electroless Nano-Ag**
   Hsiang-Wei Tsai, Yung-Sheng Lin, Chun-Wei Chang, Yun-Ching Huang, Chin-Li Kao, Ping-Hung Hsieh, I-Ting Lin, Chih-Yuan Hsu – Advanced Semiconductor Engineering, Inc.

5. **11:35 AM – Influence of H2O in Bonding Interfaces on Bonding Strength of Plasma-Activated Bonded Silicon Oxide**
   Hirotaka Yoshikawa, Nobutoshi Fuji, Takashi Shigetoshi, Takahiro Kamei, Kengo Kato, Naoki Ogawa, Tatsuya Honkiri, Shunsuke Furuse, Sotetsu Saito, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation

6. **11:55 AM – All Nanograined Copper Is Not Created Equal**
   Yun Zhang, Peipei Dong, Jing Wang, Xingping Zhang – Shin-hao Materials LLC; Klaus Leyendecker, Tsvetina Dobrovolska, Michael Herkommer, Volker Wohlfarth, Josh Liang – Unimicron Galvanotechnik GmbH
## PROGRAM SESSIONS: FRIDAY, JUNE 2, 9:30 A.M. -12:35 P.M.

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<th>Session</th>
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<th>Speakers</th>
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<tr>
<td><strong>1. 9:30 AM – Magneto-Assisted Graphene Reinforcement: A New Method to Enhance Nanostructure and Properties of Electrodeposited Copper</strong></td>
<td>Nithin Nedumthakady, Pragna Bhaskar, Vanessa Smet – Georgia Institute of Technology</td>
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<tr>
<td><strong>1. 9:30 AM – Liquid Compression Mold Underfill Optimization with Low Warpage and Narrow Gap Flow</strong></td>
<td>Tsuyoshi Kamimura, Shinichi Sato, Yuto Shigeno – NAMICS Corporation; Brian Schmaltz – NAMICS Technologies, Inc.</td>
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<tr>
<td><strong>2. 9:50 AM – ARTSims: A Robust Thermal Simulator for Advanced Integration Platforms</strong></td>
<td>Yousef Safari, Adam Corbier, Dina Al Saleh, Boris Vaidsond – McGill University</td>
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<tr>
<td><strong>2. 9:50 AM – Effects of High-Temperature Exposure on the Thermo-Mechanical Behavior of Epoxy Molding Compound and Warpage of Molded Wafers</strong></td>
<td>Junmo Kim, Myoung Song, Chang-Yeon Gu, Min Sang Ju, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sung Woo Ma, Jin Hee Lee, Woong-Sun Lee – SK hynix, Inc.</td>
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<tr>
<td><strong>3. 10:10 AM – Reduced-Order Models of Digital Twin Applications for Design Platform of Flexible Hybrid Electronics</strong></td>
<td>Chang-Chun Lee – National Tsing Hua University; Ji-Chang Chang, Chen-Tsai Yang, Chung-I Li – Industrial Technology Research Institute</td>
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<tr>
<td><strong>3. 10:10 AM – Low Temperature Fine Pitch All-Copper Interconnects Combining Photopatternable Underfill Films</strong></td>
<td>Xunru Ji, Henk Van Zeijl, Weiping Jiao, Shan He, Leiming Du, Guoqi Zhang – Delft University of Technology</td>
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<tr>
<td><strong>4. 11:15 AM – Methodology of Artificial Intelligence Aided Hybrid Modeling for Predicting Solder Joint Reliability of BGA Package</strong></td>
<td>Ling Pan, Faming Che, Yeow Hon Chong, Hong Wan Ng – Micron Semiconductor Asia Operations Pte. Ltd; Christopher Glancye, Goluk Kumar – Micron Technology, Inc.</td>
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<tr>
<td><strong>4. 11:15 AM – Novel Low Dk/Df Photoinitable Dielectric for Redistribution Layer</strong></td>
<td>Guillermo Fernandez Zapico, Fumihiko Kawauchi, Shinya Kawashita, Manabu Hirasawa, Kitaru Sato, Tsuyoshi Ima, Hidekazu Kondo, Tatsuya Makino – Renoson Corporation</td>
<td></td>
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<tr>
<td><strong>5. 11:35 AM – The Advantages of Low Temperature (&lt;400 °C) Carbon Nano-Tubes (CNTs) as Through Silicon Vias (TSVs) in Multi-Layers Stacking and Backside Power-Via Applications</strong></td>
<td>Niall Bu, X-Y. Lin, T-W. Chen, Y-C. Chan, Y-T. Tsai, H-C. Guo, T-H. Wu, P-C. Lin, Y-C. Lin, Ming-Han Liao – National Taiwan University</td>
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<tr>
<td><strong>5. 11:35 AM – Effect of Li-Ion Battery Form Factor on the SoH Degradation Under Randomized Charge-Discharge Cycles and C-Rates</strong></td>
<td>Pradeep Lall, Ved Soni – Auburn University</td>
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<tr>
<td><strong>6. 11:55 AM – Al-Based Design Framework for Warpage Control of Fan-Out Panel-Level Package</strong></td>
<td>Peilun Yao, Yonglin Zhang, Jingfei Yang – Hong Kong University of Science and Technology; Haibin CHEN, Jingshen Wu – Hong Kong University of Science and Technology (Guangzhou); Halbo Fan, Anthony Cheung – Nexperia HK, Ltd.</td>
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<tr>
<td><strong>7. 12:15 PM – Next Generation Infrared (IR) Laser Debonding / Silicon Handle Technology for Precision Chiplet Technology Applications</strong></td>
<td>Qianwen Chen, Michael Belyansky, Yair Sulehria, Akishiro Honibe, Eric Perfetto, Katsuyuki Sakuma, John Knieterbocker – IBM Corporation; Takeshi Tabara, Takayuki Ishii, Parupong Japan, Satoshi Nishimura Nishimura, Ilesk San – Tokyo Electron, Ltd.</td>
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<tr>
<td><strong>7. 12:15 PM – Thermal Characterization of 3-D Stacked Heterogeneous Integration (HI) Package for High-Power Computing Applications</strong></td>
<td>Aakrati Jain, Sathya Raghavan, Prabudhya Roy Chowdhury, Muka Ghate Farooq, Arvind Kumar, Katsuyuki Sakuma – IBM Research; Risa Miyazawa – IBM Research, Tokyo</td>
<td></td>
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*Session Co-Chairs:
1. Vidya Jayaram – Intel Corporation
2. Patrick McCluskey – University of Maryland
3. Patrick McCluskey – University of Maryland
4. Patrick McCluskey – University of Maryland
5. Patrick McCluskey – University of Maryland
6. Patrick McCluskey – University of Maryland
7. Patrick McCluskey – University of Maryland
8. Patrick McCluskey – University of Maryland
*

**Refreshment Break: 10:30 a.m.-11:15 a.m. – Mediterranean & Palazzo Foyers**
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<th>Session 33: Advances in RDL, Via, and TSV Technologies for Chiplet Integration</th>
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**Session Co-Chairs:**
- Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Khim – Amkor Technology Korea
- JiHye Kwon, JeongMin Ju, EunSook Sohn, JinYoung KilJae Lee, Sangdeok Kim – SK hynix, Inc.
- Bongchan Son, Seung-Hyun Chae, SeungKwon Noh, Lifetime Model

1. **2:00 PM – Enabling Backside Processing for Perforated Microfluidic Devices**
   - Jakob Visler, Yang Han, Evert Visker, Chi Dang Thi Thuy, Mateusz Gocyla, Jan Ackaert, Aurelie Humbert, Serge Vanhaecke, Lang Peng – imec
   - Emphasis on an Improved Solder Fatigue Cycling Profiles and Material Selections with Joint Reliability Dependent on Temperature

2. **2:20 PM – Wafer Level Chip Scale Package Technology Applied to MEMS Pressure Sensor**
   - Luca Maggi, Marco Del Sarto, Tiziano Chiarillo, Enri Duqi, Lorenzo Baldo, Adriano Abbisogno – STMicroelectronics
   - 6 µm-Pitch Cu-Cu Connections Using over-400 mm²-Large Chip on Wafer Bonding Process

3. **2:40 PM – A Novel FOWLP Method to Integrate Delicate MEMS Components**
   - Markus Woehrmann, Tanja Braun, Michael Schiffer, Martin Schneider-Ramelow – Fraunhofer IZM; Marc Dreissigacker – Technical University Berlin
   - Transient Prediction Accuracy for Mobile AP Interconnect

4. **3:45 PM – Development of High Reliability 6 µm-Pitch Cu-Cu Connections Using over-400 mm²-Large Chip on Wafer Bonding Process**
   - Takahiro Kamei, Hironaka Yoshieka, Tatsumasa Hiratsuka, Akihisa Sakamoto, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation
   - Capacitor with Embedded Package Platform

5. **4:05 PM – A Comprehensive Study of Solder Joint Reliability Depending on Temperature Cycling Profiles and Material Selections with Emphasis on an Improved Solder Fatigue Lifetime Model**
   - Development of Plasma Etching Process of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging

   - JHyre Kwon, JeongMin Ju, EunSook Sohn, JinYoung Khim – Amkor Technology Korea
   - Improvement of Warpage Characterization of Large Wafers in Fan-Out Packaging

7. **4:45 PM – Simulation-Assisted Board Level Solder Joint Reliability Optimization for Large 80 mm+ 2.5D Devices**
   - Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Glassauer – Juniper Networks; Vishnu Shukla, Tengfei Jiang – University of Central Florida
   - Fine Pitch Micro Via Interconnection with Reliable Electraclecs/Electric Cu Plating Layers Combined with High Power DUV Picosecond Laser for Organic Substrates

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**Refreshment Break: 3:00 p.m. - 3:45 p.m. – Mediterranean & Palazzo Foyers**

4. **3:45 PM – Effect of Passivation and Mechanical Constraint on Electromigration in Interconnect**
   - Xuejun Fan – Lamar University; Zhen Cui, Guoqi Zhang – Delft University of Technology

5. **4:05 PM – Improving Warpage Characterization of Large Wafers in Fan-Out Packaging**
   - Saskia Gesche Huber, Andreas Stegmaier, Marius van Dijk, Nina Nguyen, Ole Hoelck, Olaf Wittler, Martin Schneider-Ramelow – Fraunhofer IZM

   - Hwanwoo Park, Jongyu Lee, Tae-Su Kim, Sungu Kang, Sungho Mun, Jaehoon Kim, Dan Oh – Samsung Electronics Co., Ltd.

7. **4:45 PM – Fan-Out Embedded Bridge with TSV(FO-EB-T) Package Characterization and Evaluation**
   - Vito Lin, Andrew Kang, Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

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**Program Sessions: Friday, June 2, 2:00 P.M. - 5:05 P.M.**

**Program Sessions:**
- Embedded Microchannel Cooling System Based on Flexible Manifold for High-Performance Computing ICs
- On the Path to AI Hardware via High-Speed TSVs
- Development of High Density Interconnects in Advanced Packaging
- Dynamic Heating Scan: An Overlooked Second Reaction
- Advances in RDL, Via, and TSV Technologies for Chiplet Integration
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<th>Session 35: Packaging and Materials for Flexible Medical Technologies</th>
<th>Session 36: RF, Heterogeneous, and Chiplet Modules</th>
</tr>
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<td><strong>Committee:</strong> Emerging Technologies</td>
<td><strong>Committee:</strong> RF, High-Speed Components &amp; Systems</td>
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<td>Mediterranean 1</td>
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<td>Mediterranean 7 &amp; 8</td>
</tr>
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</table>

**Mediterranean 1**

**1. 2:00 PM – Laser-Assisted Bonding with Compression (LABC) Based Tiling Bonding Technology, Enabling Technology for Chiplet Integration**
Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Channim Lee, Ho-Geun Yun, Seok Hwan Moon, Ki-Seok Jang, Jin-Hyk Moon, Yuon-Hwan Moon, Yong-Sung Eom – Electronics Telecommunications Research Institute

**2. 2:20 PM – Contamination-Free Cu/SGCN Hybrid Bonding Process Development for Sub-mum Pitch Devices with Enhanced Bonding Characteristics**
Seung Ho Hahn, Wooyoung Kim, Donggup Shin, Yongin Lee, Sunin Kim, Wonyoung Choi, Kyeoengbin Lim, Bumki Moon, Minwoo Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research

**3. 2:40 PM – Integration and Process Challenges of Self Assembly Applied to Die-to-Wafer Hybrid Bonding**
Emilie Bourjot, Alice Bond, Noura Nadi, Thierry Enot, Loic Sanchez, Pierre Montmeat, Beroit Martin, Alain Beyne – imec; Thomas Uhrmann, Thomas Plach – EV Technology

**4. 3:45 PM – Critical Dimension Scattering as a Scalable Solution for Hybrid Bonding Pad Recess Metrology**

**5. 4:05 PM – Development of PMUT Array Packaging from Characterization Prototypes to Customer Samples**
Mark Andrew Shaw, Domenico Guisti, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Klug, Hitoshi Hoshibi – DISCO HITEC Europe; Vempati Srinivas Rao, Dutta Rahil, David Ho Soon Wee – Institute of Microelectronics A*STAR; Hideyuki Sandoh, Masatochi Wakahara – DISCO Corporation; Alessandro Savoia – Rama Tre University

**6. 4:25 PM – Modeling of the Temperature Profile and Residual Stress During Thermal Compression Bonding in 3D Packages**
Prabuddha Roy Chowdhury, Sathya Raghavan, Luke Darling, Aakrati Jain, Promod R. Chowdhury, Muktai Ghate Farooq, Katsuyuki Sakuma – IBM Research

**7. 4:45 PM – Impact of Thermal Annealing and Other Process Parameters on Hybrid Bonding Performance for 3D Advanced Assembly Technology**
Taiwo Ajayi, Alvin Gatinu, Chris Woods, Xavier F. Brun – Intel Corporation; Abhishek Bhat, Kay Song, Zia Karim, Charudatta Gande, Phillip Le – Yield Engineering Systems

**Mediterranean 6**

**1. 2:00 PM – Fully Portable Wireless Soft Stethoscope and Machine Learning for Continuous Real-Time Auscultation and Automated Disease Detection**
Sung Hoon Lee, Yun-Soung Kim, Woon-Yong Yeo – Georgia Institute of Technology

**2. 2:20 PM – Patch-Type Flex SiP Platform for Healthcare Application**
Ming-Hung Chen, Wei-Hao Chang, Hu-Ping Jhan, Chao-Wei Liu, Shang-Lin Wu, Yi-Chun Chou, Sung-Hung Chiang, Jung-Kai Chang, Tun-Ching Pl Wei-Chen Lee, Jen-Chieh Kao, Yung-I Yeh – ASE Corporate R&D Center

**3. 2:40 PM – Development of PMUT Array Packaging from Characterization Prototypes to Customer Samples**
Mark Andrew Shaw, Domenico Guisti, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Klug, Hitoshi Hoshibi – DISCO HITEC Europe; Vempati Srinivas Rao, Dutta Rahil, David Ho Soon Wee – Institute of Microelectronics A*STAR; Hideyuki Sandoh, Masatochi Wakahara – DISCO Corporation; Alessandro Savoia – Rama Tre University

**4. 3:45 PM – Multi-Cell Array of Nanogap Electrodes for Labelfree Detection of Biomolecules**
Musalavgari Sikkandhar, Yu Chen, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

**5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging**
Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Binghamton University

**6. 4:25 PM – 3D Printed Electronics with Multi Jet Fusion for Flexible Hybrid Electronics**
Jarid A. Wittkopf, Sanil Jhaveri, Fan Fei, Manjari Mrinal, Eric Luna-Ramirez, Lihua Zhao – HP Inc; Dylan Richmond, Dayue Jiang, Fuda Ning, Mohamed Alhendi, Deloit Smilgies, Mark Polks – Binghamton University

**7. 4:45 PM – Performance Evaluation of RF Novel Microstrip Lines Printed on Flexible Substrates**
Abdullah Obeidat, Mohammad Alhendi, Mohamed Abdelatty, Ashraf Umar, Emnuobosan Enakerako, Riadh Al-Haidari, Mark Polks – Binghamton University

**Mediterranean 7 & 8**

**1. 2:00 PM – Heterogeneous Radio Chiplet Module for 5G Millimeter Wave Application**
Agnete Ljungbro, Emil Nylander, Martin Hansson – Ericsson AB; Marcel Wieland, Jungtai (Osbon) Ok, Selaka Bulumulla – GlobalFoundries, Inc.

**2. 2:20 PM – Design and Analysis of 3D Heterogeneous Chiplet Stack for RF Front-End Module Miniaturization**
Mihai Rotaru, Chai Tai Chong, Chui King Jen – Institute of Microelectronics A*STAR; Shashank Tiwari – GlobalFoundries, Inc.; Paul Castilou – Qorvo, Inc.

**3. 2:40 PM – Embedded mm-Wave Chiplet Based Module Using Fused-Silica Stitch-Chip Technology: RF Characterization and Thermal Evaluation**
Ting Zheng, Madison Manley, Muhammad S. Bakir – Georgia Institute of Technology

**4. 3:45 PM – Critical Dimension Scattering as a Scalable Solution for Hybrid Bonding Pad Recess Metrology**

**5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging**
Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Binghamton University

**6. 4:25 PM – Optimal Channel Design for Die-to-Die Interface in Multi-Die Integration Applications**
Alexander Witcher, Hae-In Kim, Ziqi Jia, David Arnold, Yong-Kyu Yoon – University of Florida; Jia Chieh, Alex Phipps – Naval Information Warfare Center Pacific

**6. 4:25 PM – Optimal Channel Design for Die-to-Die Interface in Multi-Die Integration Applications**
Jiyong Park, Seungki Nam, Sungwook Moon, Jinho Seung Ho Hahn, Woon-Hong Yeo – Georgia Institute of Technology

**7. 4:25 PM – Highly Energy Efficient and Electromagnetic Interference Immune Coaxial Through-Substrate-Vias (cx-TSVs) for Millimeter Wave Applications**
Saeong Jeon, Hae-In Kim, Yong-Kyu Yoon – University of Florida
INTERACTIVE PRESENTATIONS: WEDNESDAY, MAY 31, 10:00 A.M. - 12:00 NOON AND WEDNESDAY, MAY 31, 2:30 P.M. – 4:30 P.M.

Wednesday May 31
Session 37: Interactive Presentations 1
Time: 10:00 a.m. – 12:00 p.m.
Committee: Interactive Presentations

Palazzo Foyer
Session Co-Chairs:
Mark Pollakis – Binghamton University
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Pradeep Lall – Auburn University
Email: lall@auburn.edu
Kristina Young – GlobalFoundries, Inc.
Email: kristina.youngfisher@gmail.com
Jae Kyu Cho – GlobalFoundries, Inc.
Email: jaekyu.cho@globalfoundries.com

1. Investigation of Cu-to-Cu and Oxide-to-Oxide Bonding
Sangmin Lee, Gwanggil Oh, Junyoung Choi, Yoonho Kim, Sangwoo Park, Sarah Kim – Seoul National University of Science and Technology

2. Doping-Selective Etching of Silicon for Wafer Thinning in the Fabrication of Backside-Illuminated Stacked CMOS Image Sensors

3. Study of Solder Resist Crack Resistance for Flip Chip Ball Grid Array Substrate
Eric Chen, Rick Yi, Wei-Kyu Teng, Yu-Cheng Ps, Yu Po Wang – Silware Precision Industries Co., Ltd.

4. Reliability Analysis on Ag and Cu Nanoparticles Sintered Discrete Power Devices with Various Frontside and Backside Interconnects
Dong Hu, Xu Liu, Sten Vollebregt, Jiajie Fan, Guoqiu Zhang – Delft University of Technology; Ali Roshanghias – Silicon Austria Labs GmbH; Xing Liu, Thomas Basler – Chemnitz University of Technology; Emil De Bruin – Boschman Advanced Packaging Technology B.V.

5. Impact of Process Parameters on Vacuum Fluidless Solder Reflow Performance in Backend Applications with Bump Pitch of 15 µm and Below
Lei Jing, Vladimir Kudriavtsev, Taylor Nguyen, Jed Hsu, Tapani Laaksoenen, Alvin Lin, Xiren Tan, Kay Song, Alex Chow, Chris Lane, Zia Karim – Yield Engineering Systems

6. Surface Modification on Hydrophobic Enhancement Using NH₄OH, NaOH and KOH on Fine-Pitch Low Temperature Cu/SiO₂ Hybrid Bonding
Ja-Juen Ong, Deepthi Kandasamy, Eng Huat Toh, Louis Lim – GlobalFoundries Singapore

7. Development and Demonstration of a Novel Immersion Two Phase Cooling High Power SiC Power Module
Gonggue Tang, Leong Ching Wai, Huicheng Feng, Haozan Chen – Institute of Microelectronics A*STAR

8. Electrochemical Deposition of Indium Bumps on Superconducting Interconnect and Thermocompression Bonding for Cryogenic and Quantum Computing
Kumin Kang – Hanyang University; Jaber Derakhshandeh – imec

9. 6-Sided Die Chipset for Chiplet Package with Multi-Layer RDL
ByungCheol Kim, Mary Maye Melgo, Riz Gacho, Jacinta Aman Lim, Hee Yeoul Yoo, Kwan Sun Oh – nespes Corporation; Cliff Sandstrom, Benedict San José – Deca Technologies, Inc.

10. Wafer Level Capping Technology for Vacuum Packaging of Microbolometers
Kai Zoschke, Charles-Alex Marier, Hermann Oppermann – Fraunhofer IZM; Dirk Meier, Nishant Malik – Integrated Detector Electronic; AS, Elke Zalkazde, Martin Daniel Michel – Fraunhofer IMS; Aviash Ray, Hoang-Vu Nguyen, Hexion Xia – University of South-Eastern Norway

11. Artificial Intelligence (AI) Based Methodology to Minimize Asymmetric Bare Substrate Warpage
Sathyi Raghavan, Griselda Bonilla, Katsuyuki Sakuma – IBM Research; Hiroyuki Mori – IBM Research, Tokyo

12. Scaling of Redistribution Layer for Heterogeneous Packaging in a Panel Level
Yoonyoung Jeon, Youngmin Kim, Hyundong Lee, Minji Kim, Woonjeon Lee, Joonsoek Oh – Samsung Electronics Co., Ltd.

13. Process Challenges During CVD Oxide Deposition on the Backside of 20 µm Thin 300-mm Wafers Temporarily Bonded to Glass Carriers
Koen Kennes, Abdelbaki Salahoueddah, Samuel Suhard, Jaber Derakhshandeh, Alain Phommahaxay, Steven Brems, Gerald Beyer, Eric Beyne – imec; Alce Guerrero, Xiao Liu – Brewer Science, Inc.

14. Electrical Characterization and Modeling of 2-µm and 1.5-µm Line-and-Space High-Density Signal Wiring in Organic Interposer
Atom Watanabe, Hiroyuki Mori, Xiaoxiong Gu, Frank Litsch, Griselda Bonilla – IBM Corporation

15. Package Integrated Vapor Chamber Heat Spreader
Cameron Nelson – Amkor Technology, Inc.; SangHyuk Kim – Amkor Technology Korea

16. Analysis of Package-to-System Interaction on Thermal Performance of Large 2.5D Packages Using 3DFabric® Platform
Po-Yao Lin, Kathy Yan, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.

17. Evaluation of Parylene-HT as Dielectric for Application in Advanced Package Substrates
Pratik Nimbalakar, Mohanalingam Kathaperumal, Madhavan Swaminathan, Rao Tummalapalli – Georgia Institute of Technology

Joon Woo Kim, Xingchen Li, Xiaofan Jin, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology

Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

20. Metal Additively Microfabricated SiPs with Embedded Microfluidic Cooling Towards Heterogeneous Integration with SoCs
Bhushan Lohani, Sheikh Dobar Hussain, Robert C. Roberts – University of Texas, El Paso

21. Large Wafer GaN on Silicon Reconstitution with Gold-to-Gold Thermocompression Bonding
Ankit Kuchhia, Krutikshah Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

Friday May 31
Session 38: Interactive Presentations 2
Time: 2:30 p.m. – 4:30 p.m.
Committee: Interactive Presentations

Palazzo Foyer
Session Co-Chairs:
Rao Bonda – Amkor Technology, Inc.
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Mohammad Enamul Kabir – Intel Corporation
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Saikat Mondal – Intel Corporation
Email: saikat.mondal@intel.com
Donna M. Noctor – Nokia Corporation
Email: donna.noctor@nokia.com

1. Advanced Overlay Metrology for CIS Bonding Applications
Florent Dettoni, Emilie Deloffre – STMicroelectronics; Yoav Grauer, Shlomo Eisenbach, Motti Penia, Arkadi Simkin, Dror Elia, Avner Safrai, Marco Polli, Francesco De Paola – KLA Corporation

2. Implementation of New Robustness Assessment Methodology for Crack Stop Constructions
Maria Heidenblut, Michael Gorol – Infineon Technologies AG

3. Hybrid Bonding Utilizing Molding Compound and Dielectric Systems
Yuki Imazu, Kazuya Katsuura – Resonac Corporation

4. A Short Time and N2-Sinterable Cu Sinter Paste with Highly Dispersed Submicron Cu Particles
Takaaki Eyama, Shuichi Inaya, Ukyo Suzuki, Masafumi Takesue – Kao Corporation

5. A Novel and Simple Method of Low Temperature, Low Process Time, Pressureless Interconnection for 3D Packaging
Jeng-Hau Huang, Po-Shao Shih, Chang-Hsien Shen, Vengudusamy Rengarathan, Simon Johannes Graefner, Yu-Chun Lin, C. Robert Kao – National Taiwan University; Chih-Li Kao, Yong-Sheng Lin, Yun-Ching Hung, Chun-Wei Chang – Advanced Semiconductor Engineering, Inc.

6. 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding by High-precision Alignment Technologies
Hajime Mitsuishi, Hiroshi Mori, Masahiko Maeda, Mikio Ushijima, Atsushi Kamashita, Masahi Okaeda, Masanori Aramatsu, Takashi Shimi, Shinya Sakamoto, Kishou Takahata, Tomohiro Chiba, Minoru Fukuda, Masahiro Kanbayashi, Toshinasa Shimoda, Isao Sugaya – Nkon Corporation

7. Multi-Stack Hybrid Cu Bonding Technology Development Using Ultra-Thin Chips
Min-Ki Kim, Hyukje Lee, Aeri Jung, Seungduk Baek, Ilwon Han, Youngjin Jee, Hyun-Chul Jung, Un-Byung Kang, Dae-Woo Kim – Samsung Electronics Co., Ltd.- Test and System Package

8. An Investigation on Particle Embedding Capability of Wafer Level Spin-on Polymer Underfill Enabling Low Temperature Bonding of Hybrid Bonding System
Hiroto Noda, Akihiro Hiro, Naoki Nishiguchi – JSR Corporation; Jaber Derakhshandeh, John Stabbeloom, Eric Beyne – imec

Wednesday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. – 3:45 p.m. – Coquina Ballroom

10. The Full-IMCs Interconnects Through Transient Liquid Phase Bonding of Ga/Cu System for Advanced Electronic Packaging
Yi Chen, Zhaoxia Zhou, Changbin Liu – Loughborough University

11. Selective Self-Assembled Monolayer for Copper Surface Protection During Plasma Activation of Hybrid-Bonded Wafers
Jack Rogers – TEL Technology Center, America, LLC

12. Development of a Heterogeneous Integration of GaN Power Device on Si-LSI
Shane Miyasaka, Yusuke Norieka, Ayano Funke, Satoshi Shinkai, Satoshi Matsumoto – Kyushu Institute of Technology

13. Integrated pH and Strain Sensors Development for Nasogastric Tube Placement Application
Ruqi Lin, Yu Chen, James Ven Wey Yap, Musafargina Bikandhar, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

14. Portable Multiple-Channel Ion-Selective Sensor
Yu Chen, Musafargina Bikandhar, James Ven Wey Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

15. Chip-to-Chip Hybrid Bonding with Larger-Oriented Cu Grains for μ-Joints Beyond 100 K
Murugesan Maranpannan, Takaaki Miyazaki, Takafumi Fukushima – Tohoku University;Masahiro Sawa, Eriko Sone – JCPU Corporation; Mitsumasa Koyanagi – T-Micro Fabrication

Xingang Yu, Zhi Fu, Isamu Morisaka, Keko Koshiba, Tomonori Izuka, Kohji Tatsumi – Waseda University

17. CMS-Composable Fine Pitch Al-Al Bonding

18. Enhancement of Go - 21.5 In – 10 Sn Eutectic Alloy Based Thermal Interface Material Incorporating Cu Flake
Jang Baeg Kim, Dong Gil Kang, Tae Joon Noh, Seo Hwan Kim, Seung-Boo Jung – Sungkyunkwan University

Rashid Mandal, Cai Tai Chong – Institute of Microelectronics A*STAR

20. High Density VR Solutions Using Immersion Cooling
Jesus G. Ruelas Flores, Arturo Sanchez Hernandez, Ernesto A Padilla Ramirez, Oscar A Del Rio Gonzalez, Carlos E Mora Flores, Andres Ramirez Macias – Intel Corporation

21. Demonstration of Eight Metal Layer Redistribution on Glass Substrate with Fine Features and Microvia
Christopher Blanche, Mohanangam Kathaperumal, Fuhan Liu, Madhavan Swaminathan – Georgia Institute of Technology

22. Novel IR Laser Cleaving for Ultra-Thin Layer Transfer and 3D Stacked Devices
Thomas Ummann, Peter Urban, Boris Povazay, Michael Josef Gruber, Julian Bravin, Daniel Burgstaller, Markus Wimpinger, Bernd Thaller – EV Group, Inc.

23. Robust Edge Coupling Probe in Wafers-Level Optical Testing
Sheng-Ho Huang, Chen-Yu Lin, Yi-Keng Fu – Industrial Technology Research Institute; Shih-Yuan Ma, Meiyu Lu, Chi-Sheng Cheng, Jian Chen – ASE Corporate R&D Center

Deng-Wu Zheng, Min-Bo Zhou, Shui Li, Chang-Bo Ke, Xin-Ping Zhang – South China University of Technology

25. Reconstituted-SiO₂, Tier with Integrated Copper Heat Spreader
Ashita Victor, Madison Marley, Shane Oh, Muhammad S. Bakir – Georgia Institute of Technology

26. Reflow Oven Zone Temperature Advisor Using the AI-Driven Smart Recipe Generator
Yangyang Lai, Junbo Yang, Jing Hwan Ha, Pengcheng Yin, Karthik A. Deo, Seungbae Park – Binghamton University

27. A Novel Polymer-Based Ultra-High Density Bonding Interconnection
Yu-Min Lin, Tsung-Yu Ou Yang, Ou-Hsiang Lee, Ching-Kuan Lee, Wei-Lan Chu, Tao-Chih Chang, Hsiang-Hung Chang – Industrial Technology Research Institute; Michael Gallagher, Po-Yao Chuang, Po-Hao Tsai, Po-Chun Huang – DuPont Electronics and Industrial; Chang-Chun Lee – National Taiwan Hua University

28. Comparison of Sintering Methodologies for 3D Printed-High-Density Interconnects (2.3 mm L/S) on Organic Substrates for High-Performance Computing Applications
Shivani Pandya, Serge Eccoffey, Yann Bellard, Dominique Drouin – University of Sherbrooke; Christophe Sarneget – Centre de Collaboration M’Orholonkisation (C2MI); Isabel De Sousa – IBM Canada, Ltd.

29. Formation and 3D Stacking Process of CMS Chips with Backside Buried Metal Power Distribution Networks
Naoya Watanabe, Yuuki Araga, Haruo Shimamoto, Katsuya Kikuchi – National Institute of Advanced Industrial Science and Technology; Makoto Nagata – Kobe University

30. Reliability and Failure Analysis of Chip-to-Substrate Cu-Pillar Interconnections with Nano-Copper–Cu Gaps
Ramon A. Sooa, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

Thursday June 1
Session 39: Interactive Presentations 3
Time: 10:00 a.m. – 12:00 p.m.
Committee: Interactive Presentations

Palazzo Foyer
Session Co-Chairs:
Patrick Thompson – Texas Instruments, Inc.
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Amanpreet Kaur – Oakland University
Email: kaurak@oakland.edu
Frank Libsch – IBM Corporation
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Yoichi Taira – Keio University
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1. Voltage Controlled Nanoscale Magnetic Devices for Non-Volatile Memory and Scalable Quantum Computing
Jieun Yu, Qian Wang, Yao Zheng, Changming Song, Junpeng Fang, Zheyan Wang, Jian Cai – Tsinghua University; Tiefu Li – Tsinghua University/Beijing Academy of Quantum Information Sciences; Haixia Wu – Beijing Academy of Quantum Information Sciences

2. Fabrication and Characterization of MEMS Interconnects for Non-Volatile Memories
Ashita Victor, Madison Marley, Shane Oh, Muhammad S. Bakir – Georgia Institute of Technology

3. Extracting Anisotropic Permittivity of PCB Substrate from VNA Measurement on a Rectangular Stripline Resonator Loaded with a Via Array
Zhaqing Chen, Hung Nguyen, Matteo Cocchini – IBM Corporation

4. Silicon Photonic Co-Packaging: Adhesive Dispense Challenge and Control
Paul Gond-Charlon, Sebastien Goun, Steve Pellerin, Richard Langlois, Patrick Jacques, Denis Blanchard, Eric Turcotte, Steve Whitehead, Elaine Cyr – IBM Corporation

5. Design of Single Miniaturized Dielectric Resonant Antenna for Millimeter Wave 5G Application
Kohji Tatsumi, Keko Koshiba, Yasunori Tanaka, Mayu Miyagawa, Xinguan Yu, Shun Furuya, Tomonori Izuka – Waseda University

6. High-Performance Amplifier Package Design for Heterogeneous Integration on Si-Interposer

7. Through-Silicon- Via Architecture of 3D Integration for Superconducting Quantum Computing Application
Jieun Yu, Qian Wang, Yao Zheng, Changming Song, Junpeng Fang, Zheyan Wang, Jian Cai – Tsinghua University; Tiefu Li – Tsinghua University/Beijing Academy of Quantum Information Sciences; Haixia Wu – Beijing Academy of Quantum Information Sciences

8. Additive Manufacturing of Millimeter Wave Passive Circuits on Thin Alumina Substrates
Ethan Kepros, Yifang Chu, Bhargav Avreni, Brian Wright, Premjeet Chahal – Michigan State University

9. Frequency Selective Surface (FSS) Based Antenna Array Design for Satellites Capable of All Four Polarizations
Li-Ting Hwang, Ming-Yuan Huang, Hung-Chih Lin – National Sun Yat-Sen University

10. Novel Low-Loss Resin Coated Copper and Core Material for Advanced IC Packages
Tomoko Mugerwa, Andi Behr, Tom Shin – Panasonic Industrial Devices Sales Company of America; Umehara Hiroaki, Saiki Yuya, Kishino Koji – Panasonic Industry Co., Ltd.

11. Deep Learning Based Refinement for Package Substrate Routing
Peng-Tai Huang, Tsutsumi Koyama, Tsung-Yi Ho – National Tsing Hua University; Keng-Tien Chang, Chih-Yi Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

12. Laser Integration on a Photonic Integrated Circuit with High Alignment Accuracy for Data Transmission
Ting Ta Chi, Zhenyu Li, Narui Li, Hong Cai, Y. M. Tobing Landozado, Haitao Yu, Senthilkumar Darshini, Jie Ok Yoo, Hwang Gilho, Jeroen Van Borkulo, Lennon Y. T. Lee, Wen Lee – Institute of Microelectronics A*STAR
15. High Density Photonic Reservoir Computing Using Optical Fiber and Polymer Waveguide
Hirotoshi Numata, Toshiyuki Yamane, Daiki Nakano – IBM Research, Tokyo/IBM Corp, Japan; Jean Heroux – IBM Systems/IBM Corp, Canada

16. Machine Learning Based PCB/Package Stack-Up Optimization for Signal Integrity
Wen-Chang Huang, Jiahuan Huang, Chulsoon Hwang – Missouri University of Science and Technology, Minseok Kim, Bumhee Bae, Subin Kim – Samsung Electronics Co., Ltd.

17. Self-Aligned Optical Connector Assembly on Polymer Waveguide Integrated Package Substrate for Co-Packaged Optics
Akhiro Noriki, Takeru Amano – National Institute of Advanced Industrial Science and Technology

18. 2.5D Silicon Photonics Interposer Flip Chip Attatch
Pushnraj Tomme, Hsiu-Che Wang, Dwayne Shirley, Roberto Cocciolo – Marvell Semiconductor, Inc.

Kyongoodun Mun, Kyung-Lim Suk, Dongwook Kim, Suchang Lee, Jihwong Kim, Wonkyoung Choi, Jeachoorn Kim – Samsung Electronics Co., Ltd.

Jugal Khoshor Bhandari, Divya Sri Rajaswet, Parmithantam V. Ramana, Rohin Kumar Yelamarthi, Mohamed Ubed, Jinin K. Jose, Anusha Veerandi, Sandhya Dharathv – LightSpeed Photonics Pte Ltd

21. Direct Paste Deposition of Inorganic Materials for Sensors Applications
Nicolas Delavault, Tauguy Ladoencomide, Remy Kalmar, Manuel Fendler – CEA Tech Grand Est; Sofiane Achache, Manuel Fendler – CEA Tech Grand Est

22. Highly Compact and High Gain 2 x 2 Patch Array Antenna with Slotted Meandered Line Loading
Hanna Jang, Payman Pahlavan, Yong-Kyu Yoon – University of Florida

23. Design of a Compact Size Bridge Connected Multiband MIMO Antenna for Automotive 5G and DSRC Communications System
Mohammad Perez, Amanpreet Kaur – Oakland University

24. A Fully Additive Fabrication Approach for sub-10-Micrometer Microvias Suitable for 3-D System-in-Package Integration
Raghavendra, Shanil Chouhan, Jerker Deling – Lulea University of Technology, Jussi Putsala, Olli Nousiainen, Juha Hugberg, Sami Myllymaki, Sarthak Acharya, Heli Jantunen – University of Oulu

25. The Performance and Reliability of Screen-Printed Flexible Multilayer Leads for Wearable Vital Sign Monitoring Devices
Udara S. Somarathna, Behnam Garakani, Mohammad Alhendi, Radh A. A-Haidari, Mark Polik – Binghamton University; Darshana L. Weerawarne – University of Alhendi, Riadh A. Al-Haidari, Mark Polik – Binghamton University

Joong Woon Kim, Nahid Asale-Araki, Fuhua Liu, Madhavan Swaminathan – Georgia Institute of Technology; Rajesh Vaddi, Garima Nagar – Corning, Inc.

27. Security Robustness of Buried Power Rail Interconnect Technology: Modeling, Analysis and Countermeasures
Shin Ogurashi, Nishant Gupta, Sai Subrahmanyam Teja Nitharpanud, M. Shih Wing, Jaydeep Kulke – University of Texas, Austin

28. Intelligent Multi-Physics Design of 3-D Leadframe-Based SiC Power Module with Die Stacking for Transportation Electrification
Emanuel Tonnes-Surilo, Christian Malin-Margaux, Vanessa Smet – Georgia Institute of Technology

Thursday June 1
Session 40: Interactive Presentations 4
Time: 2:30 p.m. – 4:30 p.m.
Committee: Interactive Presentations

Palazzo Foyer
Session Co-Chairs:
Mark Eben – Kyocera International SC
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Jeffrey Lee – iST-Integrated Service Technology, Inc.
Email: jeffrey.lee@istgroup.com
Karan Bhangaonkar – Intel Corporation
Email: karan.r.bhangaonkar@intel.com

1. Simulation of Solder Crack Phenomenon in Molding Process
Tsui Cheih Chien, Shih Kun Lo, Zong Yuan Li, Yen Hua Kuo, Ming Shaw Shy, Hui Chung Liu, Lu Ming Lai, Kuo Hsiun Chu – Advanced Semiconductor Engineering, Inc.

2. Embedded Micro-Fin Heat Sink of Two-Phase Liquid Cooling for High Heat Flux 3D ICs

3. Warpage Estimation of Panel-Level Package from Panel to Strip by Using Multi-Scaling Sub-Modeling Technique

4. A Thermally Friendly Bonding Scheme for 3D System Integration

5. Reliability in Selective Thining Technology of Solder Resist for New IC Substrate Architecture

6. Simulation, Prediction, and Verification of the Corrosion Behavior of Cu-Ag Composite Sintered Paste for Power Semiconductor Die-Attach Applications
Xinyue Wang, Zhongdong Yang, Pan Liu – Fudan University; Guoqi Zhang – Delft University; Jing Zhang – Heraeus Materials Technology Shanghai Ltd

7. Thermal Characterization and Management of GaN-on-SiC High Power Amplifier MMIC
Yang Han, Gongyue Tang, Boon Long Lou – Institute of Microelectronics A*STAR

8. A Thin-Film Reconfigurable SIC Thermal Test Chip for Reliability Monitoring in High Environments
Romina Sattari, Henk van Zelij, GuoQi Zhang – Delft University of Technology

9. Life-Prediction of SAC305/Bi-Based Hybrid Solder Joint Considering Bi-Diffused Layers with Gradual Bi Concentrations
Yongjie Jiang, Bongtae Han – University of Maryland; Hak-Sung Kim – Hanyang University

10. Thermal-Mechanical-Electrical Co-Design of Fan-Out Panel-Level SiC MOSFET Packaging with a Multi-Objective Optimization Algorithm
We Chen, Xuying Yan, Fan Fan – Fudan University; Meslin S. Ibrahim – Hong Kong Polytechnic University; Jing Jiang – Sky Chip Interconnection Technology Co., Ltd; Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology

11. Su8 Out-of-Plane Stress Reduction Via Design of Experiment and Machine Learning
Zi'ai Ja, Shuyi Shi, Yong-Kyu Yoon – University of Florida

Quang Duc Pham, Norbert Holte – Robert Bosch GmbH; Juergen Wilde – University of Freiburg

13. Optimization of the Cu Microstructure to Improve Copper-to-Copper Direct Bonding for 3D Integration
Ralf Schmidt, Christian Schwarz – Atotech (PKS Instruments)

14. Effect of Ceramic Filler in Epoxy Mold Compound on Thermomechanical Property of FilmWLP
Taejoo Noh, HakSan Jeong, Seung-Boo Jung – Sungkyunkwan University

15. Atomic Similation Study of Plasma Surface Activation in Wafer-to-Wafer Oxide Fusion Bonding
Hojin Kim, Yu-Hao Tsai, Satoshi Hashino, Iseok Son, Kaoru Masakawa, Peter Bokor, Saran Arjalagud – TEL Technology Center, America, LLC

Nelson Pirihi, Emmanuel Cherry, John Sabelkoorn, Mihály Krížbók, Andy Miller, Eric Beyne – imec; Ritwik Bhata, Ganesh Sundaram – Veeco

17. A Combined Simulation and Experimental Study on Cracking and Delamination Behavior at the Cu/Polyimide Interface of RDLs in Chiplet Package Subjected to Thermo-Mechanical Loads
By Chen, Guang-Chao Lyu, Hong-Guang Wang, Long Zheng, Yun-Kai Deng, Xin-Ping Zhang – South China University of Technology

18. Evolution of the Creep Response of SAC+Bi Lead-Free Solders Subjected to Various Thermal Exposures
Mohammad Al Ahsan, S. M. Kamrul Hasen, Jeffrey Suhling, Pradeep Lal – Auburn University

19. Modeling Grain Size Effects on Deformation Behavior of SAC Solder Joints
Debabrata Mondal, Jeffrey Suhling, Pradeep Lal – Auburn University

20. Reliability Study on High Performance Photo Imageable Dielectric for Advanced Package

21. A Novel Indium Metal Thermal Interface Material and Package Design Configuration to Enhance High-Power Advanced Si Packages Thermal Performance
Kuo-Chin Chang, Mingj-Li Kuo, Min’Lin Wang, Chien-Chang Wang, Bang-Li Wu – Taiwan Semiconductor Manufacturing Company, Ltd.

22. High Temperature Storage of Cu-Cu Joints Fabricated by Highly (111)-Oriented Nanotwinned Cu
Shi-Chi Yang, Chih Chen – National Yang Ming Chiao Tung University
Exhibition

Wednesday, May 31
9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 6:30 p.m.

Thursday, June 1
9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 4:00 p.m.

Coquina Ballroom
Booth 216  
3D Systems Packaging Research Center at Georgia Tech  
1-404-894-3340  
prc@gatech.edu  
791 Atlantic Dr.  
Atlanta, GA 30332
Madhavan Swaminathan  
madhavan.swaminathan@ece.gatech.edu

The 3D Systems Packaging Research Center (PRC) at Georgia Tech is a graduated NSF Engineering Research Center focusing on advanced packaging and system integration leading to System on Package (SoP) technologies. The center conducts research and education in all aspects of packaging that includes design, materials, process, assembly, thermal management, and integration driven by applications, which include broad areas such as high-performance computing, artificial intelligence, automotive, broadband wireless and space. The center team consists of 29 faculty from five schools, 11 research/administrative staff, 50+ graduate/ undergraduate students and several visiting engineers. This is enabled through collaboration with over 40 industry/govt. organizations and 14 universities.

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Adeia was launched as a standalone technology and intellectual property (IP) licensing company from Xperi. Adeia invents, develops and licenses fundamental innovations that shape the way millions of people explore and experience entertainment and enhance billions of devices in an increasingly connected world. Leveraging the combination of highly experienced technologists, scientists, engineers and advanced R&D labs in San Jose, California and Raleigh, North Carolina, Adeia develops industry-leading 3D integration solutions such as hybrid bonding that meet the demand for greater functionality, higher performance and smaller size for next generation electronics.

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As the nation’s first complete end-to-end silicon photonics manufacturing ecosystem, AIM Photonics provides small and medium enterprises with crucial technology on-ramps and access to strategic U.S. government, industry, and academic communities to accelerate the transition from concept to manufacturing-ready prototypes. Our state-of-the-art 300 mm test, assembly and packaging facility in Rochester, NY is the nation’s only accessible advanced wafer-level and die-level test and assembly facility offering both photonic and electronic packaging capabilities. Customers and members have access to an extensive toolkit with capabilities for standard processes such as fiber attach, wire bonding, die attach, dicing and flip chip, as well as advanced packaging, co-packaging, and heterogeneous integration capabilities.

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Our world class investors, including Infinion, Qualcomm, ASE, Nepes and SunPower provide Deca with a strong foundation for continuing innovation and growth.

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Fraunhofer IMWS core competencies lie in the area of the characterization of materials down to the atomic scale and in material development.

Our Business Unit “Electronic Materials and Components” investigates components, systems and materials of electronics and microsystem engineering, like integrated semiconductor circuits, sensors, electronic components and assemblies. These are analyzed and tested comprehensively, in order to understand the relationship between technological process and application conditions with microstructure and material properties as well as with the affected functional performance in detail. For the benefit of our customers, we master complex, powerful methods that include non-destructive analytics, high-resolution methods of electron microscopy and solid-state spectroscopy, surface and trace analysis methods, and mechanical material characterization that includes modeling and numerical simulation. Major areas of our work are the process characterization on a microstructural level complementing the introduction of innovative technologies as well as the fast and client-focused root cause analysis of faults and of defect formation. The results are incorporated into the clients’ manufacturing processes and thus help to increase the quality and reliability of these systems.

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These attributes characterize SCHOTT as a manufacturer of high-tech materials based on specialty glass. Founder Otto Schott is considered its inventor and became the pioneer of an entire industry. Always opening up new markets and applications with a pioneering spirit and passion – this is what has driven the #glasslovers at SCHOTT for almost 140 years. Represented in over 30 countries, the company is a highly skilled partner for high-tech industries: Healthcare, Home Appliances & Living, Consumer Electronics, Semiconductors & Datacom, Optics, Industry & Energy, Automotive, Astronomy & Aerospace. In the fiscal year 2022, its 17,200 employees generated sales of 2.8 billion euros. SCHOTT AG is owned by the Carl Zeiss Foundation, one of the oldest foundations in Germany. It uses the Group’s dividends to promote science. As a foundation company, SCHOTT has anchored responsibility for employees, society and the environment deeply in its DNA. The goal is to become a climate-neutral company by 2030.

Nitto Denko and Hugle Electronics. We service everything we sell.

Products include: Dicing Tape, Wafer Mounters, Wafer Expander, UV Cure, Pick and Place, Die Bonders, Cassette and Box Cleaners.

Booth 108
Scientech Corp
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scientech.com.tw
No. 182, Bade Rd.
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Contact: Eric Lee
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Scientech Corporation was established in Taipei, Taiwan in 1979. Our main products are Wet Process Equipment, Temporary bonding/ debonding systems, and wafer reclaims service, besides representative business. We are a listed company and have employees more than 750. Our main offices are in Taiwan, China, Singapore, Europe, and the USA.

Booth 401
SCREEN Holdings Co., Ltd.
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Tenjinkita-machi 1-1, Teranouchi-agaru
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SCREEN is a leading supplier of equipment and process solutions for the global semiconductor industry and related markets. Our technologies enable innovation throughout the electronics industry, and our portfolio covers a wide range of products not only for semiconductor frontend cleaning but also for panel-level coating, direct imaging lithography for substrate etc. with its global infrastructure for wide application and service. We offer wafer bonding integrated with our exclusive cleaning technology at this show. Please visit us at Booth 401 to discuss your advanced packaging requirements and challenges or contact SCREEN via e-mail (adplgs@screen.co.jp).

Booth 236
SEKISUI Chemical Co., Ltd.
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2099 Gateway Pl., Suite 310
San Jose, CA 95110
Takaihi Hiratsuuka
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SEKISUI is a Japanese chemical manufacturing company with a history of 75 years. We provide a variety of products to meet the most frontier needs of the electronic market. For the semiconductor market, we manufacture and sell interlayer insulating films used for high-spec semiconductors, TIM with unique and high heat dissipation using carbon fiber, and semiconductor process materials with temporary fixing and easy peeling.

Booth 308
Semiconductor Equipment Corporation
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semicorp.com
515 Goldsmith Ave.
Moorpark, CA 93021
Contact: Don Moore
dmoore@semicorp.com
Semiconductor Equipment Corporation is a small innovative company that has designed and manufactured back end manual equipment for the semiconductor and related industries for more than 46 years. In that time we have expanded our business to distribute products for...
combines this cutting-edge technology with its fluxless bonding technology. Fluxless LATCB’s 3600mm² large die bonding capability with its super high-speed laser heating and simple and flexible fluxless bonding technology can bring industry-leading ultra-high solder interconnection density with the highest productivity and no corrosive residues.

Booth 205
Shikoku Chemicals Corporation
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301 N. Rampart St., #C
Orange, CA 92868
Contact: Noritake Furuki
furukin@shikoku.co.jp
SHIKOKU CHEMICALS Co. has synthesized a number of unique resin crosslinking agents using our organic synthesis technology. Among them, we have discovered that the isoanuric acid skeleton has excellent electrical properties, and are developing a new crosslinking agent with this skeleton as its core structure.

Also, GiCAP is a new interface chemical developed based on our organic synthesis technology. Unique organic coating formed on copper surface directly improves adhesion between copper and resin effectively.

SHIKOKU CHEMICALS Co. will continue to design and create materials that can balance the characteristics that have become issues in the market.”

Booth 434
Shin-Etsu MicroSi, Inc
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10028 S 51st St.
Phoenix, AZ 85044
Contact: Ian Holden
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Founded in 1984 as a subsidiary of the General Electric Company, Shin-Etsu MicroSi is a driving force in both the semiconductor and microelectronics industries worldwide. By infusing science and chemistry with innovation and collaboration, we create leading-edge solutions that turn possibilities into realities—while providing the proven quality and time-tested dependability on which our customers rely.

From computers to cell phones, 5G, automobiles, coatings, and more, our products are used by companies throughout the world to make the integrated circuits and semiconductor devices that power everyday living.

Booth 139
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shinko.com
350 Cobalt Way
Sunnyvale, CA 94085
Contact: Justin Goodman
justin@goodman@shinko.com
Shinko develops and produces various “Semiconductor Packages” adapting for the miniaturization, acceleration, and performance enhancement of semiconductors.

We aim to enrich and contribute to the lives of people all over the world by providing our cutting-edge packaging technologies, for markets including IoT and AI, anticipated to become more widely used in the future, and the automotive market, in which technology development is accelerating for applications such as autonomous driving and electric vehicles (EV). Shinko also develops leading package technologies for high performance computing and data networking solutions.”

Booth 238
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SHT Smart High-Tech AB is a company focusing on producing new heat-dissipating materials reinforced with graphene with a focus on cooling electronics, processors, graphics cards, LEDs, and other heat-sensitive and heat-intensive products. This is something that is essential to be able to develop high-performance electronics that are smaller, faster and lighter with more functionality—in a sustainable way. We offer high-performance graphene-reinforced materials and associated process know-how. One example of our unique and innovative developments is our graphene-reinforced interface material “Thermal Interface Material”, called TIM, for electronics and power module cooling, which conducts heat efficiently both vertically and horizontally. TIM is found in our GT product series, which is available in different versions with different performances.

Booth 403
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Contact: Sylvia Lewis
slewis@sigray.com
Sigray is a San Francisco Bay Area based company, specializing in the development & integration of high-resolution, high-throughput X-ray analytical equipment.

Sigray Apex XCT is a 3D X-ray tomography platform designed for full wafers and large PCBs, capable of producing resolution down to the sub-micron regime while providing 3D imaging times on the order of a few minutes. The technique is completely non-destructive and suitable for a variety of FA, R&D, and production applications. Further to Apex XCT, Sigray produces other disruptive X-ray technologies, such as: AttoMap Micro-XRF, the flexible PrismaXRM 3D X-ray microscope, and QuantumLeap laboratory XAS.

Booth 204
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Siltronics offers Chip package design & assembly services from concept to NPI to volume production. We have expertise to propose, develop & implement cost effective solutions from concepts to finished products. We are located in the heart of Silicon Valley in a 10,000+ sq. ft. state of art automated facility with 10K & 1K clean rooms.

We have fully automated: Flip Chip with +/- 0.5um, Auto Dispensing and Pick/Place within +/- 3um, Auto Wire Bonders for 45um pitch, 200um wire length & 50um loop height, Auto Eutectic, Hermetic Sealing, PCB, 3D Laser Scope, Die Shear, X-ray & Wire Pull Tester for Quality Control.

Siltronics’ regularly do process development which are so advanced that there is no precedence & does not fit in a standard assembly template. Often design rules have to be pushed beyond their limits. This requires development of test vehicles, identification of right material, careful process control, monitoring of assembly parameters, DOE & investments in new equipment. Our team is ready to discuss your next project in design, process development or Chip assembly.

Booth 125
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SkyWater (NASDAQ: SKYT) is a U.S. investor-owned semiconductor manufacturer and a DMEA-accredited Category 1A Trusted Foundry. SkyWater’s Technology as a Service model streamlines the path to production for customers with development services, volume production and heterogeneous integration solutions in its world-class U.S. facilities. This pioneering model enables innovators to co-create the next wave of technology with diverse categories including mixed-signal CMOS, ROICs, rad-hard ICs, power management, MEMS, superconducting ICs, photonics, carbon nanotubes and interposers.

SkyWater serves growing markets including aerospace & defense, automotive, biomedical, cloud & computing, consumer, industrial and IoT. For more information, visit: www.skwatertechnology.com.

Booth 145
Sono-Tek Corporation
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Sono-Tek’s ultrasonic coating technology is currently being used at the package level for EMI shielding coatings. Tested and approved using market-available EMI materials, our unique non-dogging spray coating systems, followed by low temperature heat cure, offer a more cost effective and faster alternative to costly sputtering equipment. Our FlexiCoat EMI system was designed to run continuously in production at a higher throughput than sputtering, at roughly 1/10th the cost.

Sono-Tek’s ultrasonic coating technology also is well known for thin, repeatable, and low waste coatings. Other applications include: Photoresist deposition, polyimide, flux dispersing for flip chip applications, and nano suspensions (CNT, graphene, nano-wires, etc). Visit www.sono-tek.com for more information.
well as key processes for Wafer-Level Packaging, the advancement of next-generation technologies industry partners SUSS MicroTec contributes to close cooperation with research institutes and wafer bonding and photomask processing, products and solutions for backend lithography, Our portfolio covers a comprehensive range of semiconductor industry and related markets. SUSS MicroTec is a leading supplier of equipment Contact: Emyr Edwards Corona, CA 92882 2520 Palisades Dr. sus.com +1 951-880-9899

BOOTH 115
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STAr-Quest.com

1885 Lundy Ave., Suite 101 San Jose, CA 95131 Contact: Paul Meyer sales-us@STAr-Quest.com

STAr Technologies, Inc was established on August 29, 2000 and headquartered in Hsinchu City, Taiwan and has branch offices in the United States of America, Japan, Singapore, South Korea, China and India. To further its reach and support, we also engage distributors in North America, Europe, South Asia Pacific, Greater China and Japan to serve regional customers directly. STAr is the acronym for “Semiconductor Test Architect” and as in the name - we are the architects with leading technologies for semiconductor test solutions.

STAr Technologies provides intellectual property, software, hardware, consumables, service and expertise to meet the requirements and challenges within the semiconductor and optical device industries. Our expertise extends across parametric electrical tests (E-test), wafer-level and package-level reliability (WL & PLR), mixed signal tests, assembly and packaging services, probe cards, load boards, test interfaces and sockets.

Booth 132
SurfX Technologies LLC +1 310-558-0770 surfxtecologies.com 2631 Manhattan Beach Blvd. Redondo Beach, CA 90278 Contact: Alan Vucetic avucetic@surfxtecologies.com

Founded in 1999, SurfX Technologies has developed and brought to market a true low-temperature, variable chemistry, atmospheric pressure plasma. Our products incorporate the most advanced plasma technology and are covered by multiple U.S. patents. SurfX’s mission is to be the worldwide leader in the surface treatment of materials for the semiconductor, electronics assembly, aerospace, and medical device industries. We are driven by a total commitment to our customers. We take pride in our products and service. Our promise is to deliver to you the highest quality product for your manufacturing needs.

BOOTH 212
SUSS MicroTec +1 951-880-3899 suss.com 2520 Palisades Dr. Corona, CA 92882 Contact: Emyr Edwards emyr.edwards@suuss.com

SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring in the semiconductor industry and related markets. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. In close cooperation with research institutes and industry partners SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Imprint Lithography as well as key processes for Wafer-Level Packaging, MEMS and LED manufacturing. With its global infrastructure for applications and service, SUSS MicroTec supports more than 8,000 installed systems worldwide.

Booth 332
Taiyo Ink Mfg. Co., Ltd. +1 775-885-9959 taiyo-hd.co.jp/en 1731 Technology Dr., Suite 595 San Jose, CA 95110 Contact: Yuya Suzuki yuyas@taiyo-america.com

High performance and high reliability materials showcased by TAIYO INK are beneficial for advanced IC packaging, as well as conventional packaging applications. Consequently, Taiyo Ink has more than 90% market share of solder resist products for the IC packaging industry. One of the latest materials from TAIYO is a photo-imageable dry film with 10 µm resolution, PVI-3 HR100S, which has low curing temperature of 180°C, and can be applied as high-density RDL dielectrics for advanced packaging substrates & PLP/WLP. Taiyo also develops a variety of new dielectric materials with additional performance, such as magnetic, optical, or electrical performances. We look forward to talking with you at our booth.

Booth 405
TATSUTA Electric Wire & Cable Co., Ltd. +81 77466555 tattsutacom 6-5-1 Kunimidai Kizugawa Kyoto 6190216 Japan Contact: Susumu Chiba s-chiba@tatsuta.co.jp

TATSUTA Electric Wire & Cable Co., Ltd is a leading manufacturer of innovative advanced paste for high performance electronics. By using our electrically and thermally conductive paste, higher density interconnect(HDI), longer product life and outstanding reliability are achievable. With our knowledge of metal-resin formulation technology, our materials support your development cycles/ process time shorten and process temperature lower as well, which enables lower carbon emission and eco-friendly process. For more information, please visit the website and you will see our latest developments related with carbon neutrality, low temperature curing, thermal management and EMI shielding.

Booth 133
TAZMO +1 510-946-9182 tazmoinc.com 42840 Christy St., Suite 103 Fremont, CA 94538 Contact: Takashi Abe takashi.abe@tazmo.co.jp

Tazmo is a semiconductor manufacturing equipment company listed in the prime section of Tokyo Stock Market. Our main products are as follows.

(1) Semiconductor manufacturing systems for the temporary bonding and de-bonding of Silicon wafers and support glass for back grinding process.

(2) Coater/Developer for semiconductor manufacturing processes. Equipment for resist coat/develop and other chemical solutions using our accumulated technologies. Coating with highly viscous materials and other materials that are difficult to work with while achieving good coating uniformity.

(3) Cleaning tools and surface treatment for semiconductor manufacturing processes.

Cleaning machines for manufacturing of semiconductor, slurry supply units, chemical supply units and phosphoric acid recycling.

(4) Flat Panel Display Manufacturing Equipment Equipment used for manufacturing various types of flat panels. Tazmo has the largest share for LCD color filter resist coaters.

(5) Clean wafer transfer system Tazmo provides various wafer transfer systems to other semiconductor manufacturing equipment suppliers. These products include robots, aligners and EPEM.

For more information, please visit our website: / www.tazmo.co.jp/en/product

Booth 301
TDK Corporation +1 972-409-4519 product.tdk.com/en/products/fa/index.html 475 Half Day Rd., Suite 300 Lincolnshire, IL 60069 Contact: Jose Perez jose.perez@tdk.com

TDK is a leader in factory automation systems. Our products include TDK precision AFM 15 Thermosonic and AFM 15 Thermal Compression flip chip die bonders. TDK flip chip die bonder’s uses a micro scrub process to lower heat required for die attach process. TDK micro scrub process eliminates flux and supports 5~10 mm line width and 3mm spacing.

Additionally, TDK load ports feature high-performance that meet your needs for particle-free operation, high throughput and high durability of continual motion. In addition to the TAS300 load port, we also offer the TAS300 J1 and the TAS450.

Booth 436
TechSearch International Inc. +1 512-372-8887 techsearchinc.com PO Box 20285 Austin, TX 78720 Contact: Jan Vardaman jan@techsearchinc.com

TechSearch International, Inc. has a 31-year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. Research topics include WLP, FO-WLP and panel-level processing, Flip Chip, CSPs, BGs, 3DICs, Si Interposers, System-in-Package (SiP) and Heterogeneous Integration, embedded components, ADAS and automotive electronics, and power devices. In conjunction with SavanSys Solutions, wire bond, flip chip, WLP, and 3D IC cost models are offered. Multi-client and single client consulting services are offered. TechSearch International professionals have an extensive network of more than 19,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.
coating systems are lined-up. Manufacturing equipment such as high-precision equipment with high speed, and substrate accuracy from +/-0.5um. and Wafer Inspection of-the-art Flip Chip Bonding Equipment for Toray Engineering Co., Ltd. provides state-of-the-art dielectric loss 5G/mmWave applications specifically designed to be implemented for the 5G era. We also offer newly developed materials to improve device functionality, and high-speed. We offer various new materials necessary for many device manufacturers, including advanced immersion photoresists enabling the formation of several tens nanometer scale features.

Along with advancement in the micro-fabrication of an electronic circuit, our sophisticated technologies provide solutions to enhance the functionality of semiconductors, such as miniaturization, high-integration, multi-functionality, and high-speed. We offer various new materials necessary for many device manufacturers, including advanced immersion photoresists enabling the formation of several tens nanometer scale features.

Toray International America Inc +1 650-524-2735 toray.com/global/products/electronics 411 Borel Ave., Suite 520 San Mateo, CA 94402 Contact: Koichi Maruyama koichi.maruyama.p6@mail.toray Toray Industries, Inc. has devoted itself to developing new fields and materials as a basic materials manufacturer. We have supplied both film-type and coating-type materials in the semiconductor market over decades.

Film type: “FALDA” is a photo-definable adhesive film for build-up substrates and packages with cavity structures.

Coating type: “Photoneece” is a photo-definable polyimide coating for the front-end buffer and back-end re-distribution layers for WLP and TSV.

Toray’s unique polyimide and film processing technologies provide excellent reliability and performance, already proven in the market.

We also offer newly developed materials specifically designed to be implemented for the low dielectric loss 5G/mmWave applications (B-stage and liquid products available).

Toray Engineering Co., Ltd. provides state-of-the-art Flip Chip Bonding Equipment for semiconductor packaging with alignment accuracy from +/-0.5um and Wafer Inspection Equipment with high speed, and substrate manufacturing equipment such as high-precision coating systems are lined-up.

Booth 336
TOWA USA Corporation +1 408-779-4440 towajapan.co.jp/en 1430 Tully Rd., Suite 416 San Jose, CA 95122 Contact: Terence Koh tkoh@towa-usa.com TOWA is a leading company in the semiconductor: molding equipment market. We offer equipment using our high quality / flow free compression molding method and our proven transfer molding method. We also manufacture ultra-precision molds that have been highly acclaimed by customers. Together with our molding equipment, our singulation system was developed from both aspects of the dicer and product handler to provide the optimal method of singulation for each product type. The result is high quality cutting whilst improving customers’ productivity with high throughput.

Booth 117
Toyota Tsusho America, Inc. +1 248-994-3220 taimerica.com 4505 West 12 Mile Rd., Suite 200 Farmington Hills, MI 48331 Contact: Akio Azuma akio_azuma@taimericamer.com Toyota Tsusho America, Inc is the trading arm of Toyota Motor Group and we are developing the business in seven divisions such as Electronics & Chemical, Automotive, and the supporting administrative division. We have 35 locations in North America, in addition to 43 affiliate and subsidiary locations to provide valuable products and services for enterprise-level industries such as automotive, electronics, and more. As the Electronics & Chemical division, we are providing and developing services and cutting-edge products for semiconductor production such as Photoresist, CMP Slurry, High-frequency CCL, and Encapsulants to contribute to the growth of the electronics industries.

Booth 137
USHIO INC. +81 3-5657-1000 ushio.co.jp Marunouchi Kitaguchi Bldg., 1-6-5 Marunouchi Chiyoda-ku Tokyo 100-8150, Japan Contact: Yulei Sashiwa y.sashiwa@ushio.co.jp Established in 1964, USHIO INC. (TOKYO: 6925) is a leading manufacturer of light sources such as lamps, lasers, and LEDs, in a broad range from ultraviolet to visible to infrared rays, as well as optical equipment and cinema-related products that incorporate these light sources. It also makes products in the electronics field (such as semiconductors, flat panel displays and electronic components) and in the visual imaging field (including digital projectors and lighting). Many of these products enjoy dominant market shares. In recent years, USHIO has undertaken business in the life science area, such as the medical and the environmental fields. See www.ushio.co.jp/en.

Booth 129
VALID Co., Ltd 487, Cheongbuk-ro, Cheongbuk-myeon, Pyeongtaek-si, Gyeonggi-do 17791 South Korea Contact: Won Ho Noh whnoh@validinnovation.co.kr VALID Co., LTD is an integrated solution provider which has the following business areas not confined to: Development and mass production of parts for medical ultrasound diagnostic devices, medical instruments for surgical robots and orthopedic implants, automobile power-train and metal 3D printers as well as industrial measurement equipment. Its specialty consists of design, verification, prototyping and production stage with robust engineering and production capabilities. The company is located in Pyeongtaek-si within 1 hour driving distance from Seoul, S. Korea.

Booth 230
XYZTEC, Inc +1 978-880-2598 xzyttec.com 33 S. Main St., PO BOX 2189 Wolfeboro, NH 03894 Contact: Tom Haley tom.haley@xyztec.com With over 20 years of experience, we have established our name as the technology leader in bond testing throughout the world. With 100% of our focus on bond testing, Xyztec teams with customers to offer innovative solutions that address their specific bond test needs. Our mission is to take on the challenges of many different industries by offering customers products that improve their quality and increase their bottom line. We offer full automation solutions for both wire pull and shear operations. We also revolutionized the sensor exchange by mounting up to 6 sensors on a rotational measurement unit (similar to a software selected turret). Changing between tests is a matter of only a few seconds!

Among others, we support Military, Medical, industrial, automotive and microelectronic applications.

Booth 338
Yamaha Robotics Holdings Co. (Shinkawa USA) +1 408-504-4971 yamaha-robotics.com 104 S. 54th St. Chandler, AZ 85226 Contact: William Crockett crockett@yamaha-robotics.com Yamaha Robotics Holdings Integrates Back-end Semiconductor process and Creates Value-added Process technology. Integration and Streamlining Back End Semiconductor Assembly One stop solution for Intelligent Factory.

Equipment Product line includes: Flip Chip, Die bonder, wire bonder, molding, inspection and SMT.
Yole Group is an international company recognized for its expertise in the analysis of markets, technological developments, and supply chains, as well as the strategy of key players in the semiconductor, photonics, and electronics sectors. With Yole Intelligence, Yole SystemPlus and Piséo, the group publishes market, technology, reverse engineering and costing analyses and provides consulting services in strategic marketing and technology analysis. The Yole Group Finance division also offers due diligence assistance and supports companies with mergers and acquisitions.

Yole Group benefits from an international sales network. The company now employs more than 180+ people. More information on www.yolegroup.com.

Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company’s extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken’s transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company’s people—the foundation of Zuken’s success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken’s people relate to and understand each company’s unique requirements.

Zymet manufactures Adhesives & Encapsulates and has been serving the electronics industry for over 30 years. Products include rewardable undersells and edge bond adhesives for high reliability and harsh environment applications. Other products include ultra-low stress adhesives, electronically conductive adhesives, thermally conductive adhesives, and non-conductive pastes.
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IEEE 74th Electronic Components and Technology Conference • www.ectc.net
May 28 - May 31, 2024 at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, USA

The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee of ECTC.

**Applied Reliability:** Reliability of 2D, 2.5D, Si-bridge, 3D, chiplets, SIP, WLCSP, POWLP, FOPLP & heterogeneous integration; Interconnect reliability in micro-bump, micro-pillar, Cu-pillar, TSV, TGV, RDL, HDI, stacked-die, hybrid-bond, flip chip & wire bonded packages; Novel reliability test methods, life models, FA techniques & materials characterization; Component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/Hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays & memory.

**Assembly and Manufacturing Technology:** Assembly and manufacturing challenges for new markets; Die bonding methods and processes; embedded packaging and modules; Wafer level process/materials technologies; Die and package singulation manufacturing; New & next generation substrates; Smart factory/manufacturing; Design for Manufacturing; Assembly related test/yield/hardware development; Integrating advanced thermal solutions in manufacturing; Design/performance, integrating solutions, thermal materials, low stress/high thermal; Process advancements/yield enhancements; Cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/compression/injection mold; Heterogeneous integration and process: chiplets, 3D stacking, bridge technology, large body, warpage management; Shielding/ protection technologies and manufacturing.

**Emerging Technologies:** Emerging, novel and unique packaging and material technologies for: Soft and intelligent packaging; Flexible/stretchable hybrid electronics; Implantable biosensors and bioelectronics; Bio-resorbable packaging; Extreme harsh environment; Nanomanufacturing; Paper sensors/electronics pop-up/origami; MEMS & NEMS; Close-To-Motor high-voltage power electronics; Packaging for wide band gap devices; Anti-tamper, cryptography; Additive manufacturing; Packaging for quantum computing and electro-optical integration; Recyclable and sustainable electronics packaging; ML and computer vision for packaging; Point-of-care diagnostic packaging; Space hardened packaging; Green and sustainable electronics; Net zero strategy/technology.

**Interconnections:** Interconnection Technology and Processing: Hybrid/direct Cu bonding, fan-out, panel-level, chiplets, SIP, flip-chip, 2.5D/3D, Si/organic interposers, TSV, micro-bump, Cu pillar, wire bonding, thermo-compression bonding, fine-pitch/multi-layer RDL, printable interconnects, flexible substrates, photonic interconnects, quantum interconnects; Interconnection material, characterization and reliability; Conductive/non-conductive adhesives, low temperature solder, underfill, molding compounds, thermal interface materials, thermal/mechanical/electrical tests and reliability; Interconnection physical co-design and architectures for emerging applications- HPC, mobile, 5G, IoT, power and rugged electronics, medical and health, automotive, aerospace, flexible hybrid electronics, micro-LED display.

**Materials & Processing:** Wafer & panel level packaging materials; Materials for harsh environments; Packaging substrates; Flexible, stretchable, & wearable electronics; Wafer bond/debond materials; TSV; Emerging electronic materials & processes; Novel solder metallurgies; Dielectrics and underfills; Molding compounds; Thermal interface materials; Advanced wire bonding and conductive adhesives.

**Packaging Technologies:** Architectures, chiplets, and applications for 2.5 & 3D, TSV & interposer; Advanced flip-chip, SIP, CSP, PoP, MEMS, sensors & IoT; Automotive & power electronics; bio, medical, flexible & wearable packaging; Embedded & advanced substrates; Fan-out, wafer & panel level processes; Heterogeneous integration.

**Photonics:** Assembly and packaging for all applications that leverage photonics components and circuits. Packaging of Photonics Integrated Circuits (PICs) for telecom, datacom, and 5G; Co-packaged and near-packaged optics; Heterogeneous integration; Artificial intelligence; quantum systems such as processors, sensors, and networks; Medical devices; Automotive/LIDAR; Aerospace, defense, and cryogenicharsh environment; RF/MW photonics; Free-space optics; AR/VR, VD/L, and high power lasers; Micro-LEDs and 3D light-field displays; Imaging and environmental sensors; New materials, connectors; EDA tools, and test methods/equipment.

**RF, High-Speed Components & Systems:** 5G/6G, IoT, cloud computing, autonomous vehicles, AI/machine learning; Antennas, radars, sensors, power transfer, EM shielding, wireless communications, RF to THz; Electrical and multi-physics modeling, simulation and characterization of interconnects, components, modules, and heterogeneous integration; Signal/power integrity, and chip/package/board co-design.

**Thermal/Mechanical Simulation & Characterization:** Thermal/ mechanical simulation and characterization at component, board, and system levels for all packaging technologies: Reliability-related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); Material constitutive relations; Chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; Novel modeling techniques including multi-scale physics, co-design approaches; Quantum computing; Measurement methodologies, characterization and correlation, model order reduction, sensitivity analysis, optimization, statistical analysis; Application of artificial intelligence on modeling, characterization, digital twin; Simulations for virtual release.

**Interactive Presentations:** Abstracts may be submitted related to any of the already listed topics. Highly encouraged at ECTC, interactive presentations allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation papers are published and archived in equal merit with the other ECTC conference papers.

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You are invited to visit ECTC’s website to submit an abstract in which you describe the novelty, scope, content, and key points of your proposed manuscript. You can also submit an optional supporting figure or data table. Abstracts cannot contain more than 700 words and must be received by October 9, 2023, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors with your submission. The authors are notified about the abstract selection outcome by December 15, 2023.

If you have any questions, contact:
Michael Mayer, 74th ECTC Program Chair
University of Waterloo
mmayer@uwatwaterloo.ca

**Professional Development Courses**
Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From proposals received, 16 PDCs are selected for offering at the 74th ECTC on Tuesday, May 28, 2024. Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in “honored” self-study courses, tutorials, symposia, and workshops.

Using the format “Course Objectives/Course Outline/Who Should Attend,” 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 22, 2023. Authors are notified of course acceptance with instructions by December 15, 2023.

If you have any questions, contact:
Kitty Pearsall, 74th ECTC Professional Development Courses Chair – Boss Precision, Inc.
Phone: +1-512-845-3287 • E-mail: kitty.pearsall@gmail.com

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You are invited to visit ECTC’s website to submit an abstract in which you describe the novelty, scope, content, and key points of your proposed manuscript. You can also submit an optional supporting figure or data table. Abstracts cannot contain more than 700 words and must be received by October 9, 2023, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors with your submission. The authors are notified about the abstract selection outcome by December 15, 2023.

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**CONFERENCE AT A GLANCE**

**REGISTRATION**
Monday, May 29, 2023
3:00 p.m. - 6:00 p.m.
Tuesday, May 30, 2023
6:45 a.m. - 7:45 p.m.* *(AM PD Courses & Special Session Only)*
Wednesday, May 31, 2023
6:45 a.m. - 4:00 p.m.
Thursday, June 1, 2023
7:00 a.m. - 4:00 p.m.
Friday, June 2, 2023
7:00 a.m. - 12:00 Noon

ECTC Registration Desk located across from Mediterranean 3 (lobby level)

**ECTC EXHIBITION**
Wednesday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 6:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.
Thursday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 4:00 p.m.
Coquina Ballroom

**SPEAKER PREPARATION ROOM**
Tuesday – Friday
7:00 a.m. – 5:00 p.m.
Brava, lower level

**TUESDAY**

PDC Instructors and Proctors
Briefing & Breakfast
7:00 a.m. – 8:00 a.m.
Cordova 5 & 6

Professional Development Courses (PDCs)
8:00 a.m. – 12:00 p.m.
1:30 p.m. - 5:30 p.m.
See page 8 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop
8:00 a.m. – 4:30 p.m.
Palazzo E

**ECTC Special Session 1**
8:30 a.m. – 10:00 a.m.
Palazzo D

**ECTC Special Session 2**
10:30 a.m. – 12:00 p.m.
Palazzo D

**ECTC Special Session 3**
1:30 p.m. – 3:00 p.m.
Palazzo D

**ECTC Special Session 4**
3:30 p.m. – 5:00 p.m.
Palazzo D

**Refreshment Breaks**
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Mediterranean & Palazzo Foyers

**Lunch**
12 Noon – 1:15 p.m.
Mediterranean 4 & 5

**ECTC Exhibition Setup**
1:00 p.m. – 5:00 p.m.
Coquina Ballroom

**ECTC Student Reception**
5:00 p.m. – 6:00 p.m.
Outside: Mediterranean 4 & 5 Porte-Cochere

**General Chair’s Speakers Reception**
6:00 p.m. – 7:00 p.m.
Mediterranean 4 & 5
By invitation only

**Young Professionals Networking Panel**
7:00 p.m. – 7:45 p.m.
Palazzo D

**IEEE EPS Seminar**
7:45 p.m. – 9:15 p.m.
Palazzo E

**Wednesday – Friday**

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Palazzo E

**Sessions**
9:30 a.m. – 12:35 p.m. or
2:00 p.m. – 5:05 p.m.
see pages 10-21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Palazzo D

Sessions 2, 8, 14, 20, 26, 32
Palazzo A & B

Sessions 3, 9, 15, 21, 27, 33
Mediterranean 2 & 3

**37RD ECTC GALA RECEPTION**
Thursday at 6:30 p.m.
Valencia, lower level outside
(Backup Location: Mediterranean 4 & 5)

**DAILY MAINSTAGE**

ECTC Keynote
Wednesday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5

Diversity and Career Growth Panel Session
Wednesday
6:30 p.m. – 7:30 p.m.
Mediterranean 4 & 5

**EPS Plenary Session**
Thursday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5

**IEEE EPS President Panel**
Friday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5
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