# The 2023 IEEE 73rd Electronic Components and Technology Conference

May 30 – June 2, 2023

# 2023 Advance Program

JW Marriott Orlando, Grande Lakes
Orlando, Florida, USA

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

For more information visit www.ECTC.net

# INTRODUCTION FROM THE IEEE 73RD ECTC PROGRAM CHAIR FLORIAN HERRAULT

## The 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) at the JW Marriott Orlando, Grande Lakes, Orlando, Florida • May 30 - June 2, 2023

On behalf of the Program and Executive Committee, it is my pleasure to invite you to IEEE's 73rd Electronic Components and Technology Conference (ECTC), which will be held at JW Marriott Orlando, Grande Lakes, Orlando, Florida from May 30 to June 2, 2023. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1500 people attended ECTC 2022 in what was our first in-person event in three years.

At the 73rd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, chiplets, advanced substrates, assembly, materials and thermal modeling, reliability, packaging for harsh conditions, packaging for quantum and AI applications, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 73rd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature seven special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, five special sessions, 90 minutes each, are scheduled.

On Tuesday morning, May 30th at 8:30 a.m. Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH, will chair the session on Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment, followed by Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm chairing a special session at 10:30 a.m. on Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications. On Tuesday afternoon at 1:30 p.m. Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco, will host a special session on the topic of Photonic Integrated Circuit Packaging, followed by a special session on the CHIPS Act, organized by Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE. As in previous years, HIR will host a parallel track throughout the day.

On Tuesday afternoon, the Young Professionals reception will be organized by Yan Liu, Medtronic. On Tuesday evening, Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus, will co-chair the IEEE EPS Seminar on High-Density Substrates.

New this year, the following days (Wednesday-Friday) will kick off with a single-room special session from 8:00 a.m. to 9:15 a.m., which will then be followed by our traditional technical sessions with six parallel tracks.

On Wednesday May 31st at 8 a.m., join us early to receive our Welcome message from our General Chair Ibrahim Guven, followed by a captivating presentation and Q&A session by our Keynote speaker Prof. Michael Manfra from Purdue University; the title of the Keynote is "Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging". At the end of the day, at 6:30 p.m., a special session, co-hosted by ECTC and ITherm, will discuss workforce development for semiconductors and packaging. The panel will be chaired by Kim Yess, Brewer Science, Nancy Stoffel, GE Research, and Christina Amon, University of Toronto. This reception/panel event should not be missed.

On Thursday June 1st at 8 a.m., we will have the pleasure of starting the day with our ECTC Plenary Session, featuring an extensive panel of experts focused on next-generation millimeter-wave packaging. The 75-min session will be chaired by Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg Technical University.

Kitty Pearsall, Boss Precision, Inc., IEEE EPS President, and David McCann, Lyte, will chair the EPS President's ECTC panel session on Friday morning at 8 a.m. The session will focus on how photonics can enable the bandwidth densities with lower energy per bit in emerging SIP.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the ECTC Exhibition. Co-located with the IEEE ITherm Conference, the 73rd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 30th and are taught by distinguished experts in their respective fields. The ECTC Exhibition will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 73rd ECTC and to be a part of all the exciting technical and professional opportunities. I also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 73rd ECTC a success. I look forward to meeting you at the JW Marriott Orlando, Grande Lakes, Orlando, Florida, May 30 – June 2, 2023.

Florian Herrault
73rd ECTC Program Chair
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# 73rd ECTC ADVANCE REGISTRATION

## Advance Registration

**Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions, see page 32.**

Register early … save US$100 or more! All registrations received after May 5, 2023, will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Mediterranean Foyer.

## On-Site Registration Schedule

*Registration will be held in the Mediterranean Foyer on the Lobby Level.*

| | |
|---|---|
| Monday, May 29, 2023 | 3:00 p.m. – 6:00 p.m. |
| Tuesday, May 30, 2023 | 6:45 a.m. – 7:45 p.m.* |
| **6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Sessions only* | |
| Wednesday, May 31, 2023 | 6:45 a.m. – 4:00 p.m. |
| Thursday, June 1, 2023 | 7:30 a.m. – 4:00 p.m. |
| Friday, June 2, 2023 | 7:30 a.m. – 12:00 Noon |

***The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.***

## General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The JW Marriott Orlando Grande Lakes, as well as the ECTC, are both smoke free environments.

## ITherm 2023

ITherm is co-located with ECTC! All ITherm sessions and exhibits will take place in the same location, the JW Marriott Orlando Grande Lakes, as ECTC.

## Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

## ECTC Sponsors

With more than 70 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company's interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors."

To sign-up for sponsorship or to get more details, please contact Wolfgang Sauter at wsauter2@gmail.com or +1-802-922-3083.

## Hotel Accommodations

Rooms for ECTC attendees have been reserved at the JW Marriott Orlando Grande Lakes. The special conference rate for a single/double occupancy room is:

US $233.00 per night

This price includes single or double occupancy in one room.

Please note these rooms are on a first come, first served basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Please make sure to book a room as soon as possible as the conference room rate is sure to sell out! Rooms can be booked through our website at www.ectc.net/location. **If you need to cancel a reservation, please do so by 6 p.m. Eastern time, AT LEAST 5 days prior to arrival for a full refund.** Check-in time: 4 p.m. & check-out time: 11 a.m.

## Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2023 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2023 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com.

## Transportation Services

There is no complimentary transportation to and from the hotel and airport. All attendees must make their own transportation arrangements to the hotel upon arriving at the airport.

# 73rd ECTC CONFERENCE OVERVIEW

## 2023 ECTC Special Session on Advanced Packaging for Harsh Environments

### *Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities*

**Tuesday, May 30, 2023, 8:30 a.m. – 10:00 a.m.**

**Chairs: Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH**


Electronic components and systems are among the main contributors to the most innovative ideas and products of today's world. In the automotive industry, electronic components and systems are accountable for more than 80% of all innovation. When we think about highly automated and autonomous systems, advanced packaging is a must. Nowadays, most advanced electronic components such as CPUs or GPUs are being introduced into harsh environments such as automotive, avionics or space applications almost at the same time as in consumer products. Therefore, in our special session, we would like to discuss with the top experts from industry and academia what the current status and opportunities are for advanced packaging for harsh environments.

*Azeem Sarwar, General Motors*
*Giuseppe Barone, Robert Bosch GmbH*
*Vikas Gupta, ASE US, Inc.*
*Dae-Woo Kim, Samsung*
*Shin-Puu Jeng, TSMC*
*Ram Trichur, Henkel*
*Kouchi Zhang, TU Delft*
*Vanessa Smet, Georgia Tech*

## 2023 ECTC Special Session on Hybrid Bonding

### *Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications*

**Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.**

**Chairs: Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm**


This Special Session will explore the applications, requirements, and challenges of Copper Hybrid Bonds (CHB) for Chip-to-Wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand. While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

The session will include a moderator and speakers, each with a 10-minute presentation followed by a joint 20-minute Q&A session:

*Jan Vardaman, TechSearch International*
*Eric Beyne, IMEC*
*Ming Zhang, Synopsys*
*Raja Swaminathan, AMD*
*Thomas Urhmann, EVG*
*Chris Scanlan, Besi*

## 2023 ECTC Special Session on Photonics Packaging

### *Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption*

**Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.**

**Chairs: Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco**


Photonic integrated circuit (PIC) technologies are proliferating into many application spaces; from hyperscale data center, high-performance computing to sensing including LiDAR. Packaging remains the greatest challenge to high-volume manufacturing at high throughput and yield. The main challenges are: Optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability, and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC SC86C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption toward high-volume reality.

*Peter De Dobbelaere, Cisco*
*Thierry Mourier, CEA-Leti*
*Hesham Taha, Teramount*
*Alexander Janta-Polczynski, IBM*
*Peter O'Brien, Tyndall Institute*
*Colin Dankwart, Ficontec Service GmbH*

## 2023 ECTC Special Session on CHIPS Act

### *Advanced Packaging Manufacturing in North America: Building the Ecosystem*

**Tuesday, May 30, 2023, 3:30 p.m. – 5:00 p.m.**

**Chairs: Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE**



North America has companies that excel in design for electronics systems, device, and advanced packaging. However less than 2% of the packaging occurs in the US. This session will discuss the ambitious goals being set through the CHIPS ACT to bring Advanced Packaging to North America. We will review the targets and developing plans of the US government, funded through the CHIPS Act. The panelists will overview major initiatives launched in R&D and Manufacturing. We will also discuss the challenges to meeting the goals.

*Ajit Dubey, Google*
*Frank Gayle NIST, Office of Advanced Manufacturing*
*Subramanian Iyer, University of California Los Angeles*
*Carl McCants, DARPA*
*Dick Otte, Promex Industries, Inc.*
*Hem P. Takiar, Micron Technology Inc.*

## 2023 HIR Workshop at ECTC

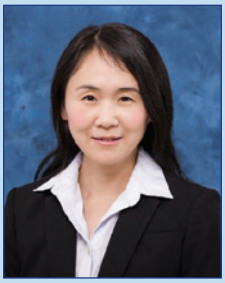
**Tuesday, May 30, 2023**

Four Technical Sessions are being developed. More details coming soon.

- *Additive Manufacturing in Post Moore Era*
- *Large Research Initiatives in Heterogeneous Integration – a Status Report*
- *MEMS & Sensor Integration at the Edge*
- *Application of AI and ML in Electronics Packaging from Co-Design to Production*

## 2023 Young Professionals Networking Panel

**Tuesday, May 30, 2023, 7:00 p.m. – 7:45 p.m.**
**Chair: Yan Liu, Medtronic**



This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

## 2023 IEEE EPS Seminar on High-Density Substrates

### *The Future of High-density Substrates – Towards Submicron Technology*

**Tuesday, May 30, 2023, 7:45 p.m. – 9:15 p.m.**

**Chairs: Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus**

Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules while Si scaling is slowing down. One of the key attributes of chiplets and HI technologies is the bandwidth of interconnection between chips within the same package. A very short-distance and high-density interconnection from one chip to another enables high-speed data transmission with low energy loss. High-density chip carrier substrate is the core technology driving the evolution of chiplets and HI technologies.

The EPS Seminar organized by TC6 (High-Density Substrate and Board) will discuss ultra-fine-pitch substrate technologies towards submicron ground rule for Chiplets and Heterogeneous Integration. We will have 5 panelists, and each panelist will give a short talk presenting insights on technology trends, technical challenges, application requirements, recent technical updates, and more covering advanced interposer technologies, followed by a panel discussion.

*Yasushi Araki, Shinko*
*Yu-Hua Chen, Unimicron*
*Satoru Kuramochi, Dai Nippon Printing (DNP)*
*Madhavan Swaminathan, Penn State University*
*Griselda Bonilla, IBM*

## 2023 Keynote Speaker

### *Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging*

**Wednesday, May 31, 2023, 8:00 a.m. – 9:15 a.m.**

**Prof. Michael J. Manfra, Purdue University**

Quantum computing will revolutionize the way we tackle certain societally relevant but currently intractable problems. To reach this promise, significant advances in quantum hardware on multiple scales are required. This keynote address will explore the challenges and opportunities in quantum computing hardware ranging from basic choice of qubit platform, through scalable control and readout, to system architecture. Technology advancement will require innovations in material science and device physics to tackle challenges on the quantum plane. Progress will also hinge on innovations in interconnect technology and advanced packaging for an integrated quantum-classical hardware system. As in classical digital computing, thermal management and reliability concerns will impact quantum system performance and must be addressed directly. In this presentation, some exemplars that demonstrate the opportunities for contributions to quantum technology from the community focused electron devices, interconnects and advanced packaging will be discussed. Development of a full-stack quantum computer necessitates industrial programs stimulated and informed by innovation generated in government labs and academic research groups.

## 2023 ECTC/ITherm Diversity and Career Growth Panel and Reception

### *Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative*

**Wednesday, May 31, 2023, 6:30 p.m. – 7:30 p.m.**

**Chairs: Kim Yess, Brewer Science / ECTC, Nancy Stoffel, GE Research / ECTC, and Christina Amon, University of Toronto / ITherm**

The electronic industry has an urgent need to increase the technical workforce and address challenges related to recruitment, inclusion and retention of diverse talents. The panelists will discuss the development of initiatives, policies and programs to increase and diversify the workforce, along with metrics to assess progress. Discussions will include the benefits of diversity in high-performing workplaces (improve productivity, innovation), strategies to build a diverse workforce, and tools for inclusion and engagement – sharing both successes and challenges associated with achieving these goals.

*Dereje Agonafer, University of Texas Arlington*
*Courtney Power, NextFlex*
*Jennifer Edwards, GE Foundation*

***These sessions are open to all conference attendees.***

## 2023 ECTC Plenary Session on mm-Wave Phased Array Packaging

***Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems***

**Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.**
**Chairs: Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg University of Technology**

Phased arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and the latest advancements in packaging and integration technologies for designing and implementing phased array front-end modules, including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, system demos/prototypes, and so on.

*Jonathan Hacker, Teledyne Scientific*
*Augusto Gutierrez-Aitken, Northrop Grumman Space Systems*
*Hasan Sharifi, HRL Laboratories, LLC*
*Madhavan Swaminathan, Pennsylvania State University*
*Shahriar Shahramian, Nokia Bell Labs*
*Alberto Valdes-Garcia, IBM Research*

## 2023 IEEE EPS President Panel on Photonics

***How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP***

**Friday, June 2, 2023, 8:00 a.m. – 9:15 a.m.**
**Chairs: Kitty Pearsall, Boss Precision, Inc., and David McCann, Lyte**

This panel will discuss the tools, technologies, and approaches that will enable the industry to enhance the bandwidth density of interconnections in SiP enabled by photonics. To be adopted, such capabilities must be provided with energy per bit that meets the roadmaps and standards targets for the interconnection protocols within the package and on the chip.

*Amr S. Helmy, University of Toronto*
*Ritesh Jain, Lightmatter*
*Ajey Jacob, University of Southern California*
*Stefano Oggioni, ATS*

## Luncheons

This year ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $75 to replace. Please come and enjoy time with other attendees and colleagues in the industry! Lunch times will vary, see below for specific details for each day.

| | |
|---|---|
| **Tuesday:** | **12:00 Noon – 1:15 p.m.** |
| **Wednesday:** | **12:45 p.m. – 2:00 p.m.** |
| **Thursday:** | **12:45 p.m. – 2:00 p.m. – Sponsored by: The IEEE Electronics Packaging Society** |
| **Friday:** | **12:45 p.m. – 2:00 p.m. – Don't miss out on this lunch! We will be raffling off a number of prizes including a hotel stay, free conference registrations, and many other industry gadgets!** |

## General Chair's Speakers Reception

**Tuesday, May 30, 2023 • 6:00 p.m. – 7:00 p.m.**
(by invitation only)

## ECTC Student Reception

**Tuesday, May 30, 2023 • 5:00 p.m. – 6:00 p.m.**
*Hosted by Texas Instruments, Inc.*

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them to be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

## Exhibitor Reception

**Wednesday, May 31, 2023 • 5:30 p.m. – 6:30 p.m.**
Open to all conference attendees.

## 73rd ECTC Gala Reception

**Thursday, June 1, 2023 • 6:30 p.m.**
All badged attendees and their guests are invited to attend a reception hosted by Gala Reception sponsors.

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# PROFESSIONAL DEVELOPMENT COURSES

## Tuesday, May 30, 2023

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## MORNING COURSES
## 8:00 a.m. – 12:00 Noon

### 1. HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

***Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech***

**Course Description:**
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail. The selection of novel alloys with reduced fragility will be presented. Crucial parameters for high reliability solder alloy for automotive industry will be presented. Electromigration, and tin whisker growth will also be discussed. The emphasis of this course is placed on the understanding of how the numerous factors contribute to the failure modes, and how the selection of proper solder alloys and surface finishes for achieving high reliability are key.

**Course Outline:**
1. Mainstream Lead-free Soldering Practices
2. Surface Finishes Issues
3. Mechanical Properties
4. Intermetallic Compounds
5. Failure modes
6. Reliability – Thermal cycle
7. Reliability - Fragility
8. Reliability – Rigidity and Ductility
9. Reliability – Composite Solder Enable Hierarchy Assembly & Shock Resistance
10. Reliability – Tin Whiskers

**IMPORTANT NOTICE**
Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

**Who Should Attend:**
Directors, managers, design engineers, process engineers, and reliability engineers who care about achieving high reliability lead-free solder joints and would like to know how to achieve it should take this course.

### 2. WAFER-LEVEL CHIP-SCALE PACKAGING (WCSP) FUNDAMENTALS

***Course Leader: Patrick Thompson – Texas Instruments, Inc.***

**Course Description:**
This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fabrication, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? What are the challenges for memory? And what about other complex devices such as ASICs and microprocessors?

**Course Outline:**
1. WLCSP Definition
2. Trends, Categories, Examples, Challenges, Supply Chain
3. Historical Overview, Package Highlights, Assembly Flow
4. Processing and Reliability: Flex, Temperature Cycling, Drop, Electromigration
5. Fan-Out Technologies
6. Embedded Technologies
7. Conclusions

**Who Should Attend:**
The course will be useful to the following groups of engineers: newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WLCSP as a potential alternative for their packaging solutions.

### 3. FUNDAMENTALS OF RF DESIGN AND FABRICATION PROCESSES OF FAN-OUT WAFER/LEVEL AND ADVANCED RF PACKAGES

***Course Leaders: Ivan Ndip – Fraunhofer IZM/Budapest Technical University and Markus Wöhrmann – Fraunhofer IZM***

**Course Description:**
Due to their myriad of advantages in system-integration, fan-out wafer/panel-level packages (FO WLPs/PLPs) and other advanced RF packages (e.g., glass interposers and chip-embedding packages) will play a key role in the development of emerging electronic systems. The fabrication processes and RF performance of these packages will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of these advanced packages for emerging RF/wireless applications.

An overview of distinct types of wafer-level packages, fan-out technologies, glass interposers and chip-embedding packages will first be given. This will be followed by a presentation of new fan-out-packaging and interposer-based concepts for emerging and future applications (e.g., 5G mmWave, mmWave radar sensors, 6G) as well as a thorough discussion of the materials and fabrication processes of FO-WLPs/PLPs, multilayered RDLs, glass interposers and chip embedding packages. The basics of efficient RF design and measurement of the fundamental building blocks of these advanced packages will be given for frequencies up to the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

**Course Outline:**
1. Overview: Different Types of Wafer-level Packages, Fan-out Technologies, and Advanced RF Packages
2. Requirements of 5G Packaging and New Fan-out Packaging Concepts for 5G mmWave Applications
3. Materials and Fabrication Processes: FO-WLPs/PLPs, Multi-layered RDLs, Glass Interposers and Chip Embedding Packages
4. Fundamentals of RF Design and Measurement: FO-WLPs/PLPs, Glass Interposers and Chip-Embedding Packages
5. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

**Who Should Attend:**
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages for emerging applications (e.g., 5G, 6G, mmwave radar sensors) should attend.

## 4. ELIMINATING FAILURE MECHANISMS IN ADVANCED PACKAGES

***Course Leader: Darvin Edwards – Edwards Enterprises***

**Course Description:**

Reliability failure mechanisms that plague semiconductor packages will be explored with an emphasis on new package technologies such as heterogeneous package integration as well as an overview of reliability issues in high volume packages. Topics studied include reliability of TSV-chip interactions, Direct Cu Bond (DCB) and micro bump mechanical reliability, high density interconnect (HDI) reliability, electromigration performance, stress induced interlevel dielectric (ILD) damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, system level drop reliability, the impact of aging on reliability performance and many more. Primary failure analysis techniques will be described. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. Characterization and implementation of test structures and design guidelines that enable reliable first pass products will be described and encouraged. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described.

**Course Outline:**

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques
4. FC-BGA Package Failure Mechanisms
5. WLCSP Package Failure Mechanisms
6. Embedded Die & Fan-Out WLP/PLP Failure Mechanisms
7. TSV Failure Mechanisms
8. High Density Interconnection Reliability
9. Direct Bond Interconnect Reliability and Testing
10. Materials, Modeling, Design Rules, and Reliability
11. Summary

**Who Should Attend:**

This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

## 5. RELIABILITY ENGINEERING TESTING METHODOLOGY AND STATISTICAL KNOWLEDGE FOR QUALIFICATIONS OF CONSUMER AND AUTOMOTIVE ELECTRONIC COMPONENTS

***Course Leader: Fen Chen – Cruise LLC (a GM company)***

**Course Description:**

The consumer electronics industry and today's fast-growing automotive industry continue to demand ever-higher product hardware reliability. This tutorial will provide an overview of reliability testing methodology and statistical knowledge for qualifications of consumers and automotive electronic components. The reliability testing management includes various Rel testing methods and their application to product development at different phases will be first introduced. Some important statistic/probabilistic concepts including uncertainty, confidence level, and how to minimize/deal with them will be discussed. An effective approach to mitigate low sample size and short test duration will be introduced. Then the tutorial will focus on the physics of failure-based acceleration life models for some common reliability testing failures. A deep dive discussion on the temperature cycling model considering dT acceleration, dwell time acceleration, ramp rate acceleration, and Tmax acceleration will be explored. Next, a typical methodology to develop a PoF-based Rel validation testing plan reference to the product field mission profile will be introduced. The mission profiles of conventional vehicles and consumer smartphones will be compared. How to develop a customized mission profile for an autonomous vehicle specifically per its deployment location will be described. Finally, some examples of hardware failure modes with their risk assessments and lifetime modeling will be presented.

**Course Outline:**

1. Reliability Engineering Product Qualification Methodology (Strategic Planning)
2. Reliability Engineering General Introduction
3. Knowledge-based and Standard-based Rel Qualification Approach
4. DfR, Rel R&R, Various Rel Testing Methods, and Their Applications During Product Development
5. Reliability Engineering Basic Knowledge of Probabilities and Statistics
6. Rel Testing Uncertainty and How to Minimize & Deal with Common Rel Engineering Statistical Concepts, Methods, and Usages
7. Reliability Engineering Acceleration Lifetime Modeling Overview (Physics of Failure)
8. Various Life Acceleration Models for Consumer Products and Automotive Components Rel Failures
9. Reliability Test Plan Development Based on Mission Profile Overview (Standards, Knowledge, and Experience)
10. Customized Mission Profile Development
11. GMW3172 Based Rel Validation Plan for Automotive Electronic Components
12. A Company Specific Reliability Validation Plan for Smartphones
13. Failure Modes and Lifetime Prediction Case Studies
14. Thermal-mechanical Interaction Impacts on the Chip Thermal Performance Case Study

**Who Should Attend:**

Engineers and tech managers already involved in the consumer product and automotive product fields, and those who need a fundamental understanding or a broad overview of the product reliability qualification.

## 6. RELIABILITY PHYSICS AND FAILURE MECHANISMS IN ELECTRONICS PACKAGING

***Course Leader: Xuejun Fan – Lamar University***

**Course Description:**

This course presents an overview of the physics of failures in electronics packaging. The course discusses key fundamental concepts of reliability physics associated with various stress conditions, including thermal degradation, thermo-mechanical stress, dynamic and vibrational loading, moisture, and humidity, as well as electrical current stress. Failure mechanisms studied include chip-package interactions, micro bump reliability, electromigration performance, inter-layer dielectric (ILD) damage under bumps and Cu pillars, solder joint reliability, drop and vibrational damage, interfacial delamination, and the impact of moisture and environmental humidity. Acceleration factor models for different failure mechanisms are introduced. Stress analysis methods using finite element analysis (FEA) with specific applications to packaging are described.

**Course Outline:**

1. Introduction to Advanced Package Reliability Physics
2. Thermal and Thermo-mechanical Driven Failure Mechanisms
3. Dynamic and Vibrational-driven Damages
4. Moisture and Humidity-induced Failures
5. Electromigration

**Who Should Attend:**

This course is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial.

## 7. RELIABLE INTEGRATED THERMAL PACKAGING FOR POWER ELECTRONICS

***Course Leader: Patrick McCluskey – University of Maryland***

**Course Description:**
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation, and the fact that power electronics have become key components of heterogeneous integration, have made it essential that the reliability of power electronics be characterized and enhanced. Furthermore, increased power levels combined with increased packaging density have led to higher heat densities in power electronic systems making thermal management more critical to performance and reliability of power electronics. This course will emphasize approaches to integrated thermal packaging that addresses performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g., organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and in the techniques for their reliability assessment.

**Course Outline:**
1. Motivation for Heterogeneously Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques
3. Application of Thermal Management Techniques to Commercial Power Systems
4. Durability Assessment (Failure Modeling, Simulation, Testing, and Health Monitoring)
5. Reliability and Thermal Packaging of Active Devices and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, including Organic Encapsulants
7. Reliability in Rigid Assembly Packaging
8. Flexible Materials, Packaging, and Thermal Management
9. Reliability of Additive Manufactured and Embedded Power Electronics

**Who Should Attend:**
This PDC is aimed at both new and veteran practicing engineers and technical managers who seek to incorporate thermal management into heterogeneously integrated power electronics packaging for use in a wide variety of power and energy generation and distribution applications.

## 8. INTRODUCTION TO PWB THERMAL ANALYSES

***Course Leader: Patrick Loney - Northrop Grumman***

**Course Description:**
Printed Wire Boards (PWBs) are present in almost every piece of electronics. This includes the SIM card in your phone, the backplane in your laptop, and the high-power card assembly in power supplies. Usage and complexity are increasing. Increasing part and power densities on PWBs necessitates increased attention to PWB thermal performance. No two PWBs are identical but the approaches needed to develop thermal models all follow good, sound, thermal engineering basics. In this course, attendees will learn how to categorize cooling techniques for PWBs, predict temperature gradients, and compare part temperature predictions with acceptable limits.

**Course Outline:**
1. Purpose of the PWB Thermal Analysis
2. Cooling Configurations Covered in this Course
3. Basic Inputs
4. Defining the Component Model
5. Harvesting Data from the Datasheet
6. Modeling the Part on the Board
7. Applying Boundary Conditions
8. The PWB Stackup
9. Determining Run Cases and Configurations
10. Augmenting Heat Transport Capability

**Who Should Attend:** The class targets the front-line thermal engineer. Since the course material focuses on the process of PWB thermal modeling, all experience levels of engineers and managers will benefit from attending.

# AFTERNOON COURSES
# 1:30 p.m. – 5:30 p.m.

## 9. ADDITIVE FLEXIBLE HYBRID ELECTRONICS – MANUFACTURING AND RELIABILITY

***Course Leader: Pradeep Lall – Auburn University***

**Course Description:**
This course will cover manufacturing, design, assembly, and accelerated testing of additively printed flexible hybrid electronics for applications in some emerging areas. Manufacturing processes for additive fabrication of flexible hybrid electronics will be discussed. Flexible hybrid electronics enable opportunities to develop stretchable, bendable, foldable form-factors in electronics applications, previously not possible with rigid electronics technologies. The manufacture of thin electronic architectures requires the integration of thin chips, flexible encapsulation, compliant interconnects, and nano-particle inks for metallization traces. Several additive-printed electronics processes for fabricating and assembling flexible hybrid electronics have become tractable. Pick-and-place of thin-silicon, and compliant interposers through interconnection processes such as reflow require an understanding of the deformation and warpage processes. Modeling operational stresses in flexible electronics requires the material behavior under large deformation and constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear, and abrasion. The failure mechanisms, failure modes, and acceleration factors in flexible electronics under operational loads of stretch, bend, fold, and loads resulting from human body proximity significantly differ from rigid electronics. Several product areas for applying flexible electronics are tractable in the near term, including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring, and automotive electronics.

**Course Outline:**
1. Additive Technologies in Flexible Electronics
2. Aerosol-jet Printing
3. Ink-jet Printing
4. Screen Printing and Gravure Printing
5. Laser-direct Sintering
6. In-mold Labeling
7. Ultra-thin Chips
8. Die-attach Materials for Flexible Semiconductor Packaging
9. Flexible Encapsulation Materials
10. Dielectric Materials for Large-area Flexible Electronics
11. Flexible Substrates
12. Stretchable Inks for Printed Traces
13. Flexible Power Sources
14. Accelerated Testing Protocols

**Who Should Attend:** The targeted audience includes scientists, engineers and managers considering the use of additively printed flexible electronics or considering moving from rigid electronics to flexible electronics, as well as reliability, product or applications' engineers who need a deeper understanding of additively printed flexible electronics: the advantages; limitations; and failure mechanisms.

## 10. FAN-OUT PACKAGING AND CHIPLET HETEROGENEOUS INTEGRATION

***Course Leader: John Lau - Unimicron***

**Course Description:**
Fan-out wafer/panel-level packaging has been getting lots of tractions since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this

lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with varied sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

**Course Outline:**

1. Formation of FOWLP: (a) Chip-first (Face-Down), (b) Chip-first (Face-up), and (c) Chip-last Fabrication of Redistribution Layers (RDLs) Formation of FOPLP: (a) Chip-first (Face-down), (b) Chip-first (Face-up), and (c) Chip-last
2. TSMC InFO: (a) InFO-PoP, and (b) InFO-AiP Driven by 5G mmWave
3. Samsung PLP: (a) PoP for SmartWatches and (b) SiP SbS for Smartphones
4. Warpages: (a) Warpage Types and (b) Allowable Warpages
5. Reliability of FOWLP and FOPLP: (a) Thermal-Cycling and (b) Drop Course - Many Examples of FOWLP and FOPLP
6. Chiplet Design and Heterogeneous Integration (HI) Packaging vs. System-on-chip (SoC) Advantages and Disadvantages of Chiplet Design and HI Packaging - Many Examples of Chiplet Design and HI Packaging
7. Chiplets Lateral Interconnects (Bridges) - Many Examples
8. Chiplet Design and HI Packaging on Organic Substrates (SiP) - Many Examples
9. Chiplet Design and HI Packaging on Silicon Substrates (TSV-Interposers) - Many Examples
10. Chiplet Design and HI Packaging on Fan-Out RDL Substrate - Many Examples
11. Assembly Technologies for Chiplet Design and HI Packaging

**Who Should Attend:** If you are involved with any aspect of the electronics industry, you should attend this course. The lectures are based on the publications by many distinguish authors and the books (by the lecturer) such as Fan-Out Wafer-Level Packaging (Springer, 2018) and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023).

## 11. PHOTONIC TECHNOLOGIES FOR COMMUNICATION, SENSING, AND DISPLAYS

***Course Leader: Torsten Wipiejewski – Huawei Technologies***

**Course Description:**

This course will provide an overview on the various photonic technologies that enable optical communication, optical sensing, and modern display applications. These applications are key for the information and communication technology of today and pave the way to the future. High speed optical communication from board level in data centers to long haul transmission requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of several types, high speed optical modulators and photodetectors as well as integration schemes such as photonic integrated circuits (PICs) and packaging aspects. Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitates the usage by end-users without specific medical knowledge. Packaging should provide high accuracy solution at low cost. Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro-LEDs as well as some features of 3D displays. Micro-LEDs for large size displays require novel assembly technologies to mount chips of only several micrometers in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

**Course Outline:**

1. Fundamental Properties of Photonic Components
2. Light Sources (LEDs, Laser Diodes, Others)
3. Transmitter and Receiver Components in Optical Communication (Lasers, Modulators, Photodetectors, Passive Optical Components, Photonic Integrated Circuits (PICs), Silicon Photonics, Optical Modules), Monolithic and Hybrid Integration, Packaging
4. Optical Sensing Elements and Applications (Spectrometers, Light Sources, Photoacoustic Sensors, Frequency Combs)
5. Display Technologies Liquid Crystal Displays (LCD), Organic Light Emitting Diode (OLED) Displays, Quantum Dot Emissive Layers, Micro-LED Arrays and Large Size Displays using Chiplet Mass Transfer and Bonding, 3D Displays
6. Summary and Outlook

**Who Should Attend:** The course addresses engineers, scientists and students who would like to get a general overview of various photonics technologies used in today's products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are and which new technologies are being developed for further improvements or aiming at technology break throughs.

## 12. FLIP CHIP TECHNOLOGIES

***Course Leaders: Shengmin Wen – HaiSemi and Eric Perfecto – IBM Research***

**Course Description:**

This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various type of wafer bumping technologies, solder joint formation, substrate selection, underfill type and selection, and reliability evaluation. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. Plenty of examples are presented to show the versatile flip chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form interconnection such as wire bond / flip chip mixed integration. Major flip chip assembly packages are discussed, such as the BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages that uses Si or organic interposers, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization and its consequence on packaging, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their project's success. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today's flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, and electromigration.

**Course Outline:**

1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Wafer Level Fan-Out; and Panel-Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

**Who Should Attend:**
The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

## 13. PACKAGING AND HETEROGENEOUS INTEGRATION FOR AUTOMOTIVE ELECTRONICS AND ADVANCED CHARACTERIZATION OF EMCS

***Course Leader: Przemyslaw Gromala – Robert Bosch GmbH***

**Course Description:**
Demand for more advanced packaging technologies is growing rapidly in the automotive, avionics and energy industries. Today, electronic components developed for the consumer market are simultaneously used in harsh environments. Advanced packaging and heterogeneous integration are major contributors to the most innovative ideas, new products, and services. These electronic components are composed of many different materials. Stress due to a mismatch in coefficient of thermal expansion (CTE) between adjacent materials is one of the main causes of reliability problems (e.g., warpage, delamination, fatigue, aging). In addition, these materials are subject to aging during long-term use. Numerical simulations are used to accelerate the development process. This course will discuss the details of how a simulation driven design allows for the efficient development of innovative electronic components and systems. You will be able to learn what is needed to select optimal materials, how to perform material characterization and modeling. I will demonstrate how to quantitatively predict the stress state in design element using multi-domain simulations. Finally, I will present the application of AI/ML techniques to create a digital twin of an electronic control module.

**Course Outline:**

1. Introduction
2. Selection of the Material
3. Curing Shrinkage
4. Coefficient of Thermal Expansion
5. Linear Viscoelastic Properties
6. Modeling of Linear Viscoelastic Behavior
7. Nonlinear Viscoelasticity
8. Fracture Test and Implementation
9. Thermal Aging
10. Digital Twin
11. Summary

**Who Should Attend:** Engineers and technical managers who are already involved in the material characterization and modelling, numerical modelling, process engineers and PhD students who need fundamental understanding or broad overview.

## 14. ANALYSIS OF FRACTURE AND DELAMINATION IN MICROELECTRONIC PACKAGES

***Course Leader: Andrew Tay - National University of Singapore***

**Course Description:**
The main objective of this course is to provide a fundamental understanding as well as techniques of applying the fracture mechanics methodology to predicting fracture and delamination in microelectronic packages. The mechanism of delamination failure due to thermal stress and moisture will be described and analyzed. Simulation of transient heat transfer and moisture diffusion processes occurring during package qualification will be described. An introduction to the fundamentals of interfacial fracture mechanics will be given together with descriptions of some numerical methods of calculating fracture mechanics parameters. Experiments which verify the methodology for predicting delamination in packages will then be described followed by some interesting case studies.

**IMPORTANT NOTICE**
Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

**Course Outline:**

1. Development of Hygrothermal Stresses in Microelectronics Packages
2. Finite Element Analysis and Stress Singularities in Microelectronic Packages.
3. Inadequacy of Maximum Stress Failure Criterion
4. Fundamentals of Fracture Mechanics Methodology
5. Computation of Fracture Mechanics Parameters
6. Measurement of Fracture Toughness
7. Experimental Verification of the Methodology
8. Case Studies on Delamination of Pad-encapsulant Interfaces, Die-attach Layers, and On-chip Interconnect Structures (BEOL)
9. Cohesive Zone Modeling of Delamination and Case Study

**Who Should Attend:** This course is designed for packaging design engineers who perform reliability analysis of microelectronics and photonics packages.

## 15. POLYMERS IN WAFER LEVEL PACKAGING

***Course Leader: Jeffrey Gotro – InnoCentrix, LLC***

**Course Description:**
The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level (FOWLP) packaging as well as Fan-Out Panel Level packaging (FOPLP). The course will provide an overview of the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be:

1) Gain insights on how polymers are used in Fan Out Packaging, specifically mold compounds and polymer redistribution layers (RDL).

2) Understand the key polymer and processes challenges in Fan-Out Wafer-Level Packaging.

3) Learn about polymers and processes used in Fan Out Panel Level Packaging including new materials for mold compounds and a detailed description of the polymers used for RDL in FOPLP.

**Course Outline:**

1. Overview of Polymers used in Fan-Out Wafer-Level Packaging (FOWLP)
2. Wafer-level Process Flows (Chip-first Versus Chip-last (RDL first))
3. Epoxy Mold Compounds for Fan-Out Packages
4. Photosensitive Polyimides and Polybenzoxazoles for RDL
5. Polymer Reliability Challenges in Fan-out Wafer-level Packaging
6. Processes and Materials for Fan-out Panel-level Packaging (FOPLP)

7. Wafer Versus Panel Processing; Polymer Challenges and Solutions
8. Pre-applied Underfills and Wafer-level Underfills, Chemistry and Process

**Who Should Attend:**
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

## 16. THERMAL MANAGEMENT OF ELECTRONICS

***Course Leader: Jaime Sanchez – Intel Corporation***

**Course Description:**
This course provides the fundamentals of heat transfer applied to the design of thermal systems used to cool electronic components with an emphasis in semiconductor packages. We start with the basic theory of heat transfer and demonstrate simple concepts used today to calculate the cooling requirements for an electronic package and the impact of various parameters on the electronic package. This course covers in-depth heat transfer theory and analysis to give the student a comprehensive understanding of the key modes of heat transfer and their applications. Practical topics such as thermal interface materials, heat sink design and advanced cooling techniques are reviewed.

**Course Outline:**
1. Fundamentals of Heat Transfer and Its Application to Electronics Cooling
2. Techniques to Determine Cooling Requirements for a Package and Its Impact
3. Simplification of Heat Transfer Equations to Analyze Cooling Solutions
4. Governing Principles of Cooling Solutions
5. Application of Numerical Methods to Calculate the Performance of Cooling Solutions
6. Introduction to Thermal Interface Materials and Their Applications
7. Techniques to Size Cooling Requirements and Trade-offs
8. Parameters that Impact the Performance of Cooling Solutions
9. Introduction to Experimental Characterization of Cooling Solutions and Instrumentation

**Who Should Attend:** This class is intended for senior undergraduate and graduate students, as well as engineers working in the field of thermal management.

**IMPORTANT NOTICE**

***Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.***

***See page 32 for registration information***

## AREA ATTRACTIONS

Make your Florida escape an extraordinary one at JW Marriott Orlando, Grande Lakes. Located on a lush, 500-acre property, our resort is the ideal base for those wishing to explore the Orlando area - or for sunny family vacations. Stretch out in modern rooms offering luxury bedding, marble bathrooms, 65-inch HDTVs and sweeping views of the resort. Unwind at our outdoor pool complex, which includes a lazy river, or try our challenging 18-hole golf course, designed by PGA legend Greg Norman. Select from several enticing in-house dining options, from luxury Italian fare at Primo to a farm-to-table menu and craft beer at Whisper Creek Farm. Take advantage of our resort's excellent location to explore gorgeous central Florida. JW Marriott Orlando, Grande Lakes provides an exceptional experience that you and your family will never forget.

# Program Sessions: Wednesday, May 31, 9:30 a.m. -12:35 p.m.

| Session 1: Heterogeneous Chiplet Integration | Session 2: High-Performance Packaging Materials | Session 3: Advancements in Copper/Silicon-Oxide Hybrid Bonding |
|---|---|---|
| **Committee:**<br>**Packaging Technologies** | **Committee:**<br>**Materials & Processing** | **Committee:**<br>**Interconnections** |
| **Session Co-Chairs:**<br>**Andrew Kim**<br>**Apple, Inc.**<br>**Email: hkim34@apple.com**<br><br>**Mike Gallagher**<br>**Dupont Electronics and Imaging**<br>**Email: michael.gallagher@dupont.com** | **Session Co-Chairs:**<br>**Yoichi Taira**<br>**Keio University**<br>**Email: taira@appi.keio.ac.jp**<br><br>**Yi Li**<br>**Intel Corporation**<br>**Email: yi.li@intel.com** | **Session Co-Chairs:**<br>**Katsuyuki Sakuma**<br>**IBM Corporation**<br>**Email: ksakuma@us.ibm.com**<br><br>**Matthew Yao**<br>**GE Aviation**<br>**Email: matthew.yao@ge.com** |
| ***1. 9:30 AM – Ultra High Density Low Temperature SoICTM With Sub-0.5 µm Bond Pitch***<br>Han-Jong Chia, Shih-Peng Tai, Ji James Cui, C. T. Wang, Chih-Hang Tung, Kuo-Chung Yee, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd. | ***1. 9:30 AM – High Modulus Photosensitive Permanent Film Utilizing Novel Polymerization System for Advanced MEMS Structure Fabrication***<br>Ken-ichi Yamagata, Shiori Yuge, Ryosuke Nakamura, HIrofumi Imai – Tokyo Ohka Kogyo Co., Ltd. | ***1. 9:30 AM – A Study on the Surface Activation of Cu and Oxide for Hybrid Bonding Joint Interface***<br>Bohee Hwang, Soohwan Lee, Youngkun Jee, Sangcheon Park, Gyeongjae Jo, Kwangbae Kim, Sungjin Han, Ilhwan Kim, Jumyong Park, Hyunchul Jung, Dongwoo Kang, Un-Byoung Kang – Samsung Electronics Co., Ltd.-Test and System Package |
| ***2. 9:50 AM – Process Integration of Photonic Interposer for Chiplet-Based 3D Systems***<br>Damien Saint-Patrice, Stephane Malhouitre, Myriam Assous, Thierry Pellerin, Remi Velard, Leopold Virot, Edouard Deschaseaux, Maria-Luisa Calvo-Munoz, Karim Hassan, Stephane Bernabe, Yvain Thonnart, Jean Charbonnier – CEA-Leti | ***2. 9:50 AM – Lithographic Performance and Insulation Reliability of a Novel i-Line Photosensitive Dielectric Material***<br>Go Inoue, Daiki Yukimori, Kaho Shibasaki, Ayano Okuda, Nobuhiro Ishikawa, Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd. | ***2. 9:50 AM – Fine Pitch Die-to-Wafer Hybrid Bonding***<br>Thomas Workman, Jeremy Theil, Gill Fountain, Dominik Suwito, Cyprian Uzoh, Guilian Gao, K. M. Bang, Bongsub Lee, Laura Mirkarimi – Adeia |
| ***3. 10:10 AM – Aggressive Pitch Scaling (Sub-0.5 µm) of W2W Hybrid Bonding Through Novel Materials and Process Innovations***<br>Tyler Sherwood, Raghav Sreenivasan, Jason Appell, Raghuveer Patlolla, Kun Li, Ki Cheol Ahn, Joe Salfelder, Ryan Ley – Applied Materials, Inc.; Thomas Kasbauer, Gernot Probst, Jurgen Burggraf, Thomas Uhrmann – EV Group, Inc. | ***3. 10:10 AM – Effect of Surface Roughness of Polymer Dielectric Materials on Resolution of Fine Line Features***<br>Pragna Bhaskar, Mohanalingam Kathaperumal, Mark Losego, Madhavan Swaminathan – Georgia Institute of Technology | ***3. 10:10 AM – Direct Die to Wafer Cu Hybrid Bonding for Volume Production***<br>Chun Ho Fan, Hoi Ping Ng, Siu Cheung So, Ming Li, Siu Wing Lau, Thomas Uhrmann, Juergen Burggraf, Mariana Pires – ASMPT Hong Kong, Ltd. |
| ***Refreshment Break: 10:30 a.m.-11:15 a.m.*** | | |
| ***4. 11:15 AM – Design Space Explore (DSE) for Over-136 GB/s Bandwidth With LPDDR5X SDRAM Packages on SOC Package in 200 mm³***<br>Heeseok Lee, Jun So Pak, James Jung, Jisoo Hwang – Samsung Electronics Co., Ltd. | ***4. 11:15 AM – A Novel High Reliability and Low Dk/Df Dielectric Material for 5G mmWave and HPC***<br>Kaori Hamada, Hiroshi Ozaki, Toshiyuki Sato, Shin Teraki, Fumikazu Komatsu, Masaki Yoshida, Hirotatsu Ikarashi – NAMICS Corporation | ***4. 11:15 AM – Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding With High Density TSV for 3D Integration Applications***<br>Jerzy Javier Suarez Berru, Stephane Nicolas, Nicolas Bresson, Myriam Assous, Stephan Borel – CEA-Leti |
| ***5. 11:35 AM – 3D Stacking of Heterogeneous Chiplets on Modified FOWLP Platform With Thru-Silicon Redistribution Layer***<br>Tai Chong Chai, Boon Long Lau, Lim Pei Siang Sharon, David Ho Soon Wee – Institute of Microelectronics A*STAR; Rob Van Kampen, Paul Castillou, lance barron, Mickael Renault, jay ko, Jonathan Hammond – Qorvo, Inc. | ***5. 11:35 AM – Single-Layer Release Material Having Laser Lift-Off and Chip Fixing Property for FO-WLP Chip First Process***<br>Okuno Takahisa, Shinjo Tetsuya, Usui Yuki, Fukuda Takuya, Yanai Masaki, Yagyu Masafumi – Nissan Chemical Industries | ***5. 11:35 AM – Cu-Cu Wiring: The Novel Structure of Cu-Cu Hybrid Bonding***<br>Yoshihisa Kagawa, Takumi Kamibayashi, Nobutoshi Fujii, Shunsuke Furuse, Taichi Yamada, Tomoyuki Hirano, Hayato Iwamoto – Sony Semiconductor Solutions Corporation |
| ***6. 11:55 AM – Same Size Mold Chase Technology for Effective Stack Die Architectures***<br>Nabankur Deb, Xavier Brun, Yoshihiro Tomita – Intel Corporation; Chris Masuyama, Naoki Hamada, Yoshikazu Hirano – Towa Corporation | ***6. 11:55 AM – Novel Photosensitive Polyimides Compositions With Low Dielectric Property and Good Flexibility Corresponding to Redistribution Layers for Advanced Heterogeneous Integration Packages***<br>Takashi Tazaki, Takashi Yamaguchi, Taiyo Nakamura, Madoka Yamashita – Arakawa Chemical Industries, Ltd. | ***6. 11:55 AM – New Cu Bulge-Out Mechanism Supporting Sub-Micron Scaling of Hybrid Wafer-to-Wafer Bonding***<br>Jo De Messemaeker, Liesbeth Witters, Boyao Zhang, Ferenc Fodor, Joeri De Vos, Gerald Beyer, Kristof Croes, Eric Beyne – imec; Yan Wen Tsau – KU Leuven |
| ***7. 12:15 PM – A Novel Chiplet Integration Architecture Employing Pillar-Suspended Bridge With Polymer Fine-Via Interconnect***<br>Yasuhiro Morikawa – ULVAC, Inc.; Meiten Koh – Taiyo Ink Mfg. Co., Ltd.; Hiroyuki Hashimoto, Takafumi Fukushima – Tohoku University; Chuantong Chen, Wangyun Li, Katsuaki Suganuma – Osaka University; Ichiro Kono – AOI Electronics; Shinji Wakisaka – Oume Electronics; Ken Ukawa – Sumitomo Bakelite Co., Ltd.; Yoichiro Kurita – Tokyo Institute of Technology | ***7. 12:15 PM – High Frequency Characteristics of Fine Copper Lines on High Rigidity Dielectrics***<br>Masataka Nishida, Hirokazu Noma, Tetsuro Iwakura, Masaki Yamaguchi, Kazuyuki Mitsukura – Resonac Corporation | ***7. 12:15 PM – Electrical Analysis of Wafer-to-Wafer Copper Hybrid Bonding at Sub-Micron Pitches***<br>Kevin Ryan, Christopher Netzband, Adam Gildea, Yuji Mimura, Satohiko Hoshino, Ilseok Son, Hirokazu Aizawa, Kaoru Maekawa – TEL Technology Center, America, LLC |

# Program Sessions: Wednesday, May 31, 9:30 a.m. -12:35 p.m.

| Session 4: Assembly and Manufacturing Process Enhancement | Session 5: Flexible Packaging and Chip-Package-Interaction | Session 6: Co-packaged Optical Assembly |
|---|---|---|
| **Committee: Assembly and Manufacturing Technology** | **Committee: Thermal/Mechanical Simulation & Characterization** | **Committee: Photonics** |
| **Session Co-Chairs:**<br>**Rameen Hadizadeh**<br>**Cirrus**<br>**Email: rameen.hadizadeh@gmail.com**<br><br>**Christo Bojkov**<br>**Qorvo, Inc.**<br>**Email: cbojkov.ectc@gmail.com** | **Session Co-Chairs:**<br>**Xuejun Fan**<br>**Lamar University**<br>**Email: xuejun.fan@lamar.edu**<br><br>**Yong Liu**<br>**ON Semiconductor**<br>**Email: Yong.Liu@onsemi.com** | **Session Co-Chairs:**<br>**Ajey Jacob**<br>**University of Southern California**<br>**Email: ajey@isi.edu**<br><br>**Takaaki Ishigure**<br>**Keio University**<br>**Email: ishigure@appi.keio.ac.jp** |
| ***1. 9:30 AM – Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application***<br>Henry Antony Martin – Chip Integration Technology Center/Delft University of Technology; Marcia Reintjes, Xiao Tang – Mintres BV; Dave Reijs, Sander Dorrestein, Martien Kengen, Sebastien Libon, Edsger Smits, Marco Koelink – Chip Integration Technology Center; Rene Poelma, Willem Van Driel, GuoQi Zhang – Delft University of Technology | ***1. 9:30 AM – Comparative Study of Process-Reliability Interaction of Additive Circuits With Low-Temperature Solders ECAs and Magnetically Oriented ACAs***<br>Pradeep Lall, Jinesh Narangaparambil, Ved Soni – Auburn University; Scott Miller – NextFlex | ***1. 9:30 AM – A Heterogeneously Integrated Wafer-Level Processed Co-Packaged Optical Engine for Hyper-Scale Data Centres***<br>Sajay Bhuvanendran Nair Gourikutty, Boon Long Lau, Wen Wei Seit, Ming Chinq Jong, David Ho Soon Wee, Jiaqi Wu, Teck Guan Lim, Ser Choong Chong, Lai Yee Chia, Surya Bhattacharya – Institute of Microelectronics A*STAR; Li Xin, Tsung-Yang Liow – Rain Tree Photonics Pte. Ltd. |
| ***2. 9:50 AM – Optimum Rc Control and Productivity Boost in Wafer-Level-Packaging Enabled by High-Throughput UBM/RDL Technology***<br>Carl Drechsel, Patrik Carazzetti, Juergen Weichart, Ewald Strolz – Evatec AG; Carl Wang – Evatec AG, Taiwan; Kay Viehweger – Fraunhofer IZM | ***2. 9:50 AM – Addressing Sub-Micron Thermal Warpage: Industrial Application***<br>Safia Benkoula – STMicroelectronics; Rodolfo Cruz, Pierre Vernhes – INSIDIX | ***2. 9:50 AM – High Density Integration Technologies for SiPh Based Optical I/Os***<br>Karlheinz Muth, Hari Potluri, Sukesh Kannan – Broadcom, Inc. |
| ***3. 10:10 AM – Assembly Challenges and Approaches for 2.5D Chiplet Based System***<br>Sharon Pei Siang Lim, Mihai Dragos Rotaru, Wen Wei Seit, Hsiao Hsiang Yao – Institute of Microelectronics A*STAR | ***3. 10:10 AM – Study on the Mechanical Behavior of Stress Holes in Multilayer RDL Fabrication of 2.5D Packages Based on Finite Element Method***<br>Hu Zhen, Chen Haijie, Liu Haoyu, Xu Hong, Liu Tao, Zhang Jincheng, Wang Changwen, Xie Jielei, Guo Liang – JCET Advanced Packaging Co., Ltd. | ***3. 10:10 AM – Photonic System Integration by Applying Microelectronic Packaging Approaches Using Glass Substrates***<br>Henning Schroeder, Oliver Kirsch – Fraunhofer IZM; Daniel Weber – Technical University Berlin; Hendrick Thiem – TOPTICA eagleyard |
| ***Refreshment Break: 10:30 a.m.-11:15 a.m.*** | | |
| ***4. 11:15 AM – A Methodology to Optimize Dicing Parameters to Maximize Dicing Quality Through Machine Learning***<br>Aakrati Jain, Sathya Raghavan, Prabudhya Roy Chowdhury, Katsuyuki Sakuma – IBM Research; Roman Doll, Kees Biesheuvel, Faysal Boughorbel, Jeroen Van Borkulo, Mark Mueller – ASM Laser Separation International B.V. | ***4. 11:15 AM – Strain-Relief Patterns for Flexible Substrate-Supported Optimized Serpentine Configurations***<br>Rui Chen, Colin Stewart, Suresh Sitaraman – Georgia Institute of Technology | ***4. 11:15 AM – CPO on Glass for 102.4 Tb/s DC Switches***<br>Lucas Yeary, Lars Brusberg, Seong-ho Seok, Jung-Hyun Noh, Alon Rozenvax, Cheolbok Kim – Corning, Inc. |
| ***5. 11:35 AM – Maskless Lithography for High-Density Package Redistribution Layers***<br>Prahalad Murali, Pratik Nimbalkar, Mohanalingam Kathaperumal, Mark D. Losego, Rao Tummala, Madhavan Swaminathan – Georgia Institute of Technology | ***5. 11:35 AM – Modeling and Measurement Correlation of the Impact of Underfill Filler Particle Density on Interfacial Delamination***<br>Yutaka Suzuki, Jaimal Williamson, Li Jiang, Rajen Murugan – Texas Instruments, Inc. | ***5. 11:35 AM – Innovative Fan-Out Embedded Bridge Structure for Co-Packaged Optics***<br>Jay Li, Sam Lin, Teny Shih, Nicholas Kao, Yu-Po Wang – Siliconware Precision Industries Co., Ltd., Ming-An Yang – Quanta Computer Co., Ltd. |
| ***6. 11:55 AM – Exploring an Additive Approach to Embed Chips in Metallic Matrix Inside a Printed Circuit Board***<br>Roberto Aga, Fahima Ouchen – KBR, Inc./U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL | ***6. 11:55 AM – A Time and Cost-Efficient Design Methodology to Estimate Effective Thermal Conductivities in System-on-Chips With Composite Materials***<br>Ki Wook Jung, Eunju Hwang, Jun Seomun, Sangyn Ed Kim – Samsung Electronics Co., Ltd.-Foundry Business | ***6. 11:55 AM – AIM Photonics Demonstration of a 300 mm Si Photonics Interposer***<br>Colin McDonough, Seth Kruger, Tat Ngai, Sarah Baranowski, David L. Harame – SUNY Research Foundation/SUNY Polytechnic Institute; Hao Yang, Skylar Deckoff-Jones, Christopher V. Poulton, Michael R. Watts – Analog Photonics |
| ***7. 12:15 PM – Micro Transfer Printing 100 µm Thick Components Directly from Dicing Tape***<br>Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd. | ***7. 12:15 PM – On the Effect of Partial Underfilling on the Fatigue Life of Flip-Chip Micro-Solder Bumps in a Heterogeneously Integrated TSI Package Using Finite Element Simulations***<br>Sasi Kumar Tippabhotla, Ji Lin – Institute of Microelectronics A*STAR | ***7. 12:15 PM – Advanced 3D Integration TSV and Flip Chip Technologies for Cost-Effective and Miniaturized Packaging of a 256 Channels Optical-Phased Array Based Beam Steering System Designed for Automotive LiDARs***<br>Thierry Mourier, Nadia Miloud-Ali, Natacha Raphoz, Yacoub Sahouane, Patrick Peray, Damien Saint Patrice, Edouard Deschaseaux – CEA-Leti; Francois Simoens – Steerlight |

# Program Sessions: Wednesday, May 31, 2:00 p.m. - 5:05 p.m.

## Session 7: Large Formfactor Dense System Integration by Fan-Out

**Committee:**
**Packaging Technologies**

**Session Co-Chairs:**
**Steffen Kroehnert**
**ESPAT Consulting, Germany**
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**Bora Baloglu**
**Intel Corporation**
**Email: bora.baloglu@intel.com**

***1. 2:00 PM – 3D Freeform Antenna-in-Package Approach for FOWLP***
Tanja Braun, Tina Thomas, Karl-Friedrich Becker, Thi Huyen Le, Christian Tschoban, Rolf Aschenbrenner – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin

***2. 2:20 PM – High-Speed Performance Validation Testing of Die-to-Die Interconnects in High-Density Fan-Out Package***
Cindy Muir, Carlton Hannah, Bernd Waidhas, Abdallah Bacha, Hui Zhang – Intel Corporation

***3. 2:40 PM – Extremely Large Area Integrated Circuit (ELAIC): An Advanced Packaging Solution for Chiplets***
Rabindra Das, Jason Plant, Alex Wynn, Matthew Ricci, Ryan Johnson, Matthew Stamplis, Brian Tyrrell, Kenneth Schultz, Paul Juodawlkis – MIT Lincoln Laboratory

***4. 3:45 PM – Advanced Fan-Out Panel Level Package (FO-PLP) Development for High-End Mobile Application***
Hyungmin Kim, Jaehoon Choi, Seok Won Lee, Eun Seok Cho, Hwasub Oh, Junho Lee, Seungsu Ha, Wonkyung Choi, Dong Wook Kim – Samsung Electronics Co., Ltd.

***5. 4:05 PM – Integrating Chiplets Using Chips First Ultra-High-Density Fan-Out With Maskless Laser Direct Imaging and Adaptive Patterning for High Performance Computing***
Benedict San Jose, Cliff Sandstrom, Erick Talain, Jan Kellar, Tim Olson – Deca Technologies, Inc.; Mary Maye Melgo, Rizi Gacho, Byung Cheol Kim – Nepes Hayyim Corporation

***6. 4:25 PM – Reliability Challenges of Large Organic Substrate With High-Density Fan-Out Package***
Rosa Lin, Laurene Yip, Charles Lai, Cooper Peng – MediaTek, Inc.

***7. 4:45 PM – Flip Chip Process Enablement in DRAM Stacked Die Package***
Chen-Yu Huang, Tsung-Han Chiang, Jungbae Lee, Kohan Lin, Chong-Leong Gan – Micron Memory Taiwan, Co., Ltd.; Travis Jensen – Micron Technology, Inc.

## Session 8: Novel Reliability Test Methods

**Committee:**
**Applied Reliability**

**Session Co-Chairs:**
**S. B. Park**
**Binghamton University**
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**Sandy Klengel**
**Fraunhofer IMWS**
**Email: sandy.klengel@imws.fraunhofer.de**

***1. 2:00 PM – A New Vibration Test Method for Automotive and Consumer Electronic Devices: Calibration and Fatigue Test***
Dongji Xie, Joe Hai – Nvidia Corporation; Andy Zhang – Texas Instruments, Inc.; Jeffrey Lee – iST-Integrated Service Technology, Inc.; Romuald Roucou – NXP Semiconductor, Inc.; Xue Shi – Bosch Automotive Products Co., Ltd.; Sushil Doranga – Lamar University; Valeriy Khaldarov – ASONIKA, LLC

***2. 2:20 PM – Magnetic Force-Based Measurement Technique to Investigation the Effect of Lead-Free Solder Intermetallic Compounds (IMC) on Interconnect Reliability***
Rui Chen, Suresh Sitaraman – Georgia Institute of Technology; Nicholas Ginga – University of Alabama in Huntsville

***3. 2:40 PM – Residual Stress Measurement of Build-Up Layer in Silicon Wafers***
Junbo Yang, Chongyang Cai, Yangyang Lai, Jong Hwan Ha, Seungbae Park – Binghamton University; Huayan Wang, Suresh Ramalingam, Gamal Refai-Ahmed – Advanced Micro Devices, Inc.

***4. 3:45 PM – Chip Level Evaluation of Wafer-to-Wafer Direct Bonding Strength With Bending Test***
Juno Kim, Kyungmin Baek, Min-soo Han, Kyeongbin Lim, Minwoo Daniel Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research

***5. 4:05 PM – In-Situ Observation of Microscale Crack-Tip Strain Field Evolution in Underfill With Different Toughening Agents and Temperatures Via SEM-DIC Coupled Method***
Xuecheng Yu, Gang Li, Yixuan Fan, Rong sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology

***6. 4:25 PM – Experimental Identification of the Failure Modes and Failure Mechanisms of Fiber Arrays Under Cyclic Tensile Loading***
Assane Dione, Jean-Francois Morissette, Julien Sylvestre, Patrick Jacques – University of Sherbrooke; Richard Langlois, Papa Momar Souare – IBM Canada, Ltd.

***7. 4:45 PM – A Predictive Metallographic Means to Identify the Relative Risk of Failure for Plated Micro Vias***
Roger Massey, Tobias Bernhard, Kilian Klaeden, Sebastian Zarwell, Edith Steinhaeuser, Sascha Dieter, Stefan Kempa, Frank Bruening – MKS Atotech

## Session 9: Innovations in Copper Chip-to-Wafer Bonding

**Committee:**
**Interconnections**

**Session Co-Chairs:**
**Wei-Chung Lo**
**Industrial Technology Research Institute**
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**Ou Li**
**Advanced Semiconductor Engineering, Inc.**
**Email: ou.li@aseus.com**

***1. 2:00 PM – Solderless Interconnection Studies for Advanced Memory Chip-to-Wafer Stacking***
Wei Zhou, Bharat Bhushan, Yingta Chiu, Ava Yang, Huimin Guo, Bret Street, Kunal Parekh, Akshay Singh – Micron Technology, Inc.

***2. 2:20 PM – Development of Copper Thermal Coefficient for Low Temperature Hybrid Bonding***
Sefa Dag, Liu Jiang, Amir Kiaee, Ying Wang, Prayudi Lianto, Jinho An, Ruiping Wang, Gilbert See, Arvind Sundarrajan, El Mehdi Bazizi, Buvna Ayyagari-Sangamalli – Applied Materials, Inc.

***3. 2:40 PM – Impact of Plasma Activation on Copper Surface Layer for Low Temperature Hybrid Bonding***
Christopher Netzband, Kandabara Tapily, Dylan Burns, Ilseok Son, Cory Wajda – TEL Technology Center, America, LLC

***4. 3:45 PM – Investigation of Cu-Cu Direct Bonding Process Utilized by High Porosity and Nanocrystal Structure***
Takuma Nakagawa, Daiki Furuyama, Sho Nakagawa, Yutaro Mori, Kotaro Iwata, Kiyotaka Nakaya, Takuma Katase – Mitsubishi Materials Corporation

***5. 4:05 PM – A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration***
Krutikesh Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

***6. 4:25 PM – Optimization of Cu Interconnects - SiCN Interfacial Adhesion by Surface Treatments***
Dong Jun Kim, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sumin Kang – Korea Institute of Machinery and Materials; Sun Woo Lee, Inhwa Lee, Seungju Park, Jun Soo Lee, Jihyun Lee, Joong Jung Kim – Samsung Electronics Co., Ltd.

***7. 4:45 PM – Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration***
Madison Manley, Ming-Jui Li, Muhannad S. Bakir – Georgia Institute of Technology; Zachary Deveraux, Nyi Myat Khine Linn, Charles Winter – Wayne State University; Andrew Kummel – University of California, San Diego

***Refreshment Break: 3:00 p.m. - 3:45 p.m.***

# Program Sessions: Wednesday, May 31, 2:00 p.m. - 5:05 p.m.

## Session 10: Packaging Interconnects

**Committee: Thermal/Mechanical Simulation & Characterization**

**Session Co-Chairs:**
**Suresh K. Sitaraman**
**Georgia Institute of Technology**
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**Jiamin Ni**
**IBM Corporation**
**Email: nijiamin8910@gmail.com**

***1. 2:00 PM – Finite Element Analysis of Shock and Vibration of a Printed Circuit Board With Multiple Ball-Grid-Array Packages Using Beam Elements to Model the Solder Joints to Achieve Design-for-Reliability***
Tieyu Zheng – Microsoft Corporation; Babu Aminjikarai – ANSYS, Inc.

***2. 2:20 PM – Modeling and Optimization of Mechanical Performance for Cu Wire Bonding Process***
Liangbiao Chen, Yong Liu – ON Semiconductor

***3. 2:40 PM – High-Temperature Creep Properties of Solder Interconnects (SnBiAgCu) and Its Thermal Fatigue Properties Under Different Potting Compounds***
Leiming Du, Guoqi Zhang – Delft University of Technology; Xiujuan Zhao, Willem Van Driel – Signify; Rene Poelma – Nexperia

## Session 11: Additive Manufacturing and Packaging for Flexible Electronics

**Committee: Emerging Technologies**

**Session Co-Chairs:**
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**Dishit Parekh**
**Intel Corporation**
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***1. 2:00 PM – Electromechanical and Thermal Characterization of Printed Liquid Metal Ink on Stretchable Substrate for Soft Robotics Multi-Sensing Applications***
El Mehdi Abbara, Mohammed Alhendi, Riadh Al-haidari, Nathaniel Gee, Mark Poliks – Binghamton University; Emily Boggs, Tan Yewteck, Deepak Trivedi – GE Research; Christopher Tabor – AFRL

***2. 2:20 PM – Electrochemical Additive Manufacturing: A Novel Approach to Thermal Management of Electronics***
Ian Winfield, Joseph Madril, Madeline Frank, Michael Matthews – Fabric8Labs

***3. 2:40 PM – Additively Manufactured Flexible Material Characterization and On-Demand Smart Packaging Topologies for 5G/mmWave Wearable Applications***
Kexin Hu, Yi Zhou, Suresh Sitaraman, Manos Tentzeris – Georgia Institute of Technology

## Session 12: mm Wave Antenna-in-Package and Arrays

**Committee: RF, High-Speed Components & Systems**

**Session Co-Chairs:**
**Jaemin Shin**
**Qualcomm Technologies, Inc.**
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**Yong-Kyu Yoon**
**University of Florida**
**Email: ykyoon@ece.ufl.edu**

***1. 2:00 PM – A Scalable Heterogeneous AiP Module for a 256-Element 5G Phased Array***
Duixian Liu, Xiaoxiong Gu, Christian Baks, Arun Paidimarri, Atom Watanabe, Alberto Valdes-Garcia – IBM Corporation; Koichiro Masuko, Yujiro Tojo, Gokul Chandran, Yuta Hasegawa, Xu Lei, Ning Guan – Fujikura, Ltd.

***2. 2:20 PM – Metamaterial Based Compact Patch Antenna Array for Antenna-in-Package Solutions in Frequency Handover Applications***
Payman Pahlavan, Suk-il Choi, Alexander Wilcher, Hae-in Kim, Hanna Jang, Yong-Kyu Yoon – University of Florida

***3. 2:40 PM – A Low-Cost Antenna-in-Package (AiP) for D-Band Application***
Hung-Chun Kuo, Po-I Wu, Sheng-Chi Hsieh, Ming-Fong Jhong, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

## Refreshment Break: 3:00 p.m. - 3:45 p.m.

***4. 3:45 PM – A Novel Stacked-Via Cu/ELK Interconnection Design Configuration to Enhance Advanced Si Package Reliability Performance***
Kuo-Chin Chang, Mirng-Ji Lii, Chieh-Hao Hsu, Wei-Hsiang Tu, Tai-Shen Yang – Taiwan Semiconductor Manufacturing Company, Ltd.

***5. 4:05 PM – Sustainable-Ink Process Recipes for the Fabrication of Additively Printed Circuits and Component Attachment***
Pradeep Lall, Jinesh Narangaparambil, Ved Soni, Shriram Kulkarni, Kartik Goyal – Auburn University; Scott Miller – NextFlex

***6. 4:25 PM – New Methodology Assessment of Copper Trace and Solder Joint Fatigue Failures in Board-Level Random Vibrations for Automotive Applications***
Valeriy Khaldarov, Alexander Shalumov – ASONIKA, LLC; Andy Zhang – Texas Instruments, Inc.; Dongji Xie, Minghong Jian – Nvidia Corporation; Jeffrey Lee – iST-Integrated Service Technology, Inc.; Xue Shi – Bosch Automotive Products Co., Ltd.; Romuald Roucou – NXP Semiconductor, Inc.; Sushil Doranga – Lamar University

***7. 4:45 PM – Physics-Driven Regression Algorithm on Solder Joint Fatigue Life Prediction for Mobile SiP Packages***
Faxing Che, Yeow Chon Ong, Hong Wan Ng, Ling Pan, Christopher Glancey, Gokul Kumar – Micron Semiconductor Asia Operations Pte. Ltd; Koustav Sinha – Micron Technology, Inc.

***4. 3:45 PM – Advanced Packaging Methods Used for Energy Storage From Intermittent Renewable Sources***
Takafumi Fukushima – Tohoku University; Tianyu Xiang, Harshit Ranjan, Niharika Tripathi, Randall Irwi, Subramanian S. Iyer – University of California, Los Angeles

***5. 4:05 PM – Advances in Conductive Features in Digitally Manufactured Electronics***
Bryce Gray, Jason Benoit, Mark Kloza, Kenneth Church – Sciperio

***6. 4:25 PM – Adhesion and Reliability Studies of the Homogeneous Integration of Conductive L.S.R. and Other Components on SIP for Bio Sensing Applications***
ChihLung (Steven) Lin, Pang Yuan Lee, Kueihao Tseng, Jenjun Chen, Harrison Chang – Advanced Semiconductor Engineering, Inc.

***7. 4:45 PM – Evaluation of Screen Printing Process in Fabrication of Small Profile Conductive Ink-Based Contact Force Sensor***
Maria Ramona Ninfa Bautista Damalerio, Ruiqi Lim, Ven Wee James Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR; Ran Young Lim – Kalos Medical, Inc.

***4. 3:45 PM – A New Millimeter-Wave Package Design Based on Pseudo-Cavity Mode Electromagnetic Wave Excitation Using 400 µm Core FCBGA***
Ryuichi Oikawa, HIDEKI SASAKI – Renesas Electronics Corporation

***5. 4:05 PM – 5G mmWave Patch Antenna Array on Extremely Low Loss Alumina Ribbon Ceramic Substrates for Antenna-in-Package (AiP)***
Cheolbok Kim, Hoon Kim, Rajesh Viddi, Eun Ju Moon, David Peters – Corning, Inc.

***6. 4:25 PM – A Novel Approach to Measure and Characterize Radiation Patterns of Antenna-in-Package***
Aditya Jogalekar, Oscar Medina, Rashaunda Henderson – University of Texas, Dallas; Mahadevan Iyer – Amkor Technology, Inc.; Rajen Murugan, Harshpreet Bakshi, Hassan Ali – Texas Instruments, Inc.

***7. 4:45 PM – Design and Fabrication of A Sub-THz Co-Reflectively Curved Patch-Reflector Antenna Array for Gain Enhancement and Near Field Focusing***
Ching-Jen Lee, Pin-Cheng Tseng, Wei-Chian Wang, Yun-Hao Liou, Yu-Ting Cheng, Chien-Nan Kuo – National Yang Ming Chiao Tung University

# Program Sessions: Thursday, June 1, 9:30 a.m. -12:35 p.m.

| Session 13: Wafer/Panel-Level and Advanced Substrate Technologies | Session 14: Advances in Heterogeneous Integration Bonding Technology | Session 15: Innovative Interposer and Through-Via Technologies |
|---|---|---|
| **Committee:**<br>**Packaging Technologies** | **Committee:**<br>**Materials & Processing** | **Committee:**<br>**Interconnections** |
| **Session Co-Chairs:**<br>**Markus Leitgeb**<br>**AT&S AG**<br>**Email: m.leitgeb@ats.net**<br><br>**Dean Malta**<br>**Micross Advanced Interconnect Technology**<br>**Email: Dean.Malta@micross.com** | **Session Co-Chairs:**<br>**Jae Kyu Cho**<br>**GlobalFoundries, Inc.**<br>**Email: jaekyu.cho@globalfoundries.com**<br><br>**Qianwen Chen**<br>**IBM Research**<br>**Email: chenq@us.ibm.com** | **Session Co-Chairs:**<br>**C. Key Chung**<br>**TongFu Microelectronics Co., Ltd**<br>**Email: chungckey@hotmail.com**<br><br>**Chuan Seng Tan**<br>**Nanyang Technological University**<br>**Email: tancs@alum.mit.edu** |
| ***1. 9:30 AM – Supercarrier Redistribution Layer to Realize Ultra High Performance 2.5D Wafer Scale Packaging by CoWoS***<br>S.Y. Hou, Chien Hsun Lee, Tsung Ding Wang, Hao Cheng Hou – Taiwan Semiconductor Manufacturing Company, Ltd. | ***1. 9:30 AM – Characterization of 300 mm Low Temperature SiCN PVD Films for Hybrid Bonding Application***<br>Xavier Brun, Md M. Hasan – Intel Corporation; Patrick Carazzetti, Carl Drechsel, Ewald Strolz – Evatec AG | ***1. 9:30 AM – Assembly-Based Through-X-Via (TXV) Integration Technology by Advanced Fan-Out Wafer-Level Packaging***<br>Atsushi Shinoda, Chang Liu, Tadaaki Hoshi, Jiayi Shen, Yuki Susumago, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima – Tohoku University |
| ***2. 9:50 AM – Development of Fine Pitch Backside Redistribution Layer (BRDL) Process in Fan-Out Panel Level Packaging (FOPLP)***<br>Hyunju Lee, Sung Keun Park, Jaemok Jung, Kwangok Jung, Ju-il Choi, Un-Byoung Kang, Dongwoo Kang – Samsung Electronics Co., Ltd. | ***2. 9:50 AM – Inorganic Temporary Direct Bonding for Collective Die to Wafer Hybrid Bonding***<br>Fumihiro Inoue, Tomoya Iwata, Koki Onishi – Yokohama National University; Shunsuke Teranishi, Naoko Yamamoto, Akihito Kawai – DISCO Corporation; Shimpei Aoki, Takashi Hare – Toray Engineering Co., Ltd.; Akira Uedono – University of Tsukuba | ***2. 9:50 AM – Three Dimensional Fan-Out Wafer-Level Packaging***<br>Guangqi Ouyang, Fukushima Takafumi, Subramanian S. Iyer – University of California, Los Angeles |
| ***3. 10:10 AM – Fabrication of Two-types Full Panel-Sized Interposers With Fine Cu Wirings and Outstanding Electrical Reliability***<br>Masaya Toba, Masashi Minami, Daisuke Yamanaka, Kazuyuki Mitsukura – Resonac Corporation | ***3. 10:10 AM – Cu Damascene Process on Temporary Bonded Wafers for Thin Chip Stacking Using Cu-Cu Hybrid Bonding***<br>Nagendra Sekhar Vasarla, Dileep Kumar Mishra, Ser Choong Chong, Srinivasa Rao Vempati – Institute of Microelectronics A*STAR; Prayudi Lianto – Applied Materials Singapore | ***3. 10:10 AM – Study of High-Speed Interconnect Bridge (HSIB) for System-in-Package Application***<br>Venkata Karthik Ceemakurthy – TU Chemnitz/ Fraunhofer ENAS; Vikas Dubey, Dirk Wuensch, Maik Wiemer, Harald Kuhn – Fraunhofer ENAS |
| ***Refreshment Break: 10:30 a.m.-11:15 a.m.*** | | |
| ***4. 11:15 AM – Warpage Modulation for Panel-Level Compression Molding Technology for Heterogeneous Integration Packaging Architectures***<br>Liang He, Jason Xie, Shishir Deshpande, Andrew Jimenez, Jung Kyu Han, Gang Duan, Rahul Manepalli – Intel Corporation | ***4. 11:15 AM – A New Adhesive for CoW Cu-Cu Hybrid Bonding With High Throughput and Room Temperature Pre-Bonding***<br>Yasuhisa Kayaba, Yuzo Nakamura, Wataru Okada, Takuo Shikama, Kahori Tamura, Satoshi Inada – Mitsui Chemicals, Inc. | ***4. 11:15 AM – Integrated Optical Interconnect Systems (iOIS) for Si Photonics Applications in HPC***<br>Harry Hsia, C.W. Tseng, Chih-Chieh Chang, Jiun Yi Wu, Shih-Peng Tai, S. W. Lu, Jason Wu, Chih-Hang Tung, C. S. Liu, Yutong Wu, K. C. Yee, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd. |
| ***5. 11:35 AM – ASE Fan-Out Panel Level Package Die-Shift Solutions***<br>Ping Ching Shen, Sheng Feng Huang, Ping Feng Yang, Jen Kuang Fang – Advanced Semiconductor Engineering, Inc. | ***5. 11:35 AM – Low-Temperature and Pressureless Cu-to-Cu Bonding by Electroless Pd Plating Using Microfluidic System***<br>Po-Shao Shih, Jeng-Hau Huang, Chang-Hsien Shen, Yu-Chun Lin, Simon Johannes Graefner, Vengudusamy Renganathan, C. Robert Kao – National Taiwan University; Chin-Li Kao, Yung-Sheng Lin, Yun-Ching Hung, Chun-Wei Chiang – Advanced Semiconductor Engineering, Inc. | ***5. 11:35 AM – Demonstration of a CMOS-Compatible, Superconducting Cryogenic Interposer for Advanced Quantum Processor***<br>King Jien Chui, Yong Chyn Ng, Ya-Ching Tseng, Hongyu Li – Institute of Microelectronics A*STAR |
| ***6. 11:55 AM – Thermal and Mechanical Characterization of Fan-Out Panel Level Packages by Use of Embedded Packaging Test Chips***<br>Gerald Weis, Timo Schwarz, Johannes Stahr, Andreas Zluc – AT&S AG; Vladimir Cherman, Geert Van der Plas – imec | ***6. 11:55 AM – Volume-Controllable Solder Bumping Technology to Package Substrate Using Injection Molded Solder for Fine-Pitch Flip Chip***<br>Toyohiro Aoki, Hiroyuki Mori, Koki Nakamura, Takashi Hisada – IBM Research, Tokyo; Katsuyuki Sakuma – IBM Research | ***6. 11:55 AM – Process Design Kit and Initial Demonstration of Digital Metal-Embedded Chip Assembly for High Density IO Fan-Out Packaging***<br>Souheil Nadri, Bor-An Clayton Tu, Hasan Sharifi, Daniel Kuzmenko, Joel Wong, Vu Phan, Courtney Wilt – HRL Laboratories, LLC; Florian Herrault – PseudolithIC, Inc.; Abdullah Khan, David Schwan, David Botticello, Sanjana Das – Cadence |
| ***7. 12:15 PM – Reliability of Heterogeneous Integration on Hybrid Substrate With Ajinomoto Build-Up Film™***<br>Channing Yang, John Lau, Gary Chen, Jones Huang, YH Chen, T. J. Tseng – Unimicron Technology Corp.; Ming Li – ASM Pacific Technology, Ltd. | ***7. 12:15 PM – Effects of Room Temperature Laser-Assisted Bonding (LAB) Process on Microstructure and Reliability of Solder Joints***<br>Yoon Hwan Moon, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, In-Seok Kye, Yong-Sung Eom, Kwang-Seong Choi – Electronics Telecommunications Research Institute; Yong-Jun Oh – Hanbat National University | ***7. 12:15 PM – 1.65 µm L/S High Density Interconnect on Organic Substrate by Advanced Semi-Additive Process for HPC Applications***<br>Hussein Hamieh, Juliano Borges, Etienne Paradis, Yann Beilliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa, Martin Laliberte – IBM Canada, Ltd. |

# Program Sessions: Thursday, June 1, 9:30 a.m. -12:35 p.m.

## Session 16: Sintering and Soldering for High-Power, High-Reliability, and RF Devices

**Committees: Assembly and Manufacturing Technology and Materials & Processing**

**Session Co-Chairs:**
**Mark Poliks**
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**Omkar Gupte**
**Advanced Micro Devices, Inc.**
**Email: Omkar.Gupte@amd.com**

***1. 9:30 AM – Understanding the Influence of Copper Substrate Oxidation on Silver Pressure Sintering Performance***
Tamira Stegmann, Andre Schwoebel, Wolfgang Schmitt, Stefan Gunst – Heraeus Germany GmbH & Co. KG; Karsten Durst – Technical University Darmstadt; Nils Neugebauer, Peter Klar – Justus Liebig University of Giessen

***2. 9:50 AM – Mechanical, Electrical and Thermal Reliability Analysis of Cu Sintered Die-Attach SiC Power Device***
Xu Liu, Shaogang Wang, Dong Hu, Guoqi Zhang – Delft University of Technology; Hai Chi, Qian-Ming Huang, Huaiyu Ye – Southern University of Science and Technology

***3. 10:10 AM – Functional Thermal Imaging and Effect of Temperature on Liquid Thermal Interface Material (LTIM) for Solid State Drive***
Vigneshwarram Kumaresan, Mutharasu Devarajan – Western Digital Corporation

***4. 11:15 AM – Risk Assessment of Hybrid Low Temperature Solder on Surface Mount Technology and Board Level Reliability for BGA Packages***
Jihyun Lee, Yongsung Park, Junho Lee, Hansung Ryu, JeeHyun Jung, Kangjoon Lee, Kilsoo Kim – Samsung Electronics Co., Ltd.

***5. 11:35 AM – An In-Containing Lower-Temperature Lead-Free Solder Paste for Wafer-Level Package Application that Outperforms SAC305***
Hongwen Zhang, Tyler Richmond, Huaguang Wang – Indium Corporation

***6. 11:55 AM – High Performance Gallium 68.5-Indium 21.5-Tin 10 Eutectic Alloy Based Thermal Interface Material Incorporating Porous Cu Layer***
Jang Baeg Kim, Dong Gil Kang, Tae Joon Noh, Sea Hwan Kim, Seung-Boo Jung – Sungkyunkwan University

***7. 12:15 PM – Influence of Microscale Tin Particles on Mechanical Properties of Silver Sintering Joints With Reduced Processing Parameters***
Steffen Hadeler, Yangyang Long, Rico Ottermann, Folke Dencker, Jens Twiefel, Marc Christopher Wurz – Leibniz University

## Session 17: Advanced Reliability Modelling and Characterization

**Committees: Thermal/Mechanical Simulation & Characterization and Applied Reliability**

**Session Co-Chairs:**
**Wei Wang**
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**Tz-Cheng Chiu**
**National Cheng-Kung University**
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***1. 9:30 AM – Fully Coupled Electromigration Modeling Using Peridynamics in Ansys Framework***
Yanan Zhang, Sundaram Vinod Anicode, Erdogan Madenci – University of Arizona; Xuejun Fan – Lamar University

***2. 9:50 AM – Predicting Reliability Behavior in HBM Packages Through Numerical Simulation***
Sangkun O, Jongpa Hong, Sangmin Lee, Seoeun Kyung, Junho Lee, Kilsoo Kim, Jihyun Park, Dan Oh – Samsung Electronics Co., Ltd.

***3. 10:10 AM – Distortion Simulation for Direct Wafer-to-Wafer Bonding Process***
Nathan Ip, Nima Nejadsadeghi – Tokyo Electron America, Inc.; Norifumi Kohama, Hayato Tanoue, Kimio Motoda – Tokyo Electron Kyushu, Ltd.

***4. 11:15 AM – Substrate Copper Trace Crack Characterization and Simulation***
Wei Yu, Faxing Che, Yeow Chon Ong, Hong Wan Ng – Micron Semiconductor Asia Operations Pte. Ltd; Vance Liu, Milly Lin, Jay Lin – Micron Memory Taiwan Co., Ltd.; Brad Rumsey – Micron Technology, Inc.

***5. 11:35 AM – Design-for-Manufacturing and Design-for-Reliability Strategies for Large 80mm+ 2.5D Devices***
Peng Su, Omar Ahmed, Leif Hutchinson, Bernard Glasauer, Gautam Ganguly – Juniper Networks

***6. 11:55 AM – A Continuum Damage Mechanics Approach for the Reliability of Lead-Free Solders Subjected to Cyclic Loading***
Golam Rakib Mazumder, Mohammad Ashraful Haq, Jeffrey Suhling, Pradeep Lall – Auburn University; Yaxiong Chen, Torsten Hauck, Abdullah Fahim – NXP Semiconductor, Inc.

***7. 12:15 PM – A Quantitative Evaluation of the Inelastic Energy Absorptions in Cu-Polyimide Interconnect and the Effect on Interface Debond Driving Force***
Chien-Yu Wang, Tz-Cheng Chiu – National Cheng-Kung University; Wei-Jie Yin, Dao-Long Chen, Tang-Yuan Chen, Chin-Li Kao – Advanced Semiconductor Engineering, Inc.

## Session 18: Advanced Photonic Packaging and Interconnect

**Committee: Photonics**

**Session Co-Chairs:**
**Richard Pitwon**
**Resolute Photonics, Ltd.**
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**Soon Jang**
**ficonTEC USA**
**Email: soon.jang@ficontec.com**

***1. 9:30 AM – Backside Optical Coupler: A Novel I/O for Mechanically Stable High Efficiency Fiber Coupling***
Sugeet Sunder, Akhilesh Jaiswal, Ajey Jacob – University of Southern California

***2. 9:50 AM – Demonstration of Planar Silicon Photonics Integrated Circuit (PIC) Using Micro-Transfer-Printed (MTP) Lasers and Modulators***
Roshanak Shafiiha, Aaron Zilkie – Rockley Photonics; Clint Schow, Xinhong Du, Viviana Arrunategui-Norvick, Yujie Xia – University of California, Santa Barbara

***3. 10:10 AM – Low-Cost, HVM Singulation of Silicon Photonic ICs For Low-Loss Waveguide-to-Fiber Array Edge Coupling***
Hiren Thacker, Tong Wang, Steve Moyer, Mary Nadeau, Sandeep Razdan, Ginni Chadha – Cisco Systems, Inc.

***4. 11:15 AM – Packaging of Ultra-Dynamic Photonic Switches and Transceivers for Integration Into 5G Radio Access Network and Datacenter Sub-Systems***
Geert Van Steenberge, Gunther Roelkens, Peter Ossieur, Jeroen Missinne – imec/Ghent University; Joris Van Campenhout – imec; Milan M. Milosevic – PHIX Photonics Assembly; Paraskevas Bakopoulos – NVIDIA; Igor Krestnikov – Innolume; Stefano Stracca – Ericsson Research; Tanja Joerg – AT&S AG; Tanja Braun – Fraunhofer IZM; Qixiang Cheng – Cambridge University

***5. 11:35 AM – Scalable Fiber-Array-to-Chip Interconnections With Sub-Micron Alignment Accuracy***
Shengtao Yu, Muhannad S. Bakir, Thomas Gaylord – Georgia Institute of Technology

***6. 11:55 AM – Realization, Multi-Field Coupled Simulation and Characterization of a Thermo-Mechanically Robust LiDAR Front End on a Copper Coated Glass Substrate***
Marcel Kettelgerdes, Amit Pandey, Gordon Elger – Technical University of Applied Science Ingolstadt; Peter Meszmer, Majid Tavakolibasti, Bernhard Wunderle – Chemnitz University of Technology; Gunnar Boettger, Michael Johannes Haeusler – Fraunhofer IZM; Hueseyin Erdogan – Continental AG; Ralph Schacht – Brandenburg University of Technology

***7. 12:15 PM – Cavity-Resonator-Integrated Guided-Mode-Resonance Mirrors for Hybrid Integration of Wavelength-Division-Multiplexed Light Source***
Akari Watanabe, Shunsuke Teranishi, Keisuke Ozawa, Aika Taniguchi, Junichi Inoue, Shogo Ura – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology

***Refreshment Break: 10:30 a.m.-11:15 a.m.***

# Program Sessions: Thursday, June 1, 2:00 p.m. - 5:05 p.m.

## Session 19: Advances in 3D Integration and Hybrid Bonding

**Committee:**
**Packaging Technologies**

**Session Co-Chairs:**
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**Juniper Networks**
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**Jaesik Lee**
**Meta Platforms, Inc.**
**Email: jaesiklee@fb.com**

***1. 2:00 PM – Thermal Improvement of HBM With Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond***
Taehwan Kim, Youngdeuk Kim, Heejung Hwang, Hwanjoo Park, Jaechoon Kim, Dan (Kyung Suk) Oh – Samsung Electronics Co., Ltd.

***2. 2:20 PM – Electrical and Thermal Analysis of Bumpless Build Cube (BBCube) 3D Using Wafer-on-Wafer (WOW) and Chip-on-Wafer (COW) for Near Memory Computing***
Norio Chujo – Hitachi Research & Development Group/Tokyo Institute of Technology; Hiroyuki Ryoson, Tomoji Nakamura, Koji Sakui, Shinji Sugatani, Takayuki Ohba – Tokyo Institute of Technology

***3. 2:40 PM – 2.5D MCM (Multi-Chip Module) Technology Development for Advanced Package***
Laurene Yip, James Tsai, Rosa Lin, Ian Hsu – MediaTek, Inc.

***4. 3:45 PM – Reliability Performance on Low Temperature Fine-Pitch SoICTM Bond***
Shih-Wei Liang, Y. R. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

***5. 4:05 PM – Development of 4 Die Stack Module Using Hybrid Bonding Approach***
Ser Choong Chong, Au Keng Yuen, Jason, Nagendra Sekhar Vasarla, Ismael Daniel Cereno, Srinivasa Rao Vempati – Institute of Microelectronics A*STAR

***6. 4:25 PM – Impact of Dielectric Types and Surface Profile on Wafer-to-Wafer Hybrid Bonding***
Vikas Dubey, Dirk Wuensch, Knut Gottfried, Tobias Fischer, Maik Wiemer, Harald Kuhn – Fraunhofer ENAS

***7. 4:45 PM – Voids-Free Die-Level Cu/ILD Hybrid Bonding***
Katsuyuki Sakuma – IBM Research; Roy Yu, John Knickerbocker, Dale McHerron, Ming Li, Siu Cheung So, So Ying Kwok, Chun Ho Fan, Siu Wing Lau – ASM Pacific Technology, Ltd.

## Session 20: Automotive/Board-Level Reliability

**Committee:**
**Applied Reliability**

**Session Co-Chairs:**
**Paul Tiner**
**Texas Instruments, Inc.**
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**Varughese Mathew**
**NXP Semiconductor, Inc.**
**Email: varughese.mathew@nxp.com**

***1. 2:00 PM – Impact of Temperature Cycling Conditions on Board Level Vibration for Automotive Applications***
Varun Thukral, Irene Bacquet, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc.; Willem Driel, G.Q. Zhang – Delft University of Technology

***2. 2:20 PM – Thermal Aging Study of Encapsulated Power Devices Under Autonomous Driving Condition and Its Effect on Board Level Reliability***
Yu-Hsiang Yang, Bongtae Han – University of Maryland; Przemek Gromala – Bosch

***3. 2:40 PM – Evolution of Fracture Resistance of the FCBGA Interfaces Under Monotonic and Fatigue Loads in Presence of Sustained Automotive High Temperatures***
Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Jeffrey Suhling – Auburn University

***4. 3:45 PM – System-Level Reliability Modeling and Validation of High-Performance Automotive and Medical IC Packages***
Li Jiang, Guangxu Li, Kejun Zeng, Jaimal Williamson, Rajen Murugan – Texas Instruments, Inc.

***5. 4:05 PM – Reliability Challenges and Mitigation Measures of Small Body-Sized Components on Complex and High-Layer Count PCBs***
Omar Ahmed, Peng Su, Arman Ahari, Leif Hutchinson, Bernard Glasauer – Juniper Networks

***6. 4:25 PM – Investigation on Fatigue Life of Non-Symmetric Solder Joints in Chip Resistors***
Jong Hwan Ha, Yangyang Lai, Junbo Yang, Pengcheng Yin, Karthik Arun Deo, Seungbae Park – Binghamton University

***7. 4:45 PM – Investigation of Acceleration Factors for SnAgCu-Bi Solder Joints Under Various Temperature Cycling Test Conditions***
Choongpyo Jeon, Youngsung Choi, Kwangwon Seo, Keunho Rhew, Jinsoo Bae, Yuchul Hwang, Sangwoo Pae – Samsung Electronics Co., Ltd.; Hyunsik Jeong – Hanyang University

## Session 21: Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections

**Committee:**
**Interconnections**

**Session Co-Chairs:**
**Nathan Lower**
**Consultant**
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**Jian Cai**
**Tsinghua University**
**Email: jamescai@tsinghua.edu.cn**

***1. 2:00 PM – Copper Pillar Voids in a Flip Chip Package During High Temperature Application***
Miao Wang, Amar Mavinkurve, Romuald Roucou, Amirul Afripin, CS Foong, Trent Uehling, Nishant Lakhera – NXP Semiconductor, Inc.

***2. 2:20 PM – Solder Joint Reliability of Fully Homogenised SAC-SnBi Low Temperature BGA Interconnections Using Solid Liquid Interdiffusion (SLID)***
Hafiz Waqas Ali, David Danovitch – University of Sherbrooke; Richard Langlois, Robert Martel – IBM Corporation

***3. 2:40 PM – Intermetallic Growth Study of Ultra-Thin Copper and Tin Bilayer for Hybrid Bonding Applications***
Gaurav Khurana – TU Dresden; Iuliana Panchenko – TU Dresden

***4. 3:45 PM – Heterogeneous Integration on Organic Interposer Substrate With Fine-Pitch RDL and 40 µm Pitch Micro-Bumps***
Katsuyuki Sakuma, Griselda Bonilla – IBM Research; Russell Kastberg – IBM Systems; Toyohiro Aoki – IBM Japan, Ltd.

***5. 4:05 PM – A Study on the Advanced Chip to Wafer Stack for Better Thermal Dissipation of High Bandwidth Memory***
Sangyong Lee, Jinwoo Park, Jong-Kyu Moon, Minsuk Kim, Gyujei Lee, Kangwook Lee – SK Hynix, Inc.

***6. 4:25 PM – Morphological and Electrical Characterization of Hard Material Microtubes Insertion in Aluminum and Indium Pads for 10 µm, 7.5 µm and 5 µm Pitches Interconnection Technology***
Natacha Raphoz, Patrick Peray, Olivier Mailliart, Frederic Berger, Cloe Desbordes – University of Grenoble Alpes/CEA-Leti

***7. 4:45 PM – Development of Fluxless Micro-Bonding and Narrow Gap Filling Process***
Sadaaki Katoh, Dongchul Kan, Keiko Ueno, Kazuyuki Mitsukura – Resonac Corporation

***Refreshment Break: 3:00 p.m. - 3:45 p.m.***

# Program Sessions: Thursday, June 1, 2:00 p.m. - 5:05 p.m.

| Session 22: Large Substrate Process Integration Challenges | Session 23: Next Generation Quantum, AI, and Secure System Design | Session 24: High-Speed Signal and Power Integrity |
|---|---|---|
| **Committee:**<br>**Assembly and Manufacturing Technology** | **Committee:**<br>**Emerging Technologies** | **Committee:**<br>**RF, High-Speed Components & Systems** |
| **Session Co-Chairs:**<br>**Valerie Oberson**<br>**IBM Canada, Ltd.**<br>**Email: voberson@ca.ibm.com**<br><br>**Jobert Van Eisden**<br>**Atotech USA, Inc.**<br>**Email: Jobert.van-Eisden@atotech.com** | **Session Co-Chairs:**<br>**Rohit Sharma**<br>**Indian Institute of Technology Ropar**<br>**Email: rohit@iitrpr.ac.in**<br><br>**Santosh Kudtarkar**<br>**Analog Devices, Inc.**<br>**Email: santosh.kudtarkar@analog.com** | **Session Co-Chairs:**<br>**Rockwell Hsu**<br>**Cisco Systems, Inc.**<br>**Email: rohsu@cisco.com**<br><br>**Chuei-Tang Wang**<br>**Taiwan Semiconductor Manufacturing Company, Ltd.**<br>**Email: ctwang10492@hotmail.com** |
| ***1. 2:00 PM – Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology***<br>Ilbok Lee, Soohyun Nam, Sungeun Kim, Sangho Shin, Younglyong Kim, Sunkyung Seo, Hae Jung Yu, Dae-Woo Kim – Samsung Electronics Co., Ltd. | ***1. 2:00 PM – Thermal-Aware SoC Macro Placement and Multi-Chip Module (MCM) Package Design With Mixed-Variable Bayesian Optimization***<br>Michael Molter, Elyse Rosenbaum – University of Illinois; Rahul Kumar, Osama Waqar Bhatti, Madhavan Swaminathan – Georgia Institute of Technology; Sonja Koller – Intel Corporation | ***1. 2:00 PM – Comprehensive PDN/PSIJ Analysis of Silicon Capacitor Use for 8.533 GT/s LPDDR5X Application***<br>Scott Powers, Jonathan Casanova, Arun Kundu, Varin Sriboonlue, Srivatsan Thiruvengadam, Jaemin Shin – Qualcomm Technologies, Inc.; Xiao Ma – Meta Platforms, Inc.. |
| ***2. 2:20 PM – Study of Fabrication and Reliability for the Extremely Large 2.5D Advanced Package***<br>Kosuke Murai, Hitoshi Onozeki, Dongchul Kang, Kazue Hirano, Mitsukura Kazuyuki – Resonac Corporation | ***2. 2:20 PM – 3D Defect Detection and Metrology of HBMs Using Semi-Supervised Deep Learning***<br>Ramanpreet Pahwa, Richard Chang, Jie Wang, Ziyuan Zhao, Chuan Sheng Foo, Xun Xu, Lile Cai, Kangkang Lu – Institute for Infocomm Research A*STAR; Sharon Lim, Ser Choong Chong, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR | ***2. 2:20 PM – Design Considerations for Power Delivery Network and Metal Insulator Metal Capacitor Integration in Bridge-Chips for 2.5-D Heterogeneous Integration***<br>Ankit Kaul, Madison Manley, Muhannad S. Bakir – Georgia Institute of Technology |
| ***3. 2:40 PM – Controlling Underfill on Die in Multi-Chip Heterogeneous Integration With Die Height Delta***<br>Ziyin Lin, Wei Li, Edvin Cetegen, Yang Guo, Nai-yuan Liu, Ifeanyi Okafor, Vipul Mehta, Xavier Brun, Shan Zhong, Hsin-yu Li, Christopher Rumer – Intel Corporation | ***3. 2:40 PM – A Si-Interposer With Buried Cu Metal Stripes and Bonded to Si-Substrate Backside for Security IC Chips***<br>Takuya Wadatsumi, Rikuu Hasegawa, Kazuki Monta, Takuji Miki, Makoto Nagata – Kobe University; Takaaki Okidono – SCU Co., Ltd. | ***3. 2:40 PM – Statistical Analysis of Off-Chip Power-Integrity for Multicore Systems***<br>Sodam Han, Sungwook Moon, Jungil Son, Seungki Nam – Samsung Electronics Co., Ltd.-Foundry Business |
| ***Refreshment Break: 3:00 p.m. - 3:45 p.m.*** | | |
| ***4. 3:45 PM – Lead Frame Versus Mold Via***<br>Rathin Mandal – Institute of Microelectronics A*STAR; Senthil Kumar Munirathinam, Jimmy Chew, Amlan Sen – PEP Innovation Pte. Ltd. | ***4. 3:45 PM – Physical Authentication of Electronic Devices Using Synthetically Generated 3D Material Signatures***<br>Tejas Ravindra Kulkarni, Nikhilesh Chawla, Ganesh Subbarayan – Purdue University | ***4. 3:45 PM – HBM3 Modules on Latest 2.3D High Density Organic Laminate: Signal Integrity Design and Analysis With Interconnect Budget Results***<br>Frank Libsch – IBM Research; Hiroyuki Mori – IBM Research, Tokyo |
| ***5. 4:05 PM – A Novel Low-Temperature Connection and High-Temperature Curing Process for Reducing the Warpage of Bonding Pair in Fan-Out Wafer Level Packaging***<br>Yun Bai, Kang Li, Cheng Zhong, Qiang Liu, Jinhui Li, Guoping Zhang, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology | ***5. 4:05 PM – Modeling and Analysis of CMOS-based Folded Memristive Crossbar Array for 3D Neuromorphic Integrated Circuits***<br>Sherin A. Thomas, Sahibia Kaur Vohra, Suyash Kushwaha, ROHIT SHARMA, Devarshi Mrinal Das – Indian Institute of Technology Ropar | ***5. 4:05 PM – Signal and Power Integrity Design and Analysis for Bunch-of-Wires (BoW) Interface for Chiplet Integration on Advanced Packaging***<br>Ram Krishna, Elyse Rosenbaum – University of Illinois; Atom Watanabe, John Golz, Ravi Bonam, Frank Libsch, Arvind Kumar – IBM Corporation |
| ***6. 4:25 PM – Package Warpage of Whole Strip Evaluation With Interface Analysis in the Flip- Chip Die Bonding Process***<br>Ian Ho, Po-Yu Liao, Teny Shih, Andrew Kang, Yu-Po Wang – Siliconware Precision Industries Co., Ltd. | ***6. 4:25 PM – Cryogenic Integration for Quantum Computer Using Diamond Color Center Spin Qubits***<br>Toshiki Iwai, Kenichi Kawaguchi, Tetsuya Miyatake, Tetsuro Ishiguro, Shoichi Miyahara, Shintaro Sato – Fujitsu, Ltd.; Salahuddin Nur, Ryoichi Ishihara – Delft University of Technology | ***6. 4:25 PM – Metaconductor-Based High Signal Integrity Interconnects for 112 Gbps SerDes Interface With Channel Analysis***<br>Hae-In Kim, Alexander Wilcher, Saeyeong Jeon, Yong-Kyu Yoon – University of Florida; Brice Achkir, Rockwell Hsu – Cisco Systems, Inc. |
| ***7. 4:45 PM – Thermal Solutions for High Performance Packages of Large Die and Large Packages***<br>Choong Kooi Chee, Sean Hsu, Janak Patel, Alaba Bamido – Marvell Semiconductor, Inc. | ***7. 4:45 PM – Characterizations of Indium Interconnects for 3D Quantum Assemblies***<br>Celine Feautrier, Edouard Deschaseaux, Alain Gueugnot, Jean Charbonnier, Aurelia Plihon, Ludovic Dupre, Franck Henry, Frederic Berger, Antoine Pagot, Sebastien Renet, Olivier Mailliart, Candice Thomas – CEA-Leti | ***7. 4:45 PM – Signal Integrity Co-Design of a High-Speed (20 Gbps) Analog Passive CMOS Bidirectional Switch***<br>Srikanth Manian, S. Shanmuganarayanan, Rajen Murugan, Sylvester Ankamah-Kusi – Texas Instruments, Inc. |

# Program Sessions: Friday, June 2, 9:30 a.m. -12:35 p.m.

| Session 25: Next Generation High-Performance Computing Architectures | Session 26: Materials Reliability | Session 27: Next Generation Wafer-to-Wafer Copper Bonding |
|---|---|---|
| **Committee:**<br>**Packaging Technologies** | **Committee:**<br>**Applied Reliability** | **Committee:**<br>**Interconnections** |
| **Session Co-Chairs:**<br>**Eric Tremble**<br>**Marvell**<br>**Email: etremble@marvell.com**<br><br>**Subhash L. Shinde**<br>**Notre Dame University**<br>**Email: sshinde@nd.edu** | **Session Co-Chairs:**<br>**Tae-Kyu Lee**<br>**Cisco Systems, Inc.**<br>**Email: taeklee@cisco.com**<br><br>**Darvin R. Edwards**<br>**Edwards Enterprise Consulting, LLC**<br>**Email: darvin.edwards1@gmail.com** | **Session Co-Chairs:**<br>**Li Li**<br>**Infinera**<br>**Email: packaging@yahoo.com**<br><br>**Dingyou Zhang**<br>**Broadcom, Inc.**<br>**Email: dingyouzhang.brcm@gmail.com** |
| ***1. 9:30 AM – CoWoS Architecture Breakthrough for Next Generation HPC Demand***<br>Yu-Min Liang, Hsieh-Pin Hu, Yu-Chen Hu, Chia-Yen Tan, Chih-Ta Shen, S. Y. Hou – Taiwan Semiconductor Manufacturing Company, Ltd. | ***1. 9:30 AM – Control of Solder Microstructure Stimulated by Interface Condition of the UBM/Solder and Enhancement of Electromigration Reliability***<br>Hariram Mohanram, Yi-Ram Kim, Geng Ni, Choongun Kim – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc. | ***1. 9:30 AM – 0.5 µm Pitch Next Generation Hybrid Bonding With High Alignment Accuracy for 3D Integration***<br>Christopher Netzband, Kevin Ryan, Ilseok Son, Hirokazu Aizawa – TEL Technology Center, America, LLC; Nathan Ip, Yuji Mimura, Xuemei Chen – Tokyo Electron America, Inc. |
| ***2. 9:50 AM – Reliability Performance of S-Connect Module (Bridge Technology) for Heterogeneous Integration Packaging***<br>HeeJun Jang, Kyun Ahn, Gamhan Yong, WonHo Choi, JiHyun Kim, Dave Hiner, TaeKyeong Hwang, Mike Kelly, WonChul Do, JinYoung Khim – Amkor Technology, Inc. | ***2. 9:50 AM – Al2O3-Coated Bond Wire With Adhesion Promoter and Electrical Insulation***<br>Soojae Park – Samsung Electronics Co., Ltd. | ***2. 9:50 AM – Low Temperature and Fine Pitch Nanocrystalline Cu/SiCN Wafer-To-Wafer Hybrid Bonding***<br>Wei-Lan Chiu, Ou-Hsiang Lee, Tzu-Ying Kuo, Hsiang-Hung Chang – Industrial Technology Research Institute; James Yi-Jen Lo, Chiang-Lin Shih, Hsih-Yang Chiu – Nanya Technology Corporation |
| ***3. 10:10 AM – Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration***<br>Lihong Cao – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang, Chih-Yi Huang – ASE Corporate R&D Center | ***3. 10:10 AM – Evolution of Propensity for High Strain-Rate Damage Accrual in Doped and Undoped SnAgCu Lead-Free Solders in Temperature Range of -65 °C to +200 °C After 1-Year Sustained High Temperatures Exposure***<br>Pradeep Lall, Vishal Mehta, Vikas Yadav, Mrinmoy Saha, Jeffrey Suhling – Auburn University | ***3. 10:10 AM – 0.5 µm Pitch Wafer-to-Wafer Hybrid Bonding With SiCN Bonding Interface for Advanced Memory***<br>Kai Ma, Nikos Bekiaris, Sesh Ramaswami – Applied Materials, Inc.; Taotao Ding, Juergen Burggraf, Gernot Probst, Thomas Uhrmann – EV Group, Inc. |
| ***Refreshment Break: 10:30 a.m.-11:15 a.m.*** | | |
| ***4. 11:15 AM – FO-EB-T Package Solution for High Performance Computing***<br>Po Yuan (James) Su, David Ho, Jacy Pu, Yu Po Wang – Siliconware Precision Industries Co., Ltd. | ***4. 11:15 AM – Reliability Investigations of Polymer Based Redistribution Layers (RDL) Protected by a Mold Layer***<br>Ji-Youn Kwak – University of Ulsan; Emmanuel Chery, John Slabbekoorn, Julien Bertheau, Joke De Messemaeker, Eric Beyne – imec | ***4. 11:15 AM – Fine-Pitch 30 µm Cu-Cu Bonding using Electroless Nano-Ag***<br>Hsiang-Wei Tsai, Yung-Sheng Lin, Chun-Wei Chiang, Yun-Ching Hung, Chin-Li Kao, Ping-Hung Hsieh, I-Ting Lin, Chih-Yuan Hsu – Advanced Semiconductor Engineering, Inc. |
| ***5. 11:35 AM – Die to Wafer Hybrid Cu Bonding for Fine Pitch 3D-IC Applications***<br>Yeongseon Kim, Juhyeon Kim, Hyoeun Kim, Dohyun Kim, Seonkyung Seo, Chajea Jo, Dae-Woo Kim – Samsung Electronics Co., Ltd. | ***5. 11:35 AM – SAC/LTS Hybrid Solder Joint in BGA Package: Identification of Mechanical Weak Spots and End-of-Life Joint Failure Prediction***<br>Lip Teng Saw, Mutharasu Devarajan, Puurnaraj Nadarajah – Western Digital Corporation | ***5. 11:35 AM – Influence of H2O in Bonding Interfaces on Bonding Strength of Plasma-Activated Bonded Silicon Oxide***<br>Hirotaka Yoshioka, Nobutoshi Fujii, Takushi Shigetoshi, Takahiro Kamei, Kengo Kotoo, Naoki Ogawa, Tatsuya Horikiri, Shunsuke Furuse, Sotetsu Saito, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation |
| ***6. 11:55 AM – Silicon Interposer Based 2.5 D Integration of TeraPHY Chiplet for Co-Packaged Optics***<br>Haiwei Lu, Chong Zhang, Chen sun, Steve Groothuis, Mark Wade, Chen Li, Chandru Ramamurthy, Norman Chan, Jie Ding, Byungchae Kim, Michael Rust, Forrest Sedgwick – Ayar Labs, Inc. | ***6. 11:55 AM – The Failure Mechanisms of Bonding Between Copper Substrate and Encapsulation Epoxy Under High-Temperature Aging***<br>Shuaijie Zhao, Chuantong Chen, Katsuaki Suganuma – Osaka University; Minoru Ueshima, Motoharu Haga – Daicel Corporation | ***6. 11:55 AM – Not All Nanograined Copper is Created Equal - In Pursuit of a Robust Low Temperature Copper to Copper Bonding Process***<br>Yun Zhang, Peipei Dong, Jing Wang, Xingxing Zhang – Shinhao Materials LLC; Klaus Leyendecker, Tsvetina Dobrovolska, Michael Herkommer, Volker Wohlfarth, Josh Liang – Umicore Galvanotechnik GmbH |
| ***7. 12:15 PM – Direct Bonded Heterogeneous Integration (DBHi): Surface Bridge Approach for Die Tiling***<br>Claudia Cristina Barrera Pulido, Divya Taneja, Philip McInnes, Isabel De Sousa – IBM Canada, Ltd.; Sayuri Kohara, Akihiro Horibe – IBM Japan, Ltd.; Aakrati Jain, Thomas Wassick – IBM Corporation | ***7. 12:15 PM – Copper Wire Degradation Under the Effect of Different Humidity Levels***<br>Michael Joo Zhong Lim, Zhong Chen, Chuan Seng Tan – Nanyang Technological University; Hai Guan Loh – Infineon Technologies Asia Pacific Pte. Ltd.; Michael Goroll – Infineon Technologies AG | ***7. 12:15 PM – A Study on Multi-Chip Stacking Process by Novel Dielectric Polymer Adhesive for Cu-Cu Hybrid Bonding***<br>Yuzo Nakamura, Kahori Tamura, Yasuhisa Kayaba, Wataru Okada, Takuo Shikama, Satoshi Inada – Mitsui Chemicals, Inc. |

# Program Sessions: Friday, June 2, 9:30 a.m. -12:35 p.m.

| Session 28: Process Enhancements in 3D, FOWLP, and TSV Technologies | Session 29: AI-based Prediction for Heterogeneous Integration and Advanced Packaging | Session 30: Trends in Encapsulants and Low Dk/Df Dielectrics |
|---|---|---|
| **Committee: Materials & Processing** | **Committee: Thermal/Mechanical Simulation & Characterization** | **Committee: Materials & Processing** |
| **Session Co-Chairs:**<br>**Vidya Jayaram**<br>**Intel Corporation**<br>**Email: vidya.jayaram@intel.com**<br><br>**Dwayne Shirley**<br>**Marvell**<br>**Email: shirley@ieee.org** | **Session Co-Chairs:**<br>**Patrick McCluskey**<br>**University of Maryland**<br>**Email: mcclupa@umd.edu**<br><br>**Rui Chen**<br>**Georgia Institute of Technology**<br>**Email: chenrui@gatech.edu** | **Session Co-Chairs:**<br>**Tanja Braun**<br>**Fraunhofer IZM**<br>**Email: tanja.braun@izm.fraunhofer.de**<br><br>**Kimberly Yess**<br>**Brewer Science, Inc.**<br>**Email: kyess@brewerscience.com** |
| ***1. 9:30 AM – Magneto-Assisted Graphene Reinforcement: A New Method to Enhance Nanostructure and Properties of Electrodeposited Copper***<br>Nithin Nedumthakady, Vanessa Smet – Georgia Institute of Technology | ***1. 9:30 AM – Feasibility Investigation of Machine Learning for Electronic Reliability Analysis Using FEA***<br>Robert David Johannes Hoehne, Yichen Qi, Oliver Albrecht, Karsten Meier, Karlheinz Bock – TU Dresden | ***1. 9:30 AM – Liquid Compression Mold Underfill Optimization With Low Warpage and Narrow Gap Flow***<br>Tsuyoshi Kamimura, Shinichi Sato, Yuto Shigeno – NAMICS Corporation; Brian Schmaltz – NAMICS Technologies, Inc. |
| ***2. 9:50 AM – Exploring Capabilities of Maskless Lithography for Dual Image Exposure in FO WLP***<br>Ksenija Varga, Thomas Uhrmann, Roman Holly, Tobias Zenger – EV Group, Inc.; Chris Milasincic, Mel Zussman, Ron Legario, Michael Knaus – HD MicroSystems L.L.C. | ***2. 9:50 AM – NAND Package Warpage Prediction and Design With Tolerance Through Machine Learning***<br>Yuhang Yang, Chaolun Zheng, Min Lin – Western Digital Technologies, Inc.; Tim Huang, Hedan Zhang, Ning Ye, Bo Yang – Western Digital Corporation | ***2. 9:50 AM – Effect of High-Temperature Exposure on the Thermo-Mechanical Behavior of Epoxy Molding Compound and Warpage of Molded Wafers***<br>Junmo Kim, Myoung Song, Chang-Yeon Gu, Min Sang Ju, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sung Woo Ma, Jin Hee Lee, Woong-Sun Lee – SK Hynix, Inc. |
| ***3. 10:10 AM – Alignment Through Thick Si Layer for High Resolution Patterning on Bonded Wafers With Tight Overlay Margin Using Immersion Lithography***<br>Arvind Sundaram, Chin Khang Tew, Guo Wei Tan, Hongyu Li, Nandini Venkataraman, Yuan-Hsing Fu, Chandra Rao Bhesetti, Navab Singh – Institute of Microelectronics A*STAR | ***3. 10:10 AM – Reduced-Order Models of Digital Twin Applications for Design Platform of Flexible Hybrid Electronics***<br>Chang-Chun Lee – National Tsing Hua University; Jui-Chang Chuang, Chen-Tsai Yang, Chung-I Li – Industrial Technology Research Institute | ***3. 10:10 AM – Low Temperature Fine Pitch All-Copper Interconnects Combining Photopatternable Underfill Films***<br>Xinrui Ji, Henk Van Zeijl, Weiping Jiao, Shan He, Leiming Du, Guoqi Zhang – Delft University of Technology |
| ***Refreshment Break: 10:30 a.m.-11:15 a.m.*** | | |
| ***4. 11:15 AM – Recent Progress in the Development of High-Density TSV for 3-Layers CMOS Image Sensors***<br>Stephan Borel, Myriam Assous, Stephane Moreau, Steve Pellerin – CEA-Leti | ***4. 11:15 AM – Methodology of Artificial Intelligence Aided Hybrid Modeling on Solder Joint Reliability Study of BGA Package***<br>ling pan, Faxing Che, Yeow Chon Ong, hong wan ng – Micron Semiconductor Asia Operations Pte. Ltd; Gokul Kumar – Micron Technology, Inc. | ***4. 11:15 AM – Novel Low Dk/Df Photoimageable Dielectric for Redistribution Layer***<br>Guillermo Fernandez Zapico, Fumihiko Kawauchi, Shinya Kawashita, Manabu Hirasawa, Kitaru Sato, Tetsuya Imai, Hidekazu Kondo, Tatsuya Makino – Resonac Corporation |
| ***5. 11:35 AM – The Advantages of Low Temperature (<400 °C) Carbon Nano-Tubes (CNTs) as Through Silicon Vias (TSVs) in Multi-Layers Stacking and Backside Power-Via Applications***<br>Nilabh Basu, H.-Y. Lin, T.-W. Chen, Y.-C. Chan, Y.-T. Tsai, H.-C. Guo, T.-H. Wu, P.-C. Lin, Y.-C. Lin, Ming-Han Liao – National Taiwan University | ***5. 11:35 AM – Effect of Li-ion Battery Form Factor on the SoH Degradation Under Randomized Charge-Discharge Cycles and C-Rates***<br>Pradeep Lall, Ved Soni – Auburn University | ***5. 11:35 AM – Novel Photo-Definable Low Dk & Df Polyimide for Advanced Package of High Frequency Application***<br>Hitoshi Araki, Akira Shimada, Hisashi Ogasawara, Masaya Jukei, Masao Tomikawa – Toray Industries, Inc. |
| ***6. 11:55 AM – A Precise Wafer Thinning Integration Flow for Nano-TSV Formation***<br>Ya-Ching Tseng, Nandini Venkataraman, King Jien Chui – Institute of Microelectronics A*STAR | ***6. 11:55 AM – AI-Enabled Molding Compound Selection Method for Warpage Control of Fan-Out Panel-Level Package***<br>Peilun Yao, Yonglin Zhang, Jinglei Yang – Hong Kong University of Science and Technology; Haibin CHEN, Jingshen Wu – Hong Kong University of Science and Technology (Guangzhou); Haibo Fan, Anthony Cheung – Nexperia HK, Ltd. | ***6. 11:55 AM – Novel Low Dk/Df Film for High Frequency Substrate and RDL***<br>Meiten Koh, Kazuyoshi Yoneda, Kazutaka Nakada, Yoshitomo Aoyama, Kasumi Hashimoto, Kota Oki – Taiyo Ink Mfg. Co., Ltd. |
| ***7. 12:15 PM – Next Generation Infrared (IR) Laser Debonding / Silicon Handle Technology for Precision Chiplet Technology Applications***<br>Qianwen Chen, Michael Belyansky, Yasir Sulehria, Akihiro Horibe, Eric Perfecto, Katsuyuki Sakuma, John Knickerbocker – IBM Corporation; Takeshi Tamura, Takayuki Ishii, Panupong Jaipan, Satoshi Nishimura Nishimura, Ilseok Son – Tokyo Electron, Ltd. | ***7. 12:15 PM – Thermal Characterization of 3-D Stacked Heterogeneous Integration (HI) Package for High-Power Computing Applications***<br>Aakrati Jain, Sathya Raghavan, Prabudhya Roy Chowdhury, Mukta Ghate Farooq, Arvind Kumar, Katsuyuki Sakuma – IBM Research; Risa Miyazawa – IBM Research, Tokyo | ***7. 12:15 PM – Properties of Low Dielectric Constant Build Up Materials Containing Micron Sized Hollow Silica***<br>Preeya Kuray – AGC Inc.; Tom McCarthy, Caleb Ancharski, Yoji Nakajima – AGC Multi Material America, Inc. |

# Program Sessions: Friday, June 2, 2:00 p.m. - 5:05 p.m.

| Session 31: MEMS Sensor, Bio, and Advanced Interconnect Reliability | Session 32: Thermo-Mechanical Modelling and Characterization | Session 33: Advances in RDL, Via, and TSV Technologies for Chiplet Integration |
|---|---|---|
| **Committees:**<br>**Packaging Technologies and Applied Reliability** | **Committee: Thermal/Mechanical Simulation & Characterization** | **Committee:**<br>**Interconnections** |
| **Session Co-Chairs:**<br>**Young-Gon Kim**<br>**Renesas Electronics America**<br>**Email: young.kim.jg@renesas.com**<br><br>**Deepak Goyal**<br>**Intel Corporation**<br>**Email: deepak.goyal@intel.com** | **Session Co-Chairs:**<br>**Pradeep Lall**<br>**Auburn University**<br>**Email: lall@auburn.edu**<br><br>**Tieyu Zheng**<br>**Microsoft Corporation**<br>**Email: tizheng@microsoft.com** | **Session Co-Chairs:**<br>**Takafumi Fukushima**<br>**Tohoku University**<br>**Email: fukushima@lbc.mech.tohoku.ac.jp**<br><br>**Bernd Ebersberger**<br>**Infineon Technologies AG**<br>**Email: bernd.ebersberger@infineon.com** |
| ***1. 2:00 PM – Enabling Backside Processing for Perforated Microfluidic Devices***<br>Jakob Visker, Yang Han, Evert Visker, Chi Dang Thi Thuy, Mateusz Gocyla, Jan Ackaert, Aurelie Humbert, Serge Vanhaelemeersch, Lan Peng – imec | ***1. 2:00 PM – Mechanical Simulation and Characterization on Flexural Fracture of Stacked Die Memory Package***<br>Yangming Liu, Ning Ye, Bo Yang, Siqi Zhang, Wei Wang, Xu Wang – Western Digital Corporation | ***1. 2:00 PM – 3D Silicon Interposer for Terabit/s Transceivers Based on High-Speed TSVs***<br>Bogdan Sirbu, Kai Zoschke, Tolga Tekin – Fraunhofer IZM; Ukyo Suzuki, Quentin Wilmart – CEA-Leti |
| ***2. 2:20 PM – Wafer Level Chip Scale Package Technology Applied to MEMS Pressure Sensor***<br>Luca Maggi, Marco Del Sarto, Tiziano Chiarillo, Enri Duqi, Lorenzo Baldo, Adriano Abbisogni – STMicroelectronics | ***2. 2:20 PM – Simulation of Device Structure Impacts on Bonding Wave and Strain in Wafer to Wafer Cu-Cu Hybrid Bonding***<br>Takaaki Hirano, Taichi Yamada, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation | ***2. 2:20 PM – Creative Design and Structure Applied to Chiplets Packaging***<br>Chen-Chao Wang, Chih-Yi Huang, Chih-Pin Hung, Chung-Hung Lai, Hung-Hsien Huang, Hung-Chun Kuo, Ming-Fong Jhong, Fu-Chen Chu – Advanced Semiconductor Engineering, Inc. |
| ***3. 2:40 PM – A Novel FOWLP Method to Integrate Delicate MEMS Components***<br>Markus Woehrmann, Tanja Braun, Michael Schiffer, Martin Schneider-Ramelow – Fraunhofer IZM; Marc Dreissigacker – Technical University Berlin | ***3. 2:40 PM – Investigation of Cure Kinetics of Advanced Epoxy Molding Compound Using Dynamic Heating Scan: An Overlooked Second Reaction***<br>Ran Tao, Aaron M. Forster – National Institute of Standards and Technology; Sukrut Prashant Phansalkar, Bongtae Han – University of Maryland | ***3. 2:40 PM – TSV-Based Stacked Silicon Capacitor With Embedded Package Platform***<br>Kyojin Hwang, Heeseok Lee, Junso Pak – Samsung Electronics Co., Ltd. |
| ***Refreshment Break: 3:00 p.m. - 3:45 p.m.*** | | |
| ***4. 3:45 PM – Development of High Reliability 6 µm-pitch Cu-Cu Connections Using Over-400 mm²-Large Chip on Wafer Bonding Process***<br>Takahiro Kamei, Hirotaka Yoshioka, Tatsumasa Hiratsuka, Akihisa Sakamoto, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation | ***4. 3:45 PM – Effect of Passivation and Mechanical Constraint on Electromigration in Interconnect***<br>Xuejun Fan – Lamar University; Zhen Cui, Guoqi Zhang – Delft University of Technology | ***4. 3:45 PM – Ultra-Fine Pitch RDL (UFPRDL) Using Polymer Dual Damascene Processing***<br>Nelson Pinho, Emmanuel Chery, Nicolas Pantano, John Slabbekoorn, Andy Miller, Eric Beyne – imec |
| ***5. 4:05 PM – A Comprehensive Study of Solder Joint Reliability Dependent on Temperature Cycling Profiles and Material Selections With Emphasis on an Improved Solder Fatigue Lifetime Model***<br>Bongchan Son, Seung-Hyun Chae, SeungKwon Noh, KilJae Lee, Sangdeok Kim – SK Hynix, Inc. | ***5. 4:05 PM – Improving Warpage Characterization of Large Wafers in Fan-Out Packaging Technology***<br>Saskia Gesche Huber, Andreas Stegmaier, Marius van Dijk, Nina Nguyen, Ole Hoelck, Olaf Wittler, Martin Schneider-Ramelow – Fraunhofer IZM | ***5. 4:05 PM – Development of a Plasma Etching Process of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging***<br>Juliano Borges, Maxime Darnon, Yann Beilliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa – IBM Canada, Ltd. |
| ***6. 4:25 PM – Electromigration Performance of Fine-Line Cu Redistribution Layer (RDL) for High-Density Fan-Out Packaging***<br>JiHye Kwon, JeongMin Ju, EunSook Sohn, JinYoung Khim – Amkor Technology Korea | ***6. 4:25 PM – Enhancement of Thermal Transient Prediction Accuracy for Mobile AP Package***<br>Hwanjoo Park, Jonggyu Lee, Taehwan Kim, Sunggu Kang, Sungho Mun, Jaechoon Kim, Dan Oh – Samsung Electronics Co., Ltd. | ***6. 4:25 PM – On the Path to AI Hardware Via Chiplet Integration Enabled by High Density Organic Substrates***<br>Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar – IBM Systems |
| ***7. 4:45 PM – Simulation-Assisted Board Level Solder Joint Reliability Optimization for Large 80 mm+ 2.5D Devices***<br>Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Glasauer – Juniper Networks; Vishnu Shukla, Tengfei Jiang – University of Central Florida | ***7. 4:45 PM – FO-EB-T Package Characterization and Evaluation***<br>Vito Lin, Andrew Kang, Yu-Po Wang – SPIL | ***7. 4:45 PM – Fine Pitch Microvia Interconnection With Reliable Electroless/ Electric Cu Plating Layers Combined With High Power DUV Picosecond Pulse Laser for Organic Substrates***<br>Ming-chun Hsieh, Zheng Zhang, Masahiko Nishijima, Aiji Suetake, Chuantong Chen, Hiroyoshi Yoshida, Wanyun Li, Reiko Okumura, Katsuaki Suganuma – Osaka University; Hidekazu Homma, Koji Kita – Okuno Chemical Industries Co., Ltd.; George Okada – Spextronix Corp., Ltd. |

# Program Sessions: Friday, June 2, 2:00 p.m. - 5:05 p.m.

| Session 34: Bonding Assembly - Novel Packaging, Process, and Characterization | Session 35: Packaging and Materials for Flexible Medical Technologies | Session 36: RF, Heterogeneous, and Chiplet Modules |
|---|---|---|
| **Committee:**<br>**Assembly and Manufacturing Technology** | **Committee:**<br>**Emerging Technologies** | **Committee:**<br>**RF, High-Speed Components & Systems** |
| **Session Co-Chairs:**<br>**Jason Rouse**<br>**Taiyo America, Inc.**<br>**Email: jhrouse@taiyo-america.com**<br><br>**Zia Karim**<br>**Yield Engineering Systems**<br>**Email: zkarim@yieldengineering.com** | **Session Co-Chairs:**<br>**Vaidyanathan Chelakara**<br>**Acacia Communications**<br>**Email: cvaidyanathan@acacia-inc.com**<br><br>**Dongming He**<br>**Qualcomm Technologies, Inc.**<br>**Email: dhe@qti.qualcomm.com** | **Session Co-Chairs:**<br>**Amit Agrawal**<br>**Microchip Technology**<br>**Email: amit.agrawal@microchip.com**<br><br>**Craig Gaw**<br>**NXP Semiconductor, Inc.**<br>**Email: c.a.gaw@ieee.org** |
| ***1. 2:00 PM – Laser-Assisted Bonding With Compression (LABC) Based Tiling Bonding Process, Enabling Technology for Chiplet Integration***<br>Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ho-Gyeong Yun, Seok Hwan Moon, Ki-Seok Jang, Jin-Hyuk Moon, Yoon-Hwan Moon, Yong-Sung Eom – Electronics Telecommunications Research Institute | ***1. 2:00 PM – Fully Portable Wireless Soft Stethoscope and Machine Learning for Continuous Real-Time Auscultation and Automated Disease Detection***<br>Sung Hoon Lee, Yun-Soung Kim, Woon-Hong Yeo – Georgia Institute of Technology | ***1. 2:00 PM – Heterogeneous Radio Chiplet Module for 5G Millimeter Wave Application***<br>Agneta Ljungbro, Emil Nylander, Martin Hansson – Ericsson AB; Marcel Wieland, Selaka Bulumulla – GlobalFoundries, Inc. |
| ***2. 2:20 PM – Contamination-Free Cu/SiCN Hybrid Bonding Process Development for Sub-µm Pitch Devices With Enhanced Bonding Characteristics***<br>Seung Ho Hahn, Wooyoung Kim, Donggap Shin, Yongin Lee, Sumin Kim, Wonyoung Choi, Kyeongbin Lim, Bumki Moon, Minwoo Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research | ***2. 2:20 PM – Patch-Type Flex SiP Platform for Healthcare Application***<br>Ming-Hung Chen, Wei-Hao Chang, Hui-Ping Jian, Chao-Wei Liu, Shang-Lin Wu, Yi-Chun Chou, Sung-Hung Chiang, Jung-Kai Chang, Tun-Ching Pi, Wei-Chun Lee, Jen-Chieh Kao, Yung-I Yeh – ASE Corporate R&D Center | ***2. 2:20 PM – Design and Analysis of 3D Heterogeneous Chiplet Stack for RF Front-End Module Miniaturization***<br>Mihai Rotaru, Chai Tai Chong, Chui King Jien – Institute of Microelectronics A*STAR; Shashank Tiwari – GlobalFoundries, Inc.; Paul Castillou – Qorvo, Inc. |
| ***3. 2:40 PM – Integration and Process Challenges of Self-Assembly Applied to Die-to-Wafer Hybrid Bonding***<br>Emilie Bourjot, Alice Bond, Noura Nadi, Thierry Enot, Loic Sanchez, Pierre Montmeat, Benoit Martin, Alain Campo, Frank Fournel – CEA-Leti; Feras Eid, Johanna Swan – Intel Corporation | ***3. 2:40 PM – Development of PMUT Array Packaging from Characterisation Prototypes to Customer Samples***<br>Mark Andrew Shaw, Domenico Giusti, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Klug, Hitoshi Hoshino – DISCO HiTec Europe; Vempati Srinivasa Rao, Dutta Rahul, David Ho Soon Wee – Institute of Microelectronics A*STAR; Hideyuki Sandoh, Masatoshi Wakahara – DISCO Corporation; Alessandro Savoia – Roma Tre University | ***3. 2:40 PM – Embedded mm-Wave Chiplet Based Module Using Fused-Silica Stitch-Chip Technology: RF Characterization and Thermal Evaluation***<br>Ting Zheng, Madison Manley, Muhannad S. Bakir – Georgia Institute of Technology |
| ***Refreshment Break: 3:00 p.m. - 3:45 p.m.*** | | |
| ***4. 3:45 PM – OCD Scatterometry as a Scalable Solution for Hybrid Bonding Pad Recess Metrology***<br>Haris K. Niazi, Botao Zhang, Xavier F. Brun, Xavier F. Brun – Intel Corporation; Krishnan Shankar – KLA Corporation | ***4. 3:45 PM – Multi-Cell Array of Nanogap Electrodes for Label-Free Detection of Biomolecules***<br>Musafargani Sikkandhar, Yu Chen, Ming-Yuan Cheng – Institute of Microelectronics A*STAR | ***4. 3:45 PM – Surface Micromachined Integrable High Efficiency Ridge Gap Waveguide Bandpass Filter for G-Band 6G Applications***<br>Alexander Wilcher, Hae-in Kim, Ziqi Jia, David Arnold, Yong-Kyu Yoon – University of Florida; Jia Chieh, Alex Phipps – Naval Information Warfare Center Pacific |
| ***5. 4:05 PM – A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage***<br>Serena Iacovo, Oguzhan Orkut Okudur, Koen D'Have, Johan Meersschaut, Liesbeth Witters, Thierry Conard, Alain Phommahaxay, Steven Brems, Gerald Beyer, Eric Beyne – imec; Thomas Uhrmann, Thomas Plach – EV Group, Inc. | ***5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging***<br>Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Binghamton University | ***5. 4:05 PM – Amplified and Filtered x2 Multiplier Chip***<br>Elizabeth Kunkee, Dah-Weih Duan, Ricardo Medina, Nancy Lin, R. Yogi, Chunbo Zhang, Robert Mendoza, Kevin Leong, Alex Zamora, Scott Sing, David Miller – Northrop Grumman Corp. |
| ***6. 4:25 PM – Optimization of Temperature Profile and Residual Stresses During Thermal Compression Bonding in 3D Packages***<br>Prabudhya Roy Chowdhury, Sathya Raghavan, Luke Darling, Aakrati Jain, Promod R. Chowdhury, Mukta Ghate Farooq, Katsuyuki Sakuma – IBM Research | ***6. 4:25 PM – 3D Printed Electronics With Multi Jet Fusion for Flexible Hybrid Electronics***<br>Jarrid Wittkopf, Sanil Jhaveri, Fan Fei, Manjarik Mrinal, Eric Luna-Ramirez, Sunil Kothari – HP Inc.; Dylan Richmond, Dayue Jiang, Fuda Ning, Mohamed Alhendi, Detlef Smilgies, Mark Poliks – Binghamton University | ***6. 4:25 PM – Optimal Channel Design for Die-to-Die Interface in Multi-Die Integration Applications***<br>Jiyoung Park, Seungki Nam, Sungwook Moon, Jinho Kim – Samsung Electronics Co., Ltd. |
| ***7. 4:45 PM – Impact of Thermal Annealing and Other Process Parameters on Hybrid Bonding Performance for 3D Advanced Assembly Technology***<br>Taiwo Ajayi, Alvin Gatimu, Chris Woods, Xavier F. Brun – Intel Corporation; Abhishek Bhat, Kay Song, Zia Karim, Charudatta Galande, Phillip Le – Yield Engineering Systems | ***7. 4:45 PM – Performance Evaluation of RF Novel Microstrip Lines Printed on Flexible Substrates***<br>Abdullah Obeidat, Mohamed Abdelatty, Ashraf Umar, Emuobosan Enakerakpo, Riadh Al-Haidari, Mohammed Alhendi, Mark Poliks – Binghamton University | ***7. 4:45 PM – 3D MIM Ultra-Small Silicon Capacitor Design for High Capacitance Density With Extremely Low ESR and ESL***<br>Wisnu Murti, Jihoon Cha, Dongki Lee, Taedong Kim, Sarah Kim, Yeong Lyeol Park, Seunggu Lim, Willy Choi – Elohim, Inc. |

## Interactive Presentations: Wednesday, May 31, 10:00 a.m. - 12:00 Noon and Wednesday, May 31, 2:30 p.m. - 4:30 p.m.

**Wednesday May 31, 2023, 10:00 a.m. – 12:00 Noon**

**Session 37: Interactive Presentations 1**

**Committee: Interactive Presentations**

**Session Co-Chairs:**
**Mark Poliks – Binghamton University**
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**Jae Kyu Cho – GlobalFoundries, Inc.**
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***1. Signal Integrity of 2-µm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System***
Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.; Tomoya Sasagawa – DNP America, LLC

***2. Investigation of Cu-to-Cu and Oxide-to-Oxide Bonding***
Sangmin Lee, Gwangsik Oh, Junyoung Choi, Yoonho Kim, Sangwoo Park, Sarah Kim – Seoul National University of Science and Technology

***3. Doping-Selective Etching of Silicon for Wafer Thinning in the Fabrication of Backside-Illuminated Stacked CMOS Image Sensors***
Nandini Venkataraman, Navab Singh, Darshini Senthilkumar – Institute of Microelectronics A*STAR; Benedikt Risse – Nexgen Wafer Systems GmbH; Gregorio Decierdo – Nexgen Wafer Systems Pte. Ltd.; Deepthi Kandasamy, Eng Huat Toh, Louis Lim – GlobalFoundries Singapore

***4. Study of Solder Resist Crack Resistance for Flip Chip Ball Grid Array Substrate***
Eric Chen, Rick Ye, Wen-Yu Teng, Yu-Cheng Pei, Yu Po Wang – Siliconware Precision Industries Co., Ltd.

***5. Reliability Analysis on Ag and Cu Nanoparticles Sintered Discrete Power Device With Various Frontside and Backside Interconnect***
Dong Hu, Xu Liu, Sten Vollebregt, Jiajie Fan, Guoqi Zhang – Delft University of Technology; Ali Roshanghias – Silicon Austria Labs GmbH; Xing Liu, Thomas Basler – Chemnitz University of Technology; Emiel De Bruin – Boschman Advanced Packaging Technology B.V.

***6. Wafer Level Batch Fabrication of an MRI Compatible Neural Probe With Electrical, Optical, and Microfluidic Functions***
Ziqi Jia, Shuyu Shi, Yong-Kyu Yoon – University of Florida

***7. High Reliability Design of Ag Sinter Joining on a Softened Crackless Ni-P /Pt/Ag Metallization AMB Substrate During Aging and Harsh Thermal Cycling***
Chuantong Chen, Yang Liu, Hupeng Huo, Katsuaki Suganuma – Osaka University; Minoru Ueshima, Takeshi Sakamoto – Daicel Corporation; Yukinori Oda – C. Uyemura & Co., Ltd.

***8. Impact of Process Parameters on Vacuum Fluxless Solder Reflow Performance in Backend Applications With Bump Pitch of 15 µm and Below***
Lei Jing, Vladimir Kudriavtsev, Taylor Nguyen, Jed Hsu, Tapani Laaksonen, Alvin Lin, Xinxuan Tan, Kay Song, Alex Chow, Chris Lane, Zia Karim – Yield Engineering Systems

***9. Reliability Performance Study of Molding Compounds on High Voltage Molded Leaded Package***
April Joy Garete, Zhiwen Li, Yee Wai Fung, Wai Man Wong – Nexperia

***10. Surface Modification on Hydrophilicity Enhancement Using $NH_4OH$, NaOH and KOH on Fine-Pitch Low Temperature Cu/$SiO_2$ Hybrid Bonding***
Jia-Juen Ong, Dinh-Phuc Tran, Yu-An Chen, Chih Chen – National Chiao Tung University; Wei-Lan Chiu, Ou-Hsiang Lee, Hsiang-Hung Chang – Industrial Technology Research Institute

***11. Development and Demonstration of a Novel Immersion Two Phase Cooling High Power SiC Power Module***
Gongyue Tang, Leong Ching Wai, Huicheng Feng, Haoran Chen – Institute of Microelectronics A*STAR

***12. Electrochemical Deposition of Indium Bumps on Superconducting Interconnect and Thermo-Compression Bonding for Cryogenic and Quantum Computing***
Kumin Kang – Hanyang University; Jaber Derakhshandeh – imec

***13. Ultra-Precise Deposition: Additive Manufacturing Process for Advanced Packaging and Heterogeneous Integration***
Lukasz Witczak, Jolanta Gadzalinska, Iwona Gradzka-Kurzaj, Mateusz Lysien, Ludovic Schneider, Aneta Wiatrowska, Karolina Fiaczyk, Piotr Kowalczewski, Lukasz Kosior, Filip Granek – XTPL SA

***14. Influence of High Temperature Thermal Annealing on Silver-Based backside Metallization Stack for Power Electronic Die-Attach Packaging Applications***
Goran Miskovic, Mohamed Lamine Faycal Bellaredj – Silicon Austria Labs GmbH

***15. 6-Sided Die Protection for Chiplet Package With Multi-Layer RDL***
ByungCheol Kim, Mary Maye Melgo, Rizi Gacho, Jacinta Aman Lim, Hee Yeoul Yoo, Kwan Sun Oh – nepes Corporation; Cliff Sandstrom, Benedict San Jose – Deca Technologies, Inc.

***16. Wafer Level Capping Technology for Vacuum Packaging of Microbolometers***
Kai Zoschke, Charles-Alix Manier, Hermann Oppermann – Fraunhofer IZM; Dirk Meier, Nishant Malik – Integrated Detector Electronic AS; Elahe Zakizade, Marvin Daniel Michel – Fraunhofer IMS; Avisek Roy, Hoang-Vu Nguyen, Hexin Xia – University of South-Eastern Norway

***17. Artificial Intelligence (AI) Based Methodology to Minimize Asymmetric Bare Laminate Warpage***
Sathya Raghavan, Griselda Bonilla, Katsuyuki Sakuma – IBM Research; Hiroyuki Mori – IBM Research, Tokyo

***18. Scaling of Redistribution Layer for Heterogeneous Packaging in a Panel Level***
Yoonyoung Jeon, Youngmin Kim, Hyundong Lee, Minji Kim, Woongkeon Lee, Joonseok Oh – Samsung Electronics Co., Ltd.

***19. Process Challenges During CVD Oxide Deposition on the Backside of 20-µm Thin 300-mm Wafers Temporarily Bonded to Glass Carriers***
Koen Kennes, Abdellah Salahouelhadj, Samuel Suhard, Jaber Derakhshandeh, Alain Phommahaxay, Steven Brems, Gerald Beyer, Eric Beyne – imec; Alice Guerrero, Xiao Liu – Brewer Science, Inc.

***20. Electrical Characterization and Modeling of 2-µm and 1.5-µm Line-and-Space High-Density Signal Wiring in Organic Interposer***
Atom Watanabe, Hiroyuki Mori, Xiaoxiong Gu, Frank Libsch, Griselda Bonilla – IBM Corporation

***21. Package Integrated Vapor Chamber Heat Spreaders***
Cameron Nelson – Amkor Technology, Inc.; SangHyuk Kim – Amkor Technology Korea

***22. Study on Single-Digit Micro Bump Patterning for 2.5D Silicon Interposer***
Masaki Mizutani, Yusuke Tokuyama, Hiromi Suda, Ken-Ichiro Shinoda, Ken-Ichiro Mori – Canon, Inc.; Douglas Shelton – Canon U.S.A., Inc.

***23. C2W Hybrid Bonding Interconnect Technology for High Density and Better Thermal Dissipation of HBM***
Kibum Kim – SK Hynix, Inc.

***24. Large 2.5D Package-to-System Interaction Analysis from Thermal Perspective Based on 3DFabric™ Platform***
Po-Yao Lin, Kathy Yan, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.

***25. Electrical and Thermo-Mechanical Analysis of TSVs With Air Gap-Isolation for RF/mmWave Applications***
Shane Oh, Ting Zheng, Wanshu Zeng, Geyu Yan, Muhannad S. Bakir – Georgia Institute of Technology

***26. Evaluation of Parylene-HT as Dielectric for Application in Advanced Package Substrates***
Pratik Nimbalkar, Mohanalingam Kathaperumal, Madhavan Swaminathan, Rao Tummala – Georgia Institute of Technology

***27. D2W Hybrid Bonding Using High Accuracy Carrier Solutions for 3D System Integration***
Thomas Uhrmann, Mariana Pires, Juergen Burggraf, Julian Bravin, Markus Wimplinger – EV Group, Inc.; Chun Ho Fan, Hoi Ping Ng, Siu Cheung So, Ming Li, Siu Wing Lau – ASMPT Hong Kong, Ltd.

***28. SiC Power Module Packaging and Interconnections Using Flexible Hybrid Electronics Materials and Processes***
Riadh Al-Haidari, Mohammed Alhendi, Dylan Richmond, El Mehdi Abbara, Abdullah Obeidat, Mark Poliks, Mark Schadt – Binghamton University; Arun Gowda, Jeffrey Erlbaum, Han Xiong, Collin Hitchcock – GE Research

***29. Bottom Side Cooling for Glass Interposer With Chip Embedding Using Double-Sided Release Process for 6G Wireless Applications***
Joon Woo Kim, Xingchen Li, Xiaofan Jia, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology

***30. Demonstration of TSV-less Efficient and Cost-Effective Power Delivery for Large Interposers and Wafer-Scale Systems***
Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

***31. Metal Additively Microfabricated SiPs With Embedded Microfluidic Cooling Towards Heterogeneous Integration With SoCs***
Bhushan Lohani, Sheikh Dobir Hossain, Robert C. Roberts – University of Texas, El Paso

***32. The Factors Influencing Underfill's Reliability in Large-Size Packages***
Guolin Zhao, Wenhui Zhu – Central South University; Pengli Zhu – Chinese Academy of Science-Shenzhen Institute of Advanced Technology; Chingping Wong – Georgia Institute of Technology

***33. Wafer-Scale III-V on Silicon Reconstitution With Metal-Metal Thermocompression Bonding***
Ankit Kuchhangi, Krutikesh Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

**Wednesday May 31, 2023, 2:30 p.m. – 4:30 p.m.**

**Session 38: Interactive Presentations 2**

**Committee: Interactive Presentations**

**Session Co-Chairs:**
**Rao Bonda – Amkor Technology, Inc.**
**Email: rao.bonda@amkor.com**

**Mohammad Enamul Kabir – Intel Corporation**
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**Saikat Mondal – Intel Corporation**
**Email: saikat.mondal@intel.com**

**Donna M. Noctor – Nokia Corporation**
**Email: donna.noctor@nokia.com**

***1. Advanced Overlay Metrology for CIS Bonding Applications***
Florent Dettoni, Emilie DELOFFRE – STMicroelectronics; Yoav Grauer, Shlomo Eisenbach, Motti Penia, Arkadi Simkin, Dror Elka, Avner Safrani, Marco Polli, Francesco De Paola – KLA Corporation

***2. Implementation of New Robustness Assessment Methodology for Crack Stop Constructions by Using Dedicated Binning in Automated Optical Inspection***
Maria Heidenblut, Michael Goroll – Infineon Technologies AG

***3. Comparable Study for Redistribution Layers in FO POP RDL First and Last (Fan-Out Package on Package)***
Kuei Hsiao Kuo, Derrick Tai, Sam Peng, Feng Lung Chien – SPIL

***4. Hybrid Bonding Utilizing Molding Compound and Dielectric Systems***
Yuki Imazu, Kazuyuki Mitsukura – Resonac Corporation

***5. A Short Time and N2-sinterable Cu Sinter Paste With Highly Dispersed Submicron Cu Particles***
Takaaki Eyama, Shuichi Inaya, Ukyo Suzuki, Masafumi Takesue – Kao Corporation

***6. A Novel and Simple Method of Low Temperature, Low Process Time, Pressureless Interconnection for 3D Packaging***
Jeng-Hau Huang, Po-Shao Shih, Chang-Hsien Shen, Vengudusamy Renganathan, Simon Johannes Graefner, Yu-Chun Lin, C. Robert Kao – National Taiwan University; Chin-Li Kao, Yung-Sheng Lin, Yun-Ching Hung, Chun-Wei Chiang – Advanced Semiconductor Engineering, Inc.

***7. 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding by High-Precision Alignment Technologies***
Hajime Mitsuishi, Hiroshi Mori, Hidehiro Maeda, Mikio Ushijima, Atsushi Kamashita, Masashi Okada, Masanori Aramata, Takashi Shiomi, Shinya Sakamoto, Kishou Takahata, Tomohiro Chiba, Minoru Fukuda, Masahiro Kanbayashi, Toshimasa Shimoda, Isao Sugaya – Nikon Corporation

## Interactive Presentations: Wednesday, May 31, 2:30 p.m. - 4:30 p.m. and Thursday, June 1, 10:00 a.m. - 12:00 Noon

***8. Multi-Stack Hybrid Cu Bonding Technology Development Using Ultra-Thin Chips***
Min-Ki Kim, Hyuekjae Lee, Aeni Jang, Seungduk Baek, Ilhwan Kim, Youngkun Jee, Hyun-Chul Jung, Un-Byoung Kang, Dae-Woo Kim – Samsung Electronics Co., Ltd.-Test and System Package

***9. An Investigation on Particle Embedding Capability of Wafer Level Spin-on Polymer Underfill Enabling Low Temperature Bonding of Hybrid Bonding System***
Hiroto Noda, Akito Hiro, Naoki Nishiguchi – JSR Corporation; Jaber Derakhshandeh, John Slabbekoorn, Eric Beyne – imec

***10. Effect of Chip Metallization and Process Parameters on the Die Attach Properties of Direct Bonded Power Devices***
Michael Curkin, Marius Koehler, Nicolas Heuck – Hamm-Lippstadt University of Applied Sciences; Silke Kraft, Jens Mueller, Kurt-Georg Besendoerfer – SEMIKRON Elektronik GmbH & Co. KG

***11. Full-IMC Interconnects Through Transient Liquid Phase Bonding Process of Ga/Cu System for Advanced Electronic Packaging***
Yi Chen, Zhaoxia Zhou, Changqing Liu – Loughborough University

***12. Selective Self-Assembled Monolayer for Copper Surface Protection During Plasma Activation of Hybrid-Bonded Wafers***
Jack Rogers – TEL Technology Center, America, LLC

***13. Development of a Heterogeneous Integration of GaN Power Device on Si-LSI***
Shinei Miyasaka, Yusuke Norihide, Ayano Furue, Satoko Shinkai, Satoshi Matsumoto – Kyushu Institute of Technology

***14. Seed Layer Etching, Thermal Reflow and Bonding of Cu-Sn Micro Bumps With 5 µm Diameters***
Yunfan Shi, Zilin Wang, Zheyao Wang – Tsinghua University

***15. Integrated pH and Strain Sensors Development for Nasogastric Tube Placement Application***
Ruiqi Lim, Yu Chen, James Ven Wee Yap, Musafargani Sikkandhar, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

***16. Portable Multiple-Channel Ion-Selective Sensor***
Yu Chen, Musafargani Sikkandhar, James Ven Wee Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

***17. Chip-to-Chip Hybrid Bonding with Larger-Oriented Cu Grains for µ-Joints Beyond 100 K***
Murugesan Mariappan – GINTI, Tohoku University; Masahiro Sawa, Eriko Sone – JCU; Takamichi Miyazaki, Takafumi Fukushima – Tohoku University; Mitsumasa Koyanagi – T-Micro

***18. Application of Nickel Micro-Plating Bonding (NMPB) Technology to Crystalline Silicon Solar Cell Interconnection***
Xinguang Yu, Zhi Fu, Isamu Morisako, Keiko Koshiba, Tomonori Iizuka, Kohei Tatsumi – Waseda University

***19. Embedded Microchannel Cooling System Based on Flexible Manifold for High-Performance Computing ICs***
Jie Wang, Yanmei Kong, Binbin Jiao, Ruiwen Liu, Yuxin Ye, Xiangbin Du, Lihang Yu, Yulin Shi, Shichang Yun, Dichen Lu, Ziyu Liu, Jingping Qiao – Institute of Microelectronics Chinese Academy of Sciences

***20. CMOS-Compatible Fine Pitch Aluminum to Aluminum Bonding***
Hemanth Kumar Cheemalamarri, Binni Varghese, Sharma Jaibir, Hongyu Li, B. S. S. Chandra Rao, Navab Singh, Srinivasa Rao Vempati, King-Jien Chui – Institute of Microelectronics A*STAR

***21. Forming of Advanced THT-Interconnects Using SB² Laser Solder Jetting Process***
Matthias Fettke, Anne Fisch, Georg Friedrich, Moshir Nasser, Thorsten Teutsch – Pac Tech GmbH

***22. Board Level FEA Reliability and Stress Modeling for Chip-to-Wafer Bonded Chiplet Package***
Rathin Mandal, Chai Tai Chong – Institute of Microelectronics A*STAR

***23. High Density VR Solution Using Immersion Cooling***
Jesus G. Ruelas Flores, Arturo Sanchez Hernandez, Ernesto A Padilla Ramirez, Oscar A Del Rio Gonzalez, Carlos E Mora Flores, Andres Ramirez Macias – Intel Corporation

***24. Demonstration of Eight Metal Layer Redistribution on Glass Substrate With Fine Features and Microvias***
Christopher Blancher, Mohanalingam Kathaperumal, Fuhan Liu, Madhavan Swaminathan – Georgia Institute of Technology

***25. Novel IR Laser Cleaving for Ultra-Thin Layer Transfer and 3D Stacked Devices***
Thomas Uhrmann, Peter Urban, Boris Povazay, Michael Josef Gruber, Julian Bravin, Daniel Burgstaller, Markus Wimplinger, Bernd Thallner – EV Group, Inc.

***26. Robust Edge Coupling Probe Applied in Wafer-Level Optical Testing***
Sheng-Ho Huang, Chen-Yu Lin, Yi-Keng Fu – Industrial Technology Research Institute; Mei-Ju Lu, Sin-Yuan Mu, Chia-Sheng Cheng, Jihan Chen – ASE Corporate R&D Center

***27. An Intensive Study of Effects of Orientations of Single Crystal Cu Bumps on Cu-Cu Direct Bonding for 3D Integration by Molecular Dynamics Simulation***
Deng-Wu Zheng, Min-Bo Zhou, Shuai Liu, Chang-Bo Ke, Xin-Ping Zhang – South China University of Technology

***28. Reconstituted-$SiO_2$ Tier With Integrated Copper Heat Spreader***
Ashita Victor, Madison Manley, Shane Oh, Muhannad S. Bakir – Georgia Institute of Technology

***29. Reflow Oven Zone Temperature Advisor Using the AI-Driven Smart Recipe Generator***
Yangyang Lai, Junbo Yang, Jong Hwan Ha, Pengcheng Yin, Karthik A. Deo, Seungbae Park – Binghamton University

***30. A Technical Review on State of the Art In-Plane and Out-of-Plane Deformation Measurement Techniques for Microelectronic Packages***
Karthik Arun Deo, Yangyang Lai, Junbo Yang, Jong Hwan Ha, Pengcheng Yin, Seungbae Park – Binghamton University

***31. A Novel Polymer-Based Ultra-High Density Bonding Interconnection***
Yu-Min Lin, Tsung-Yu Ou Yang, Ou-Hsiang Lee, Ching- Kuan Lee, Wei-Lan Chiu, Tao-Chih Chang, Hsiang-Hung Chang – Industrial Technology Research Institute; Michael Gallagher, Po-Yao Chuang, Po-Hao Tsai, Po-Chun Huang – DuPont Electronics and Industrial; Chang-Chun Lee – National Tsing Hua University

***32. Comparison of Sintering Methodologies for 3D Printed High-Density Interconnects (2.3 µm L/S) on Organic Substrates for High-Performance Computing Applications***
Shrivani Pandiya, Serge Ecoffey, Yann Beilliard, Dominique Drouin – University of Sherbrooke; Christophe Sansregret – Centre de Collaboration MiQroInnovation (C2MI); Isabel De Sousa – IBM Canada, Ltd.

***33. Formation and 3D Stacking Process of CMOS Chips With Backside Buried Metal Power Distribution Networks***
Naoya Watanabe, Yuuki Araga, Haruo Shimamoto, Katsuya Kikuchi – National Institute of Advanced Industrial Science and Technology; Makoto Nagata – Kobe University

***34. Cu Pillar With Nanoporous Copper Cap: A Step Towards Chip-to-Substrate Hybrid Bonding***
Ramon A. Sosa, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

**Thursday June 1, 2023, 10:00 a.m. – 12:00 Noon**

**Session 39: Interactive Presentations 3**

**Committee: Interactive Presentations**

**Session Co-Chairs:**
**Patrick Thompson – Texas Instruments, Inc.**
**Email: patrick.thompson@ti.com**

**Amanpreet Kaur – Oakland University**
**Email: kaur4@oakland.edu**

**Frank Libsch – IBM Corporation**
**Email: libsch@us.ibm.com**

**Yoichi Taira – Keio University**
**Email: taira@appi.keio.ac.jp**

***1. Voltage Controlled Nanoscale Magnetic Devices for Non Volatile Memory and Scalable Quantum Computing***
Jayasimha Atulasimha, Md Mahadi Rajib – Virginia Commonwealth University

***2. Polymer Optical Waveguide Type 3-D MUX Device for Mode Division Multiplexing Links***
Ryoto Ichinose, Takumi Kowatari, Takaaki Ishigure – Keio University

***3. Extracting Anisotropic Permittivity of PCB Substrate From VNA Measurement on a Rectangular Stripline Resonator Loaded With a Via Array***
Zhaoqing Chen, Hung Nguyen, Matteo Cocchini – IBM Corporation

***4. Silicon Photonic Co-Packaging: Adhesive Dispense Challenge and Control***
Paul Gond-Charton, Sebastien Gouin, Steve Pellerin, Richard Langlois, Patrick Jacques, Denis Blanchard, Eric Turcotte, Steve Whitehead, Elaine Cyr – IBM Corporation

***5. Design of Single Miniaturized Dielectric Resonant Antenna for Millimeter Wave 5G Application***
Chia-Chu Lai, Sam Lin, Teny Shih, Yu-Po Wang, Tom Tang, Mike Tsai, Ryan Chiu, Kevin Chang, Yu-Chang Dong – Siliconware Precision Industries Co., Ltd.

***6. Inverse Prediction of Capacitor Multiphysics Dynamic Parameters Using Generative Model***
Kart Leong Lim, Rahul Dutta, Mihai Rotaru – Institute of Microelectronics A*STAR

***7. New Interconnection Technologies Based on Ni Nano-Particle and Ni Micro-Plating Bonding Method***
Kohei Tatsumi, Keiko Koshiba, Yasunori Tanaka, Mayu Miyagawa, Xinguan Yu, Shun Furuya, Tomonori Iizuka – Waseda University

***8. High-Performance Amplifier Package Design for Heterogeneous Integration on Si-Interposer***
Teck Guan Lim, Lin Zhou, Haoran Chen, Eva Leong Ching Wai, Sasi Kumar Tippabhotla, Lin Ji, Gongyue Tang – Institute of Microelectronics A*STAR; Wei Jia Lu, Chee Heng Goh, Jun Wei Agnes Loh – DSO National Laboratories

***9. Through-Silicon-Via Architecture of 3D Integration for Superconducting Quantum Computing Application***
Jiexun Yu, Qian Wang, Yao Zheng, Changming Song, Junpeng Fang, Zheyao Wang, Jian Cai – Tsinghua University; Tiefu Li – Tsinghua University/Beijing Academy of Quantum Information Sciences; Haihua Wu – Beijing Academy of Quantum Information Sciences

***10. Additive Manufacturing of Millimeter Wave Passive Circuits on Ultra-Thin Alumina Substrates***
Ethan Kepros, Yihang Chu, Bhargav Avireni, Brian Wright, Premjeet Chahal – Michigan State University

***11. Frequency Selective Surface (FSS) Based Antenna Array Design for Satellites Capable of All Four Polarizations***
Lih-Tyng Hwang, Ming-Yuan Huang, Hung-Chih Lin – National Sun Yat-Sen University

***12. Novel Low-Loss IC Substrate Material for 5G IC Packaging***
Tomo Mugurma, Andy Behr, Tom Shin – Panasonic Industrial Devices Sales Company of America; Umehara Hiroaki, Saeki Yuya, Kishino Koji – Panasonic Industry Co., Ltd.

***13. Deep Learning Based Refinement for Package Substrate Routing***
Peng-Tai Huang, Tsubasa Koyama, Tsung-Yi Ho – National Tsing Hua University; Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

***14. Laser Integration on Photonic Integrated Circuit With High Alignment Accuracy for Data Transmission***
Ting Ta Chi, Zhenyu Li, Nanxi Li, Hong Cai, Y. M. Tobing Landobasa, Haitao Yu, Senthilkumar Darshini, Jae Ok Yoo, Hwang Gilho, Jeroen Van Borkulo, Lennon Y. T. Lee, Wen Lee – Institute of Microelectronics A*STAR

***15. Copper Nanowired Interconnection for Embedding Power Dies in PCB***
Caio Cesar De Oliveira Mendes, Julien Morand, Guillaume Lefevre – Mitsubishi Electric R&D Centre Europe; Vincent Bley, Jean-Pascal Cambronne – University of Toulouse-LAPLACE

***16. High Density Photonic Reservoir Computing Using Optical Fiber and Polymer Waveguide***
Hidetoshi Numata, Toshiyuki Yamane, Daiju Nakano – IBM Research, Tokyo/IBM Corp., Japan; Jean Heroux – IBM Systems/IBM Corp., Canada

***17. Machine Learning Based PCB/Package Stack-Up Optimization for Signal Integrity***
Wenchang Huang, Jiahuan Huang, Chulsoon Hwang – Missouri University of Science and Technology; Minseok Kim, Bumhee Bae, Subin Kim – Samsung Electronics Co., Ltd.

***18. Self-Aligned Optical Connector Assembly on Polymer Waveguide Integrated Package Substrate for Co-Packaged Optics***
Akihiro Noriki, Takeru Amano – National Institute of Advanced Industrial Science and Technology

***19. Solder Paste Stamping Process Investigation for Heterogeneous Integration of III-V Lasers on a 300 mm Si Photonics Platform***
Sarah Baranowski, Javery Mann, Lewis Carpenter, Amit Dikshit, Colin McDonough, David Harame – SUNY Research Foundation

***20. 2.5D Silicon Photonics Interposer Flip Chip Attach***
Pushkraj Tumne, Joseph Wang, Dwayne Shirley, Roberto Coccioli – Marvell Semiconductor, Inc.

***21. A Study of the Design and Parameter Effects on System Level Characteristics of Advanced Fan-Out Wafer Level Package (FOWLP): Results from In-Situ Analysis***
Kyoung-Lim Suk, Jihwang Kim, Suchang Lee, Jaechoon Kim, Wonkyung Choi, Dongwook Kim – Samsung Electronics Co., Ltd.

***22. Development of Electronic-Photonic 3D System in Package: Architecture, Integration, and Scaling***
Jugal Kishore Bhandari, Venkata Ramana Pamidighantam, Divya Sri Rajeswari, Rohin Kumar Yeluripati – LightSpeed Photonics Pte Ltd

***23. Additive Manufacturing of Strain Gages for High Temperature Application***
Nicolas Delavault, Tanguy Lacondemine, Remy Kalmar, Manuel Fendler – CEA Tech Grand Est; Sofiane Achache, Frederic Sanchette – UTT LASMIS

***24. Highly Compact and High Gain 2 x 2 Patch Array Antenna With Slotted Meanderline Loading***
Hanna Jang, Payman Pahlavan, Yong-Kyu Yoon – University of Florida

***25. Highly Energy Efficient and Electromagnetic Interference Immuned Coaxial Through-Substrate-Vias (cx-TSVs) for Millimeter Wave Applications***
Saeyeong Jeon, Hae-In Kim, Yong-Kyu Yoon – University of Florida

***26. Design of a Compact Size-Bridge Connected Multiband MIMO Antenna for Automotive 5G and DSRC Communications System***
Mohammad Pervez, Amanpreet Kaur – Oakland University

***27. A Fully Additive Fabrication Approach for Creating Small Microvia With Diameter < 10 µm Suitable for 3-D System-in-Package Integration***
Roghayeh Imani, Shailesh Chouhan, Jerker Delsing – Lulea University of Technology; Sarthak Acharya, Jussi Putaala, Juha Hagberg, Sami Myllymaki, Olli Nousiainen, Heli Jantunen – University of Oulu

***28. The Performance and Reliability of Flexible Screen-Printed Multilayer Conductive Leads for Wearable Vital Sign Monitoring Devices***
Kankanige Udara Somarathna, Behnam Garakani, Mohammed Alhendi, Mark Poliks – Binghamton University; Darshana Weerawarne – University of Colombo; Matthew Misner, Andrew Burns, Gurvinder Khinda, Azar Alizadeh – GE Global Research

***29. First Demonstration of Die-Embedded Alumina Ribbon Ceramic (ARC) Packaging for 6G Wireless Applications***
Joon Woo Kim, Nahid Aslani-Amoli, Fuhan Liu, Madhavan Swaminathan – Georgia Institute of Technology; Rajesh Vaddi, Garima Nagar – Corning, Inc.

***30. Security Robustness of Buried Power Rail Interconnect Technology: Modeling, Analysis and Countermeasures***
Sirish Oruganti, Nishant Gupta, Sai Subrahmanya Teja Nibhanupudi, Meizhi Wang, Jaydeep Kulkarni – University of Texas, Austin

***31. Intelligent Multi-Physics Design and Demonstration of Compact, Leadframe-Based SiC Power Modules for Transportation Electrification***
Emanuel Torres Surillo, Christian Molina-Mangual, Vanessa Smet – Georgia Institute of Technology

**Thursday June 1, 2023, 2:30 p.m. – 4:30 p.m.**

**Session 40: Interactive Presentations 4**

**Committee: Interactive Presentations**

**Session Co-Chairs:**
**Mark Eblen – Kyocera International SC**
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**Kuo-Ning Chiang – National Tsing Hua University**
**Email: knchiang@pme.nthu.edu.tw**

**Jeffrey Lee – iST-Integrated Service Technology, Inc.**
**Email: jeffrey_lee@istgroup.com**

**Karan Bhangaonkar – Intel Corporation**
**Email: karan.r.bhangaonkar@intel.com**

***1. Simulation of Solder Crack Phenomenon in Molding Process***
Tzu Chieh Chien, Shih Kun Lo, Zong Yuan Li, Yen Hua Kuo, Ming Shaw Shy, Hui Chung Liu, Lu Ming Lai, Kuang Hsiung Chen – Advanced Semiconductor Engineering, Inc.

***2. Automated Solder Joint Failure Mode Analysis Based on Dry and Pry Image Processing***
Yinan Lu, Chun-Sean Lau, Zhi Zhang Koh, Chaolun Zheng, Bo Yang – Western Digital Corporation

***3. Embedded Micro-Pin Fin Heat Sink of Two-Phase Liquid Cooling for High Heat Flux 3D ICs***
Huicheng Feng, Gongyue Tang, Xiaowu Zhang, Boon Long Lau, Ming Chinq Jong, Keng Yuen Jason Au, King Jien Chui – Institute of Microelectronics A*STAR; Jing Lou, Hongying Li, Duc Vinh Le – Institute of High Performance Computing A*STAR

***4. Warpage Estimation of Panel-Level Package from Panel to Strip by Using Multi-Scaling Sub-Modeling Technique***
Chang-Chun Lee, Chi-Wei Wang, Che-Pei Chang, Jui-Chang Chuang – National Tsing Hua University

***5. A Thermally Friendly Bonding Scheme for 3D System Integration***
Gordon Kuo, J. Y. Chen, C. C. Hsieh, C. J. Lee, Jason Wu, James Cui, Y. L. Kuo, C. H. Tung, KC Yee, Doug Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

***6. Effects of Twin Boundary and Precipitates on Board Level Reliability in Sn-Ag-Cu (SAC) Solder Joints Through EBSD Analysis***
DaJin Yoon, Byoungdo Lee, Jihye Kim, Sungho Hyun, Gyujei Lee, Kangwook Lee – SK Hynix, Inc.

***7. Optimization of 2.2D Underfill Process by Novel Methodology and Direct Observation of Capillary Underfill Process***
Chia-Peng Sun, Yu-En Liang – CoreTech System (Moldex3D); Dyi-Chung Hu, Er-Hao Chen – SiPlus Co., Ltd.; Jeffrey ChangBing Lee – iST-Integrated Service Technology, Inc.; Srikar Vallury – Moldex3D Northern America, Inc.

***8. Reliability in Selective Thinning Technology of Solder Resist for New IC Substrate Architecture***
Yuya Suzuki – Taiyo Ink Mfg. Co., Ltd.; Yuji Toyoda – Mitsubishi Paper Mills Ltd.

***9. Simulation, Verification, and Prediction of the Corrosion Behavior of Cu-Ag Composite Sintered Paste for Power Semiconductor Die-Attach Applications***
Xinyue Wang, Zhoudong Yang, Pan Liu – Fudan University; Guoqi Zhang – Delft University of Technology; Jing Zhang – Heraeus Materials Technology Shanghai Ltd.

***10. Thermal Characterization and Management of GaN-on-SiC High Power Amplifier MMIC***
Yong Han, Gongyue Tang, Boon Long Lau – Institute of Microelectronics A*STAR

***11. A Thin-Film Reconfigurable SiC Thermal Test Chip for Reliability Monitoring in Harsh Environments***
Romina Sattari, Henk van Zeijl, GuoQi Zhang – Delft University of Technology

***12. Life-Prediction of SAC305/Bi-Based Hybrid Solder Joint Considering Bi-Diffused Layers With Gradual Bi Concentrations***
Yongrae Jang, Bongtae Han – University of Maryland; Hak-Sung Kim – Hanyang University

***13. Thermal-Mechanical-Electrical Co-Design of Fan-Out Panel-Level SiC MOSFET Packaging With Multi-Objective Optimization Algorithm***
Wei Chen, Xuyang Yan, Jiajie Fan – Fudan University; Mesfin S. Ibrahim – Hong Kong Polytechnic University; Jing Jiang – Sky Chip Interconnection Technology Co., Ltd.; Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology

***14. SU8 Out of Plane Stress Control Via Design of Experiment and Machine Learning***
Ziqi Jia, Shuyu Shi, Yong-Kyu Yoon – University of Florida

***15. Mold Flow Simulation on Wire Sweep for Two-Stack NAND BGA Package***
Hengxu Yu, Yangming Liu, Shenghua Huang, Bo Yang, Ning Ye – Western Digital Corporation

***16. Assessment Methods for the Characterization of Flux Material Systems Toward Water Absorption***
Quang-Duc Pham, Norbert Holle – Robert Bosch GmbH; Juergen Wilde – University of Freiburg

***17. Optimization of the Cu Microstructure to Improve Cu-to-Cu Direct Bonding for 3D Integration***
Ralf Schmidt, Christian Schwarz – Atotech (MKS Instruments)

***18. Addressing Sub-Micron Thermal Warpage: Industrial Application***
Safia Benkoula – STMicroelectronics; Rodolfo Cruz, Pierre Vernhes – INSIDIX

***19. Long-Term Reliability Evaluation on Single-Phase Immersion Cooling Based Server With Electronic Fluorinated Liquid***
Yangfan Zhong, Fangzhi Wen, Rui Guo, XiaoPeng Li, Dan Liu, YongBao He – Alibaba Group; Haifeng Gong – Intel Corporation

***20. Effect of Ceramic Filler in Epoxy Mold Compound on Thermomechanical Property of FOWLP***
Taejoon Noh, Haksan Jeong, Seung-boo Jung – Sungkyunkwan University

***21. ARTSim: A Robust Thermal Simulator for Heterogeneous Integration Platforms***
Yousef Safari, Adam Corbier, Dima Al Saleh, Boris Vaisband – McGill University

***22. Atomistic Simulation Analysis of Plasma Surface Activation in Wafer-to-Wafer Oxide Fusion Bonding***
Hojin Kim, Yu-Hao Tsai, Satohiko Hoshino, Ilseok Son, Kaoru Maekawa, Peter Biolsi, Sitaram Arkalgud – TEL Technology Center, America, LLC

***23. Inorganic Capping Layers in Advanced Photosensitive Polymer Based RDL Processes: Processing and Reliability***
Nelson Pinho, Emmanuel Chery, John Slabbekoorn, Mikhail Krishtab, Andy Miller, Eric Beyne – imec; Ritwik Bhatia, Ganesh Sundaram – Veeco

***24. A Combined Simulation and Experimental Study on Cracking and Delamination Behavior at the Cu/Polyimide Interface of RDLs in Chiplet Package Subjected to Thermos-Mechanical Loads***
Bin Chen, Guang-Chao Lyu, Hong-Guang Wang, Long Zheng, Yun-Kai Deng, Xin-Ping Zhang – South China University of Technology

***25. Evolution of the Creep Response of SAC+Bi Lead Free Solders Subjected to Various Thermal Exposures***
Mohammad Al Ahsan, S. M. Kamrul Hasan, Jeffrey Suhling, Pradeep Lall – Auburn University

***26. Modeling Grain Size Effects on Deformation Behavior of SAC Solder Joints***
Debabrata Mondal, Jeffrey Suhling, Pradeep Lall – Auburn University

***27. Reliability Study on High Performance Photo Imageable Dielectric for Advanced Package***
Okseon Yoon, Jinyoung Kim, Kiseok Kim, Seonghyun Yoo, Jihye Shim, Suchang Lee, Hyoeun Lee, Sueryeon Kim – Samsung Electronics Co., Ltd.

***28. A Novel Indium Metal Thermal Interface Material and Package Design Configuration to Enhance High-Power Advanced Si Package Thermal Performance***
Kuo-Chin Chang, Mirng-Ji Lii, Kuan-Min Wang, Chien-Chang Wang, Bang-Li Wu – Taiwan Semiconductor Manufacturing Company, Ltd.

***29. High Temperature Storage of Cu-Cu Joints Fabricated by Highly (111)-Oriented Nanotwinned Cu***
Shih-Chi Yang, Chih Chen – National Yang Ming Chiao Tung University

## Interactive Presentations: Thursday, June 1, 2:30 p.m. - 4:30 p.m and Friday, June 2, 10:00 a.m. - 12:00 p.m.

***30. Ionic Sensor Package Design for the Survivability in Drop-Impact During Deployment***
Pengcheng Yin, Jong Hwan Ha, Junbo Yang, Yangyang Lai, Seungbae Park – Binghamton University; Biju Jacob, Arun Gowda – GE Research

***31. Time-Dependent Bulk Behavior of Partially Cured Epoxy Molding Compound***
Sukrut Prashant Phansalkar, Bongtae Han – University of Maryland, College Park

***32. High-Performance, Multilayer Copper-Graphene Micro-Foam Wicks for Vapor Chambers***
James Moss, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

***33. Module, Antenna, and Package Design Considerations for mm-Scale IoT devices***
Arun Paidimarri, Duixian Liu, Christian Baks, Bodhisatwa Sadhu, Alberto Valdes-Garcia – IBM Research

***34. 9W/cm$^2$/K Heat Transfer Coefficient Vapor Chamber for HPC Server Cooling Applications***
Takashi Funakoshi, Katsunori Komehana – Fujikin, Inc.; Hiroyoki Ryoson, Kosuke Suzuki, Tomoji Nakamura, Takayuki Ohba – Tokyo Institute of Technology

**Friday June 2, 2023, 10:00 a.m. – 12:00 Noon**

**Session 41: Student Interactive Presentations**

**Committee: Interactive Presentations**

**Session Co-Chairs:**
**Alan Huffman – SkyWater Technology**
**Email: alan.huffman@ieee.org**

**Biao Cai – IBM Corporation**
**Email: biaocai@us.ibm.com**

**Pavel Roy Paladhi – IBM Corporation**
**Email: rpaladhi01@gmail.com**

**Jin Yang – Samsung Electronics**
**Email: jin1.yang@ieee.org**

***1. An Ultra-Fine Wiring Method for Polymer-Based Embedded Silicon Fan-Out Packaging (P-eSiFO)***
Lang Chen, Bo Wen, Xiao Han, JinWen Zhang, Wei Wang, Chenxi Lin – Peking University-Institute of Microelectronics

***2. Grain Orientation, Microstructure Evolution and Fatigue Life Prediction of Solder Joints Under Thermal Shock Test for Fan-Out Wafer Level Packaging***
Shuye Zhang, Xinyi Jing, Peng He – Harbin Institute of Technology; Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

***3. Warpage Modeling and Optimization for Polymer-Based Embedded Silicon Fan-Out Packaging (P-eSiFO) During Thermal Process Loadings***
Jianyu Du, Lang Chen, Han Xu, jinwen Zhang, Wei Wang – Peking University

***4. Alternative Copper-to-Copper Direct Bonding Process Using Current-Induced Bonding Method***
Byungkwan Kwak, Jinhyun Lee, Sanghwa Yoon, Bongyoung Yoo – Hanyang University

***5. Secure and Scalable Key Management for Waferscale Heterogeneous Integration***
Yousef Safari – McGill University/University of California, Los Angeles; Pooya Aghanoury, Subramanian S. Iyer, Nader Sehatbakhsh – University of California, Los Angeles

***6. A Method to Improve 3D Interconnections Resource Utilization and Reliability in Hybrid Bonding Process Considering the Effects on Signal Integrity***
Ang Li, Jianfei Jiang, Qin Wang, Zizheng Dong, Shuya Ji, Xiulan Cheng, Yuhang Zhao – Shanghai Jiao Tong University

***7. Wafer-Level Integration of Atomic Vapor Cell Chip With Thermal and RF Modules***
Ziji Wang, Jintang Shang – Southeast University

***8. Optimization of Embedded Manifold Cooling Characteristic Parameters for GaN HEMT***
Dichen Lu, Yuxin Ye, Mei Wu, Ruiwen Liu, Xiangbin Du, Lihang Yu, jie Wang, Jingping Qiao, Ziyu Liu, Yulin Shi, Binbin Jiao, Yanmei Kong – Chinese Academy of Science-Institute of Microelectronics

***9. Low-Stress TSVs for High-Density 3D Integration***
Jingping Qiao, Binbin Jiao, Shiqi Jia, Ruiwen Liu, Shichang Yun, Yanmei Kong, Yuxin Ye, Xiangbin Du, Lihang Yu, Dichen Lu, Ziyu Liu – Chinese Academy of Science-Institute of Microelectronics; Jie Wang – Institute of Microelectronics, Chinese Academy of Science, Beijing, China

***10. Low Dk/Df Thermosetting Siloxane Hybrid Material for Fabrication of Microwave Communication Printed Circuit Board***
Seung-Mo Kang, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology

***11. Optimization of Si Phononic MEMS Nanowires for Ultra-Low Thermal Conductivity***
Sunghyun Hwang, James D. Overmeyer, S. M. Enamul Hoque Yousuf, Philip X.-L. Feng, Yong-Kyu Yoon – University of Florida; William N. Carr – Phononic MEMS, Inc.

***12. Rapid Formation of High-Strength Sintered Silver Joints With High Reliability***
Xu Zhang, Pengli Zhu, Tao Zhao, Liang Xu, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology

***13. Reference Thermal Chips for 2D and 3D Co-Packaging Process Development***
Parnika Gupta, Robert Bernson, Noreen Nudds, Sean Collins, Kamil Gradkowski, Padraic E. Morrissey, Peter O' Brien – Tyndall National Institute-Photonic Packaging

***14. Wideband Circular Polarized FOWLP Antenna in Package for Satellite Communications***
KaiBo Zheng, Mei Sun – Institute of Microelectronics A*STAR; Yongxin Guo – National University of Singapore

***15. A High Precision Analysis Method Based on Thermal Test Chip for Thermal Characteristics of Thermal Interface Materials***
Yulin Shi, Binbin Jiao, Qixing Hao, Yanmei Kong, Ruiwen Liu, Shichang Yun, Yuxin Ye, Lihang Yu, Xiangbin Du, Jie Wang, jingping Qiao, Dichen Lu – Chinese Academy of Science-Institute of Microelectronics

***16. A Bionic Sweating Cooling Method for High Power Chip Based on Evaporation and Convection***
Lihang Yu, Binbin Jiao, Yuxin Ye, Xiangbin Du, Yanmei Kong, Ruiwen Liu, Shichang Yun, Yulin Shi, Jie Wang, Dichen Lu, Ziyu Liu, Jingping Qiao – Institute of Microelectronics Chinese Academy of Sciences

***17. Generative Adversarial Network Based Adaptive Transmitter Modeling***
Priyank Kashyap, Prasanth Prabu Ravichandiran, Dror Baron, Chau-Wai Wong, Tianfu Wu, Paul Franzon – North Carolina State University

***18. FISHI: Fault Injection Detection in Secure Heterogeneous Integration Via Power Noise Variation***
Tao Zhang, Md Latifur Rahman, Hadi Mardani Kamali, Kimia Zamiri Azar, Mark Tehranipoor, Farimah Farahmandi – University of Florida

***19. Wafer-Level Vacuum Packaging for Micro-Spherical Atomic Vapor Cell***
Wenqi Li, Jintang Shang, Ziji Wang, Jin Zhang – Southeast University

***20. Design and Fabrication of Manifold Microfluidic Cooling Package Structure Based on Embedded Silicon Fan-Out (eSiFO)***
Yuchi Yang, Peijue Lyu, Jianyu Du, Lang Chen – Peking University; Zhou Yang – China University of Geosciences Beijing

***21. RFID Based Vehicular Positioning System for Safe Driving Under Adverse Weather Conditions***
Bhargav Avireni, Yihang Chu, Ethan Kepros, Premjeet Chahal – Michigan State University

***22. Fingerprint Extrication With Near-Field Terahertz Time-Domain Spectroscopy (THz-TDS) for IC Hardware Assurance***
Chengjie Xi, John True, Navid Asadizanjani – University of Florida

***23. Additively Manufactured Near Chip Scale Interposers for DC and RF Applications***
Emily Lamport, Andrew M. Luce, Yuri Piro, Alkim Akyurtlu – UMass Lowell; Susan Trulli – Raytheon Technologies

***24. Evaluation of Electromechanical Performance of a Flexible Hybrid Electronics Temperature Monitor***
Zhi Dou, Dylan Richmond, Mark Schadt, Mohammed Alhendi, Mark Poliks – Binghamton University; Rafael Tudela – Tapecon, Inc.

***25. Comparative Mechanical Behavior of Sn-Bi based Low Temperature Solder Alloys Under Different Pad Surface Finish and Pretest Aging Conditions***
Sukshitha Achar P L, Colin Greene, Sean Lai, Radu Radulescu, Hannah Fowler, John Blendell, Corol Handwerker, Ganesh Subbarayan – Purdue University; Nilesh Badwe – Indian Institute of Technology Roorkee; Raiyo Aspandiyar – Intel Corporation

***26. New Concentrated Photovoltaic (CPV) Module Architecture***
Konan Kouame, Maxime Darnon, Gwenaelle Hamon – University of Sherbrooke

***27. Characterization of Packaging, Electronic, and Photonic Materials at Cryogenic Temperatures Using a Multi-Angle Backscattering Mueller-Matrix Ellipsometer***
Christopher Lewis, Jacob Marchio, Drew Sellers, Michael Hamilton – Auburn University

***28. A Comparison of Dual-Band Wearable Metasurfaces***
Adria Kajenski, Guinevere Strack, Alkim Akyurtlu – University of Massachusetts, Lowell; Shahriar Khushrushahi – Notch, Inc.

***29. TrueAdapt™ - AI Based Maskless Patterning to Compensate for Die-Shift in Fan-Out Wafer Level Packaging***
Golam Sabbir, Subramanian S. Iyer, Lenny Wu, Henry Sun – University of California, Los Angeles

***30. Optimization of Copper Filled Through Package Via Geometry to Minimize Thermal Induced Stresses at Glass - TPV interface in Borosilicate Glass Interposer***
Krishna Bhavana Sivaraju, Viswanatham Puligandla, Rabin Bhandari, Dereje Agonafer – University of Texas, Arlington; Akhil R. K. Kalapala – Intel Corporation

***31. Fabrication of Flexible and Stretchable Highly Conductive Ag-PDMS Tri-Layer Interconnect and Its Integration Into Li-ion Pouch Cells***
Mayukh Nandy, Siyang Liu, Hongbin Yu – Arizona State University

***32. High-Density Array of 50 µm-Pitch Compressible MicroInterconnects in a Replaceable Integrated Chiplet Assembly***
Michael Nieves Calderon, Shengtao Yu, Muhannad S. Bakir – Georgia Institute of Technology

***33. Die Embedded Glass Interposer With Minimum Warpage for 5G/6G Applications***
Xingchen Li, Xiaofan Jia, Joon Woo Kim, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology; Matthew Jordan – Sandia National Laboratories

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The 2023 ECTC Exhibition is pleased to showcase dozens of companies and organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, exhibitors and attendees will enjoy continual interactions with conference attendees. We are also excited to introduce the new ECTC Lounge, where attendees and exhibitors can take a few minutes to relax or converse with colleagues. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, May 31, 2023, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, June 1, 2023. Exhibit booth remaining availability is extremely limited for 2023. The 2023 Exhibit Application can be found at www.ectc.net and by clicking the 'Exhibits' link. For additional information or questions, please contact Alan Huffman, ECTC Exhibits Chair at +1-336-380-5124 or email alan.huffman@ieee.org and exhibits@ectc.net.

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**JW Marriott Orlando, Grande Lakes • 4040 Central Florida Parkway**
**Orlando, FL 32837, USA**

Hotel reservations for ECTC 2023 can be made one of two ways:

1) Contact the JW Marriott Orlando, Grande Lakes at +1-800-266-9432 and reference the ECTC Conference to receive the conference rate of US$233 per night.

or …

2) Log onto www.ectc.net and click on the Location tab near the top of the page to find a special online hotel registration link.

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Attendees should note that only reputable sites should be used to book a hotel room for the 2023 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2023 from 3rd party companies. These emails and sites are not to be trusted. **The only formal communication ECTC** will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com.

# 73rd Electronic Components & Technology Conference

| 2023 ECTC REGISTRATION INFORMATION | | | |
|---|---|---|---|
| **Conference Registration** | | **Advance Registration (until May 5)** | **Door Registration (May 6 and beyond)** |
| IEEE Member | Attendee (full ECTC conference) | US $825 | US $950 |
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| | Single PDC (a.m. or p.m.) | $490 | $490 |
| Student | Full PDC (both a.m. and p.m.) or Single PDC | $150 | $150 |
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| Extra Luncheon Tickets | | $75 | $75 |
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There will be no refunds or cancellations after May 5, 2023. Please note that a $50 cancellation fee will be in effect for all cancellations made on or prior to May 5, 2023. Substitutions can be made at any time.

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# CONFERENCE OVERVIEW

**May 30, 2023**

**Morning Professional Development Courses**
**8:00 a.m. - 12:00 p.m.**

1. High Reliability of Lead-Free Solder Joints – Materials Considerations
2. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals
3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Level and Advanced RF Packages
4. Eliminating Failure Mechanisms in Advanced Packages
5. Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components
6. Reliability Physics and Failure Mechanisms in Electronics Packaging
7. Reliable Integrated Thermal Packaging for Power Electronics
8. Introduction to PWB Thermal Analysis

**ECTC Special Session on Advanced Packaging for Harsh Environment**
**8:30 a.m. - 10:00 a.m.**
"Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities"

**ECTC Special Session on Hybrid Bonding**
**10:30 a.m. - 12:00 p.m.**
"Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications"

**Afternoon Professional Development Courses**
**1:30 p.m. - 5:30 p.m.**

9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability
10. Fan-Out Packaging and Chiplet Heterogeneous Integration
11. Photonic Technologies for Communication, Sensing, and Displays
12. Flip Chip Technologies
13. Packaging and Heterogeneous Integration for Automotive Electronics and Advanced Characterization of EMCs
14. Analysis of Fracture and Delamination in Microelectronic Packages
15. Polymers in Wafer Level Packaging
16. Thermal Management of Electronics

**ECTC Special Session on Photonics Packaging**
**1:30 p.m. - 3:00 p.m.**
"Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption"

**ECTC Special Session on CHIPS Act**
**3:30 p.m. - 5:00 p.m.**
"Advanced Packaging Manufacturing in North America: Building the Ecosystem"

**Young Professionals Networking Panel**
**7:00 p.m. - 7:45 p.m.**

**ECTC EPS Seminar on High-Density Substrates**
**7:45 p.m. - 9:15 p.m.**
"The Future of High-Density Substrates – Towards Submicron Technology"

**May 31, 2023**

**ECTC Keynote**
**8:00 a.m. - 9:15 a.m.**
"Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging"

**Technical Sessions**
**9:30 a.m. - 12:35 p.m.**

1. Heterogeneous Chiplet Integration
2. High-Performance Packaging Materials
3. Advancements in Copper/Silicon-Oxide Hybrid Bonding
4. Assembly and Manufacturing Process Enhancement
5. Flexible Packaging and Chip-Package-Interaction
6. Co-packaged Optical Assembly

**Interactive Presentation Session 37**
**10:00 a.m. - 12:00 p.m.**

**Wednesday Luncheon**
**12:45 p.m. - 2:00 p.m.**

**Technical Sessions**
**2:00 p.m. - 5:05 p.m.**

7. Large Formfactor Dense System Integration by FanOut
8. Novel Reliability Test Methods
9. Innovations in Copper Chip-to-Wafer Bonding
10. Packaging Interconnects
11. Additive Manufacturing and Packaging for Flexible Electronics
12. mm Wave Antenna-in-Package and Arrays

**Interactive Presentation Session 38**
**2:30 p.m. - 4:30 p.m.**

**ECTC/ITHERM Diversity and Career Growth Panel and Reception**
**6:30 p.m. - 7:30 p.m.**
"Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative"

**June 1, 2023**

**ECTC Plenary Session on mm-Wave Phased Array Packaging**
**8:00 a.m. - 9:15 a.m.**
"Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems"

**Technical Sessions**
**9:30 a.m. - 12:35 p.m.**

13. Wafer/Panel-Level and Advanced Substrate Technologies
14. Advances in Heterogeneous Integration Bonding Technology
15. Innovative Interposer and Through-Via Technologies
16. Sintering and Soldering for High-Power, High-Reliability, and RF Devices
17. Advanced Reliability Modelling and Characterization
18. Advanced Photonic Packaging and Interconnect

**Interactive Presentation Session 39**
**10:00 a.m. - 12:00 p.m.**

**EPS Awards Luncheon**
**12:45 p.m. - 2:00 p.m.**

**Technical Sessions**
**2:00 p.m. - 5:05 p.m.**

19. Advances in 3D Integration and Hybrid Bonding
20. Automotive/Board-Level Reliability
21. Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections
22. Large Substrate Process Integration Challenges
23. Next Generation Quantum, AI, and Secure System Design
24. High-Speed Signal and Power Integrity

**Interactive Presentation Session 40**
**2:30 p.m. - 4:30 p.m.**

**June 2, 2023**

**ECTC EPS President Panel Session on Photonics**
**8:00 a.m. - 9:15 a.m.**
"How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP"

**Technical Sessions**
**9:30 a.m. - 12:35 p.m.**

25. Next Generation High-Performance Computing Architectures
26. Materials Reliability
27. Next Generation Wafer-to-Wafer Copper Bonding
28. Process Enhancements in 3D, FOWLP, and TSV Technologies
29. AI-based Prediction for Heterogeneous Integration and Advanced Packaging
30. Trends in Encapsulants and Low Dk/Df Dielectrics

**Student Interactive Presentations Session 41**
**10:00 a.m. - 12:00 p.m.**

**Raffle Prize Luncheon**
**12:45 p.m. - 2:00 p.m.**

**Technical Sessions**
**2:00 p.m. - 5:05 p.m.**

31. MEMS Sensor, Bio, and Advanced Interconnect Reliability
32. Thermo-Mechanical Modelling and Characterization
33. Advances in RDL, Via, and TSV Technologies for Chiplet Integration
34. Bonding Assembly - Novel Packaging, Process, and Characterization
35. Packaging and Materials for Flexible Medical Technologies
36. RF, Heterogeneous, and Chiplet Modules

## Session Summary by Interest Area

**Packaging Technologies**
S1, S7, S13, S19, S25, S31

**Applied Reliability**
S8, S17, S20, S26, S31

**Assembly & Manufacturing Technology**
S4, S16, S22, S34

**Emerging Technologies**
S11, S23, S35

**RF, High-Speed Components & Systems**
S12, S24, S36

**Interconnections**
S3, S9, S15, S21, S27, S33

**Materials & Processing**
S2, S14, S16, S28, S30

**Thermal/Mechanical Simulation & Characterization**
S5, S10, S17, S29, S32

**Photonics**
S6, S18

**Interactive Presentations**
S37, S38, S39, S40, S41


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