Advance Program & Registration

Don't miss out on electronic packaging's premier conference!

ECTC

The 2020 IEEE 70th Electronic Components and Technology Conference

May 26 - May 29, 2020

Walt Disney World Swan & Dolphin Resort
Lake Buena Vista, Florida

For more information, visit: www.ectc.net

Sponsored by:

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

INTRODUCTION FROM THE IEEE 70TH ECTC PROGRAM CHAIR ROZALIA BEICA

The 70th Electronic Components and Technology Conference (ECTC)
Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, FL USA • May 26 - May 29, 2020

On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE's 70th Electronic Components and Technology Conference (ECTC), which will be held at Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida, USA from May 26 - 29, 2020. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions, and universities, all under one roof. More than 1,500 people have attended ECTC in each of the last three years.

At the 70th ECTC, around 380 technical papers are scheduled to be presented in 36 oral sessions and five interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, advanced substrates, assembly, materials modeling, reliability, packaging for harsh conditions, power packaging, interconnections, packaging for high speed and high bandwidth, photonics, and flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 70th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature six special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, May 26 at 9:30 a.m., Pavel Roy Paladhi and Nicholas Bronn will chair a special session covering "Bridge to Quantum Computing," On the same day at 2 p.m., Rena Huang and Harry Kellz will chair a session focusing on "Cutting-Edge Technology on Integrated Photonics and Packaging." Tuesday evening will also include the ECTC Panel Session at 7:30 p.m. chaired by IEEE EPS President Christopher Bailey and Karlheinz Bock, where young researchers will share their visions of future packaging technologies and participate in discussions with experts in the field.

This conference will also feature our prestigious Luncheon Keynote on Wednesday, May 27. We are pleased to have Douglas Yu from Taiwan Semiconductor Manufacturing Company addressing new and innovative packaging technologies. His talk is titled "Innovative Heterogeneous Integration Technologies Initiate a New Semiconductor Era."

We are continuing our tradition and bringing back the networking events focused on young professionals and diversity. Adeel Bajwa will chair on Tuesday, May 26, 6:30 p.m. the Young Professional Panel. The Diversity and Career focused Panel and Reception, jointly organized by ECTC and ITherm, will take place on Wednesday, May 27 at 6:30 p.m. The panel will be chaired by Kitty Pearsall and Cristina Amon and will focus on some of the specifics of inclusion in a diverse workforce. On the same day at 7:30 p.m., Michael Mayer will chair the ECTC Plenary Session titled "3DIC: Past, Present and Future." In this plenary session, experts will address the evolution of 3D integration, new applications and opportunities for using 3DIC technology as well as its challenges along the value chain. On Thursday, May 28 at 8 p.m., the IEEE EPS Seminar entitled "Future Semiconductor Packages for Artificial Intelligence Hardware" will be moderated by Yasumitsu Orii and Shigenori Aoki. The seminar will focus on brain inspired devices and integration technologies.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference, the 70th ECTC will offer eighteen PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 26 and are taught by distinguished experts in their respective fields. The Technology Corner exhibits will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 70th ECTC and to be a part of all the exciting technical and professional opportunities. I also take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 70th ECTC a success. I look forward to meeting you in Lake Buena Vista, Florida, on May 26 –29, 2020.

Rozalia Beica
70th ECTC Program Chair
AT&S
Email: rbeica.semi@gmail.com

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70th ECTC ADVANCE REGISTRATION

Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions see page 32.

Register early … save US$100 or more! All applications received after May 4, 2020, will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Dolphin Convention Center on the Lobby Level in front of Australia 3. ***Please note that the Swan and Dolphin are two separate buildings, and all ECTC meetings will be taking place in the Walt Disney World Dolphin Resort.***

On-Site Registration Schedule

Registration will be held in the Dolphin Convention Center on the Lobby Level in front of Australia 3.

Monday, May 25, 2020	3:00 p.m. – 5:00 p.m.
Tuesday, May 26, 2020	6:45 a.m. – 5:00 p.m.*
**6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Session only*	
Wednesday, May 27, 2020	6:45 a.m. – 4:00 p.m.
Thursday, May 28, 2020	7:30 a.m. – 4:00 p.m.
Friday, May 29, 2020	7:30 a.m. – 12:00 Noon

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. *****Please note that the Walt Disney World Swan and Dolphin Resort are two separate buildings, and ALL ECTC meetings will be taking place in the Walt Disney World Dolphin Resort. While booking your hotel reservation, please make sure to specify that you require to be placed in the Walt Disney World DOLPHIN Resort.*** While these two buildings are located adjacent to each other and share many of the same social / resort function areas, we want to ensure you have a very convenient experience while at ECTC 2020.**

ITherm 2020

This year ITherm is co-located with ECTC! All ITherm sessions will take place in the SWAN building of the Walt Disney World Swan and Dolphin Resort. ALL ECTC sessions, and the co-location of exhibits, will take place in the DOLPHIN building!

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

ECTC Sponsors

With 69 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Special and Program Sponsors, and several other sponsorship options that can be customized to your company's interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors."

To sign-up for sponsorship or to get more details, please contact **Wolfgang Sauter at wsauter2@gmail.com or +1-802-922-3083.**

Hotel Accommodations

Rooms for ECTC attendees have been reserved at the Walt Disney World Dolphin, of the Walt Disney World Swan and Dolphin Resort. The special conference rate is:

$199.00 / Run of the House + $14 Resort Services Fee Daily

Please note these rooms are on a first-come, first-served basis. If this specific category is no longer available, attendees will be offered the next best available accommodation. These prices include single or double occupancy in one room. Please note that rooms offering two beds are limited and subject to availability and should be requested at the time of reservations.

The conference rate of $199/night will only be available until Friday, May 1, 2020 at 5pm ET or until rooms run out, whichever comes first. To ensure our preferred conference rate, please make your reservation online through **www.ectc.net** or by directly contacting the hotel. All reservations made after the conference rate is no longer available will be accepted on a space and rate available basis. If you need to cancel a reservation, please do so AT LEAST 5 DAYS prior to arrival for a full refund. Each attendee is subject to the terms and policies set by each hotel.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2020 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2020 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC's only authorized site for reserving a room is through our website (**www.ectc.net**). You may, however, use other trusted sites that you personally have used in the past to book travel. Please be advised, there are scam artists out there, and if it's too good to be true, it likely is. Should you have any questions about booking a hotel room, please contact ECTC staff at: **lrenzi@renziandco.com**

Transportation Services

Enjoy a complimentary water taxi from the resorts' dock, running to and from **Epcot®** and **Disney's Hollywood Studios™**.

Complimentary shuttle buses also transport guests from the hotel entrance to **Magic Kingdom®** Park, **Disney's Animal Kingdom®** Theme Park, **Downtown Disney®** area, and **Disney' Blizzard Beach** Water Park, and **Disney's Typhoon Lagoon** Water Park.

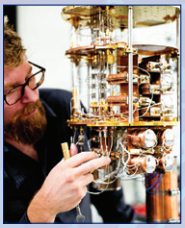
There is, unfortunately, no courtesy transportation between the hotel and the airport.

2020 ECTC Special Session

Bridge to Quantum Computing

Tuesday, May 26, 2020, 9:30 a.m. – 11:30 a.m.

Chairs: Nicholas Bronn – IBM Research and Pavel Roy Paladhi – IBM Systems



Quantum computers can provide a platform to solve hard problems which are computationally intractable with traditional computer architecture. Research on quantum computing over the past few decades has led to many breakthroughs and as a result, the field of quantum computing has come to a stage where implementing quantum computers to solve real life problems on a large scale is drawing nearer and nearer. However, to exploit the full potential of this emerging field, quantum computing needs to seamlessly integrate with traditional computer hardware and architecture. This session will focus on quantum computer systems and how they relate to traditional computing systems. Areas that need to be researched and tailored to prepare for large scale quantum computation implementation of higher time complexity algorithms will be identified. Aspects of both hardware and software development will be explored. Experts from the industry and academia will present and discuss some of the key challenges and directions that the research should be focused on. It is anticipated that this topic will become very significant to the computer packaging industry as well as the quantum computing world and this panel gives an opportunity for the ECTC community to be informed and ready to contribute.

1. *Nicholas Bronn – IBM Research, Yorktown Heights*
2. *Prof. Paul Franzon – North Carolina State University*
3. *Amir Jafari-Salim – SeeQC*
4. *Rabindra Das – MIT Lincoln Laboratory*

2020 Photonics Special Session

Cutting-Edge Technology on Integrated Photonics and Packaging

Tuesday, May 26, 2020, 2:00 p.m. – 4:30 p.m.

Chairs: Rena Huang – Rensselaer Polytechnic Institute and Harry Kellzi – Micropac Industries

The special session aims to capture the latest technology advancements in the fast evolving photonics areas that have wide interest to industry, academia and government laboratories worldwide. The session will comprise of two sub-sections focused on photonic integrated circuits and wideband RF over fiber circuits:

• *Photonic Integrated Circuits (PICs)* will focus on the integration of photonic integrated functions of both active and passive functions developed both in Indium Phosphide (InP) and Silicon wafer technologies for information signals transmission applications, such as tunable lasers, modulated lasers and transmitters and integrated receivers.

• *Wideband RF over Fiber Circuits* will address the conversion of electronics and electromagnetics traditional copper to light over wideband Fiber transmission with maximum BW, Low Noise Figure and High dynamic range of various applications, such as Microwave links, SATCOM, Wireless communications and others.

Invited speakers will discuss various photonic related topics, sharing their visions on the technology advancement and future trends.

1. *Kazuhiko Kurata – AIO Core, Photonics Electronics Technology Research Association*
2. *M. J. Soileau - CREOL, The College of Optics and Photonics, University of Central Florida*

Additional speakers will be announced at a later date.

2020 Young Professional Networking Panel

Tuesday, May 26, 2020, 6:30 p.m. - 7:45 p.m.

Chair: Adeel Bajwa - Kulicke and Soffa Industries Inc.

PANELISTS:
EPS Board of Governors members
Chris Bailey, David McCann, Sam Karikalan, Ravi Mahajan, Jeff Suhling, Pat Thompson, Alan Huffman, Kitty Pearsall, Eric Perfecto, Avi Bar-Cohen, William Chen and Subramanyan S. Iyer

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2020 ECTC Panel Session

Future (Visions) of Electronics Packaging

Tuesday, May 26, 2020, 7:30 p.m. – 9:00 p.m.

Chairs: Christopher Bailey, EPS President – University of Greenwich and Karlheinz Bock – TU Dresden

The session of the IEEE EPS president explores the path of packaging technologies towards the future. Visions of future packaging technologies are presented and discussed with experts in the field of electronics packaging. The best selected submissions and their authors of the EPS packaging technology vision conquest are also planned to be invited for a presentation and to join the discussion panel of this session. Addressing, in particular, new future electronics packaging technologies and involve our young colleagues and their way of thinking as early as possible into the discussion within the EPS society and outside, opens new perspectives. The intention of this panel is also to support and motivate our young colleagues to actively contribute and to identify significant future packaging technologies in order to best serve IEEE and the electronics community as early as possible in the discussion.

2020 ECTC Plenary Session

3DIC: Past, Present and Future

Wednesday, May 27, 2020, 7:30 p.m. – 9:00 p.m.

Chair: Michael Mayer – University of Waterloo

Driven by the ever increasing degree of miniaturization and the need for lower cost, researchers and visionaries in the manufacturing of microelectronics hardware have thought of extending planar integrated circuits (ICs) into the third dimension. Such 3D IC have been the source of inspiration for technologies such as stacked die and through-silicon-via (TSV). Challenges include process economics and the power/cooling tradeoff. This plenary session explores the evolution and state of the art of semiconductor 3D technology and discusses details of its current challenges and future promise.

1. *Douglas Yu – TSMC*
2. *Eric Beyne – IMEC*
3. *Mitsumasa Koyanagi – Tohoku University*
4. *Peter Ramm – Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT*

These sessions are open to all conference attendees.

2020 ECTC/ITherm Diversity and Career Growth Panel and Reception

Diversity and Inclusion Drives Innovation and Productivity

Wednesday, May 27, 2020, 6:30 p.m. – 7:30 p.m.

Chairs: Kitty Pearsall – Boss Precision, Inc. and Cristina Amon – University of Toronto

Diversity in today's workplace and academia must be more inclusive than just race, gender, and ethnicity. There are religious, political, educational, and cultural differences. Adding to this mix are varied socioeconomic backgrounds, sexual orientation, and people with disabilities. The GDP (Global Diversity Practice) Consultancy Group puts forth the following: "Openness to diversity widens our access to the best talent. Inclusion allows us to engage talent effectively. Together, this leads to enhanced innovation, creativity, productivity, reputation, engagement and results." The panel will discuss their experiences, challenges and best practices that have delivered positive outcomes.

1. Amy S. Fleischer – California Polytechnic State University

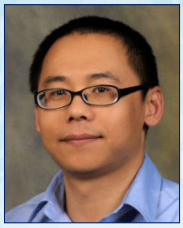
Additional speakers will be announced at a later date.

2020 Florida Photonics Cluster Session

Research, Manufacturing and Applications of Advanced Photonics Technologies within the Florida Photonics Cluster

Thursday, May 28, 2020, 9:00 a.m. – 11:00 a.m.

Chairs: Xiaoming Yu – CREOL, College of Optics & Photonics, University of Central Florida



This special session will highlight ongoing activities within the Florida Photonics Cluster (FPC). The mission of FPC is to support the growth and profitability of the photonics industry through the strength of a unified voice and to make Florida the place to go for photonics solutions. Speakers from universities, institutes and industries will be invited in a panel discussion to introduce the recent progress related to the research, design, manufacturing, and applications of photonics technologies.

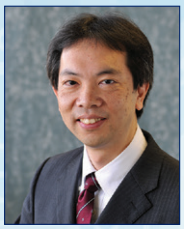
Speakers will be announced at a later date.

2020 IEEE EPS Seminar

Future Seminconductor Packages for Artificial Intelligence Hardware

Thursday, May 28, 2020, 8:00 p.m. – 9:30 p.m.

Chairs: Yasumitsu Orii - Nagase, Japan and Sheigenori Aoki - Fujitsu



An overwhelming amount of data is generated daily, out of which 90% is unstructured. Such data cannot be easily stored in a traditional column-row database, therefore, it is not easily searchable and more difficult to analyze. Today, artificial intelligence (AI) has the ability to analyze unstructured data, however, it also requires a high amount of energy. AI is expected to become one of the biggest energy consumers on the planet. A brain-inspired devices and quantum devices are very attractive to support a future AI due to its low power consumption. In this session, the panelists will discuss the future semiconductor packages in the era of a brain-inspired devices and quantum devices.

To show the product requirements:

1. *Hiroyuki Akinaga – The National Institute of Advanced Science and Technology (AIST)*
2. *Rama Divakaruni – IBM T. J. Watson Research, Albany NY*
3. *Subramanian S. Iyer – University of California, Los Angeles, "CHIPS"*
4. *Swaminathan Madhavan – Georgia Institute of Technology*
5. *Takashi Hisada – IBM Research Tokyo*

ECTC Luncheon Keynote

Innovative Heterogeneous Integration Technologies Initiate a New Semiconductor Era

Wednesday, May 27, 2020

Douglas Yu – Taiwan Semiconductor Manufacturing Company

In the supply chain for IC, which follows the path of Moore's Law with system-on-chip, packaging technology used to play mainly a protection role. Chip scaling is becoming more challenging and, at the same time, integration of more functions such as memory, sensors and passives, as well as other components for new applications such as AI and 5G, etc. is required. Innovative heterogeneous integration technologies are being proposed for system-on-package to provide critical Performance, Power and Area (PPA) values for the micro-systems. New, far-reaching changes are being made, which initiate an exciting new semiconductor era and create a new industry landscape.

Mark Your Calendar for ECTC 2021

Sheraton San Diego Hotel and Marina
San Diego, California, USA
June 1-4, 2021

Luncheons

Tuesday PDC Luncheon
All individuals attending a PDC are invited to join us for lunch. Proctors and instructors are welcome, too! Those attending a special session on Tuesday may purchase a lunch ticket for $65 on our website

Wednesday Conference Luncheon
Please be sure not to miss our Wednesday luncheon with guest speaker Douglas Yu, Vice President of Research and Development from TSMC. All conference attendees are welcome!

Thursday EPS Luncheon
Our sponsor, the IEEE Electronics Packaging Society, will be sponsoring lunch on Thursday for all conference attendees!

Friday Program Chair Luncheon
Please attend Friday's lunch hosted by the 70th ECTC Program Chair. We will honor conference paper award recipients and raffle off a vast array of prizes including a hotel stay, free conference registrations, and many other attractive items!

General Chair's Speakers Reception

Tuesday, May 26, 2020 • 6:00 p.m. – 7:00 p.m.
(by invitation only)

ECTC Student Reception

Tuesday, May 26, 2020 • 5:00 p.m. – 6:00 p.m.
Hosted by Texas Instruments, Inc.

Texas Instruments

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise! Sponsored by Texas Instruments, Inc.

Exhibitor Reception

Wednesday, May 27, 2020 • 5:30 p.m. – 6:30 p.m.
All badged attendees are invited to attend a reception in the exhibition hall.

70th ECTC Gala Reception

Thursday, May 28, 2020 • 6:30 p.m.
All badged attendees and their guests are invited to attend a reception hosted by the Gala Reception sponsors.

Executive Committee

General Chair
Christopher Bower
X Display Company, Inc.
chris@xdisplay.com
+1-919-522-3230

Vice General Chair
Nancy Stoffel
GE Research
nstoffel1194@gmail.com
+1-518-387-4529

Program Chair
Rozalia Beica
AT&S
rbeica.semi@gmail.com

Assistant Program Chair
Ibrahim Guven
Virginia Commonwealth University
iguven@vcu.edu
+1-804-827-3652

Jr. Past General Chair
Mark Poliks
Binghamton University
mpoliks@binghamton.edu
+1-607-727-7104

Sr. Past General Chair
Sam Karikalan
Broadcom, Inc.
sam.karikalan@broadcom.com
+1-949-926-7296

Sponsorship Chair
Wolfgang Sauter
Marvell Semiconductor, Inc.
wsauter2@gmail.com

Finance Chair
Patrick Thompson
Texas Instruments, Inc.
patrick.thompson@ti.com
+1-214-567-0660

Publications Chair
Henning Braunisch
Intel Corporation
braunisch@ieee.org
+1-480-552-0844

Publicity Chair
Eric Perfecto
eperfecto@gmail.com
+1-845-894-4400

Treasurer
Tom Reynolds
T3 Group LLC
t.reynolds@ieee.org
+1-850-897-7323

Exhibits Chair
Alan Huffman
Micross Advanced Interconnect Technology
alan.huffman@micross.com
+1-919-248-9216

IT Coordinator
Karlheinz Bock
TU Dresden
karlheinz.bock@tu-dresden.de
+49-351-463-36345

Professional Development Course Chair
Kitty Pearsall
Boss Precision, Inc.
kitty.pearsall@gmail.com
+1-512-845-3287

Conference Management
Lisa Renzi Ragar
Renzi & Company, Inc.
lrenzi@renziandco.com
+1-703-863-2223

EPS Representative
C. P. Wong
Georgia Institute of Technology
cp.wong@mse.gatech.edu
+1-404-894-8391

Packaging Technologies

Chair
Luke England
GLOBALFOUNDRIES
luke.england@globalfoundries.com
+1-518-222-1860

Assistant Chair
Markus Leitgeb
AT&S
m.leitgeb@ats.net
+43-676-8955-4087

Daniel Baldwin
H.B. Fuller Company

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Amkor Technology, Inc.

Jie Fu
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DuPont Electronic and Imaging

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Taiwan Semiconductor Manufacturing Company, Ltd.

Applied Reliability

Chair
Darvin R. Edwards
Edwards Enterprise Consulting, LLC
darvin.edwards1@gmail.com
+1-972-571-7638

Assistant Chair
Keith Newman
AMD
keith.newman@amd.com
+1-(408) 749-5566

Seung-Hyun Chae
SK Hynix

Tz-Cheng Chiu
National Cheng Kung University

Deepak Goyal
Intel Corporation

Vikas Gupta
Texas Instruments, Inc.

Sandy Klengel
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Auburn University

Pei-Haw Tsao
Taiwan Semiconductor Manufacturing Company, Ltd.

Dongji Xie
NVIDIA Corporation

Assembly & Manufacturing Technology

Chair
Jin Yang
Intel Corporation
jin1.yang@ieee.org
+1-971-214-9041

Assistant Chair
Christo Bojkov
Qorvo
cpb2016@sbcglobal.net
+1-972-994-8229

Sai Ankireddi
Maxim Integrated

Mark Gerber
Advanced Semiconductor Engineering Inc.

Habib Hichri
Suss Microtech Photonic Systems, Inc.

Paul Houston
Engent

Li Jiang
Texas Instruments

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Intel Corporation

Wei Xu
Huawei

Tonglong Zhang
Nantong Fujitsu Microelectronics, Ltd.

High-Speed, Wireless & Components

Chair
Lianjun Liu
NXP Semiconductor, Inc.
lianjun.liu@NXP.com
+1-480-413-4022

Assistant Chair
Yong-Kyu Yoon
University of Florida
ykyoon@ece.ufl.edu
+1-352-392-598

Amit P. Agrawal
Microsemi Corporation

Kemal Aygun
Intel Corporation

Wendem Beyene
Intel Corporation

Eric Beyne
IMEC

Prem Chahal
Michigan State University

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Manos M. Tentzeris
Georgia Institute of Technology

Maciej Wojnowski
Infineon Technologies AG

Emerging Technologies

Chair
Benson Chan
Binghamton University
chanb@binghamton.edu
+1-607-777-4349

Assistant Chair
W. Hong Yeo
Georgia Institute of Technology
whyeo@gatech.edu
+1-404-385-5710

Isaac Robin Abothu
Siemens Healthineers

Meriem Akin
Volkswagen

Vasudeva P. Atluri
Renavitas Technologies

Karlheinz Bock
Technische Universitat Dresden

Vaidyanathan Chelakara
Acacia Communications

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Qualcomm Technologies, Inc.

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Ramakrishna Kotlanka
Analog Devices

Santosh Kudtarkar
Analog Devices

Kevin J. Lee
Qorvo Corporation

Zhuo Li
Fudan University

Chukwudi Okoro
Corning

C. S. Premachandran
GLOBALFOUNDRIES

Jintang Shang
Southeast University

Rohit Sharma
IIT Ropar

Nancy Stoffel
GE Research

Liu Yang
IBM Corporation

Jimin Yao
Intel Corporation

Hongqing Zhang
IBM Corporation

Interconnections

Chair
Dingyou Zhang
Broadcom Inc.
dingyouzhang.brcm@gmail.com

Assistant Chair
Chuan Seng Tan
Nanyang Technological University
tancs@alum.mit.edu
+65-67905636

Thibault Buisson
Yole Développement

Jian Cai
Tsinghua University

Zhang Chaoqi
Qualcomm Inc

William Chen
Advanced Semiconductor Engineering, Inc.

David Danovitch
University of Sherbrooke

Rajen Dias
Amkor Technology, Inc.

Bernd Ebersberger
Infineon Technologies

Takafumi Fukushima
Tohoku University

Tom Gregorich
Zeiss Semiconductor Manufacturing Technology

Chung C. Key
Advanced Packaging Division, Corp. R&D, SPIL Ltd.

Seung Yeop Kook
GLOBALFOUNDRIES

Li Li
Cisco Systems, Inc.

Changqing Liu
Loughborough University

Wei-Chung Lo
ITRI

Nathan Lower
Collins Aerospace

James Lu
Rensselaer Polytechnic Institute

Peter Ramm
Fraunhofer EMFT

Katsuyuki Sakuma
IBM Corporation

Lei Shan
IBM Corporation

Ho-Young Son
SK Hynix

Jean-Charles Souriau
CEA Leti

Xin Yan
Intel

Matthew Yao
GE Aviation

Materials & Processing

Chair
Tanja Braun
Fraunhofer IZM
tanja.braun@izm.fraunhofer.de
+46-304-6403244

Assistant Chair
Kimberly Yess
Brewer Science
kyess@brewerscience.com
+1-573-201-8669

Yu-Hua Chen
Unimicron

Qianwen Chen
IBM Research

Jae Kyo Cho
GLOBALFOUNDRIES

Bing Dang
IBM Research

Yung-Yu Hsu
Apple, Inc.

Lewis Huang
Senju Electronic

C. Robert Kao
National Taiwan University

Alvin Lee
Brewer Science

Yi (Grace) Li
Intel Corporation

Ziyin Lin
Intel Corporation

Yan Liu
Medtronic Inc. USA

Mikel Miller
Apple, Inc.

Praveen Pandojirao-S
Johnson & Johnson

Mark Poliks
Binghamton University

Dwayne Shirley
Inphi

Ivan Shubin
RAM Photonics

Bo Song
HP Inc.

Yoichi Taira
Keio University

Lejun Wang
Analog Devices

Frank Wei
Disco Japan

Lingyun (Lucy) Wei
Dupont

Myung Jin Yim
Apple, Inc.

Hongbin Yu
Arizona State University

Zhangming Zhou
Qualcomm

Thermal/Mechanical Simulation & Characterization

Chair
Przemyslaw Gromala
Robert Bosch GmbH
Przemyslawjakub.gromala@de.bosch.com
+49-162-8514983

Assistant Chair
Ning Ye
Western Digital
ning.ye@wdc.com
+1-408-801-1278

Christopher J. Bailey
University of Greenwich

Kuo-Ning Chiang
National Tsinghua University

Xuejun Fan
Lamar University

Nancy Iwamoto
Honeywell Performance Materials and Technologies

Pradeep Lall
Auburn University

Chang-Chun Lee
National Tsing hua University (NTHU)

Sheng Liu
Wuhan University

Yong Liu
ON Semiconductor

Erdogan Madenci
University of Arizona

Tony Mak
Wentworth Institute of Technology

Karsten Meier
Technische Universität Dresden

Erkan Oterkus
University of Strathclyde

Suresh K. Sitaraman
Georgia Institute of Technology

Wei Wang
Qualcomm Technologies, Inc.

G. Q. (Kouchi) Zhang
Delft University of Technology (TUD)

Tieyu Zheng
Microsoft Corporation

Jiantao Zheng
Hisilicon

Photonics

Chair
Z. Rena Huang
Rensselaer Polytechnic Institute
zrhuang@ecse.rpi.edu
+1-518-276-6086

Assistant Chair
Harry G. Kellzi
Micropac Industries
harrykellzi@micropac.com
+1-972-272-371

Mark Beranek
Naval Air Systems Command

Stephane Bernabe
CEA Leti

Fuad Doany
IBM Research

Gordon Elger
Technische Hochschule Ingolstadt

Takaaki Ishigure
Keio University

Ajey Jacob
GLOBALFOUNDRIES

Soon Jang
ficonTEC, USA

Richard Pitwon
Resolute Photonics Ltd

Alex Rosiewicz
A2E Partners

Henning Schroeder
Fraunhofer IZM

Andrew Shapiro
JPL

Masato Shishikura
Oclaro Japan

Masao Tokunari
IBM Corporation

Shogo Ura
Kyoto Institute of Technology

Stefan Weiss
II-VI Laser Enterprise GmbH

Feng Yu
Huawei Technologies Japan

Thomas Zahner
OSRAM Opto Semiconductors GmbH

Ping Zhou
LDX Optronics, Inc.

Interactive Presentations

Chair
Pavel Roy Paladhi
IBM Corporation
rpaladhi01@gmail.com
+1-512-286-9677-

Assistant Chair
Michael Mayer
University of Waterloo
mmayer@uwaterloo.ca
+1-519-888-4024

Rao Bonda
Amkor Technology, Inc.

Mark Eblen
Kyocera International SC

Ibrahim Guven
Virginia Commonwealth University

Alan Huffman
Micross Advanced Interconnect Technology

Jeffrey Lee
iST-Integrated Service Technology Inc.

Nam Pham
IBM Corporation

Mark Poliks
Binghamton University

Patrick Thompson
Texas Instruments, Inc.

Kristina Young-Fisher
GLOBALFOUNDRIES

Professional Development Courses

Chair
Kitty Pearsall
Boss Precision, Inc.
kitty.pearsall@gmail.com
+1-512-845-3287

Co-Chair
Jeffrey Suhling
Auburn University
jsuhling@auburn.edu
+1-334-844-3332

Deepak Goyal
Intel Corporation

Lakshmi N. Ramanathan
Microsoft Corporation

PROFESSIONAL DEVELOPMENT COURSES

Tuesday, May 26, 2020

Kitty Pearsall, Chair
Boss Precision, Inc.
kitty.pearsall@gmail.com
+1-512-845-3287

Jeff Suhling, Assistant Chair
Auburn University
jsuhling@auburn.edu
+1-334-844-3332

MORNING COURSES
8:00 a.m. – 12:00 Noon

1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS -- MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – Indium Corporation

Course Objective:
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in details. The selection of novel alloys with reduced fragility will be presented. Crucial parameters for high reliability solder alloy for automotive industry will be presented. Electromigration and tin whisker growth will also be discussed. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how the selection of proper solder alloys and surface finishes for achieving high reliability are key.

Course Outline:
1. Main Stream Lead-free Soldering Practice
2. Surface Finishes Issues
3. Mechanical Properties
4. Intermetallic Compounds
5. Failure Modes
6. Reliability - Thermal Cycle
7. Reliability - Fragility
8. Reliability – Rigidity & Ductility
9. Reliability - Electromigration
10. Reliability - Tin Whisker

Who Should Attend:
Directors, managers, design engineers, process engineers, and reliability engineers who care about achieving high reliability lead-free solder joints and would like to know how to achieve it should take this course.

IMPORTANT NOTICE
It is extremely important to register in advance to prevent delays at door registration. Course sizes are limited.

2. INTRODUCTION TO FAN-OUT WAFER LEVEL PACKAGING

Course Leader: Beth Keser – Intel Corporation

Course Objective:
Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 10 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wire bond and bump interconnections, substrates, lead-frames, the traditional flip chip or wire bond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking.

Course Outline:
1. Current Challenges in Packaging
2. Definition and Advantages
3. Applications
4. Package Structures
5. Process
6. Material Challenges
7. Equipment Challenges
8. Design Rule Roadmap
9. Reliability
10. Benchmarking

Who Should Attend:
Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability, and package design should attend this course. Suppliers who are interested in supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

3. FUNDAMENTALS OF GLASS TECHNOLOGY AND APPLICATIONS FOR ADVANCED SEMICONDUCTOR PACKAGING

Course Leaders: Prakash Gajendran and Joseph Canale – Corning, Inc.

Course Objective:
This course is intended to guide technologists toward a deeper understanding of how to leverage engineered glass as a material for advanced IC packaging applications. Following a review of the fundamental principles of glass structure, composition, and properties, we will discuss the unique attributes that make glass an enabling material: including strength and reliability, chemical durability, thermal behavior, associated thermal relaxation behavior, and electrical properties. In addition, we will review the "glass toolkit" as a platform alternative for semiconductor packaging development including various manufacturing (glass melting and forming) approaches, the diversity of compositional options, and a survey of glass processing approaches that can be adapted from adjacent glass technology spaces to advanced semiconductor packaging. Finally, a series of case studies will illustrate how glass is contributing to emerging technologies in the microelectronics' space and explore current and potential applications in advanced semiconductor packaging, consumer electronics, and internet of things (IoT) applications. Examples include the role of glass as a carrier for temporary bonding, integrated glass wafers for optical sensors and augmented reality, key components in RF communications, as well as glass interposers for 2.5D and 3D packaging.

Course Outline:
1. Fundamentals of Glass
   - What is Glass?
   - Overview of Glass Attributes
2. Versatility of Glass
   - Glass Composition Review
   - Melting and Forming Process
   - Overview of Major Forming Processes
   - Secondary Processes
   - Options for Enhanced Properties
3. Major Applications and Markets
   - Wafer-Level Optics
   - Semiconductor
   - Case Studies

Who Should Attend:
Engineers, technical managers, scientists, buyers, and managers involved in materials, research and development, as well as advanced semiconductor packaging should attend. We welcome individuals or companies with little or no experience in using glass.

4. POST-MOORE'S LAW AND QUANTUM ELECTRONICS (PMQE)

Course Leader: Rao Tummala – Georgia Institute of Technology

Course Objective:
Moore's law has been the driving engine for science, technology, manufacturing, hardware, software, systems, and applications, contributing to the prosperity of thousands of individuals, hundreds of corporations, and dozens of countries. As Moore's Law begins to come to an end, not only for fundamental reasons but also for computing performance, power, cost, and investments, it is becoming clear that a different vision for electronics systems must emerge. So, while transistor integration to a 20 billion-transistor-chip on individual ICs so far was the basis of Moore's Law for ICs, this can be extended in 2.5D and 3D by means of new paradigms in electronic and optoelectronic interconnections, in the short term. This is referred to as Moore's Law for Packaging or interconnections. Just like Moore's Law has both the doubling of transistors and simultaneous cost reduction from node to node, every 18-24 months, Moore's Law for Packaging can do the same.

Interconnections have been driven by computing systems and within computing systems, between logic and memory, consistent with Von Neumann's architecture. The new era of artificial intelligence mimicking the human brain, with several orders of magnitude of better computer performance than with the current electronics, is yet another reason for the end of Moore's Law. The human brain is the ultimate system packaging for the highest performance in the smallest size with the lowest power. A typical human brain has about 90 billion nerve cells interconnected by trillions of synapses providing trillions of pathways for the brain to process the information along with petabyte memory. Thus the human brain is the new standard in packaging density and computing performance-power efficiency. This is more than the current 3D electronic architectures. There is no such electronics equivalent. Therefore the new PMQE law must duplicate this architecture.This tutorial describes a vision for post-Moore's Law and Quantum Electronics (PMQE) from current era of

Moore's Law for ICs to the next era of electronic and photonic interconnections, and eventually to quantum electronics and computing. All large corporations such as Google, IBM, Microsoft, Intel and advanced countries such as the U.S., Europe, Japan, and China have targeted quantum electronics as the next Moore's Law. Quantum electronics consist of Quantum devices with superconducting interconnections that operate at absolute zero degrees Kelvin. Unlike current computing, which operates with binary 0 or 1, quantum operates with both simultaneously. This is referred to as Qubits. This leads to an exponential increase in computing power, as demonstrated by IBM and Google. Currently Qubits are only at about 50. Post-Moore's Law electronics is highly interdisciplinary, requiring a team of scientists and engineers to work together from electrical, mechanical, thermal, optical, bio and nanomaterials, and chemical process disciplines. The PMQE provides a new opportunity for the electronics industry to continue, not on Moore's Law path, but on a computing roadmap.

Course Outline:

1. Current Approach to Devices and Systems
2. Moore's Law for ICs, Its Evolution and Its Future
3. Reasons for Moore's Law Coming to an End
4. What Will Replace Moore's Law?
5. Moore's Law for Electronic and Photonic Packaging as the 2nd Moore's Law
6. Quantum Electronics for the Next Computing Wave

Who Should Attend:

R&D executives as well as senior technical and marketing managers involved in all aspects of electronics R&D, supply-chain for ICs, packages and systems manufacturing, marketing, investments and users who deal with strategic directions for their company.

5. NANO MATERIALS AND POLYMER COMPOSITES FOR ELECTRONIC PACKAGING

Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation

Course Objective:

Nano materials and polymer composites are widely used in electronic and photonic packaging as adhesives, encapsulants, thermal interface materials, insulators, dielectrics, molding compounds, and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance encapsulants for flip-chip, chip scale packaging (CSP), system in a package (SIP) and 3D packaging, conductive adhesives (both ICA and ACA), embedded passives (high K polymer composites), and nano particles and nano-functional materials such as CNTs (some with graphenes). It is imperative that both material suppliers, formulators and their users have a thorough understanding of polymeric materials and the recent advances on nano materials and their importance in the advances of the electronic packaging and interconnect technologies.

Course Outline:

1. Introduction to Nanotechnology
2. Nano Solder
3. Carbon Nanotube
4. Nano Materials for Wafer Level Packaging
5. Super Hydrophobic Surface
6. Surface Functionalization
7. Functionalized Graphene for Energy Storage and Electrocatalysis
8. Electrically Conductive Adhesives
9. Conductive Nano Composites
10. Conductive Nano-ink
11. Transparent Nanocomposite

Who Should Attend:

Students, researchers, engineers, scientists and managers who are involved in research and development, designing, processing and manufacturing of microelectronic and optoelectronic components and packages, and suppliers and developers of materials for semiconductor and electronic packaging should attend.

6. FUNDAMENTALS OF RF DESIGN AND FABRICATION PROCESSES OF FAN-OUT WAFER/PANEL LEVEL PACKAGES AND INTERPOSERS

Course Leaders: Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM

Course Objective:

Due to their myriad of advantages in system-integration, fan-out wafer/panel level packages (FO WLPs/PLPs) and interposers will play a key role in the development of emerging electronic systems, especially for 5G applications. The fabrication processes and RF performance of these advanced packages, especially their multi-layered redistribution layers (RDLs), required for the interconnection of the chips and other system components, will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of FO WLPs/PLPs and interposers, including their multi-layered RDLs.

An overview of different types of wafer-level packages, fan-out technologies and interposers will first be given. This will be followed by a presentation of new fan-out-packaging and interposer-based concepts for emerging applications (e.g., 5G) as well as a thorough discussion of the materials and fundamentals of the fabrication processes of FO-WLPs/PLPs, multilayered RDLs and glass/silicon interposers. The basics of efficient RF design and measurement of the fundamental building blocks of FO-WLPs/PLPs and glass/silicon interposers will be given for frequencies right up in the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

Course Outline:

1. Overview of Different Types of Wafer-Level Packages, Fan-Out Technologies and Interposers
2. Requirements of 5G Packaging
3. New Fan-Out Packaging and Interposer-Based Concepts for 5G Applications
4. Materials and Fabrication Processes: FO-WLPs/PLPs, Multi-layered RDLs, and Silicon/Glass Interposers
5. Fundamentals of RF Design and Measurement: FO-WLPs/PLPs, RDLs, and Silicon/Glass Interposers
6. Comparison of RF Performance of Interconnects in FO-WLPs/PLPs and Silicon/Glass Interposers
7. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

Who Should Attend:

Engineers, scientists, researchers, designers, managers and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages for emerging applications (e.g., 5G) should attend.

7. ELIMINATING PACKAGE FAILURE MECHANISMS FOR IMPROVED RELIABILITY

Course Leader: Darvin Edwards – Edwards Enterprises

Course Objective:

Past and present reliability failure mechanisms that plague semiconductor packages will be explored. Major reliability challenges and failure mechanisms are detailed in critical emerging and high-volume package technologies such as TSVs, FOWLPs, WLCSPs, FC-BGAs, plastic leaded, and no lead packages. Topics studied include reliability of TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and wire bonds, Cu vs. Au wire bond reliability comparisons, complications associated with package delamination, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. Fundamental failure analysis fault isolation techniques are described. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for faster time to market. Characterization and implementation of test structures and design guidelines that enable reliable first pass products will be described and encouraged. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described.

Course Outline:

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques and Fault Isolation
4. FC-BGA Package Failure Mechanisms
5. Molded and Leaded Package Failure Mechanisms
6. WLCSPs Package Failure Mechanisms
7. Embedded Die & Fan-Out WLP Failure Mechanisms
8. TSV Failure Mechanisms
9. Materials, Modeling, Design Rules, and Reliability
10. Common Test Structures for Failure Mechanism Identification
11. Qualification by Similarity (QBS)
12. Summary

Who Should Attend:
This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions

8. CHARACTERIZATION OF ADVANCED EMCS FOR FO-WLP, HETEROGENEOUS INTEGRATION, AND AUTOMOTIVE ELECTRONICS

Course Leaders: Przemyslaw Gromala – Robert Bosch GmbH; Bongtae Han – University of Maryland

Course Objective:
Epoxy-based molding compounds (EMCs) are widely used in the semiconductor industry as one of the most important encapsulating materials. For the advanced packaging technologies, in particular, FO-WLP technologies and heterogeneous integrations, EMCs play a more significant role than for the conventional plastically-encapsulated packages because of thin profiles and complex process conditions required for the advanced packaging technologies. In the automotive industry where demand for more advanced packaging technologies increases rapidly for autonomous and connected cars, EMCs are often used to protect not only individual IC components but also entire electronic control units (ECUs), or power modules.

The stress caused by the mismatch of the coefficient of thermal expansion (CTE) between EMCs and adjacent materials is one of the major causes of reliability problems (e.g., excessive warpage, delamination, BRL, etc.). During assembly or even operating conditions, EMCs are subjected to temperatures beyond the glass transition temperature. Around the glass transition temperature, EMCs exhibit significant volumetric and isochoric viscosity, which leads to nonlinear viscoelastic behavior. In contrast, at low temperatures, EMCs show linear viscoelastic behavior. This complex material characteristic in the full temperature range of interest renders the design of electronic devices a nontrivial task. The mechanical behavior of EMCs has to be understood clearly to offer predictive simulation strategies, which has become an integral part of product development process.

This training will address details of such strategies, summarizes the required material characterization procedure, and closes with some representative examples.

Course Outline:
1. Introduction
2. Selection of the Material (Preliminary Qualitative Analysis)
3. Material Characterization
4. Cure Kinetics
5. Curing Shrinkage
6. Coefficient of Thermal Expansion
7. Linear Viscoelastic Properties
8. Master Curve and Shift Factor of Young's Modulus
9. Master Curve and Shift Factor of Bulk Modulus
10. Viscoelastic Behavior in the Non-linear Domain
11. Summary

Who Should Attend:
Engineers and technical managers who are already involved in the material characterization and modelling, numerical modelling, process engineers and PhD students who need fundamental understanding or broad overview should attend.

9. RELIABLE INTEGRATED THERMAL PACKAGING FOR POWER ELECTRONICS

Course Leader: Patrick McCluskey – University of Maryland

Course Objective:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics.

This course will emphasize approaches to integrated thermal packaging that address performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g. organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and in the techniques for their reliability assessment.

Course Outline:
1. Motivation for Integrated Thermal Packaging for Reliable Power Electronic Systems and Heterogeneous Integration
2. Simulation and Assessment of Active Thermal Management Techniques: Air; Single Phase Liquid; Two Phase; Heat Pipes; and, Thermoelectric
3. Application of Thermal Management Techniques to Commercial Power Systems
4. Durability Assessment: Failure Modeling; Simulation; Testing; and, Health Monitoring
5. Reliability and Thermal Packaging of Active Devices: Si; SiC; GaN; and, Interconnects
6. Reliability and Thermal Packaging of Switching Modules, including organic encapsulants
7. Reliability in Rigid Assembly Packaging: PCBs; Solders; and, Passives
8. Flexible Materials, Packaging, and Thermal Management: Flex circuit and OLED
9. Reliability of Additive Manufactured and Embedded Power Electronics

Who Should Attend:
This course is intended for engineers and managers who want to learn more about the thermal limitations and reliability concerns involved in the heterogeneous integration and packaging of power electronic devices and systems.

AFTERNOON COURSES
1:15 p.m. – 5:15 p.m.

10. FLIP CHIP TECHNOLOGIES

Course Leaders: Eric Perfecto – IBM Corporation and Shengmin Wen – Synaptics Inc.

Course Objective:
This course will cover the fundamentals of all aspects of flip chip assembly technology, including wafer bumping, substrate selection, solder joint formation in various assembly processes, underfill, and reliability evaluation. The course is divided into two major sections.

The first section focuses on the key steps of flip chip assembly processes and their respective equipment that are involved. Plenty of examples are presented to show the versatile flip-chip applications to single-die, monolithic multi-die, multi-level multi-die flip chip integration, as well as multi-form interconnection such as wire bond / flip chip mixed integration – the SiP integration. At the same time, major flip chip assembly packages are discussed, such as BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, and the important roles of electrical and mechanical simulation, Si die floor plan optimization and its consequence on packaging, among others. Students will understand the versatility of flip chip technologies and learn a range of criteria that they can apply to their daily work needs. This section also provides the trend in the flip chip assembly technologies.

The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies that are used in today's flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

Course Outline:
1. Introduction to Flip-Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Waver Lever Fan-Out; and, Panel Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-Bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology

12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend:
The goal of this course is to provide the students with a list of options to apply to their particular flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

11. WAFER-LEVEL CHIP-SCALE PACKAGING (WCSP) FUNDAMENTALS

Course Leader: Patrick Thompson – Texas Instruments, Inc.

Course Objective:
This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? What are the challenges for memory and other complex devices such as ASICs and microprocessors?

Course Outline:
1. WL-CSP definition
2. Trends, Categories, Examples, Challenges, Supply Chain
3. Historical Overview, Package Highlights, Assembly Flow
4. Processing and Reliability: Flex, Temperature Cycling, Drop, Electromigration
5. Fan-Out Technologies
6. Embedded Technologies
7. Conclusions

Who Should Attend:
The course will be useful to the following groups of engineers: newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and, those considering WLCSP as a potential alternative for their packaging solutions.

12. ADDITIVE FLEXIBLE HYBRID ELECTRONICS – MANUFACTURING AND RELIABILITY

Course Leader: Pradeep Lall – Auburn University

Course Description:
In this course, manufacture, design, assembly, and accelerated testing of additively-printed flexible hybrid electronics for applications in some of the emerging areas will be covered. Manufacturing processes for additive-fabrication of flexible hybrid electronics will be discussed. Flexible hybrid electronics opens the possibilities for the development of stretchable, bendable, foldable form-factors in electronics applications, which have not been possible with the use of rigid electronics technologies. Flexible electronics may be subjected to strain magnitudes in the neighborhood of 50-150 percent during normal operation. The integration processes and semiconductor packaging architectures for flexible hybrid electronics may differ immensely in comparison with those used for rigid electronics. The manufacture of thin electronic architectures requires the integration of thin-chips, flexible encapsulation, compliant interconnects, and stretchable inks for metallization traces. A number of additive manufacturing processes for the fabrication and assembly of flexible hybrid electronics have become tractable. Processes for handling, pick-and-place operations of thin silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes for development of robust process parameters which will allow for acceptable levels of yields in high-volume manufacture. Modeling of operational stresses in flexible electronics requires the material behavior knowledge under loads including: constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear, and abrasion. The strains imposed on flexible stretchable electronics may far exceed those experienced in rigid electronics requiring the consideration of finite-strain formulation in development of predictive models. The failure mechanisms, failure modes, acceleration factors in flexible electronics under operational loads of stretch, bend, fold, and loads resulting from human body proximity are significantly different than rigid electronics. The testing, qualification and quality assurance protocols to meaningfully inform manufacturing processes and ensure reliability and survivability under exposure to sustained harsh environmental operating conditions, may differ in flexible electronics as well. A number of product areas for the application of flexible electronics are tractable in the near-term including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring, and automotive electronics.

Course Outline:
1. Additive Technologies in Flexible Electronics
2. Laser-Direct Sintering
3. In-Mold Labeling
4. Aerosol-Jet Printing
5. Ink-Jet Printing
6. Screen-Printing and Gravure Printing
7. Ultra-Thin Chips
8. Die-Attach Materials for Flexible Semiconductor Packaging
9. Compliant Interconnects
10. Flexible Encapsulation Materials
11. Dielectric Materials for Large-Area Flexible Electronics
12. Flexible Substrates
13. Stretchable Inks for Printed Traces
14. Pick-and-Place and Material Handling Processes for Thin Chips
15. Reflow and Printing Processes
16. Accelerated Testing Protocols

Who Should Attend:
The targeted audience includes scientists, engineers, and managers considering the use of additively-printed flexible electronics or considering moving from rigid electronics to flexible electronics, as well as reliability, product or applications engineers who need a deeper understanding of additively-printed flexible electronics: the advantages; limitations; and, failure mechanisms.

13. FAN-OUT WAFER/PANEL LEVEL PACKAGING AND 3D IC HETEROGENEOUS INTEGRATIONS

Course Leader: John Lau – Unimicron Technology Corporation

Course Objective:
Recent advances in fan-out wafer/panel level packaging (TSMC's InFO-WLP and Fraunhofer IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration, 3D CIS/IC integration, and 3D MEMS/IC integration will be discussed in this presentation. Emphasis is placed on various FO-WLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FO-WLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor, SPIL/Xilinx, ASE, MediaTek, Intel, ITRI, Shinko, Cisco/eSilicon, Sony's TSV-less CIS, and Samsung/Hynix (HBM3) will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:
1. Formation of FOWLP: (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First)
2. Fabrication of Redistribution Layers (RDLs): (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu Damascene + CMP, (c) Hybrid RDLs, and (d) ABF/LDI and PCB Cu-plating + Etching
3. Warpages: (a) Warpage Types and (b) Allowable of Warpages
4. Reliability of FOWLP: (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations

5. TSMC InFO: (a) InFO-PoP, and (b) InFO_AiP/RF-Chip Driven by 5G
6. Samsung PLP: (a) PoP for Smart Watches and (b) SiP SbS for Smartphones
7. Formation of FOPLP: (a) PCB + SAP, (b) PCB + LDI, (c) PCB + TFT-LCD, and (d) PCB/ABF/SAP + LDI
8. Wafer vs. Panel: (a) Application Ranges of FOWLP and FOPLP, and (b) Critical Issues of FOPLP
9. Trends in FOWLP and FOPLP
10. System-on-Chip (SoC)
11. Heterogeneous Integrations or SiPs
12. Heterogeneous Integrations vs. SoC
13. Heterogeneous Integrations on Organic Substrates
14. Heterogeneous Integrations on Silicon Substrates (TSV-Interposers)
15. Heterogeneous Integrations on Silicon Substrates (TSV-Less Interposers)
16. Heterogeneous Integrations on Fan-Out RDL Substrates: STATSChipPac's FOFC-eWLB, ASE's FOCoS, MediaTek's FO-RDLs, Samsung's Si-Less RDL Interposer, and TSMC's InFO_oS, and InFO_MS
17. Heterogeneous Integration of (a) PoP, (b) Memory Stacks, (c) Chip-to-Chip Stacks, (d) CIS and Logic Chip, (e) LED and TSV-Interposers, (f) MEMS and Logic Chip, and (g) VESCL and PD
18. Trends in Heterogeneous Integrations

Who Should Attend:
If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer's books and the papers published by others.

14. POLYMERS IN WAFER LEVEL PACKAGING

Course Leader: Jeffrey Gotro –InnoCentrix, LLC

Course Objective:
The course will provide an overview of polymers used in wafer level packaging and the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be: 1) understand the types of polymers used in wafer level packages, including underfills (pre-applied and wafer applied), mold compounds, and substrate materials; 2) gain insights on how polymers are used in Fan Out Wafer Level Packaging, specifically mold compounds and polymer redistribution layers (RDL); and, 3) learn the key polymer and processes challenges in Fan Out Wafer Level Packaging including panel level processing. We will cover in more depth the chemistries, material properties, process considerations, and reliability testing for polymers used in wafer level packaging including epoxy mold compounds and dielectric redistribution layers (RDL) for eWLP. The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level packaging such as chip first and chip last (RDL first).

Course Outline:
1. Overview of Polymers Used in Wafer Level Packaging
2. Wafer Level Process Flows (Chip First Versus Chip Last (RDL First))
3. Epoxy Mold Compounds for eWLP
4. Photosensitive Polyimides and Polybenzoxazoles
5. Pre-Applied Underfills and Wafer Level Underfills, Chemistry and Process
6. Polymer Challenges in Fan-Out Wafer Level Packaging
7. Reliability Testing for Fan-Out Wafer Level Packaging
8. Wafer Versus Panel Processing; Polymer Challenges and Solutions
9. Polymers Used in Heterogeneous Integration Fanout Panel Level Packaging (FO-PLP)

Who Should Attend:
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

15. RELIABILITY MECHANICS AND MODELING FOR IC PACKAGING

Course Leaders: Ricky Lee - HKUST and Xuejun Fan – Lamar University

Course Objective:
This course aims to present a comprehensive coverage of reliability mechanics and modeling under various loading conditions. In addition to the introduction of fundamentals, the course contents are arranged in four modules. Module 1 covers modeling under thermal loading, such as problems related to mismatch of thermal expansion or non-uniform temperature distribution. Module 2 deals with the modeling under mechanical loading, such as mechanical bending and/or drop impact. Module 3 will cover modeling under humidity/moisture loading for moisture related problems, such as failures in soldering reflow as well as under HAST and biHAST. Module 4 will introduce multi-physics modeling that involves the combined thermal, moisture, electrical, and mechanical loading. Theoretical foundation, modeling implementation, and the best practices for numerical simulations will be covered. Emerging trend and future perspective in reliability mechanics and modeling will be discussed.

Course Outline:
1. Fundamentals of Stress Analysis and Computational Modeling for IC Packaging
2. Reliability Issues and Modeling Under Thermal Loading
3. Reliability Issues and Modeling Under Mechanical Loading
4. Reliability Issues and Modeling Under Moisture/Humidity Loading
5. Reliability Issues and Modeling Under Combined Loading – Multi-Physics Modeling

Who Should Attend?
This course is intended for technical managers and staff members, reliability engineers, scientific researchers, and graduate students who are involved in thermal/mechanical modeling, package design, material selection, qualification and reliability assessment of chip-package interaction, package, and package/board interaction.

IMPORTANT NOTICE
It is extremely important to register in advance to prevent delays at door registration. Course sizes are limited.

16. POWER ELECTRONICS FOR AUTOMOTIVE APPLICATIONS

Course Leader: Mervi Paulasto-Kröckel – Aalto University

Course Objective:
The amount of electronics in vehicles has increased dramatically over the last several years and will continue to increase further in the future. Power electronics plays a major role in controlling automotive electronics and with the transition to energy-efficient forms of mobility its importance is even greater. E-mobility also strongly increases power-levels of related converters, such as HEV/EV main inverters and other high-voltage systems requiring new type of high-power module packages. The new package concepts and technologies have to be qualified to meet the reliability and automotive standards safety while simultaneously increasing life time requirements. This course provides an overview of what kind of power technologies, packaging concepts and materials are currently being used in different products from power semiconductors to power modules. What are the prevailing trends and challenges that power electronic packaging engineers face in automotive applications? This course will start by reviewing application areas for different power semiconductor technologies. Then different power packages and interconnect technologies used in these automotive applications will be introduced. Power module packaging concepts will be explained, and the requirements and possible concepts for e-mobility will be presented. The lecture will then proceed to reliability issues of the power packages and modules. In this context, robustness validation and design for reliability is covered. Finally, new developments in terms of materials and their implications on performance, thermal management, and reliability will be discussed.

Course Outline:
1. Power Electronics for Automotive – What and Where?
2. Background Power Semiconductors and Power Conversion
3. Power Electronics Packaging
   - – Requirements and Challenges
   - – Interconnects for Power Devices: Die Attach and Pb-Rich Solder Interconnects; and, Wire Bonding and Low RDSon Interconnects
   - – Thermal Management in Power Packaging
   - – Chip Embedding in Laminate Packaging
   - – Power Modules structure and Interconnects
   - – WBG Semiconductors – What is Changing?
4. Typical Failure Mechanisms in Power Packages
5. Robustness Validation and Design for Reliability – Examples of DfR and RV
6. Summary

Who Should Attend:
This PDC is dedicated to engineers and managers already involved in the field of reliability of electronics packaging especially for automotive electronics and for those who need a fundamental understanding of robustness validation and design for reliability.

17. FROM WAFER TO PANEL LEVEL PACKAGING

Course Leaders: Tanja Braun and Michael Töpper – Fraunhofer IZM

Course Objective:

Panel Level Packaging (PLP) is one of the latest trends in microelectronics packaging. Technology developments towards heterogeneous integration, including multiple die packaging, passive component integration in package and redistribution layer or package-on-package also approach larger substrates formats. These are targeted in this course. Manufacturing is currently done on wafer levels up to 12"/300 mm and 330 mm respectively. For higher productivity and therewith lower costs, larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP has the opportunity to adapt processes, materials and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when moving from wafer to panel level is not possible. Materials, equipment, and processes have to be further developed or at least adapted. This course will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging including Fan-out Panel Level Packaging substrate embedding approaches. This will include materials discussion, technologies, applications and market trends as well as cost modelling.

Course Outline:

1. Introduction to Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-Out Wafer Level: Material; Processes; and, Applications
4. Introduction and Definition of Panel Level Packaging
5. Fan-out Panel Level Packaging: Technologies, Challenges and Opportunities
6. Substrate Embedding Technologies

Who Should Attend:

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging should attend. Engineers and managers are welcome as detailed technology descriptions, market trends, applications, and cost modelling are presented.

18. THERMAL MANAGEMENT OF ELECTRONICS

Course Leader: Jaime Sanchez – Intel Corporation

Course Objective:

This course provides the fundamentals of heat transfer applied to the design of thermal systems used to cool electronic components with an emphasis in semiconductor packages. We start with the basic theory of heat transfer and demonstrate simple concepts used today to calculate the cooling requirements for an electronic package and the impact of various parameters on the electronic package. This course covers in-depth heat transfer theory and analysis to give the student a comprehensive understanding of the key modes of heat transfer and their applications. Practical topics such as thermal interface materials, heat sink design and advanced cooling techniques are reviewed.

Course Outline:

1. Fundamentals of Heat Transfer and Its Application to Electronics Cooling
2. Techniques to Determine Cooling Requirements for a Package and Impact of Boundary Conditions
3. Simplification of Heat Transfer Equations to Analyze Cooling Solutions
4. Governing Principles of Cooling Solutions
5. Application of Numerical Methods to Calculate the Performance of Cooling Solutions
6. Introduction to Thermal Interface Materials and Their Applications
7. Techniques to Size Cooling Requirements and Trade-Offs
8. Parameters that Impact the Performance of Cooling Solutions
9. Introduction to Experimental Characterization of Cooling Solutions and Instrumentation
10. Fan Selection

Who Should Attend:

This class is intended for senior undergraduate and graduate students, as well as engineers working in the field of thermal management.

IMPORTANT NOTICE

Morning PD Courses 1 through 9 or afternoon PD Courses 10 through 18 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrent, attendance is only allowed at one session in the morning and one session in the afternoon.

See page 32 for registration information

CONTINUING EDUCATION UNITS

The IEEE Electronics Packaging Society (EPS) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 70th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

AREA ATTRACTIONS

In the heart of the Walt Disney World® Resort, the award-winning Walt Disney World Swan and Dolphin Resort is your gateway to Central Florida's greatest theme parks and attractions. The resort is located in between Epcot® and Disney's Hollywood Studios™, and nearby Disney's Animal Kingdom® Theme Park and Magic Kingdom® Park. Come discover our 17 world-class restaurants and lounges, sophisticated guest rooms with Westin Heavenly Beds® and the luxurious Mandara Spa. Enjoy five pools, two health clubs, tennis, nearby golf, and many special Disney benefits, including complimentary transportation to Walt Disney World Theme Parks and Attractions, and the Extra Magic Hours benefit.

Just minutes from the Walt Disney World Swan and Dolphin Resort is Downtown Disney's West Side and Marketplace. Downtown Disney's West Side showcases top-notch restaurants, a 24-screen AMC Pleasure Island movie theater, and other uncommon shops. Here you'll also find the exquisite Cirque du Soleil La Nouba live entertainment show and the DisneyQuest Indoor Interactive theme park.

Downtown Disney Marketplace provides an appealing place to take a break from Disney Theme Parks and Water Parks. Check out the largest Disney character store in the world. Or, for more of a respite, relax and dine at a lakeside restaurant.

Should you decide to explore outside the Greater Lake Buena Vista area, Orlando boasts other parks and recreation areas tailor-made for whatever your pleasure. Favorites include Universal Orlando, SeaWorld, Gatorland, and Winter Park.

Program Sessions: Wednesday, May 27, 8:00-11:40 a.m.

Session 1: Fan-Out Technologies for System Integration	Session 2: Innovation on WLCSP and 3D Packaging	Session 3: Antenna-in-Package for 5G and Radar Systems
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: High-Speed, Wireless & Components**
Session Co-Chairs: **Beth Keser** **Intel Corporation** **Email: beth.keser@intel.com** **Bora Baloglu** **Amkor Technology, Inc.** **Email: bora.baloglu@amkor.com**	**Session Co-Chairs:** **Yung-Yu Hsu** **Apple, Inc.** **Email: yungyu.hsu@gmail.com** **Lewis Huang** **Senju Electronic** **Email: lewis@senju.com.tw**	**Session Co-Chairs:** **Maciej Wojnowski** **Infineon Technologies AG** **Email: maciej.wojnowski@infineon.com** **Hideki Sasaki** **Renesas Electronics Corporation** **Email: hideki.sasaki.xv@renesas.com**
1. 8:00 AM - InFO_SoW (System-on-Wafer) for High-Performance Computing Shu-Rong Chun, Hao-Yi Tsai, Chung-Shi Liu, Chuei-Tang Wang, Jeng-Shien Hsieh, Tsung-Shu Lin, Terry Ku, and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Extreme Wafer Thinning and Nano-TSV Processing for 3D Heterogeneous Integration*** Anne Jourdain, Filip Schleicher, Joeri De Vos, Michele Stucchi, Emmanuel Chery, Andy Miller, Gerald Beyer, Geert Van der Plas, and Eric Beyne – IMEC; Edward Walsby, Kerry Roberts, Huma Ashraf, and Dave Thomas – SPTS	***1. 8:00 AM - Glass-Based IC-Embedded Antenna-Integrated Packages for 28-GHz High-Speed Data Communications*** Atom Watanabe, Muhammad Ali, Siddharth Ravichandran, Rao Tummala, and Madhavan Swaminathan – Georgia Institute of Technology; Takenori Kakutani – Taiyo Inc.; Markondeya Pulugurtha – Florida International University
2. 8:25 AM - Fan-Out Wafer Level Packaging of GaN Components for RF Applications Tanja Braun, Thanh Duy Nguyen, Steve Voges, Markus Wöhrmann, Robert Gernhardt, Karl-Friedrich Becker, and Rolf Aschenbrenner – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin; Dirk Schwantuschke – Fraunhofer IAF; Michael Pretl – Rohde & Schwarz	***2. 8:25 AM - Chemical Thinning Approach for High-Topography Glass Wafers*** Messaoud Bedjaoui and Jean Brun – CEA-LETI	***2. 8:25 AM - 3D Integrated Through Fused Silica Via (TFV) Based Array Antenna for mm Wave Communications*** Renuka Bowrothu and Yong Kyu Yoon – University of Florida
3. 8:50 AM - Scalable Chiplet Package using Fan-Out Embedded Bridge C.Key Chung, Ally Liao, Ying Ju Lu, Jia Shuang Chen, Joe Lin, and Daniel Ng – Siliconware Precision Industries Co., Ltd.	***3. 8:50 AM - Material Optimization of Permanent and Temporary Adhesives for Wafer-Level Three-Dimensional Integration*** Naoko Araki and Shinji Maetani – DAICEL Corp.; Toshiaki Hirota – TAZMO Co., Ltd.; YoungSuk Kim – DISCO Corp.; Takayuki Ohba – Tokyo Institute of Technology	***3. 8:50 AM - A Novel Packaging and System-Integration Platform with Integrated Antennas for Scalable, Low-Cost and High-Performance 5G mm Wave Systems*** Ivan Ndip, Stefan Kosmider, Thi Huyen Le, Uwe Maaß, Marco Rossi, Andreas Ostmann, and Klaus-Dieter Lang – Fraunhofer IZM; Kristoffer Andersson – Ericsson
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Design, Process and Reliability of Face-Up 2-Layer Molded FOWLP AiP Tai Chong Chai, Teck Guan Lim, Yong Han, Faxing Che, David Ho, and Ser Choong Chong – Institute of Microelectronics, A-STAR	***4. 10:00 AM - Fabrication and Reliability Demonstration of 5 µm Redistribution Layer (RDL) Using Low-Stress Dielectric Dry Film*** Pratik Nimbalkar, Fuhan Liu, and Mohan Kathaperumal – 3D Systems Packaging Research Center; Cheng Ping Lin, Fukuya Naohito, and Toshiyuki Makita – Panasonic Corporation, Japan; Naoki Watanabe – Panasonic Industrial Devices Sales Company of America, USA	***4. 10:00 AM - High Performance mm-Wave MIMO Radar with Integrated Antenna-on-Package*** Meysam Moallem, Zachary Crawford, Marc Dewilde, Ross Kulak, Cathy Chi, Athena Lin, and Brian Ginsburg – Texas Instruments
5. 10:25 AM - Functional RDL of FOPLP by using LTPS-TFT Technology for ESD Protection Application Terry Wang, Hsin-Cheng Lai, Yu-Hua Chung, Chieh-Wei Feng, Liang-Cyuan Chang, Jui-Wen Yang, Tzu-Hao Yu, Shao-An Yan, Yuh-Zheng Lee, and Steve Chiu – Industrial Technology Research Institute (ITRI)	***5. 10:25 AM - A Novel Design of Temporary Bond Debond Adhesive Technology for Wafer-Level Assembly*** Dingying Xu, Hsin-Wei Wang, Jigneshkumar Patel, Hirota Kosuke, and Xavier Brun – Intel Corporation; Elliott Capsuto – Shin-Etsu Microsi, Inc.; Hideto Kato and Michihiro Sugo – Shin-Etsu Chemical	***5. 10:25 AM - mmWave AiP Measurement Turnkey Solution in Millimeter-Wave Wireless Communication Applications*** Chen Chao Wang – Advanced Semicondutor Engineering, Inc.
6. 10:50 AM - Development of Embedded Glass Wafer Fan-Out Package with 2D Antenna Arrays for 77GHz Millimeter-Wave Wireless Communication Tian Yu, Xiaodong Zhang, Daquan Yu, and Xiaoli Ren – Xiamen Sky Semiconductor; Zongming Duan – East China Research Institute of Electronic Engineering	***6. 10:50 AM – Development of Self-Releasing Adhesive Tape as a Temporary Bonding Material for 3D Integration*** Taro Shiojima, Munehiro Hatai, Daihei Sugita, and Ryoichi Watanabe – Sekisui Chemical Co., Ltd.	***6. 10:50 AM - Imprint-Through Mold Via (i-TMV) with High Aspect Ratio and Narrow Pitch for Antenna in Package*** Xinrong Li, Tsuyoshi Ogawa, Tomoaki Shibata, Satoshi Yoneda, Naoya Suzuki, and Toshihisa Nonaka – Hitachi Chemical Co., Ltd.
7. 11:15 AM - Flexible Fan-Out Wafer Level Packaging of Ultra-Thin Dies Jean-Charles Souriau, Laetitia Castagné, and Carine Ladner – CEA, Leti	***7. 11:15 AM - Novel Low Temperature Curable Photo-Patternable Low Dk/Df for Wafer Level Packaging (WLP)*** Katherine Han, Yasumasa Akatsuka, Jenna Cordero, Shinya Inagaki, and Daniel Nawrocki – Kayaku Advanced Materials, Inc.	***7. 11:15 AM - One-Dimensional Steerable End-Fire Orthogonal Beams for 5G Millimeter Wave Applications by L-Shape Antenna Element Arrangement in Active Antenna-in-Packaging Design*** Kuan-Hsun Wu, Zhao-He Lin, and Hsi-Tseng Chou – National Taiwan University; Pin-Zhong Shen and Ding-Bing Lin – National Taiwan University of Science and Technology; Li-Chih Fang, Ji-Cheng Lin, Chao-Shun Yang, Chieh-Wei Chou, Chi-Liang Pan, and Chun-Te Lin - Powertech Technology, Inc.

Program Sessions: Wednesday, May 27, 8:00-11:40 a.m.

Session 4: Advanced Photonic Integration Packaging	Session 5: Advanced Bonding Methods and Processing	Session 6: Interconnect Modeling
Committee: Photonics	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Rena Huang** **Rensselaer Polytechnic Institute** **Email: zrhuang@ecse.rpi.edu** **Harry Kellzi** **Micropac Industries** **Email: harrykellzi@micropac.com**	**Session Co-Chairs:** **Christo Bojkov** **Qorvo** **Email: cpb2016@sbcglobal.net** **Paul Houston** **Engent** **Email: paul.houston@engentaat.com**	**Session Co-Chairs:** **Yong Liu** **ON Semiconductor** **Email: Yong.Liu@onsemi.com** **Przemyslaw Gromala** **Robert Bosch GmbH** **Email: Przemyslawjakub.gromala@de.bosch.com**
1. 8:00 AM - Automated Assembly of High Port Count Silicon Photonic Switches Nicolas Boyer, Elaine Cyr, Fuad Doany, Christian W. Baks, Nicolas Dupuis, Benjamin G. Lee, and Isabel De Sousa – IBM Corporation	***1. 8:00 AM - Low Temperature Direct Bonding of SiN and SiO Interfaces for Advanced Packaging*** Xavier Brun – Intel Corporation; Jurgen Burggraf – EV Group	***1. 8:00 AM - Numerical Model for Understanding Failure Mechanism of Back End of Line (BEOL) in Bump Shear*** Wei Wang, Wei Zhao, Mark Nakamoto, Mark Schwarz, Dongming He, Xuefeng Zhang, Lily Zhao, and Ahmer Syed – Qualcomm Technologies, Inc.
2. 8:25 AM - Electro-Optical Co-Integration of Chip-Components in Optical Transceivers for Optical Inter-Chip Communication Krzysztof Nieweglowski, Lukas Lorenz, Mircea Catuneanu, Kambiz Jamshidi, and Karlheinz Bock – Technische Universität Dresden	***2. 8:25 AM - Development of Multi-Die Stacking with Cu-Cu Interconnects using Gang Bonding Approach*** Ser Choong Chong, Hongyu Li, Ling Xie, and Seow Huang Lim – Institute of Microelectronics	***2. 8:25 AM - Combined Peridynamic Theory and Kinetic Theory of Fracture for Solder Joint Fatigue Life Prediction*** Erdogan Madenci, Cagan Diyaroglu, and Yanan Zhang – University of Arizona
3. 8:50 AM - Integrated Optical Single-Mode Waveguide Structures in Thin Glass for Flip-Chip PIC Assembly and Fiber Coupling Julian Schwietering and Martin Schneider-Ramelow – Technical University of Berlin; Christian Herbst, Oliver Kirsch, Norbert Arndt-Staufenbiel, Philipp Wachholz, and Henning Schröder – Fraunhofer IZM	***3. 8:50 AM - Bond At The End: A Comprehensive Study of a New High-Throughput Bonding Process*** Salwa Ben Jemaa, Jean-Francois Morissette, and Julien Sylvestre – Université de Sherbrooke; Pascale Gagnon – IBM Bromont	***3. 8:50 AM - Board Level Reliability Enhancement with Considerations of Solder Ball, Substrate and PCB*** Yangming Liu – China; Ning Ye and Bo Yang – Western Digital
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Multi-channel Single-Mode Polymer Waveguide Fabricated by the Mosquito Method Realizing Low Connection Loss with Single Mode Optical Fiber Arrays Sho Yakabe, Hitomi Matsui, Yui Kobayashi, and Takaaki Ishigure – Keio University	***4. 10:00 AM - A Reliable Copper-free Wafer Level Hybrid Bonding Technology for High-Performance Medical Imaging Sensors*** Amandine Jouve, Emmanuelle Lagoutte, Romain Crochemore, Gaelle Mauguen, Thierry Flahaut, Viorel Balan, Frank Fournel, and Florence Servant – CEA, LETI; Thomas Bodner, Alessandro Faes, and Jens Hofrichter – AMS AG	***4. 10:00 AM - Property-Performance Relationships for Sustained High Temperature Operation of Electronics*** Pradeep Lall, Madhu Kasturi, and Yunli Zhang – Auburn University; Jaimal Williamson – Texas Instruments
5. 10:25 AM - Integrated Silicon Photonic True-Time Delay Beam-Former for Wide-Band Phased-Array Antenna Stephen Anderson and Weimin Zhou – Combat Capabilities Development Command Army Research Lab; Amir Begović, Alex Chen, and Z. Rena Huang – Rensselaer Polytechnic Institute	***5. 10:25 AM - Nanotwinned Copper Hybrid Bonding and Wafer-On-Wafer (WOW) Integration*** Wei-Lan Chiu, Kai-Wei Chou, and Hsiang-Hung Chang – Industrial Technology Research Institute (ITRI)	***5. 10:25 AM - Investigation of Thermo-Mechanical and Phase-change Behavior in Sn/Cu Interconnects during Self-Propagating Exothermic Reaction Bonding*** Shuibao Liang, Yi Zhong, Stuart Robertson, Allan Liu, Zhaoxia Zhou, and Changqing Liu – Loughborough University
6. 10:50 AM - Hybrid Vanadate Silicon Nanophotonic Platform for Extreme Light Management at Telecom Bands Yusheng Bian, Ajey Jacob, Bo Peng, and Michal Rakowski – GLOBALFOUNDRIES	***6. 10:50 AM - Novel Cu/SiCN Surface Topography Control for 1 µm Pitch Hybrid Wafer-to-Wafer Bonding*** Soon-Wook Kim, Ferenc Fodor, Nancy Heylen, Serena Iacovo, Joeri De Vos, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC	***6. 10:50 AM - Novel Piezoelectric Force Sensor Array for Investigation of Ultrasonic Wire Bonding*** Matthias Arndt, Folke Dencker, Jannik Reimann, and Marc Christopher Wurz – Institute of Micro Production Technology; Yangyang Long and Jens Twiefel – Institute of Dynamics and Vibration Research
7. 11:15 AM - High-Brightness Displays Made using Micro-Transfer-Printed Flip-Chip microLEDs Christopher Bower, Matt Meitl, Salvatore Bonafede, Erich Radauscher, Erik Vick, Brook Raymond, Chris Verreen, Tiffany Weeks, and Andrew Pearson – X-Celeprint	***7. 11:15 AM - Formation of Smooth Au Surfaces Produced by Multiple Thin-Film Transfer Process Based on Template Stripping for Low-Temperature Bonding*** Michitaka Yamamoto, Ryutaro Nishimura, Tadatomo Suga, and Toshihiro Itoh – The University of Tokyo; Takashi Matsumae, Yuichi Kurashima, Hideki Takagi, and Eiji Higurashi – National Institute of Advanced Industrial Science and Technology	***7. 11:15 AM - A Comprehensive Study of Electromigration in Lead-Free Solder*** Jiefeng Xu, VanLai Pham, Chongyang Cai, Huayan Wang, Ke Pan, and S.B. Park – Binghamton University

Program Sessions: Wednesday, May 27, 1:30-5:10 p.m.

Session 7: Advances in Packaging at the Wafer/ Panel Level	Session 8: High-Density RDL for Advanced Interconnects	Session 9: Power Delivery and Conversion
Committee: Packaging Technologies and Assembly & Manufacturing Technology	**Committee: Interconnections**	**Committee: High-Speed, Wireless & Components**
Session Co-Chairs: **Andrew Kim** **Intel Corporation** **Email: hyoung.il.kim@intel.com** **Jan Vardaman** **Techsearch International** **Email: jan@techsearchinc.com**	**Session Co-Chairs:** **David Danovitch** **University of Sherbrooke** **Email: David.Danovitch@USherbrooke.ca** **Zhang Chaoqi** **Qualcomm, Inc.** **Email: chaoqi.gt.zhang@gmail.com**	**Session Co-Chairs:** **Rockwell Hsu** **Cisco Systems, Inc.** **Email: rohsu@cisco.com** **Markondeya Raj** **Florida International University** **Email: mpulugur@fiu.edu**
1. 1:30 PM - A Production-Worthy Fan-Out Solution – ASE FOCoS Chip Last Peng Yang – Taiwan; Min-Lung Huang, Hung-Jung Tu, Wen-Long Lu, and Peng Yang – Advanced Semiconductor Engineering Inc.	***1:30 PM - Hybrid Fanout Package for Vertical Heterogeneous Integration*** Po-Yao Chuang, M. L. Lin, S. T. Hung, Y. W. Wu, Techi Wong, M. W. Chou, M. C. Yew, C. K. Hsu, P. H. Tsai, S. M. Chen, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 1:30 PM - Design and Analysis of Logic-HBM2E Power Delivery System on CoWoS Platform with Deep Trench Capacitor*** Wei-Ting Chen, Chia-Chia Lin, Chung-Hao Tsai, Harry Hsia, Kuo-Chiang Ting, Shang-Yun Hou, Chi-Hsi Wu, Chuei-Tang Wang, and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.
2. 1:55 PM - Introduction of a New Carrier System for Collective Die-to-Wafer Hybrid Bonding and Laser-Assisted Die Transfer. Koen Kennes, Alain Phommahaxay, Samuel Suhard, Pieter Bex, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero and Xiao Liu – Brewer Science, Inc.; Olga Bauder and Thomas Schmidt – SUSS MicroTec Lithography GmbH	***2. 1:55 PM - Fan-Out RDL-First Pane-Level Packaging for Heterogeneous Integration*** John Lau, C. T. Ko, J. J. Chen, and T. J. Tseng – Unimicron	***2. 1:55 PM - Performance Improvement for FPGA due to Interposer Metal Insulator Metal Decoupling Capacitors (MIMCAP)*** Myongseob Kim, Dmitry Klokotov, Hing Yan To, and Cheang-Whang Chang – Xilinx
3. 2:20 PM - A Study on the Mechanical Debonding Process of Temporary Carriers for 3D TSV Wafer Level Packages (WLPs) Hyeong Gi Lee, Junghyun Cho, Junghyuk Lee, Minho Kim, and Dongwook Kim – Samsung Electronics Company, Ltd.	***3. 2:20 PM - Effect of Dielectric Process on the Interfacial Adhesion of RDL for FOWLP*** Kirak Son, Gahui Kim, and Young-Bae Park – Andong National University; Hyun-Kyu Ryu – SK Hynix Inc.	***3. 2:20 PM - Three-Dimensional Capacitors Embedded in Fully Cu-Filled Through-Silicon Vias and Its Thermo-Mechanical Reliability for 5G Application*** Ye Lin, Anak Agung Alit Apriyana, and Chuan Seng Tan – Nanyang Technological University; Hong Yu Li – Institute of Microelectronics, Agency for Science, Technology
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Study of Submicron Patterning Exposure Tool for Fine 500 mm Panel Size FOPLP Kenichiro Mori, Yoshio Goto, Hiromi Suda, Hiroyuki Wada, Hideo Tanaka, and Seiya Miura – Canon, Inc.; Douglas Shelton – Canon U.S.A., Inc.	***4. 3:30 PM - A Comparative Study of 2.5D and Fan-out Chip on Substrate: Chip First and Chip Last*** Meng-Kai Shih and Wei-Hong Lai, Penny Yang, David Tarng, and C. P. Hung – Advanced Semiconductor Engineering, Inc.	***4. 3:30 PM - Magnetic Inductor Arrays for Intel Fully Integrated Voltage Regulator (FIVR) on 10th Generation Intel® Core™ SoCs*** Malavarayan Sankarasubramanian, Kaladhar Radhakrishnan, Yongki Min, Ashay Dani, Ryan Mesch, Leigh Wojewoda, Jose Chavarria, William Lambert, and Michael Hill – Intel Corporation
5. 3:55 PM - Photolithography Solution That Overcomes Significant Die Placement Error for Advanced Packaging Tong Yang and Zhiyang Li – ONTO Innovation	***5. 3:55 PM - Electromigration Failure Study of a Fine-pitch 2μm/2μm L/S Cu Redistribution Line Embedded in Polyimide for Advanced High-Density Fan-Out Packaging*** Chien-Lung Liang and Kwang-Lung Lin – National Cheng Kung University; Yung-Sheng Lin, Chin-Li Kao, David Tarng, Shan-Bo Wang, and Yun-Ching Hung – Advanced Semiconductor Engineering, Inc., Kaohsiung; Kwang-Lung Lin - National Cheng Kung University	***5. 3:55 PM - Design and Demonstration of Single and Coupled Embedded Toroidal Inductors for 48V to 1V Integrated Voltage Regulators*** Claudio Alvarez, Srinidhi Suresh, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology; Daisuke Sasaki, Kazuki Watanabe, Ryo Nagatsuka, Cheng Ping Lin, and Tatsuyoshi Wada – Panasonic Corporation; Naoki Watanabe – Panasonic Industrial Devices
6. 4:20 PM – Better Thermal, Mechanical, and Physical Properties of Cured Polymer Using Low-Pressure Vacuum Cure Processing Zia Karim, Kenneth Sautter, Charudatta Galande, Sung Yeon Lee, Kay Song, and Kaushal Singh – Yield Engineering Systems; Ron Legario and Melvin Zussman – HD MicroSystems	***6. 4:20 PM - Versatile Electrochemical Plating Process Development for Heterogeneous WLP Structures*** Jianwen Han, Stephan Braye, Pingping Ye, David Shaffer, Kyle Whitten, Thomas Richardson, and Elie Najjar – MacDermid Alpha	***6. 4:20 PM - Ultra Low Profile Thin Film Capacitor for High-Performance Electronic Packages*** Kenichi Yoshida, Hitoshi Saita, and Takashi Kariya – TDK Corporation
7. 4:45 PM - Advanced Packaging Cost Reduction by Selective Copper Metallization Rashid Mavliev – Ipgrip, Inc.; Knut Gottfried – Fraunhofer ENAS; Rob Rhoades – Revasum	***7. 4:45 PM - Molded Interconnect Substrate (MIS) Technology for Semiconductor Packages*** Michael Liu – JCET Group	***7. 4:45 PM - Co-Optimization of PDN Design for Tri-cluster Multiple CPU Cores of SOC with Various Types of Decoupling Capacitor Integrated in Small Form-Factor Package*** Jisoo Hwang, Heeseok Lee, and Hoi-Jin Lee – Samsung Electronics

Program Sessions: Wednesday, May 27, 1:30-5:10 p.m.

Session 10: MEMS and Sensors	Session 11: Reliability of Next-Generation Interconnects	Session 12: Modeling for Heterogeneous Integration: From Wafer to Board Level
Committee: Packaging Technologies	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Ning Ge** **Consultant** **Email: greene.ge@gmail.com** **Allyson Hartzell** **Veryst Engineering** **Email: AHartzell@veryst.com**	**Session Co-Chairs:** **Lakshmi N. Ramanathan** **Microsoft Corporation** **Email: laramana@microsoft.com** **Deepak Goyal** **Intel Corporation** **Email: deepak.goyal@intel.com**	**Session Co-Chairs:** **Karsten Meier** **Technische Universität Dresden** **Email: karsten.meier@tu-dresden.de** **Chang-Chun Lee** **National Tsing hua University** **Email: cclee@pme.nthu.edu.tw**
1. 1:30 PM - Hybrid Package for High-Performance Inertial Measurement Units Marco Del Sarto, Nicolo Manca, Roseanne Duca, Yiyi Ma, Tom Quoc Lao, Doug Logsdon, David Cheng, and Alex Gritti – STMicroelectronics	***1. 1:30 PM - Electromigration Induced Interfacial Microstructure Evolution of Solder Joints in Electronic Packaging*** Pilin Liu, Deepak Goyal, and Alan Overson – Intel Corporation	***1. 1:30 PM - A Novel Warpage Reinforcement Architecture with RDL Interposer for Heterogeneous Integrated Packages*** Puru Bruce Lin and Cheng-Ta Ko – Unimicron Technology Corporation; Chia-Yu Peng, Chi-Wei Wang, Oscar Chuang, and Chang-Chun Lee – National Tsing Hua University
2. 1:55 PM - Cap Fabrication and Transfer Bonding Technology for Hermetic and Quasi Hermetic Wafer Level MEMS Packaging Kai Zoschke, Piotr Mackowiak, Kevin Kröhnert, Hermann Oppermann, and Nils Jürgensen – Fraunhofer IZM; Matthias Wietstruck, Alexander Göritz, Selin Tolunay Wipf, and Mehmet Kaynak – IHP – Leibniz Institut für Innovative Mikroelektronik; Klaus-Dieter Lang - Technische Universität Berlin	***2. 1:55 PM - Electromigration in Cu-Cu Bonds and 2 µm Redistribution Layer Lines with Highly <111>-Oriented Nanotwinned Cu*** I-Hsin Tseng, Kai-Cheng Shie, and K. N. Tu – National Chiao Tung University; Benson Lin and Chia-Cheng Chang – MediaTek, Inc.	***2. 1:55 PM - Electromechanical Reliability of Flexible Leadset Components of Wearable Electrocardiogram Sensors*** Benjamin Stewart, Gabriel Cahn, David Samet, Olivier Pierron, Samuel Graham, and Suresh Sitaraman – Georgia Institute of Technology; Shannon Dugan and Carrol Lapinski – Dupont Electronic Materials; Matthew Misner and Azar Alizadeh – GE Global Research; Mark Poliks – Binghamton University
3. 2:20 PM - Giant Magneto-Resistive Effect based Sensor on Laser Direct Structured MID Substrates Eike Fischer, Sebastian Bengsch, Sascha de Wall, and Marc Wurz – Leibniz Universität Hannover	***3. 2:20 PM - Intermetallic Morphology Evolution and Void Formation in Ni/Sn/Ni Microjoints*** Sanoop Thekkut, Ronit Das, Michael Njuki, Jiaxin Li, Rajesh Sivasubramony, Nikolay Dimitrov, and Peter Borgesen – Binghamton University; Ninad Shahane and Patrick Thompson – Texas Instruments; Kabir Mirpuri – NXP Semiconductors	***3. 2:20 PM - Thermal Analysis of a 3D Stacked High-Performance Commercial Microprocessor using Face-to-Face Wafer Bonding Technology*** Rahul Mathur, Xiaoqing Xu, Andy Chao, Pranavi Chandupatla, Shawn Hung, Nikhil Tadepalli, and Saurabh Sinha – Arm Inc.; Jaydeep Kulkarni – The University of Texas at Austin
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Low-Temperature Metallic Joints for Strain Sensing Sensor Dies Markus Feisst, Joscha Hoffmann, and Juergen Wilde – University of Freiburg - IMTEK	***4. 3:30 PM - Investigation and Comparison of Aging Effects in SAC+X Solders Exposed to High Temperatures*** Jing Wu, Mohammad Alam, K. M. Rafidh Hassan, Jeffrey Suhling, and Pradeep Lall – Auburn University	***4. 3:30 PM - Thermal, Mechanical and Reliability Assessment of Hybrid Bonded Stacks*** Vladimir Cherman, Stefaan Van Huylenbroeck, Melina Lofrano, Xinyue Chang, Herman Oprins, Mario Gonzalez, Geert Van der Plas, Gerald Beyer, Kenneth June Rebibis, and Eric Beyne – IMEC
5. 3:55 PM - Fan-Out Ultrasound Transducer Array in Substrate Lu Yao and Lixi Wan – Institute of Microelectronics, Chinese Academy of Sciences	***5. 3:55 PM - Corrosion of Copper Wirebonded Packages by Chlorine Containing Foreign Particles*** Varughese Mathew and Sheila Chopin – NXP Semiconductors; Enakshi Wikramanayake – The University of Texas at Austin	***5. 3:55 PM - A Numerical Technique to Evaluate Warpage Behavior of Double Sided Rigid-Flex Board Assemblies during Reflow Soldering Process*** Chun Sean Lau, Ning Ye, Yi Chun Tan, and Choon Kuai Lee – Western Digital
6. 4:20 PM - Development and Reliability Study of 3D WLCSP for Automotive CMOS Image Sensor using TSV Technology Shuying Ma, Fengxia Zhen, Aimo Xiao, And Xiaobing Yang – Huantian Technology (Kunshan) Electronics Co., Ltd.	***6. 4:20 PM - Thermal Aging Reliability of Socketable, Surface-Modified Solder BGAs with and without Polymer Collars*** Omkar Gupte, Rao Tummala and Vanessa Smet – Georgia Institute of Technology; Gregorio Murtagian and Srikant Nekkanty – Intel Corporation	***6. 4:20 PM - Thermomechanical Deformations of Power Modules with Sintered Metal Buffer Layers under Consideration of the Operating Time and Conditions*** Alexander Schiffmacher and Jürgen Wilde – IMTEK - University of Freiburg
7. 4:45 PM - Long-Term Encapsulation of Platinum Metallization Using A PDMS-HfO2 ALD Layer for Non-hermetic Active Implants Kambiz Nanbakhsh, Wouter Serdijn and Vasiliki Giagka – Delft University of Technology; Riina Ritasalo – Picosun Oy	***7. 4:45 PM - Key Takeaways and Relevance of Extrinsic Corrosion Mechanisms during Extended Biased HAST*** Amar Mavinkurve, Kittikorn Kasuriya, Rene Rongen, Jan Gulpen, Pantumwadee Jirachutiroj, Nara Tappetch, and Michiel van Soestbergen – NXP Semiconductors	***7. 4:45 PM - Bonding Integrity Enhancement in Wafer-to-Wafer Fine Pitch Hybrid Bonding by Advanced Numerical Modelling*** Lin Ji, Faxing Che, Hongmiao Ji, Hongyu Li, And Masaya Kawano – Institute of Microelectronics Singapore

Program Sessions: Thursday, May 28, 8:00-11:40 a.m.

Session 13: 2.5D and 3D Technology Enabling High Performance Computing	Session 14: Materials for High-Speed/Frequency and 5G	Session 15: Flexible and Printed Electronics
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: Assembly & Manufacturing Technology**
Session Co-Chairs: **Subhash L. Shinde** **University of Notre Dame** **Email: sshinde@nd.edu** **Peng Su** **Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs:** **Qianwen Chen** **IBM Research** **Email: chenq@us.ibm.com** **Lingyun (Lucy) Wei** **Dupont** **Email: lingyun.wei@dupont.com**	**Session Co-Chairs:** **Jin Yang** **Intel Corporation** **Email: jin1.yang@ieee.org** **Li Jiang** **Texas Instruments** **Email: l-jiang1@ti.com**
1. 8:00 AM - Deep Partition with High Density SoIC(TM) Front-End 3D Integration Chih-Chia Hu, Ming-Fa Chen, Wen-Chih Chiou, Chuei-Tang Wang, Chung-Hao Tsai, Chun-Chiang Kuo, Chen-Sheng Lin, and C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - High Aspect Ratio, High Resolution, and Broad Process Window Description of a Low Loss Photodielectric for 5G HS/HF Applications Using High and Low Numerical Aperture Tools*** Colin Hayes – Dupont Electronics and Imaging; Keith Best, Corey Shay, and Christain Ayala – Rudolph Technologies; Kevin Wang, Rosemary Bell, Colin Calabrese, Michael Gallagher, Kirk Thompson, and Robert Barr – DuPont	***1. 8:00 AM - Direct Patterning of Conductive Layers Embedded In 3D Printed Large Parts*** Vincens Gjokaj, Cameron Crump, Brian Wright, and Premjeet Chahal – Michigan State University
2. 8:25 AM - Waferscale Superconducting MCM for High-Performance Computing Rabindra Das, Vladimir Bolkhovsky, Alexander Wynn, Ravi Rastogi, Scott Zarr, Dmitri Shapiro, Manuel Docanto, and Leonard Johnson – MIT Lincoln Laboratory	***2. 8:25 AM – Active Antenna Subsystem Integration of Steerable Boresight Radiation Beams for 5G Millimeter Wave Applications by System-in-Packaging Process*** Pin-Zhong Shen and Ding-Bing Lin – National Taiwan University of Science and Technology; Zhao-He Lin, Hsi-Tseng Chou, and Kuan-Hsun Wu – National Taiwan University; Li-Chih Fang, Chao-Shun Yang, Chieh-Wei Chou, Chi-Liang Pan, Chun-Te Lin, and Ji-Cheng Lin – Powertech Technology, Inc.	***2. 8:25 AM - Remateable and Deformable Area-Array Interconnects in 3D Smart Wireless Sensor Packages*** Jose Solis Camara, Sepehr Soroushiani, Juan Bermudez, Daniel Wilding, Sk Yeahia Been Sayeed, M. M. Monshi, John L. Volakis, Shubhendu Bhardwaj, and P. M. Raj - Florida International University
3. 8:50 AM - Die to Wafer Stacking with Low Temperature Hybrid Bonding Guilian Gao, Laura Mirkarimi, Gill Fountain, Thomas Workman, Jeremy Theil, Gabe Guevara, Cyprian Uzoh, Dominik Suwito, Ping Liu, and Bongsub Lee – Xperi	***3. 8:50 AM - Low Permittivity and Dielectric Loss Polyimide with Patternability for High Frequency Applications*** Hitoshi Araki, Yohei Kiuchi, Akira Shimada, Hisashi Ogasawara, Masaya Jukei, and Masao Tomikawa – Toray Industries, Inc.	***3. 8:50 AM - A Heterogeneously Integrated, High Resolution and Ultra-Flexible Inorganic microLED Display using Fan-Out Wafer-Level Packaging*** Goutham Ezhilarasu and Subramanian Iyer – University of California, Los Angeles; Ajit Paranjpe – Veeco Instruments, Inc.; Jay Lee – DISCO Corporation, Japan; Frank Wei – DISCO Hi-Tec America, Inc.
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Face to Face Hybrid Wafer Bonding for Fine Pitch Applications Daniel Fisher, Sarah Knickerbocker, Daniel Smith, John Garant, Jorge Lubguban, Vilmarie Soler, and Norman Robson – GLOBALFOUNDRIES, Inc.	***4. 10:00 AM - Development of New Dielectric Material to Reduce Transmission Loss*** Isao Nishimura, Shintarou Fujitomi, Yuutoku Yamashita, Naoyuki Kawashima, and Nobuyuki Miyaki – JSR Corp.	***4. 10:00 AM - An Ultra-fast R2R Printing Technology for Flexible Devices*** Ying Zhong – University of South Florida
5. 10:25 AM - High Frequency Characteristics of Glass Interposer Satoru Kuramochi and Takahiro Tai – Dai Nippon Printing; Yoichiro Sato and Nobutaka Kidera – AGC	***5. 10:25 AM - Evaluation of Package-Level EMI Shielding using Conformally Coated Conductive and Magnetic Materials in Low and High Frequency Ranges*** Kisu Joo, Kyu Jae Lee, Hyun Jun Sung, Seung Jae Lee, Se Young Jeong, and Yoon-Hyun Kim – Ntrium, Inc.; Hyun Ho Park – The University of Suwon	***5. 10:25 AM - Evaluation of Component Embedded Substrates for use in High Reliability Applications*** Daniel Flintoft, Laura Kent, Martin Wickham, and Adam Lewis – National Physical Laboratory; Vlad Stolojan and Robert Dorey – University of Surrey
6. 10:50 AM - An Integrated 2-Tier Embedded 3D Capacitor with High Aspect Ratio TSV King Jien Chui – Institute for Microelectronics A*STAR; I-Ting Wang, Faxing Che, Lin Ji, Zhixian Chen, Yao Zhu, and Jen-Chieh Liu	***6. 10:50 AM - Advanced Low Loss Dielectric Material on Glass Substrate: Reliability and Filter Characteristics at High Frequency for mmWave Applications*** Takenori Kakutani, Daichi Okamoto, Zhong Guan, and Yuya Suzuki – TAIYO INK MFG. Co., Ltd.; Atom Watanabe, Muhammad Ali, Ravichandran Siddharth, Mohanalingam Kathaperumal, and Madhavan Swaminathan – Georgia Institute of Technology	***6. 10:50 AM - Interposing of Microelectronics by Micro Transfer Printing to Create 3D Structures*** Kevin Oswalt, James Thostenson, Tanya Moore, David Gomez, Carl Prevatte, Matthew Meitl, Salvatore Bonafede, Julia Roe, and Christopher Bower – X-Celeprint
7. 11:15 AM - 10 and 7 µm Pitch Thermo-Compression Solder Joint using a Novel Solder Pillar and Metal Spacer Process Jaber Derakhshandeh, Giovanni Capuz, Vladimir Cherman, Fumihiro Inoue, Inge De Preter, Lin Hou, Pieter Bex, Tomas Webers, Julien Bertheau, and Alain Phommahaxay – IMEC;	***7. 11:15 AM - W-band and D-band Transmission Lines on Glass Based Substrates for Sub-THz Modules*** Mutee ur Rehman, Siddharth Ravichandran, and Madhavan Swaminathan – Georgia Institute of Technology	***7. 11:15 AM - High Aspect Ratio Heterogenous Sn-Ag Bump Structure using a Sequential Electroplating Process and Novel Barrier*** Abderrahim El Amrani, Etienne Paradis, David Danovitch, and Dominique Drouin – Université de Sherbrooke

Program Sessions: Thursday, May 28, 8:00-11:40 a.m.

Session 16: Sintering and Interconnect Reliability	Session 17: Automotive and Harsh Environment Reliability	Session 18: Emerging Flexible Hybrid Electronics Committee: Emerging Technologies
Committee: Interconnections	**Committee: Applied Reliability**	**Committee: Emerging Technologies**
Session Co-Chairs: **Katsuyuki Sakuma** **IBM Corporation** **Email: ksakuma@us.ibm.com** **Takafumi Fukushima** **Tohoku University** **Email: fukushima@lbc.mech.tohoku.ac.jp**	**Session Co-Chairs:** **Varughese Mathew** **NXP Semiconductors** **Email: Varughese.mathew@nxp.com** **Vikas Gupta** **Consultant** **Email: Gvikas.Gupta@outlook.com**	**Session Co-Chairs:** **Jong-Hoon Kim** **Washington State University** **Email: jh.kim@wsu.edu** **Santosh Kudtarkar** **Analog Devices** **Email: santosh.kudtarkar@analog.com**
1. 8:00 AM - Microstructure Evolution and Acceleration Factor of Micro-Solder Bumps in Through-Silicon-via (TSV) in High Temperature Storage (HTS) Conditions Yoosun Kim, Joowan Hong, Yeonji Park, Sungho Hyun, Minsoo Park, Jaehyun Son, Gyujei Lee, Hoyoung Son, Namseok Kim, and Jin-Wook Jang – SK Hynix	***1. 8:00 AM - Reliability Assessment of mmWave Modules*** Laura Wambera, Karsten Meier, and Karlheinz Bock – Technische Universität Dresden; Christian Götze and Marcel Wieland – GLOBALFOUNDRIES	***1. 8:00 AM - RDL-first Flexible FOWLP Technology with Dielets Embedded in Hydrogel*** Noriyuki Takahashi, Tetsu Tanaka, Takafumi Fukushima, Yuki Susumago, and Hisashi Kino – Tohoku University
2. 8:25 AM - Electro-Migration Evaluation between Organic Interposer and Build-up Substrate on 2.3D Organic Packages Kei Murayama, Shota Miki, Hiromi Sugahara, and Kiyoshi Oi – Shinko Electric Industries Company, Ltd.	***2. 8:25 AM - Studies of Reliability Enhanced Electronic Module Used in Robotaxi and Autonomous Truck Applications*** Dongji Xie, Joe Hai, Jack Huang, Zhongming Wu, Vivienne Zou, and Manthos Economou – Nvidia	***2. 8:25 AM - Wafer Scale Flexible Interconnect Transfer for Heterogeneous Integration*** Pan Liu – Fudan University; Jian Li, Henk van Zeijl, and Guoqi Zhang – Delft University of Technology
3. 8:50 AM - Study of Electromigration Failure in Solder Interconnects under Low Frequency Pulsed DC Condition Yi Ram Kim, Allison Osmanson, Hossein Madanipour, and Choong-Un Kim – University of Texas at Arlington; Patrick Thompson and Qiao Chen – Texas Instruments, Inc.	***3. 8:50 AM - Influence of Cu Wire Material Additive Elements to the Reliability of Wire-Bonded Contacts*** Robert Klengel, Sandy Klengel, Jan Schischka, and Tino Stephan – Fraunhofer IMWS; Motoki Eto, Noritoshi Araki, and Takashi Yamada – Nippon Micrometal Corporation	***3. 8:50 AM - Heterogeneous Integration of MEMS Gas Sensor using FOWLP: Personal Environment Monitors*** Samatha Benedict, Arsalan Alam, Goutham Ezhilarasu, Michael Molter, and Subramanian S. Iyer – University of California Los Angeles; Murugaiya Sridar Ilango, Chandra Shekhar Prajapati, Thejas, and Navakanta Bhat – Indian Institute of Science
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Low Temperature Au-Au Bonding using Ag Nanoparticles as Intermediate Junpeng Fang, Jian Cai, Qian Wang, and Zhiting Geng – Tsinghua University	***4. 10:00 AM - Extreme Cold-Temperature High-Strain Rate Properties of SAC Solder Alloys*** Pradeep Lall, Vikas Yadav, Vishal Mehta, and Jeff Suhling – Auburn University; Ken Blecker – United States Army CCDC Armaments Center	***4. 10:00 AM - Development of Next Generation Stretchable Materials for Flexible Hybrid Electronics (FHE)*** Kenneth Araujo, Toshiaki Ogiwara and Toshiaki Oigwara – NAMICS Technologies, Inc.; Benson Chan – Binghamton University; Isabelle Quelhas, Benny Rajan, and Andrew Stemmerman – Sun Ray Scientific LLC
5. 10:25 AM - Micron-Silver Sinter Paste Developed for Direct Bonding on Bare Cu Surface by Non-Pressure Sintering in Inert Atmosphere Ly May Chew, Tamira Stegmann, Erika Schwenk, and Wolfgang Schmitt – Heraeus Deutschland GmbH & Co. KG	***5. 10:25 AM - Considerations on a Smart Strategy for Simultaneously Testing Multiple PCB Assemblies in Board Level Vibration*** Varun Thukral, Romuald Roucou, Stéphanie Sauze, Jeroen Zaal, Jeroen Jalink, and Rene Rongen – NXP Semiconductors	***5. 10:25 AM - High-Density Embedded Electronics in Textiles with 3D Flex Package Transfer*** Md Monshi, Jose-Solis Camara, Shubhendu Bhardwaj, John Volakis, and Markondeyaraj Pulugurtha – Florida International University
6. 10:50 AM - Plating-Free Bumping by Cu Nanopaste and Injection Molded Solder (IMS) for Fine Pitch Flip Chip Joining Toyohiro Aoki, Kuniaki Sueoka, Sayuri Kohara, Chinami Marushima, and Takashi Hisada – IBM Research - Tokyo; Ryouta Yamaguchi, Nobuhiro Sekine, Kenichi Yatsugi, and Makoto Yada – DIC Corporation	***6. 10:50 AM - Low Temperature Vibration Reliability of Lead-free Solder Joints*** Karsten Meier, Maximilian Ochmann, and Karlheinz Bock – Technische Universität Dresden; David Leslie and Abhijit Dasgupta – University of Maryland	***6. 10:50 AM - Development of Dry EEG Head Cap and Dry EEG Electrodes for Neuro Monitoring*** Maria Ramona Damalerio and Ming-Yuan Cheng – Institute of Microelectronics, A-STAR
7. 11:15 AM - Facile Preparation of Cu-Ag Micro-Nano Composite Paste for High-Power Device Packaging Jiaxin Liu, Yun Mou, and Yang Peng – Huazhong University of Science and Technology	***7. 11:15 AM - Board Level Reliability Study of mWLCSP with 5-Sided and 6-Sided Protection*** Yen Yao Chi, N. W. Liu, and Benson Lin – MediaTek, Inc.; Chieh Lung Lai, Jun Yi Huang, Chia Yu Kuo, Yih Jenn Chang, Hong da Chang, and C. Key Chung – Siliconware Precision Industries Co., Ltd.	***7. 11:15 AM - Computational Modeling of Flexible, Biocompatible and Biodegradable Devices*** Rachel Waxman, Ibrahim Guven, and Vamsi Yadavalli – Virginia Commonwealth University

Program Sessions: Thursday, May 28, 1:30-5:10 p.m.

Session 19: Embedded and Heterogeneous Integration	Session 20: Materials and Processes for FOWLP and PLP	Session 21: High Speed in Signal Integrity
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: High-Speed, Wireless & Components**
Session Co-Chairs: **John Knickerbocker** **IBM Corporation** **Email: knickerj@us.ibm.com** **Steffen Kroehnert** **ESPAT Consulting** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs:** **Kimberly Yess** **Brewer Science** **Email: kyess@brewerscience.com** **Bing Dang** **IBM Research** **Email: dangbing@us.ibm.com**	**Session Co-Chairs:** **Rajen M Murugan** **Texas Instruments** **Email: r-murugan@ti.com** **Amit Agrawal** **Microsemi Corporation** **Email: amit.agrawal@microsemi.com**
1. 1:30 PM - SoIC(TM) for Low-Temperature, Multi-Layers 3D Memory Integration Chih-Chia Hu, Ming-Fa Chen, Wen-Chih Chiou, Chuei-Tang Wang, Chung-Hao Tsai, Chun-Chiang Kuo, Chen-Sheng Lin, and C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 1:30 PM - Reliability Investigation of 2 um Line Copper Routing for Multi-Layer Fan-Out Routing*** Aleksandr Keller, Hans Walter, Astrid Gollhardt, Martin Schneider-Ramelow, Klaus-Dieter Lang, and Markus Woehrmann – Fraunhofer IZM	***1. 1:30 PM - EMI Shielding Technology in 5G RF System in Package Module*** Jay Li, Mike Tsai, Ryan Chiu, Eric He, Alex Hsieh, Frank Chu, J. Y. Chen, Shunyu Jian, Simon Chen, and Yu-Po Wang – Siliconware Precision Industries Co. Ltd.
2. 1:55 PM - Ultra-low ESL Capacitor based on Silicon Technology with Embedded Substrate Platform Jung Hwa Kim, Heeseok Lee, Jongkyu Yoo, and Jisoo Hwang – Samsung Electronics Co. Ltd.	***2. 1:55 PM - Polyimide Fine-via Etching and Low-Damage Surface-Modification Process for High-Density Fan-Out Wafer Level Package*** Yasuhiro Morikawa – ULVAC, Inc.	***2. 1:55 PM - Complex Permittivity Measurements in a Wide Temperature Range for Printed Circuit Board Material used in Millimeter Wave Band*** Kazuki Takahashi, Shunichi Kikuchi, Akiko Matsui, Mitsunori Abe, and Kouhei Chouraku – Japan
3. 2:20 PM - Amazing Compressed Solutions in X, Y, Z Axis with Embedded Silicon Capacitor Catherine le Martret Bunel and Mickael Pommier – MURATA	***3. 2:20 PM - Effect of Annealing on the Toughness of 40-um-wide Nanotwinned Cu Lines*** Wei-You Hsu, Yu-Jin Li, I-Hsin Tseng, and Chih Chen – National Chiao Tung University; Benson Lin and Chia-Cheng Chang – MediaTek, Inc.	***3. 2:20 PM - A Study of Temperature Effect on 53Gbps PAM4 Serial Link System-Level Behavior in Very Short Reach Application*** Fanghui Ren, Xuanyi Dong, Liang Xue, and Long Yang – Cisco Systems, Inc.
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Fine-Pitch Interconnection and Highly Integrated Assembly Packaging with FOMIP (Fan-out Mediatek Innovation Package) Technology Ming-Che Hsieh, Ming-Che Hsieh, KeonTaek Kang, and Seung Wook Yoon – JCET Group Co. Ltd.; Stanley Lin, Chi-Yuan Chen, and Kevin Yu – Mediatek Inc.	***4. 3:30 PM - Two-Layer Solder Resist Film with Low Young's Modulus for High Reliability*** Ying Hsuan Chou, Daichi Okamoto, and Hidekazu Miyabe – TAIYO INK MFG. CO., LTD.	***4. 3:30 PM - CTLE Adaptation Using Deep Learning in High-Speed SerDes Link*** Bowen Li and Paul Franzon – North Carolina State University; Brandon Jiao, Chih-Hsun Chou, and Romi Mayder – Xilinx Inc.
5. 3:55 PM - Demonstration of Vertically Integrated POP using FOWLP Approach Ser Choong Chong, Leong Ching Wai, Pei Siang Lim, Siak Boon Lim, and Tai Chong Chai – Institute of Microelectronics	***5. 3:55 PM - Novel Photosensitive Dielectric Material with Superior Electric Insulation and Warpage Suppression for Organic Interposers in Reliable 2.1D Package*** Shunsuke Katagiri, Seiji Shika, Yune Kumazawa, Katsuhiko Shimura, Takuya Suzuki, Tsuyoshi Kida, and Shu Yoshida – Mitsubishi Gas Chemical Company, Inc.	***5. 3:55 PM - An Efficient and Fast 112Gbps/ PAM4 Signal Line Design with Conventional FCBGA Substrate based on a 3D Component Library*** Ryuichi Oikawa – Renesas Electronics Corporation
6. 4:20 PM - Design and Demonstration of Large-Body Sized Glass-based Active Interposer for High-Performance Computing Siddharth Ravichandran, Mohanalingam Kathaperumal, Vanessa Smet, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology	***6. 4:20 PM - Feedforward Adaptive Shot Technology to Address Severe Lithography Challenges for Advanced FOPLP*** Keith Best, John Chang, Jian Li, Mike Marshall, and Burhan Ali – Rudolph Technologies	***6. 4:20 PM - Optimization of High-Speed Package Design on Statistical Domain*** Il-Joon Kim, Manho Lee, Gyoungbum Kim, Dae-Woo Kim, and Dan Kyung Suk Oh – Samsung Electronics Co., Ltd.; Ki Jin Han – Dongguk University
7. 4:45 PM - Heterogeneous Integration using Organic Interposer Technology Curtis Zwenger, Nathan Whitchurch, Curtis Zwenger, and Mike Kelly – Amkor Technology, Inc.; JaeHun Bae, MinJae Yi, WonMyoung Ki, JongHyun Jeon, and SangHyoun Lee – Amkor Technology Korea	***7. 4:45 PM - Low Warpage Liquid Compression Molding (LCM) Material for High-Density Fan-out and Wafer Level Packaging Applications*** Jay Chao, Rong Zhang, Ramachandran Trichur, and Lirong Chao – Henkel Corporation	***7. 4:45 PM - OpenCAPI Memory Interface Simulation and Test for Differential DIMM Channel with SNIA SFF-TA-1002 Connector*** Biao Cai, Jose Hejase, Kevin McIlvain, Kyle Giesen, Zhaoqing Chen, Junyan Tang, Megan Nguyen, and Hongqing Zhang – IBM Corporation; Zhineng Fan – Amphenol ICC; Victor Mahran – Smart Modular

Program Sessions: Thursday, May 28, 1:30-5:10 p.m.

Session 22: Advanced Biosensors and Bioelectronics	Session 23: Advanced Dicing and Laser-Assisted Bonding	Session 24: Material and Interface Modeling
Committee: Emerging Technologies	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Jae-Woong Jeong** **KAIST** **Email: jjeong1@kaist.ac.kr** **Zhuo Li** **Fudan University** **Email: zhuo_li@fudan.edu.cn**	**Session Co-Chairs:** **Valerie Oberson** **IBM Canada Ltd** **Email: voberson@ca.ibm.com** **Paul Tiner** **Texas Instruments** **Email: p-tiner@ti.com**	**Session Co-Chairs:** **Kuo-Ning Chiang** **National Tsinghua University** **Email: knchiang@pme.nthu.edu.tw** **Xuejun Fan** **Lamar University** **Email: xuejun.fan@lamar.edu**
1. 1:30 PM - Smart and Connected Physiological Monitoring Enabled by Stretchable Bioelectronics and Deep-Learning Algorithm Musa Mahmood, Young-Tae Kim, Yun-Soung Kim, and Woon-Hong Yeo – Georgia Institute of Technology	***1. 1:30 PM - Laser-Assisted Bonding (LAB) and De-bonding (LAdB) as an Advanced Process Solution for Selective Repair of 3D and Multi-Die Chip Packages*** Matthias Fettke, Andrej Kolbasow, Timo Kubsch, Alexander Frick, and Thorsten Teutsch – PacTech GmbH; Vinith Bejugam – PacTech US Inc.	***1. 1:30 PM - A Direct Multi-Field Coupling Methodology for Modeling Moisture-Induced Stresses and Delamination in Electronic Packages*** Liangbiao Chen and Yong Liu – ON Semiconductor; Xuejun Fan – Lamar University
2. 1:55 PM - Stretchable Epidermal Electronics on Skin Sweat Monitoring Zhibo Chen and Jie Hu – Hong Kong University of Science and Technology	***2. 1:55 PM - High-Performance Flip-Chip Bonding Mechanism Study with Laser Assisted Bonding*** Minho Gim, Choong Hoe Kim, Seok Ho Na, Dong Su Ryu, Kyung Rok Park, and Jin Young Kim – Amkor Technology	***2. 1:55 PM - Accuracy, Hysteresis and Extended Time Stability of Additively Printed Temperature and Humidity Sensors*** Pradeep Lall, Kartik Goyal, and Jinesh Narangaparambil – Auburn University
3. 2:20 PM - A High Spatial Resolution Surface Electromyography (sEMG) System Using Fan-Out Wafer-Level Packaging Arsalan Alam, Michael Molter, Amir Hanna, Randall Irwin, Samatha Benedict, Goutham Ezhilarasu, and Subramanian S. Iyer – University of California, Los Angeles; Bilwaj Gaonkar and Luke Macyszyn – David Geffen School of Medicine	***3. 2:20 PM - Development of Digital Signage Modules Composed of Mini-LEDs using Laser-Assisted Bonding (LAB) Technology*** Kwang-Seong Choi, Jiho Joo, Ki-Seok Jang, Yong-Sung Eom, and Gwang-Mun Choi – ETRI; Jong-Sun Kim – SiliconInside Co., Ltd; Ji-Hoon Choi – AQLASER Co., Ltd; Shin Choi – LBLusem Co.; Sang-Ki Kim – HS Semicon; Sehoon Yoo – KITECH	***3. 2:20 PM - Viscoelastic Modeling for Heterogeneous Fan-Out Wafer Molding Process*** Shu-Shen Yeh, P. Y. Lin, K. C. Lee, W. Y. Lin, M. C. Yew, C. C. Yang, J. H. Wang, C. K. Hsu, S. K. Cheng, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Microfabricated SERF Atomic Magnetometers for Bio-Magnetic Measurements Kangni Liu and Jintang Shang – Southeast University	***4. 3:30 PM - Step Coverage Improvement for Electromagnetic Interference (EMI) Shield Film by Forming Bevel-Shaped Packages*** Byeongdeck Jang, Naotaka Oshima, Fumio Uchida, Shigenori Harada, Shigeru Ishii, Satoshi Sawaki, Takuya Kaminaga, Hayato Kiuchi, Tomoharu Takita, and Youngsuk Kim – DISCO CORPORATION	***4. 3:30 PM - A Mechanistic Study of Underfill Cracks by the Confocal-DIC Method*** Ying Yang, Fakhreddine Habib, Papa Momar Souare, and Julien Sylvestre – 3IT, University of Sherbrooke; Eric Duchesne – IBM Bromont
5. 3:55 PM - Development of Long Term Stable Multiple-Ion-Selective Sensors for Agriculture and Aquaculture Applications Yu Chen, Ramona Damalerio, Weiguo Chen, and David Choong – Institute of Microelectronics, A*STAR; Shermin Goh, Jason Lim, Lionel Moh, Georgina Seah, and Angeline Tan – Institute of Materials Research and Engineering, A*STAR	***5. 3:55 PM - Low-Damage Singulation of Ultra-Thin Wafers using Stealth Dicing*** Natsuki Suzuki and Yuta Kondo – Hamamatsu Photonics K. K.; Takayuki Ohba – Tokyo Institute of Technology	***5. 3:55 PM - Mechanical Characterization of Dual Curable Adhesives*** Sukrut Phansalkar, Changsu Kim, and Bongtae Han – University of Maryland
6. 4:20 PM - 3D Heterogeneous and Flexible Package Integration for Zero-Power Wireless Neural Recording Sk Yeahia Been Sayeed, Satheesh Bojja Venkatakrishnan, MD Monshi, John Volakis, and Pulugurtha Markondeya Raj – Florida International University	***6. 4:20 PM - In-Process Measurement of the Grinding Force in Silicon Wafer Grinding Process*** Lixiang Zhang, Fei Qin, Pei Chen, Tong An, Yanwei Dai, and Yanpeng Gong – Beijing University of Technology	***6. 4:20 PM - 2.3D Advanced Substrate Fabrication with Low-Temperature Cu-Cu Direct Bonding Technique*** Puru Bruce Lin, Kai-Ming Yang, Chen-Hao Lin, Chia-Hao Chang, and Cheng-Ta Ko – Unimicron Technology Corporation; Chi-Wei Wang and Chang-Chun Lee – National Tsing Hua University
7. 4:45 PM - A Compact Wireless Passive Breath Analyzer for Health Monitoring Saranraj Karuppuswami, Saikat Mondal, Deepak Kumar, and Premjeet Chahal – Michigan State University	***7. 4:45 PM - High Expansion Tapes for Fan-Out WLP Applying a Novel Stress-Strain Curve Measuring Methods*** Ken Takano, Tadatomo Yamada, Toshiaki Menjo, and Shinya Takyu – LINTEC Corporation	***7. 4:45 PM - Electromechanical Characterization of Ecoflex and Carbon Nanotube Composites Using Biaxial Inflation*** Benjamin Stewart and Suresh Sitaraman – Georgia Institute of Technology; Nicholas Ginga – The University of Alabama in Huntsville

Program Sessions: Friday, May 29, 8:00-11:40 a.m.

Session 25: High Density Fan-Out Technology	Session 26: Breakthroughs in TSV and TGV Technologies	Session 27: WLP and Advanced Technology Reliability
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: Applied Reliability**
Session Co-Chairs: **Dean Malta** **Micross Advanced Interconnect** **Email: Dean.Malta@micross.com** **Jie Fu** **Apple Inc.** **Email: fujie6@gmail.com**	**Session Co-Chairs:** **Tom Gregorich** **Zeiss Semiconductor Manufacturing** **Email: tmgregorich@gmail.com** **Chung C. Key** **Silicon Precision Industries Company, Ltd.** **Email: chungckey@hotmail.com**	**Session Co-Chairs:** **Darvin R. Edwards** **Edwards Enterprise Consulting, LLC** **Email: darvin.edwards1@gmail.com** **René Rongen** **NXP Semiconductors** **Email: rene.rongen@nxp.com**
1. 8:00 AM - Process Window Enhancement of Via Holes for Fine Pitch RDL by Design Optimization Cliff McCold, Robert Hsieh, Ha-Ai Nguyen, and Warren Flack – Veeco Instruments, Inc.; John Slabbekoorn and Andy Miller – IMEC	***1. 8:00 AM - Trench Isolation Technology for Cost-Effective Wafer-Level 3D Integration with One-Step TSV*** Masaya Kawano, Xiang-Yu Wang, and Qin Ren – Institute of Microelectronics, A*STAR	***1. 8:00 AM - A Mechanics Model for the Moisture Induced Delamination in Fan-Out Wafer-Level Package*** Tz-Cheng Chiu, Ji-Yen Wu, Wei-De Liu, and Chang-Wei Liu – National Cheng Kung University; Dao-Long Chen, MengKai Shih, and David Tarng – Advanced Semiconductor Engineering, Inc.
2. 8:25 AM - Applications and Reliability Study of InFO_UHD (Ultra-High-Density) Technology Ting-Chu Ko, Han-Ping Pu, Yung-Ping Chiang, Hung Jui Kuo, Chuei-Tang Wang, Chung-Shi Liu, and Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***2. 8:25 AM - Coaxial Through-Silicon-Vias using Low-κ SiO2 Insulator*** Pengbo Yu, Changming Song, Jian Cai, Qian Wang, and Zheyao Wang – Tsinghua University; Hongxiao Lin and Zhiwei He – China Agricultural University	***2. 8:25 AM – WLCSP Solder Ball Interconnection Enhancement for High Temperature Stress Reliability*** Stephen Chen, Cake Chen, Paul Wu, P. H. Tsao, and S. T. Leu – Taiwan Semiconductor Manufacturing Company, Ltd.
3. 8:50 AM - Fine-Pitch RDL Integration for Fan-Out Wafer-Level Packaging Prayudi Lianto, Chin Wei Tan, Xundong Dai, Khai Mum Peter Fung, and Guan Huei See – Applied Materials; Ser Choong Chong, Soon Wee David Ho, and Siew Boon Serine Soh – Institute of Microelectronics; Mingsheng Zhang – Institute of Materials Research and Engineering; Henry Leong - WinTech Nano-Technology Services Pte. Ltd.	***3. 8:50 AM - Study of the Impact of Pitch Distance on the Statistical Variation of TSV Extrusion and the Underlying Mechanism*** Golareh Jalilvand, Ruslan Kuliiev, Nina Orlovskaya, Omar Ahmed, Nicolas Dube, and Tengfei Jiang – University of Central Florida	***3. 8:50 AM - Investigation into the Failure Mechanism of Silver Nanowire Network Film under Electrical Stress*** Kaiqing Wang, Xiaocun Wang, Jianzhong Wang, and Fei Xiao – Department of Materials Science, Fudan University; Yunxia Jin – National University of Singapore
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Advances in High Performance RDL Technologies for Enabling IO Density of 500 IOs/mm/layer and 10-µm IO Pitch Using Low-k Dielectrics Fuhan Liu, Rui Zhang, Bartlet DeProspo, Pratik Nimbalkar, Shreya Dwarakanath, Mohanalingam Kathaperumal, Rao Tummala, and Madhavan Swaminathan – Georgia Institute of Technology	***4. 10:00 AM - Defect Localization in Through-Si-Interposer Based 2.5DICs*** Sajay Bhuvanendran Nair Gourikutty, Danpeng Xie, Ratan Bhimrao Umralkar, and Surya Bhattacharya – Institute of Microelectronics, A*STAR, Singapore; Yew Meng Chow and Haonan Bai – Xilinx Asia Pacific Pte Ltd.	***4. 10:00 AM - Damage Accumulation in Printed Interconnects on Flex Under Combinations of Bending and Tension with Different Amplitudes*** Rajesh Sivasubramony, Manu Yadav, Arun Raj, Mohammed Alhendi, Mark Poliks, and Peter Borgesen – Binghamton University
5. 10:25 AM - Challenges of Large Fan-Out Multi-Chip Module and Fine Cu Line Space C. Key Chung, GuanHua LU, Ching Hung Tseng, Hong Da Chang, and Chih Hsun Hsu – Siliconware Precision Industries Co., Ltd.	***5. 10:25 AM - A Comprehensive Study of Interfacial Crack Propagation and Delamination in Cu-filled TSV Structure by Incorporating Cohesive Zone Model and Finite Element Method*** Jiubin Fei, Tao Xu, Jie-Ying Zhou, Chang-Bo Ke, and Xin-Ping Zhang – South China University of Technology	***5. 10:25 AM - Photo-Sensitive Polymer Reliability for Fine Pitch RDL Applications*** Emmanuel Chery, Fabrice Duval, Michele Stucchi, John Slabbekoorn, Kristof Croes, and Eric Beyne – IMEC
6. 10:50 AM - Fan-In Panel-Level with Multiple Diced Wafers Packaging John Lau, C. T. Ko, and T J. Tseng – Unimicron	***6. 10:50 AM - Fabrication and Characterization of Through-Glass Vias (TGV) based 3D Spiral and Toroidal Inductors by Cost-Effective ECDM Process*** Harindra Kumar Kannojia, Dileep Mishra, Julfekar Arab, and Pradeep Dixit – Indian Institute of Technology Bombay	***6. 10:50 AM - Dual Damascene: A Solution to Avoid Electrochemical Migration and Cu Oxidation in Fine Line RDLs*** Robert Gernhardt, Markus Woehrmann, and Karin Hauck – Fraunhofer IZM; Habib Hichri and Markus Arendt – Süss MicroTec Photonic Systems, Inc.; Klaus-Dieter Lang – Technische Universität Berlin
7. 11:15 AM - Development of Mold-First Fan-Out Panel-Level Packaging (FO-PLP) on 600mm x 600mm Size Panel Srinivasa Rao Vempati, Ser Choong Chong, and Kazunori Yamamoto – Institute of Microelectronics	***7. 11:15 AM - Low-Temperature Multichip-to-Wafer 3D Integration based on Via-Last TSV using OER-TEOS-CVD and Microbump Bonding without Solder Extrusion*** Kousei Kumahara, Yuki Miwa, Sungho Lee, Rui Liang, Hisashi Kino, Takafumi Fukushima, and Tetsu Tanaka – Tohoku University	***7. 11:15 AM - Process-Consistency-Performance Relationships for Additively Printed Z-Axis Interconnects in Multilayer Circuits*** Pradeep Lall, Kartik Goyal, Nakul Kothari, and Jeff Suhling – Auburn University

Program Sessions: Friday, May 29, 8:00-11:40 a.m.

Session 28: Enhanced Manufacturing and Process Integration	Session 29: Advances in Bonding Materials and Processes	Session 30: RF and Power Components and Modules
Committee: Assembly and Manufacturing Technology	**Committee: Materials & Processing**	**Committee: High-Speed, Wireless & Components**
Session Co-Chairs: **Mark Gerber** **Advanced Semiconductor Engineering, Inc.** **Email: mark.gerber@aseus.com** **Habib Hichri** **Suss Microtech Photonic Systems, Inc.** **Email: Habib.Hichri@suss.com**	**Session Co-Chairs:** **Ziyin Lin** **Intel Corporation** **Email: ziyin.lin@intel.com** **Zhangming Zhou** **Qualcomm** **Email: zhou.zhming@gmail.com**	**Session Co-Chairs:** **Yong-Kyu Yoon** **University of Florida** **Email: ykyoon@ece.ufl.edu** **Craig Gaw** **NXP Semiconductor** **Email: c.a.gaw@ieee.org**
1. 8:00 AM - Varied Ball BGA Technology to Eliminate Solder Ball Bridging Defects in SMT Xiao Lu – Intel Corporation; Heuijong Ju – SSP	***1. 8:00 AM - Development of Bonding Process for Flexible Devices with Fine-pitch Interconnection using Anisotropic Solder Paste (ASP) and Laser-Assisted Bonding (LAB) Technology*** Jiho Joo, Yong-Sung Eom, Ki-Seok Jang, Gwang-Mun Choi, and Kwang-Seong Choi – ETRI	***1. 8:00 AM - A Metamaterial-Inspired Dual-Function Loop Antenna for Wireless Power Transfer and Wireless Communications*** Woosol Lee and Yong-Kyu Yoon – University of Florida
2. 8:25 AM - Full Low Temperature Solder BGA Development for Large Size BGA Package Masateru Koide, Kenji Fukuzono, Seiki Sakuyama, Manabu Watanabe, and Tsuyoshi Yamamoto – Fujitsu Advanced Technologies Limited	***2. 8:25 AM - Demonstration of a Collective Hybrid Die-to-Wafer Integration*** Samuel Suhard, Alain Phommahaxay, Koen Kennes, Pieter Bex, Ferenc Fodor, Maarten Liebens, John Slabbekoorn, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC	***2. 8:25 AM - Power Integrity Performance Gain of a Novel Integrated Stack Capacitor (ISC) Solution for High-End Computing Applications*** Eunseok Song, Dan (Kyung Suk) Oh, Seung-Yong Cha, Jaejune Jang, Taejoo Hwang, Jongkook Kim, Kilsoo Kim, Dae-Woo Kim, Sunghwan Min, and Seungwook Yoon – Samsung Electronics Company, Ltd.
3. 8:50 AM - Thermo-Compression Bonding with Pre-Applied Underfill for Very Large Dies Divya Taneja and David Danovitch – University of Sherbrooke; Catherine Dufort and Pascale Gagnon – IBM Corporation	***3. 8:50 AM - A Novel Low-Temperature Cu-Cu Direct Bonding with Cr Wetting Layer and Au Passivation Layer*** Demin Liu, Po-Chih Chen, and Kuan-Neng Chen – National Chiao Tung University	***3. 8:50 AM - Integrating Magnetic Cores in FOWLP and Their Applications*** Xiao Sun, John Slabbekoorn, Dimitrios Velenis, Inge de Pieter, Pieter Bex, Fabrice Duval, Tom Sterken, Giacomo Talmelli, Christoph Adelmann, Andy Miller, Geert Van der Plas, and Eric Beyne – IMEC
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Thermo Compression Bonding for Large Dies under Protective Atmosphere Stephan Bulacher, Jonathan Abdilla, Birgit Brandstaetter, and Andreas Mayr – Besi Austria GmbH; Ruurd Boomsma – Besi Switzerland AG	***4. 10:00 AM - Direct Bonding of GaN to Diamond Substrate at Room Temperature*** Tadatomo Suga and Fengwen Mu – Meisei University	***4. 10:00 AM - Multi-Physical Simulations and Modelling of an Integrated Module Concept Using GaN-on-Si for Millimetre-Wave Communications*** Kimmo Rasilainen, Koen Buisman, and Christian Fager – Chalmers University of Technology; Kristoffer Andersson – Ericsson AB
5. 10:25 AM - The Effect of Solder Paste Volume on Passive Components Solder Joint Shape and Self-Alignment Ke Pan, Jong Hwan Ha, Lai Pham, Jiefeng Xu, and S. B. Park – Binghamton University	***5. 10:25 AM - Development of Extremely High Thermal Conductivity TIM for Large Electronics Package in the 4th Industrial Revolution Era*** Mi Kyeong Choi, Ron Huemoeller, Hyun Hye Jung, Yong Do Kweon, Mike Kelly Kwang Seok Oh, Dong Su Ryu, Won Chul Do, Kyung Rok Park, and Jin Young Khim – Amkor Technology, Inc.	***5. 10:25 AM - Heterogeneous Integration of 5G and Millimeter-Wave Diplexers with 3D Glass Substrates*** Muhammad Ali, Atom Watanabe, Rao Tummala, and Madhavan Swaminathan – Georgia Institute of Technology; Takenori Kakutani – Taiyo; Markondeya Raj Pulugurtha – Florida International University
6. 10:50 AM - Achieving Selective Cleaning on Semiconductors Packaging Using Atmospheric Pressure Plasma Sagung Kencana, Clarissa Changraini, Wei-Shang Lin, and Yu-Lin Kuo – National Taiwan University of Science and Technology; Wallace Chuang, Eckart Schellkes, and Ken Chang – Robert Bosch Taiwan Co., Ltd.	***6. 10:50 AM - Pressureless Sintering Process of Silver Sinter Paste Using Convection Reflow Oven in Nitrogen for Die Attach*** Guangyu Fan – Indium Corporation	***6. 10:50 AM - Modeling and Characterization of Through-Silicon-Vias (TSVs) in Radio Frequency Regime in Advanced Foveros Technology*** Arian Rahimi, Pratheesh Somarajan, and Kalyan Kolluru – Intel Corporation
7. 11:15 AM - An Additive Production Approach for Microvias and Multilayered Polymer Substrate Patterning of 1µm Feature Sizes Sarthak Acharya, Shailesh Singh Chouhan, and Jerker Delsing – Luleå Technical University	***7. 11:15 AM - A Novel Permanent Bonding Material*** Reihaneh Mohammadi Sejoubsari, Xiao Liu, Srinivas Thanneeru, and Trevor Stanley – Brewer Science	***7. 11:15 AM - Package Co-Design of a Highly Integrated, High Performance, 16-Channel Pulsers and Tx/Rx Switches for Ultrasound Imaging Systems*** Prashuk Jain, Rajen Murugan, Nimran Vajeed, and Aravind Miriyala – Texas Instruments, Inc.

Program Sessions: Friday, May 29, 1:30-5:10 p.m.

Session 31: Automotive and Power Electronics Packaging	Session 32: Stacking and Bonding Technologies	Session 33: Advances in Reliability Assessment
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: Applied Reliability**
Session Co-Chairs: **Young-Gon Kim** **Renesas Electronics America** **Email: young.kim.jg@renesas.com** **Mike Gallagher** **DuPont Electronic and Imaging** **Email: michael.gallagher@dupont.com**	**Session Co-Chairs:** **Nathan Lower** **Collins Aerospace** **Email: nathan.lower@collins.com** **Seung Yeop Kook** **GLOBALFOUNDRIES** **Email: seung-yeop.kook@globalfoundries.com**	**Session Co-Chairs:** **Sandy Klengel** **Fraunhofer Institute for Microstructure of Materials and Systems** **Email: sandy.klengel@imws.fraunhofer.de** **Toni Mattila** **Aalto University** **Email: toni.mattila@aalto.fi**
1. 1:30 PM - Reliability Enhancement of a High-Temperature Double-Sided Power Electronics Module by Topology Optimization Yanghe Liu, Danny Lohan, Yuqing Zhou, Shailesh Joshi, and Ercan Dede – Toyota Corporation	***1. 1:30 PM - A Novel Intermetallic Compound Insertion Bonding to Improve Throughput for Sequential 3D Stacking*** Lin Hou, Jaber Derakhshandeh, Giovanni Capuz, Eric Beyne, Ingrid De Wolf, Andy Miller, and Gerald Beyer – IMEC	***1. 1:30 PM - Investigation on the Mechanical Behavior Evolution Occuring in Lead-Free Solder Joints Exposed to Thermal Cycling*** Abdullah Fahim, S. M. Kamrul Hasan, Jeffrey Suhling, and Pradeep Lall – Auburn University
2. 1:55 PM - Very Low Parasitic Inductance Double Side Cooling Power Modules Based on Ceramic Substrates and GaN Devices Christine Laurant, Benoit Thollin, Johan Delaine, Pierre Périchon, Charley Lanneluc, Antoine Izoulet, and Manon Porlan – CEA; Céline Feautrier – Intitek	***2. 1:55 PM - Ultra-Fine Pitch Au-Sn Interconnections for Packaging and 3D-IC Integration Applications*** Murugesan Mariappan, K. Mori, M. Koyanagi, and T. Fukushima – Tohoku University	***2. 1:55 PM - Reliability of Homogeneous Sn-Bi and Hybrid Sn-Bi/SAC BGAs*** Chongyang Cai, Jiefeng Xu, Huayan Wang, and Seungbae Park – Binghamton University
3. 2:20 PM - Advanced SiC Power Module Packaging Technology Direct on DBA Substrate for High-Temperature Applications: Ag Sinter Joining and Encapsulation Resin Adhesion Chuantong Chen, Zheng Zhang, and Katsuaki Suganuma – Osaka University	***3. 2:20 PM – 7-µm-thick NCF Technology with Low-Height Solder Microbump Bonding for 3D Integration*** Yuki Miwa, Mariappan Murugesan, Sungho Lee, Rui Liang, Kousei Kumahara, Hisashi Kino, Takafumi Fukushima, and Tetsu Tanaka – Tohoku University	***3. 2:20 PM - Empirical Model for the Degradation of IMC in SACQ Solder Bumps during High-Temperature Storage*** Romuald Roucou, Amar Mavinkurve, and René Rongen – NXP Semiconductors; Corinne Bestory – Nexperia
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - High Thermal Die-Attach Paste Development for Analog Devices Kiichiro Higaki, Toru Takahashi, and Akinori Ono – Amkor Technology Japan; Daisuke Koike and Masahiko Hori – Toshiba Electronic Device & Storage Corporation; Keiichi Kusaka, Takayuki Nishi, and Takeshi Mori – Sumitomo Bakelite Co., Ltd.	***4. 3:30 PM - Near-BEOL Chiplet Integration Enabled by High-Density Low-Temperature Interconnections for 3D Heterogeneous Integration: Modeling and Technology Demonstration*** Ankit Kaul, Youngtak Lee, Sreejith Kochupurackal Rajan, Md Obaidul Hossen, and Muhannad S. Bakir – Georgia Institute of Technology	***4. 3:30 PM - Package on System Level Solder Joint Stress Analysis Under Shock Test*** Meng-Kai Shih, Sean Shih, Ryan Chen, David Tarng, and C. P. Hung – Advanced Semiconductor Engineering, Inc.; Wesley Chang and York Liao – Universal Global Scientific Industrial Co., Ltd.
5. 3:55 PM - Demonstration of Package Level 3D-printed Direct Jet Impingement Cooling Applied to High Power, Large Die Applications Tiwei Wei, Herman Oprins, Vladimir Cherman, Geert Van der Plas, and Eric Beyne – IMEC; Zhi Yang, Katie Rivera, Bartlomiej Jan Pawlak, Luke England – GLOBALFOUNDRIES; Martine Baelmans – KU Leuven	***5. 3:55 PM - Quasi-Ambient Bonding Multiple Components in Power Electronics Integration*** Yi Zhong, Shuibao Liang, Stuart Robertson, Allan Liu, Zhaoxia Zhou, and Changqing Liu – Loughborough University	***5. 3:55 PM - An Effective and Application-Specific Evaluation of Low-k Integration Integrity using Cu Pillar Shear Testing*** Arman Ahari and Lee Tae-Kyu – Portland State University; Omar Ahmed and Tengfei Jiang – University of Central Florida; Peng Su and Bernard Glasauer – Juniper Networks
6. 4:20 PM – Sintered Micro-Silver Paste Doped with Indium for Die Attachment Applications of Power ICs Chin-Hao Tsai, Wei-Chen Huang, and C. Robert Kao – National Taiwan University; Ly May Chew and Wolfgang Schmitt – Heraeus Deutschland GmbH & Co. KG; Hiroshi Nishikawa – Joining and Welding Research Institute, Osaka Univ	***6. 4:20 PM - Development of CMOS-Compatible Low Temperature Cu Bonding Optimized by the Response Surface Methodology*** Hae-Sung Park, Han Kyeol Seo, and Sarah Kim – Seoul National University of Science and Technology;	***6. 4:20 PM - Thermal Aging Induced Underfill Degradation and Its Effect on Reliability of Advanced Packaging*** Faxing Che and Lin Ji – IME, Singapore; Xueren Zhang – Xilinx Asia Pacific Pte. Ltd.
7. 4:45 PM - Direct Bonding of Diamond and Si Substrates at Low Temperatures Under Atmospheric Conditions Takashi Matsumae, Yuichi Kurashima, Hitoshi Umezawa, and Hideki Takagi – National Institute of Advanced Industrial Science and Technology	***7. 4:45 PM - Characterization of Low-Temperature Cu-Cu Thermocompression Bonded Interfaces of the Silicon Interconnect-Fabric*** Pranav Ambhore, Umesh Mogera, Ujash Shah, and Subramanian Iyer – University of California, Los Angeles	***7. 4:45 PM - Burn-in Testing (BIT): Is It Always Needed?*** Ephraim Suhir – Portland State University and ERS Co.; Johann Nicolics – Technical University, Vienna, Austria; Sung Yi – Portland State University

Program Sessions: Friday, May 29, 1:30-5:10 p.m.

Session 34: Emerging Materials and Processing	Session 35: Additive Manufacturing and Innovative Materials for Packaging	Session 36: Multiphysics and AI-Enhanced Modeling Approaches
Committee: Materials & Processing	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Jae Kyo Cho** **GLOBALFOUNDRIES** **Email: jaekyu.cho@globalfoundries.com** **Tanja Braun** **Fraunhofer IZM** **Email: tanja.braun@izm.fraunhofer.de**	**Session Co-Chairs:** **Liu Yang** **IBM** **Email: yangliu@us.ibm.com** **Tengfei Jiang** **University of Central Florida** **Email: Tengfei.jiang@ucf.edu**	**Session Co-Chairs:** **Pradeep Lall** **Auburn University** **Email: lall@auburn.edu** **Ning Ye** **Western Digital** **Email: ning.ye@wdc.com**
1. 1:30 PM - Effect of a Backing Material on Bendability of SMD Components on Flexible Substrates Kartik Sondhi, Z. Hugh Fan, and Toshikazu Nishida – University of Florida; Sai Guruva Reddy Avuthu and Nathaniel Richards – Jabil Inc.	***1. 1:30 PM - A Comparative Study of Aerosol Jet Printing on Polyimide and Liquid Crystal Polymer Substrates for RF Applications*** Mohammed Alhendi, Darshana Weerawarne, Ryan Cadwell, Ashraf Umar, El Mehdi Abbara, Mark Poliks and Nancy Huang – Binghamton University; Joseph Iannotti and Nancy Stoffel – GE Global Research	***1. 1:30 PM - Prediction of Fan-out Panel Level Warpage using Neural Network Model with Edge Detection Enhancement*** S. K. Panigrahy and K. N. Chiang – National Tsing Hua University
2. 1:55 PM - Effects of Anchoring Polymer Layer (APL) Anisotropic Conductive Films (ACFs) Properties on the Bending Reliability of Ultra-Fine Pitch Chip-on-Flex (COF) Packages Yan Pan, Seung-Jin Oh, Taek-Soo Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology	***2. 1:55 PM - Design Study of Additively Manufactured Ultrasonic Sensors for Automotive Applications*** Yamini Devidas Kotriwar, Premjeet Chahal, and Sunil Chakrapani – Michigan State University; Mahmoud Ghannam – Ford Motor Company	***2. 1:55 PM - Implementation of General Coupling Model of Electromigration in ANSYS*** Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology
3. 2:20 PM - Highly Sensitive Flexible Pressure Sensor Based on Conducting Elastic Microspheres Jianing Wu – Fudan University	***3. 2:20 PM - Investigation of Pressureless Sintered Interconnections on Plasma Based Additive Copper Metallization for 3-Dimensional Ceramic Substrates for Surface Acoustic Wave Sensors in High Temperature Applications*** Christian Schwarzer, Frederik Roth, and Michael Kaloudis – Aschaffenburg University of Applied Sciences; Alexander Hensel and Joerg Franke – Friedrich-Alexander-University Erlangen-Nuremberg	***3. 2:20 PM - Learning the Stress-Strain Relationships of Ultra-Thin Package Materials using a Bayesian Approach*** Cheryl Selavanayagam, Pham Luu Trung Duong, and Nagarajan Raghavan – Singapore University of Technology and Design
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Panel Packaging Approach to Hermetic Sealing Micro Thin Film Battery for Healthcare and Internet of Things (IoT) Applications Qianwen Chen, Leanna Pancoast, Jae-woong Nah, Bing Dang, and John Knickerbocker – IBM Corporation; Andy Shih, Bo Wen Cheng, Kai Liu, Mengnian Niu, and Simon Nieh – Front Edge Technologies	***4. 3:30 PM - Electrical Isolation Performance of Microgasket Technology for Implant Packaging*** Paritosh Rustogi and Jack Judy – University of Florida	***4. 3:30 PM - Numerical Study of Edge Condensation in Wafer-to-Wafer Bonding Process with Lattice Boltzmann Approach*** Jung Shin Lee, Jun Hyung Kim, and Minwoo Daniel Rhee – Samsung Electronics Company, Ltd.
5. 3:55 PM - Embedded Power Inductor in Organic Substrate with Novel Magnetic Epoxy Harrison Chang and Thomas Wang – Advanced Semiconductor Engineering, Inc.	***5. 3:55 PM - Thermomechanical Reliability Enhancement of High-Power MEMS with Movable Structure Based on Implanted Skin Hairs*** Yunna Sun, Yongpeng Wu, Hongfang Li, Yan Wang, Zhuoqing Yang, Guifu Ding, and Yuzhuo Fu – Shanghai Jiao Tong University	***5. 3:55 PM - Experimental-Numeric Approaches in the Dynamic Characterization and Fatigue Strength Derivation of Viscoelastic Thermal Interface Layers*** Alaa Fezai and Anuj Sharma – Robert Bosch GmbH; André Zimmermann – University of Stuttgart
6. 4:20 PM - Extreme Thin Peltier Modules Fabricated by the Printed Electronics Method Yuta Seki, Masaya Todaka, Wataru Morita, Kunihisa Kato, Tsuyoshi Mutou, and Koichi Nagamoto – LINTEC Corporation	***6. 4:20 PM - Integrated and Discrete Ultra-Thin Capacitors Based on Carbon Nanofibers with High Capacitance Density*** Rickard Andersson, Maria Bylund, Sascha Krause, Victor Marknas, Amin Saleem, Mohammad Kabir, and Vincent Desmaris – Smoltek	***6. 4:20 PM - Coupled Thermal Mechanical Simulation Methodology to Estimate BGA Reliability of 2.5D Packages*** Manish Nayini and Janak Patel – Marvell; Timothy Horn and Lloyd Burrell – GLOBALFOUNDRIES
7. 4:45 PM - The Demonstration of High-Quality Carbon Nano-Tubes (CNTs) and Advanced Patterned Technique for the Application in Vertically 3D Integrated Technologies M. H. Liao, P. Y. Lu, Y. R. Li, T. H. Chan, C. M. Yen, Y. J. Feng, Y. H. Wang, and K. Y. Wang – National Taiwan University; C. C. Lee – National Tsing Hua University; M. H. Lee – National Taiwan Normal University	***7. 4:45 PM - Role of Grain Size on the Effective Resistivity of Cu-Graphene Hybrid Interconnects*** Rahul Kumar, Sunil Pathania, Somesh Kumar, Surila Guglani, Amit Kumar, Sourajeet Roy, and Rohit Sharma – Indian Institute of Technology, Ropar	***7. 4:45 PM - Three-dimensional Simulation of Effects of Electro-Thermo-Mechanical Multi-Physical Fields on Cu Protrusion and Performance of Micro-Bump Joints in TSVs Based High Bandwidth Memory (HBM) Structures*** Jie-Ying Zhou, Zheng Wang, Cheng Wei, Jiu-Bin Fei, Chang-Bo Ke, and Xin-Ping Zhang – South China University of Technology

Interactive Presentations: Wednesday, May 27, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, May 27, 2020

Session 37: Interactive Presentations 1
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Session Co-Chairs:
Mark Eblen
Kyocera Corporation
Email: mark.eblen@kyocera.com

Jeffrey Lee
iST-Integrated Service Technology, Inc.
Email: jeffrey_lee@istgroup.com

High Bandwidth Low Power 2.5D Interconnect Modeling and Design
Qian Ding, Jenny Jiang, Yee Huan Yew, and Hui Liu – Intel Corporation

Autocatalytic Tin – How to Overcome Process Limitations to Introduce a New Solution for Thick Tin Plating
Britta Schafsteller, Gustavo Ramos, Kadir Tuna, and Sandra Nelle – Atotech Deutschland GmbH

Processing Glass Substrate for Advanced Packaging using Laser Induced Deep Etching
Jean-Pol Delrue, Rafael Santos, Norbert Ambrosius, Roman Ostholt, and Stephan Schmidt – LPKF Laser & Electronics AG

Chip Package Interaction (CPI) Risk Assessment of 22FDX® Wafer Level Chip Scale Package (WLCSP) using 2D Finite Element Analysis Modeling
Kashi Vishwanath Machani, Frank Kuechenmeister, Dirk Breuer, and Christian Klewer – GLOBALFOUNDRIES Dresden Module One LLC & Co. KG; Jae Kyu Cho and Kristina Young-Fisher – GLOBALFOUNDRIES Inc.

Integration of GaN-LEDs with Heterogeneous Device Components by Epitaxial Film Bonding
Mitsuhiko Ogihara – JFE Shoji Electronics Corporation; Yoshiteru Amemiya and Shin Yokoyama – Hiroshima University

Characteristics of Dielectric Film Surfaces for Low-Temperature Direct Wafer Bonding
Seongmin Son, Junhong Min, Hoechul Kim, Hyungjun Kim, Seokho Kim, Hoonjoo Na, Sangjin Hyun, and Kihyun Hwang – Samsung Electronics Company Ltd.; Kihyun Kim and Geun Young Yeom – Sungkyunkwan University

A Study on Laser-Assisted Bonding (LAB) to Luminescence Characteristics of Blue and YAG Phosphor Encapsulated InGaN LEDs
Matthias Fettke, Andrej Kolbasow, Timo Kubsch, Alexander Frick, and Thorsten Teutsch – PacTech GmbH; Vinith Bejugam – PacTech US Inc.; Yu-Chung Wang Wang and Juha Rantala – Inkron Ltd.

Demonstration of a High-Bandwidth (>1 Tbps/mm) Fine-pitch (≤10 µm) Assembly on the Silicon Interconnect Fabric
Siva Chandra Jangam, Uneeb Rathore, Sumeet Nagi, Dejan Markovic, and Subramanian Iyer – University of California, Los Angeles

Evaluation of the Effect of Pad Surface Finish and Isothermal Aging on the Mechanical Behavior of Sn-Bi Solder Alloys
Travis Dale, Sukshitha Achar, Yaohi Fan, Yifan Wu, Ganesh Subbarayan, and Carol Handwerker – Purdue University; Nilesh Badwe – Intel Corporation

High Speed Ultra Accurate Direct C2W Bonding and Insitu Bonding Behavior Observation
Ruurd Boomsma – Besi Switzerland AG; Peter Unterwaditzer, Birgit Brandstaetter, Norbert Bilewicz, Hubert Selhofer, and Andreas Mayr – Besi Austria GmbH

Growth Mechanism of Interfacial IMCs on (111) Preferred Orientation Nanotwinned Cu UBM for 3D Packaging
Mingliang Huang and Yang Wu – Dalian University of Technology

A Study of the Electrical and Mechanical Behaviors of Printed Conductive Interconnects on Stretchable Textiles for Smart Clothing Applications
Kankanige Udara Somarathna, Behnam Garakani, Mohammed Alhendi, Peter Borgesen, and Mark Poliks – Binghamton University; Azar Alizadeh – GE Global Research

Curekinetic Modeling of Interfacial Reactions between Epoxy and Silica Filler Suspension System in Non-Conductive Paste for 3DIC TSV Packaging
Minwoo Rhee – Samsung Electronics Company, Ltd.

Molded Optical Platform for Highly Precise Integrated Optical Packages
Sebastian Bengsch, Eike Fischer, Sascha de Wall, and Marc Wurz – Leibniz Universität Hannover

High-Bandwidth and Multi-Channel Power over Coaxial Filters for Automotive LVDS Interconnect
Yutaka Uematsu and Hideyuki Sakamoto – Hitachi Ltd.

Warpage and Void Simulation of System in Packages (SiP)
Eric Ouyang, Yonghyuk Jeong, and Jae Myong Kim – JCET; Susan Lin, Jay Vang, and Anthony Yang – Moldex3D

A Pen-Writable Electroless Plating Method for Large-Area RF Circuit Applications
Yihang Chu, Nicholas Bannon, and Premjeet Chahal – Michigan State University

Thermal and Power Delivery Aware Floor-Planning for Heterogeneous Multiple Cores Design
Yunhyeok Im, Hoi-Jin Lee, Young-Sang Cho, Heeseok Lee, and Yohan Kwon, Jisoo Hwang, James Jeong, and Heejung Choi – Samsung Electronics Company, Ltd.

A New C-FDFD Method Capturing Per-unit Distance Line Parameter Matrix for Crosstalk Analysis with Reducing Computational Resource
Heeseok Lee, Jisoo Hwang, and Taekeun An – Samsung Electronics Company, Ltd.

Robustness of Carbon Nanofiber-based MIM Capacitors with Ultra-High Capacitance Density to Electrical and Thermal Stress
Maria Bylund, Rickard Andersson, Maria Bylund, Victor Marknas, Mohammad Kabir, Amin Saleem, and Vincent Desmaris – Smoltek

Constant Poisson's Ratio of Thermosetting Polymers: Is It Reasonable for Accurate Thermal Stress Analyses?
Bongtae Han, Sukrut Phansalkar, and Hyun Seop Lee – University of Maryland

Panel Warpage and Die Shift Simulation and Characterization of Fan-Out Panel-Level Packaging
Faxing Che, Kazunori Yamamoto, and Vempati Srinivasa Rao – Institute of Microelectronics

Effective Thermal Solution via Wafer Level Packaging Materials
Junghwa Kim, Jungseob Kim, Woo-Chul Na, Donghwan Lee, and Sang Kyun Kim – Samsung Electronics Company Ltd.

Assembly Technologies for Piezoelectric Sensors up to 1000°C
Fabian Kohler and Jürgen Wilde – Department of Microsystems Engineering (IMTEK)

Tri-axis Polarized Dual-band Loop Antenna in 3D-SiP for mmWave Wireless Inter/Intra Chip Communications
Hae-in Kim and Yong-Kyu Yoon – University of Florida

Thermo Co-design of RF Power Amplifier on Fan-Out with Thermal Simulation and Optimization
Shihwen Lu, Harrison Chang, and Jifuh Liang – Advanced Semiconductor Engineering, Inc.

Impact of PVD and EL-Ni Seed Layers on Cu-Bottom-Up Electroplating in High Aspect Ratio (>10) TSVs for 3D-IC Packaging Applications
Murugesan Mariappan, K. Mori, and T. Fukushima – Tohoku University; Y. Hara, E. Webb, J. Sukamto, and M. Kodera – MLI

Effects of Process Parameters on Electromechanical Reliability of Screen-Printed Silver Interconnect on High-Density Polyethylene Fibers for Wearable Electronics
Behnam Garakani, K. Udara S. Somarathna, Mohammed Alhendi, Mark Poliks, and Peter Borgesen – Binghamton University; Azar Alizadeh – GE Global Research

Wednesday, May 27, 2020

Session 38: Interactive Presentations 2
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Rao Bonda
Amkor Technology, Inc.
Email: rao.bonda@amkor.com

Pat Thompson
Texas Instruments, Inc.
Email: patrick.thompson@ti.com

Controls on the Transport of Particles/Cells in Deterministic Lateral Displacement via Symmetric Airfoil with Angle of Attacks
Jong-Hoon Kim, Brian Senf, and Jong-Hoon Kim – Washington State University

Moisture Effect on Physical Failure of Plastic Molded SiP Module
Jeffrey Lee and ChengChih Chen – iST-Integrated Service Technology, Inc.

Selective EMI Shielding Technologies for Current and Next Generation System-in-Package (SiP) Modules
Udara Silva, Heedong Lee, Wonyong Choi, Minku Park, Heung-gu Kim, Sanghyun Kim, Icksu Hwang, and Junam Moon – Genesem, Inc.

Thermal Analysis, Characterization and Material Selection for SiC Based Intelligent Power Modules
Gongyue Tang, Leong Ching Wai, Siak Boon Lim, Boon Long Lau, Kazunori Yamamoto, and Xiaowu Zhang – Institute of Microelectronics

A Study of the Board Level Reliability of Large 16FF Wafer Level Package for RF Transceivers
Andreas Wolter, Thomas Wagner, Bernd Waidhas, Horst Baumeister, and Ceren Yeni – Intel Deutschland GmbH; Beth Keser – Intel Corporation

Finite Element Modeling Methodology for Monotonic Bend Test of Flip-Chip BGA Package
Scott McCann, Tom Lee, and Suresh Ramalingam – Xilinx

Study of Solder Interconnect Configurations and Performance of Vertical Laser Assisted Assembled 3.5D Packages
Andrej Kolbasow, Matthias Fettke, Timo Kubsch, Alexander Frick, and Thorsten Teutsch – PacTech GmbH; Vinith Bejugam – PacTech US, Inc.

Lifetime Modeling of Flexible Batteries under Dynamic Folding with Varying C-Rates and Temperatures
Pradeep Lall and Ved Soni – Auburn University

Imaging Sub-Surface Defects in Power Electronic Modules using Shear-force Microscopy
Vishnu Baba Sundaresan – The Ohio State University; Shailesh Joshi – Toyota Engineering & Manufacturing North America, Inc.

A Green Sonochemical Synthesis of Cu@ Ag Core-Shell Nanoparticles for Power and Flexible Printed Electronics
Hongjun JI – Harbin Institute of Technology at Shenzhen

3D FOWLP Integration
Teck Guan Lim, David Soon Wee Ho, Tai Chong Chai, and Surya Bhattacharya – Institute of Microelectronics A*STAR

New Molding Technology Enabling Advanced Packaging Technology
Takashi Saito, Tokuyuki Kitajima, Makoto Kawaguchi, and Shinya Tajima – Apic Yamada

Development of Compression Molding Process for Fan-Out Wafer Level Packaging
Julien Bertheau, Fabrice Duval, Tadashi Kubota, Pieter Bex, Koen Kennes, Alain Pommahaxaay, Arnita Podpod, Eric Beyne, Andy Miller, and Gerald Beyer – IMEC

Evolution of the Properties of SAC-Bi-Ni-Sb Lead-Free Solder During Mechanical Cycling
Mohd Aminul Hoque, Mohammad Ashraful Haq, Md Mahmudur Chowdhury, Jeffrey Suhling, and Pradeep Lall – Auburn University

Thermomechanical Analysis of a Hybridized Flip-Chip IR FPA including Warpage and XRD Stress Measurements at Cryogenic Temperature
Lucas Duperrex, Raphaël Pesci, and Pascal Le Boterf – Lynred; Olivier Mailliart – CEA LETI

Application of Package-Level High-Performance EMI Shield Material with a Novel Nozzleless Spray Coating Technology
Stuart Erickson – Ultrasonic Systems, Inc.; Mike Sakaguchi – Tatsuta Electric Wire & Cable Co., Ltd.

The Influence of Different-Sized Ni Micro- and Nanopowders on the Processing and Microstructural Properties of Sn-Ag-Cu-Solder with Low Ag Content
Simon Florian Keim, Ulrich Tetzlaff, and Gordon Elger – Technische Hochschule Ingolstadt

Maleimide Molding Film for High-Temperature Applications and Its Reliabilities
Kazuhiro Kikuchi, Yasunori Karasawa, Yasutaka Watanabe, and Takashi Sugino – Lintec Corporation; Tadashi Suetsugu – Fukuoka University

Embedded 3D-IPD Technology based on Conformal 3D-RDL: Application for Design and Fabrication of Compact, High-Performance Diplexer and Ultra-Wide Band Balun
Ayad Ghannam, Alessandro Magnani, David Bourrier, and Thierry Parra – 3DiS Technologies

Effect of Ni(P) Thickness of Ultrathin ENEPIG on the Interfacial Reaction and Board Level Reliability of Solder Joints
Yibo Wang, Charles Nan-Cheng Chen, Ming Li, and Liming Gao – Shanghai Jiaotong University

Development of Integrated Pressure and Temperature Sensing Strips for Monitoring Venous Leg Ulcer Application
Ruiqi Lim, David Sze Wai Choong, and Ming-Yuan Cheng – Institute of Microelectronics

45RFSOI WLCSP Board Level Package Risk Assessment and Solder Joint Reliability Performance Improvement
Haojun Zhang, Zhuo-Jie Wu, John Malinowski, Millete Carino, Kristina Young-Fisher, Jean Trewhella, and Patrick Justison – GLOBALFOUNDRIES

Development of Nano-Capsuled Thermal Interface Material using Graphene Coated Nanoparticles
Caroline Sunyong Lee, Hyo Jun Kim, and Caroline Sunyong Lee – Hanyang University; Sarah Eunkyung Kim – Seoul National University of Science and Technology

An Embedded SiC Module with using NMPB Interconnection for Chevron-shaped Cu Lead and Chip Electrodes
Kohei Tatsumi – Waseda University

Flexible Inkjet Printed Patch Antenna Array on Mesoporous PET Substrate for 5G Applications with Stable RF Performance after Mechanical Stress Cycling
Gurvinder Singh Khinda, Ashraf Umar, Mohammed Alhendi, Mark Poliks, and Ryan Cadwell – Binghamton University; Nancy Stoffel – GE Global Research

LTCC PoP Technology-Based Novel Approach for Next-Generation mm-Wave 5G Communication System
Surender Singh, Taranjit Kukal, and John Park – Cadence

Design and Verification of Air Corrosion Acceleration Test on Dram Memory Modules at Data Center Environments
Yuchul Hwang, Mubo Keum, and Kunhan Kim – Samsung Electronics Company, Inc.

Thursday, May 28, 2020

Session 39: Interactive Presentations 3
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Session Co-Chairs:
Michael Mayer
University of Waterloo
Email: mmayer@uwaterloo.ca

Kristina Young-Fisher
GLOBALFOUNDRIES
Email: Kristina.Young-Fisher@globalfoundries.com

Stripline-Slotline Rectangular Resonators for Measurement of Uniaxial Anisotropic Permittivity of Composite PCB Dielectric Material
Zhaoqing Chen – IBM Corporation

A Handling Solution for Easy Processing of Thin Glass with TGV
Shelby Nelson, David Levy, and Aric Shorey – Mosaic Microsystems

Bending Effects on a Fabric-Based Antenna for Wearable Applications
Hsuan-Ling Kao and Chun-Hsiang Chuang – Chang Gung University

"Molded-Package-Last" Process for Fan-Out System in Package (FO-SiP)
Tomoaki Shibata, Tsuyoshi Ogawa, Satoshi Yoneda, Xinrong Li, Naoya Suzuki, and Toshihisa Nonaka – Hitachi Chemical Co., Ltd.

Printing Uniform QDs Polymer Thin Films for QLED Applications
Ning TU, Jeffery C.C. Lo, and Shi Wei Lee – Hong Kong University of Science & Technology

A New RDL-First PoP Fan-Out Wafer-Level Package Process with Chip-to-Wafer Bonding Technology
Seung Nam Son – Amkor Technology Korea, Inc.

The Bonding Properties of Various Surface Finishes with Cu Paste for Pressure Sintering
Junglae Jo, Kei Anai, Shinichi Yamauchi, Takashi Hattori, and Takahiko Sakaue – Mitsui Mining & Smelting Co., Ltd.

Nickel Dependence of Hydrogen Co-Deposition and Nanoporosity for Electroless Deposited Cu-Films
Tobias Bernhard, Kay Wurdinger, Lutz Stamp, and Frank Brüning – Atotech Deutschland GmbH

Alternative Interposer Package-On-Package with Adhesive Application
JaeYun Kim, Gyu Wan Han, Se Hwan Hong, SeungJae Yu, Dong Joo Park, Kyung Rok Park, and Jin Young Khim – Amkor Technology Korea, Inc.; Corey Reichman – Amkor Technology, Inc.

Pressureless Transient Liquid Phase Sintering Bonding using SAC305 with Hybrid Ag Particles for High-Temperature Packaging Applications
Byeong-Uk Hwang, Kyung Deuk Min, Choong-Jae Lee, Kwang-Ho Jung, Jae-Ha Kim, and Seung-Boo Jung – Sungkyunkwan University

Low Power SOC Based on High-Density MIM Capacitor for beyond Moore Era by Robust Power Integrity Achievement
Jisoo Hwang, Heeseok Lee and Hoi-Jin Lee – Samsung Electronics Company, Ltd.

Strategies Relating to CMP for Die to Wafer Interconnects utilizing Hybrid Direct Bonding
Jonatan Sierra Suarez, John Mudrick, Crystal Sennett, Tom Friedmann, Shawn Arterburn, Matthew Jordan, Lisa Caravello, Jordan Gutierrez, and Michael David Henry – Sandia National Laboratories

The Board Level Reliability Performance and Process Challenges of Ultra-Thin WLP (Package Height < 250 µm)
Kuei Hsiao Kuo, Chun Yi Chiang, Kuang Hsin Chen, Stan Chen, and Feng Lung Chien – Silicon Precision Industries Company, Ltd.

Turbulent Flows Impingement on High Power Multi-Chip Bare Die Package
Prabhakar Subrahmanyam and Ying-Feng Pang – Intel Corporation

Effects of Two-Step Plasma Treatment on Cu and SiO2 Surfaces for 3D Bonding Application
Han Kyeol Seo, Hae Sung Park, and Sarah Kim – Seoul National University of Science and Technology; Ga Hee Kim and Young Bae Park – Andong National University

Ultrasonically Assisted Nano Ag-Al Binary Alloy Sintering to Enable Low-cost, High-Temperature Electronic Interconnections for Wide-Band-Gap Device Integration
Canyu Liu, Allan Liu, Yi Zhong, Stuart Robertson, Zhaoxia Zhou, and Changqing Liu – Loughborough University

Design of Optical Transmitter Module for O-band Silicon Photonic Engine
Hsien Wu, Jau-Ji Jou, Yaw-Dung Wu, Po-Jui Chiang, Ting-Jen Hsueh, and Tien-Tsorng Shih – National Kaohsiung University of Science and Technology; Pei-Hao Tseng – Teratech Optical Communication Inc.; Chun-Nien Liu and Wood-Hi Cheng – National Chung Hsin University

Nanowire Impregnated Poly-dimethyl Siloxane for Flexible, Thermally Conductive Fan-Out Wafer-Level Packaging
Randall Irwin, Yuan Hu, Arsalan Alam, Samatha Benedict, Goutham Ezhilarasu, Guangqi Ouyang, Timothy Fisher, and Subramanian Iyer – University of California, Los Angeles

Beamforming Design Using Millimeter Wave Dual-Polarized Transmit-Array for 5G Small Cell Base-Station Applications
Lih-Tyng Hwang – NSYSU; Chung-Yi Hsu and Hung-Wei Chung – National Sun Yat-sen University

Design and Simulation of Symmetric Direct Wafer-to-Wafer Bonding Compensating a Gravity Effect
Kyeongbin Lim, Minsoo Han, Gwanghee Jo, Hyeonjun Yun, Jewon Lee, Jun Hyung Kim, SeungDae Seok, and Minwoo Daniel Rhee – Samsung Electronics

The Creep Behavior and Electrical Resistance Analysis of Serpentine Carbon-Polymer Conductor for Flexible Wearables
Chong Ye, Anuja Kandare, and Suresh Sitaraman – Georgia Institute of Technology

Thermal Management of Multi-Chip Glass Panel Embedded Packages: Package Architecture vs. Heat Flux Density
Ryan Wong, Siddharth Ravichandran, and Vanessa Smet – Georgia Institute of Technology

Visualization and Modeling of Microstructural Evolution in SAC305 BGA Joints During Extreme High Temperature Aging
KM Rafidh Hassan, Mohammad Alam, Jing Wu, Jeffrey Suhling, and Pradeep Lall – Auburn University

Electromechanical Finite Element Analysis for Designed Low-frequency MEMS Piezoelectric Vibration Energy Harvester
Ling Xu, Shengrui Zhou, Yingfei Xiang, and Yinglin Yang – Fudan University

Minimally Invasive Fixtures for Multi Gb/s Channel Characterization with a Logic Analyzer
Matteo Cocchini, Khaalid McMillan, Wiren Becker, Michael Cracraft, Matt Doyle, and Jason Bjorgaard – IBM Corporation

Thursday, May 28, 2020

Session 40: Interactive Presentations 4
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Nam Pham
IBM Corporation
Email: npham@us.ibm.com

Pavel Roy Paladhi
IBM Corporation
Email: Pavel.Roy.Paladhi@ibm.com

Study on Advanced Substrate for Double-Side Package to Reduce Module Size
Ji-Hee Kim, Kwan-Sun Yoon, Jong-Young Park, Kwang-Seop Youm, Eun-Chul Ahn, Young-Hwan Shin, and Young-Jae Kim – Daeduck Electronics Co., Ltd.

Extracting Power Supply Current Profile by using Interposer-Based Low-Noise Probing Technique for PDN Design of High-Density POP
Heeseok Lee, Hoijin Lee, and Jisoo Hwang – Samsung Electronics Company, Ltd

Design and Fabrication of Band-Pass Filter on Glass IPD for 5G New Radio
Yu-Chang Hsieh, Yu-Chang Hsieh, Cheng-Yuan Kung, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

Antenna on Interconnect Fabric
Arpan Dasgupta, Yu-Tao Yang, Umesha Mogera, and Subramanian S. Iyer – University of California, Los Angeles

Design and Validation of Reliability Physics for Interconnect Architectures Induced from Inclusive TM/SM/EM Effects
Jui-Chang Chuang – National Tsing Hua University

Synthesis of Boron Nitride Coated Silica Filler for Preparing Thermally Conductive Epoxy Composites
Jiaxiong Li, Kyoung-sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

Evaluation of ICP Sputter Etch with Reducing Atmosphere for the Improvement of Rc in UBM/RDL Applications
Patrik Carazzetti, Juergen Weichart, Andreas Erhart, Mohamed Elghazzali, and Ewald Strolz – Evatec

Low Loss BT Resin for Substrates in 5G Communication Module
Katsuya Yamamoto, Shouta Koga, Saori Seino, Kazuyuki Higashita, Keiichi Hasebe, Eisuke Shiga, Tsuyoshi Kida, and Syu Yoshida – Mitsubishi Gas Chemical Company, Inc.

Ultra -Thin Atomic Layer Deposited Al2O3 for Encapsulation of the Silicon Interconnect Fabric
Niloofar Shakoorzadeh Chase, Yu-Tao Yang, and Subramanian S. Iyer – University of California, Los Angeles

Demonstration of Superconducting Interconnects on the Silicon Interconnect Fabric Using Thermocompression Bonding
Yu-Tao Yang, Peng Zhang, Umesha Mogera, Kang L. Wang, and Subramanian Iyer, Chaowei Hu, Jazmine Green, Ni Ni, Niloofar Shakoorzadeh, and Pranav Ambhor – University of California, Los Angeles

Chip/Package/Board Co-Design Methodology Applied to Full-Custom Heterogeneous Integration
Thomas Brandtner and Natalia Floman, Klaus Pressel, Michael Schultz, and Michael Vogl – Infineon Technologies AG

Guided-Mode Resonance Filter for Micro-Optic Spectrometer
Junichi Inoue and Shogo Ura – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology

Wideband Low-Profile AMC-based Patch Antenna for 5G Antenna-in-Package Application
Weikang Wan, Mei Xue, Liqiang Cao, Tianchun Ye, and Qidong Wang – Institute of Microelectronics of Chinese Academy of Sciences

Investigation of Mechanical Behavior and Aging Effects of SAC305 Solder Joints at Extreme High Temperatures Using Nanoindentation
Mohammad Alam, KM Rafidh Hassan, Abdullah Fahim, Jing Wu, Sudan Ahmed, Jeffrey Suhling, and Pradeep Lall – Auburn University

A Design and Fabrication of Transmission Line Based on eSiFO for Millimeter-wave Applications
Shengjuan Zhou, Jian Cai, Qian Wang, Xuesong Zhang, and Yu Chen – Tsinghua University

Irregular Bumps Design Planning for Modern Ball Grid Array Packages
Ya-Ying Chien, Hung-Ming Chen, Jyun-Ru Jiang, and Ya-Ying Chien – National Chiao Tung University, Taiwan; Yun-Chih Kuo, Hsien-Ting Tsai, and Simon Yi-Hung Chen – MediaTek Inc.

Progress and Applications of Embedded System in Chip (eSinC®) Technology
Shuying Ma, Jianwei Chen, Jiao Wang, Daquan Yu, Aimo Xiao, and Xiaobing Yang – Huantian Technology (Kunshan) Electronics Co., Ltd.

Development of UV Curable Wafer Back Side Protection-Film for Wafer Level Chip Size Package
Yuichiro Komasu, Rikiya Kobashi, Mirei Usuba, Daisuke Yamamoto, Naoya Saiki, and Shinya Takyu – Lintec Corporation

Outstanding Reliability Performances of Silicon Capacitors for 200°C Automotive Applications
Sébastien Jacqueline, Laurent Lengignon, and Catherine Bunel – Murata

3D Composite Glass-Silicon Interposer Integrated with Polymer Arrayed Waveguide Grating
Ziji Wang – Southeast University

A Highly Reliable Die Bonding Approach for High-Power Devices by Low-Temperature Pressureless Sintering Using a Novel Cu Nanoparticle Paste
Hai-Jun Huang, Xue Wu, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

Growth Kinetics of Intermetallic Compound Layers at the Interface during Laser-Assisted Bonding Depending on Surface Finish
Hong-Sub Joo – Samsung Electronics Company, Ltd.; Kyung Deuk Min, Choong-Jae Lee, Byung-Uk Hwang, and Seung-Boo Jung – Sungkyunkwan University

Development of 3D DRAM Packaging Approach with Assistance of Prefabricate TSV Chips and Fan-Out Technology
Chengqian Wang, Wenxue Tang, Rongzhen Zhang, Xuefei Ming, Yan Huang, and Yang Li – The 58th Research Institute of China Electronics Technology

Influence of the Vibration Direction in Ultrasonic Assisted Low-Temperature Sintering
Henning Seefisch, Jens Twiefel, and Jörg Wallaschek – Leibniz Universität Hannover, IDS

3D Micro Bump Interface Enabling Top Die Interconnect to True Circuit Through Silicon Via Wafer
Nistec Chang, Key Chung, Yu-Po Wang, P. J. Su, Teny Shih, and Nicholas Kao – Siliconware Precision Industries Co., Ltd.

Molecular Dynamics Study of the Influence of Aggregation and Percolation in Al2O3/ Polyethylene Oxide Nanofluids on the Effective Thermal Conductivity
Barbara Poliks and Bahgat Sammakia – Binghamton University

Design, Fabrication, and Characterization of a Q-band Patch Antenna Integrated on Stacked Interposers
Yunheng Sun and Yufeng Jin – Peking University Shenzhen Graduate School; Shenglin Ma, Dan Gong, and Xinxin Hu – Xiamen University; Wei Wang and Jing Chen – Peking University; Liulin Hu and Shuwei He – Chengdu Ganide Technology

Friday, May 29, 2020

Session 41: Student Interactive Presentations
Time: 8:30 AM – 10:30 AM

Committee: Interactive Presentations

Session Co-Chairs:
Ibrahim Guven
Virginia Commonwealth University
Email: iguven@vcu.edu

Alan Huffman
Micross Advanced Interconnect Technology
Email: alan.huffman@micross.com

A Design Flow for Micro Bump and Stripe Planning on Modern Chip-Package Co-Design
Ming-Yu Huang, Hung-Ming Chen, and Kuan-Neng Chen – National Chiao Tung University; Shih-Hsien Wu – Industrial Technology Research Institute

Local Hot Spot Cooling by Planar-Radial Structure TEC Device on Mobile Electronics
Cheol Kim, Sungtae Kim, and Young-Chang Joo – Seoul National University; Jeonglim Yoon and Youngcheol Joo – Soonchunhyang University; Hai-shan Shen and Hoojeong Lee – Sungkyunkwan University

Preparation of Autonomously Self-Healing Electrode Based on Double-Network Supramolecular Elastomer
Miao Tang and Zhuo Li – Fudan University

Investigation of Underfilling BGAs Packages-Thermal Fatigue
Vanlai Pham, Jiefeng Xu, Ke Pan, and Seungbae Park – Binghamton University; Huayan Wang – Xilix Inc.; Charandeep Singh – Corning Inc.

Design and Fabrication of an Ultra-Thin Silicon Vapor Chamber for Compact Electronic Cooling
Quentin Struss – STMicroelectronics; Perceval Coudrain and Jean-Philippe Colonna – CEA; Abdelkader Souifi and Christian Gontrand – INSA Lyon; Luc G. Fréchette – Université de Sherbrooke

Impact of Viscoelastic Properties of Low Loss Printed Circuit Boards (PCBs) on Reliability of WCSP Packages under Drop Test
Akshay Boovanahally Lakshminarayana, Abel Misrak, Rabin Bhandari, ASM Raufur R Chowdhury, Tushar Jashvanthbhai Chauhan, and Dereje Agonafer – University of Texas at Arlington

Design of 4-Channel 25 Gbaud/s PAM-4 Optical Transmitter Module for Short Reach Applications
I-Cheng Hou, Chung-Han Chang, Jau-Ji Jou, Tien-Tsorng Shih, Ting-Jen Hsueh, Po-Jui Chiang, and Yaw-Dung Wu – National Kaohsiung University of Science and Technology; Pei-Hao Tseng – Teratech Optical Communication, Inc.

Effects of Magnetic Field on Dispersion of Conductive Particles in Anchoring Polymer Layer (APL) Anisotropic Conductive Films (ACFs) for Ultra-Fine Pitch Interconnection
Dal-Jin Yoon, EunKyoung Ko, EunHo Lee, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

First Principle Analysis of Li-Doped Armchair Graphene Nanoribbons for Nanoscale Metal Interconnect Applications
Vipul Nishad, Atul Nishad and Rohit Sharma – Indian Institute of Technology, Ropar

Fabrication of High Q-Factor Resonators using a Hybrid Rigid-Flex Process
Vincens Gjokaj and Premjeet Chahal – Michigan State University

A Wireless Battery-Less Seat Sensor for Autonomous Vehicles
Saikat Mondal, Saranraj Karuppuswami, Kanishka Wajiwardena, Deepak Kumar, and Premjeet Chahal – Michigan State University; Mahmoud Ghannam and Mark Cuddihy – Ford Motor Company

Deep Trench Capacitors in Silicon Interconnect Fabric
Kannan Kalappurakal Thankappan and Subramanian Iyer – University of California, Los Angeles

Strain and Surface Warping Detection of Interconnect Microstructures via Laser Diffraction
Todd Houghton and Hongbin Yu – Arizona State University

Inverse Design of Substrate from Warpage Surrogate Model Using Global Optimisation in Ultra-Thin Packages
Cheryl Selvanayagam, Pham Luu Trung Duong, and Nagarajan Raghavan – Singapore University of Technology and Design

Identification of Polymer Materials in Electronic Packages including Counterfeit Prevention
Junbo Yang, Jiefeng Xu, and Seungbae Park – Binghamton University

Novel Approach of Highly Conductive Interconnects for 3D-Printed Microsystems
Ahmad Alforidi and Dean Aslam – Michigan State University; Da Li and Xiaogan Liang – University of Michigan

Molecular Simulation on Mechanical Behaviors of Polydimethylsiloxane (PDMS)
Chaoyue Ji, Zhiwen Chen, and Sheng Liu – The Institute of Technological Sciences, Wuhan University; Chenyang Wang – School of Mechanical Science & Engineering, Huazhong University; Li Liu – School of Materials Science and Engineering, Wuhan University

Non-Linear Mechanical Properties of Polydimethylsiloxane (PDMS) for Flexible Electronics
Chenyang Wang – Huazhong University of Science and Technology; Chaoyue Ji, Wenli Lu, Zhiwen Chen, Sheng Liu, and Li Liu – Wuhan University

Screen-Printed Inductive Silver Ink Strain Sensor on Stretchable TPU Substrate
Connor Smith, Kartik Sondhi, Beatriz Jimenez, Z. Hugh Fan, Toshikazu Nishida, and David Arnold – University of Florida

Thermal Analysis of a Light Emitting Diode (LED) Package Manufactured Using POL-kW Packaging Technology
Anisha Walwaikar, Krishnaswami Srihari, and Daryl Santos – Binghamton University; Christopher Kapusta – GE Global Research; Kaustubh Nagarkar – GE Ventures

2020 TECHNOLOGY CORNER EXHIBITS

The 2020 ECTC Technology Corner will host over 100 organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of our technical program, the Technology Corner provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. Over 1,500 conference attendees are expected for 2020. With scheduled refreshment breaks and social events that take place in the Technology Corner hall, exhibitors and attendees enjoy continual interactions. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, May 27, 2020, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, May 28, 2020. Exhibit booth availability is extremely limited for 2020. The 2020 Exhibit Application, 2019 exhibitor list, and the 2020 exhibit space layout can be found at www.ectc.net and clicking the 'Exhibits' link. For additional information or questions, please contact Alan Huffman, ECTC Exhibits Chair at +1-919-248-9216 or email alan.huffman@micross.com or ectc.exhibits@gmail.com.

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1) Contact The Walt Disney World Swan and Dolphin Resort at +1-800-227-1500. Reference the ECTC Conference to receive the conference rate of $199/night. In addition, please request your room be reserved in the Walt Disney World Dolphin Resort, as the Swan and Dolphin are two separate buildings.

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or …

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	Speaker or Chair One-Day Registration	$430	$430
Student	Attendee or Speaker (full conference)	$315	$315
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CONFERENCE OVERVIEW

May 26, 2020

Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.

1. Achieving High Reliability of Lead-Free Solder Joints -- Materials Considerations
2. Introduction to Fan-Out Wafer Level Packaging
3. Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging
4. Post -Moore's Law and Quantum Electronics
5. Nano Materials and Polymer Composites for Electronic Packaging
6. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers
7. Eliminating Package Failure Mechanisms for Improved Reliability
8. Characterization of Advanced EMCs for FO-WLP, Heterogeneous Integration, and Automotive Electronics
9. Reliable Integrated Thermal Packaging for Power Electronics

Afternoon Professional Development Courses
1:15 p.m. - 5:15 p.m.

10. Flip Chip Technologies
11. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals
12. Additive Flexible Hybrid Electronics – Manufacturing and Reliability
13. Fan-Out Wafer/Panel Level Packaging and 3D IC Heterogeneous Integrations
14. Polymers in Wafer Level Packaging
15. Reliability Mechanics and Modeling for IC Packaging
16. Power Electronics for Automotive Applications
17. From Wafer to Panel Level Packaging
18. Thermal Management of Electronics

ECTC Special Session
9:30 a.m. - 11:30 a.m.
"Bridge to Quantum Computing?"

Photonics Special Session
2:00 p.m. - 4:30 p.m.
"Cutting-Edge Technology on Integrated Photonics and Packaging"

ECTC Panel Session
7:45 p.m. - 9:15 p.m.
"Future (Visions) of Electronics Packaging"

May 27, 2020

Technical Sessions
8:00 a.m. - 11:40 a.m.

1 Fan-Out Technologies for System Integration
2 Innovation on WLCSP and 3D Packaging
3 Antenna-in-Package for 5G and Radar Systems
4 Advanced Photonic Integration Packaging
5 Advanced Bonding Methods and Processing
6 Interconnect Modeling

Interactive Presentation Sessions 37 & 38
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

ECTC Luncheon Keynote
Innovative Heterogeneous Integration Technologies Inititate a New Semicondutor Era

Technical Sessions
1:30 p.m. - 5:10 p.m.

7 Advances in Packaging at the Wafer/Panel Level
8 High-Density RDL for Advanced Interconnects
9 Power Delivery and Conversion
10 MEMS and Sensors
11 Reliability of Next-Generation Interconnects
12 Modeling for Heterogeneous Integration: From Wafer to Board Level

ECTC/ITHERM Diversity and Career Growth Panel and Reception
6:30 p.m. - 7:30 p.m.
"Diversity and Inclusion Drives Innovation and Productivity"

ECTC Plenary Session
7:30 p.m. - 9:00 p.m.
"3DIC: Past, Present and Future"

May 28, 2020

Technical Sessions
8:00 a.m. - 11:40 a.m.

13 2.5D and 3D Technology Enabling High Performance Computing
14 Materials for High-Speed/ Frequency and 5G
15 Flexible and Printed Electronics
16 Sintering and Interconnect Reliability
17 Automotive and Harsh Environment Reliability
18 Emerging Flexible Hybrid Electronics

Interactive Presentation Sessions 39 & 40
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.

19 Embedded and Heterogeneous Integration
20 Materials and Processes for FOWLP and PLP
21 High Speed in Signal Integrity
22 Advanced Biosensors and Bioelectronics
23 Advanced Dicing and Laser-Assisted Bonding
24 Material and Interface Modeling

IEEE EPS Seminar
8:00 p.m. - 9:30 p.m.
"Future Semiconductor Packages for Artificial Intelligence Hardware"

May 29, 2020

Technical Sessions
8:00 a.m. - 11:40 a.m.

25 High Density Fan-Out Technology
26 Breakthroughs in TSV and TGV Technologies
27 WLP and Advanced Technology Reliability
28 Enhanced Manufacturing and Process Integration
29 Advances in Bonding Materials and Processes
30 RF and Power Components and Modules

Student Interactive Presentations Session 41
8:30 a.m. - 10:30 a.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.

31 Automotive and Power Electronics Packaging
32 Stacking and Bonding Technologies
33 Advances in Reliability Assessment
34 Emerging Materials and Processing
35 Additive Manufacturing and Innovative Materials for Packaging
36 Multiphysics and AI-Enhanced Modeling Approaches

Session Summary by Interest Area

Fan-Out Topics
S1, S20

Packaging Technologies
S1, S7, S10, S13, S19, S25, S31

Applied Reliability
S11, S17, S27, S33

Assembly & Manufacturing Technology
S5, S7, S15, S23, S28

Emerging Technologies
S18, S22, S35

High-Speed, Wireless & Components
S3 S9, S21, S30

Interconnections
S8, S16, S26, S32

Materials & Processing
S2, S14, S20, S29, S34

Thermal/Mechanical Simulation & Characterization
S6, S12, S24, S36

Photonics
S4

Interactive Presentations
S37, S38, S39, S40, S41

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