Don’t miss out on electronic packaging’s premier conference!

ECTC
The 2019 IEEE 69th Electronic Components and Technology Conference
May 28 - May 31, 2019
The Cosmopolitan of Las Vegas
Las Vegas, Nevada, USA

For more information, visit: www.ectc.net

Program Supported by:

Sponsored by:
Greetings:

As Mayor, I am very pleased to welcome you to America’s most dynamic, entertaining, and intriguing city! You could not have chosen a better locale. I am convinced that once you get a taste of what the city has to offer, you will never want to leave. Las Vegas continues to capture the world’s imagination as the city where anything is possible. With world-class hotels, award-winning restaurants, luxurious spas, fantastic shopping, the finest golf courses, and spectacular entertainment, Las Vegas remains one of the most electrifying destinations in the world.

At its heart Las Vegas is all about making sure residents and visitors are well taken care of, treated courteously, and shown a great time. Beyond the neon of the fabulous Strip and the Fremont Street Experience, there is another Las Vegas—one in which we are building a world-class city featuring the best in arts, culture, sporting opportunities, and quality medical care. The Smith Center for the Performing Arts has set a high standard for art and culture in our city, and I encourage everyone to take in a concert or Broadway show at this magnificent venue. Regardless of your age, a must-visit spot is the children’s interactive Discover Museum adjacent to the Smith Center. Buzzing with excitement is the Fremont East Entertainment District, a place with an energy and enthusiasm through its taverns, restaurants, and music venues.

The city also offers beautiful weather and outdoor activities, from top class golfing to opportunities for world-class hiking and rock climbing at the Red Rock Canyon National Conservation Area, to skiing at Mount Charleston, and a visit to the awe-inspiring Hoover Dam at the Lake Mead National Recreation Area. If history is more your speed, you are in luck because the National Museum of Organized Crime and Law Enforcement and the Neon Museum are two of the most interesting and unique experiences in the country.

I want to thank you for choosing Las Vegas and look forward to seeing you around town. I know you will have a fabulous time enjoying our great city and everything it has to offer. Now what are you waiting for? The party has already started! Welcome.

Sincerely,

Carolyn G. Goodman
Mayor, City of Las Vegas
On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the 69th Electronic Components and Technology Conference (ECTC), which will be held at The Cosmopolitan of Las Vegas in Las Vegas, Nevada from May 28-31, 2019. This premier international conference brings together key stakeholders of the global microelectronics packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, materials suppliers, research institutions and universities all under one roof.

For the 69th ECTC, the ECTC Program Committee has selected over 350 papers which will be presented in 36 oral sessions and five interactive presentation sessions including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as fan-out packaging, wafer-level packaging, flip-chip packaging, 3D/TSV technologies, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, materials and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work.

Authors from over twenty countries are expected to present their work at the 69th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature six special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, May 28 at 9 a.m., W. Hong Yeo and Mikel Miller will chair a special session covering “Transient Electronics: A Green Revolution for Packaging.” On the same day at 2 p.m., Rena Huang and Soon Jang will chair a session focused on “Photonics on the Cutting-Edge of Technology Evolution.” Tuesday evening will also include the ECTC Panel Session “Future (Visions) of Electronic Packaging” at 7:45 p.m. chaired by IEEE EPS President Avi Bar-Cohen and Karlheinz Bock, where young researchers will share their visions of future packaging technologies and participate in discussions with experts in the field.

This conference will also feature a Women’s Panel and Reception jointly organized by ECTC and ITherm on Wednesday, May 29 at 6:30 p.m. This year, panelists from around the globe will share their perspectives on efforts to enhance the participation of women in engineering, and the panel will be chaired by Kristina Young-Fisher and Cristina Amon. On the same day at 7:30 p.m., Tanja Braun will chair the ECTC Plenary Session titled “Sensors and Packaging for Autonomous Driving.” In this plenary session, experts will address the challenges and demands for sensors and packages for autonomous driving along the value chain. On Thursday, May 30 at 8 p.m., the IEEE EPS Seminar titled “Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements” will be moderated by Yasumitsu Orii and Shigenori Aoki from the High-Density Substrates & Boards Technical Committee of the IEEE EPS Society.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the Technology Corner exhibits. Co-located with the IEEE IThERM Conference this year, the 69th ECTC will offer eighteen PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 28 and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons and nightly receptions.

Whether you are an engineer, a manager, a student or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We invite you to join us during the 69th ECTC to be a part of all the 69th ECTC and be a part of all the exciting technical and professional opportunities. We also take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 69th ECTC a success. Once again, thank you for being a part of the 69th ECTC.

Mark Poliks
69th ECTC General Chair
Binghamton University
mpoliks@binghamton.edu

Nancy Stoffel
69th ECTC Program Chair
General Electric Research Center
stoffel@ge.com
On behalf of the IEEE Electronics Packaging Society, it is my great pleasure and privilege to welcome you to the 69th Electronic Components and Technology Conference – the largest Packaging Conference in the world.

Building on the long history of ECTC and its predecessor Conferences, begun 69 years ago, this conference, and the electronic packaging community we serve, continue to grow in size and in impact. We expect attendance at this year’s ECTC, and ITherm - the co-located EPS Thermal Phenomena Conference - to well exceed 2000 packaging professionals. Including the forthcoming EPS Asia-Pacific Flagship Conference, EPTC, in December, and the other sponsored and co-sponsored conferences and workshops, EPS is on track to serve more than 5000 Conference attendees world-wide in 2019.

I would like to take this opportunity to thank all of you for attending ECTC and our volunteers on the ECTC Executive and Program Committees, members of the Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their commitment and dedication to making the 69th ECTC and its associated activities the premier annual event of the electronic packaging community. We are fortunate to have so many of you actively engaged in this conference, and we are indebted to the large, skilled and enthusiastic team that keeps finding new ways to serve the electronic packaging community.

It is very rewarding to see the impact of these technical events and networking activities on the EPS Society, our industry, and our members. My deepest thanks and appreciation to all of you for the opportunity to work with you to develop the breakthroughs in packaging technology that will continue to drive innovation in the microelectronic industry!

Avram Bar-Cohen
EPS President 2018-2019

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ECTC Luncheon Keynote

**Soft Electronic and Microfluidic Systems for the Skin**

*Wednesday, May 29, 2019 • Belmont 3, 4th Floor*

**John A. Rogers – Director of Center for Bio-Integrated Electronics, Northwestern University**

Recent advances in materials, mechanics, and manufacturing establish the foundations for high-performance classes of electronics and other microsystems technologies that have physical properties precisely matched to the human epidermis. The resulting devices can integrate with the skin in a physically imperceptible fashion to provide continuous, clinical-quality information on physiological status. This talk will summarize the key ideas and presents specific examples in wireless monitoring for neonatal intensive care, and in capture, storage, and biomarker analysis of sweat.

ECTC Mobile App

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The ECTC app is available for iOS and Android devices through the QuickMobile Events app available in the respective app stores. After downloading the app, search for “ECTC19” as the event ID, and follow the instructions to set up your account.

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*A path changing direction for temporary bonding*

![Diagram of bonding process](image)

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Registration
ECTC registration will be open at the ECTC Registration Desk located in The Cosmopolitan Las Vegas in Las Vegas, NV, 4th floor in the Belmont Commons Foyer.

Monday, May 27, 2019 • 3:00 p.m. – 5:00 p.m.
Tuesday, May 28, 2019 • 6:45 a.m. – 8:15 a.m.*
(AM PD Courses & Special Session Only)*
Tuesday, May 28, 2019 • 8:15 a.m. – 5:00 p.m.
(All conference attendees)
Wednesday, May 29, 2019 • 6:45 a.m. – 4:00 p.m.
Thursday, May 30, 2019 • 7:30 a.m. – 4:00 p.m.
Friday, May 31, 2019 • 7:30 a.m. – 12:00 Noon

On Tuesday, May 28th light morning refreshments will be provided from 6:45 a.m. – 7:15 a.m. Come register and grab a bite to eat before the PDCs start!

*The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees
Door Registration includes a Proceedings on USB drive
IEEE Member JOINT Registration (full ECTC + Itherm conference) ……. $1160
IEEE Member Full Registration ………………………………………….. $860
IEEE Member Speaker / Session Chair ……………………………… $765
IEEE Member One Day ………………………………………………… $565
IEEE Member Speaker One Day ……………………………………… $430
Exhibit Booth Attendant ……………………………………………… $0
Non-Member JOINT Registration (full ECTC + Itherm conference) … $1375
Non-Member Full Registration ………………………………………….. $1055
Non-Member Speaker / Session Chair ……………………………… $765
Non-Member One Day ………………………………………………… $565
Non-Member Speaker One Day ……………………………………… $430
Exhibit Booth Attendant ……………………………………………… $0
Student…………………………………………………………………… $315
Student Speaker………………………………………………………… $315
Exhibits Only……………………………………………………………… $25

Tuesday Professional Development Courses
IEEE Members and Non-Members
Tuesday AM or PM Course with luncheon ……………………. $500
Tuesday All-Day Courses with luncheon ……………………… $710
Tuesday Student All-Day Courses with luncheon ……………… $130
Extra Luncheon Tickets for Each Day …………………………… $65
Extra Proceedings with Registration ……………………………… $100

Professional Development Course Instructors Breakfast
PDC Instructors and Proctors are required to attend a briefing breakfast.
7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Belmont 3, 4th floor)

Session Chairs and Speakers Breakfast
Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows and Microsoft Office.

7:00 a.m. Wednesday thru Friday
(Room Location: Belmont 3, 4th floor, Wednesday – Thursday)
(Room Location: Belmont 5, 4th floor, Friday)

Speaker Prep Room
Speakers should prepare and review their digital presentations within the allotted times below:
7:00 a.m. – 5:00 p.m., Tuesday – Friday
(Room Location: Yaletown 2, 4th floor)
(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)
### MISCELLANEOUS INFORMATION

**Hotel Concierge**
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one.

**Press Room**
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

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### LUNCHEONS

**Tuesday, May 28, 2019**
**12PM**
Belmont 3, 4th floor
Our Tuesday lunch is provided for anyone attending a Professional Development Course, whether you attend just a single course or both a morning and afternoon course. PDC Proctors, session speakers, committee members or anyone else with a Tuesday lunch ticket is more than welcome to join! Possession of a lunch ticket is required for admission.

**Wednesday, May 29, 2019**
**12PM**
Belmont 3, 4th floor
This year’s Wednesday luncheon will feature Dr. John A. Rogers, Director for the Center for Bio-Integrated Electronics at Northwestern University. We will also be celebrating award winners for Best and Outstanding Papers of 2018! Don’t miss it! Possession of a lunch ticket is required for admission.

**Thursday, May 30, 2019**
**12PM**
Belmont 3, 4th floor
The IEEE Electronics Packaging Society will host our Thursday luncheon for conference attendees. The EPS awards will be presented. Possession of a lunch ticket is required for admission.

**Friday, May 31, 2019**
**12PM**
Belmont 3, 4th floor
Do NOT MISS Friday’s luncheon! It’s our annual ECTC Program Chair luncheon where lots of high dollar, valuable, and useful prizes will be raffled off! Each year the prizes seem to get better and better. Remember you must be present to win. Possession of a lunch ticket is required for admission.

Please note that due to increased attendance ECTC will have an overflow lunch room on Wednesday & Thursday located in Castellana 2, 3rd floor.
Please make sure to be in line for lunch early if your preference is the main lunch room.

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**Heterogeneous Integration Roadmap Workshop**

*Tuesday, May 28, 2019 • 8:00 a.m. - 5:00 p.m.*

**Moderators:** William Chen – ASE, Bill Bottoms – 3MT Solutions and Ravi Mahajan – Intel

Condesa 3, 2nd Floor

Our industry has reinvented itself through multiple disruptive changes in technologies, products, and markets. Our industry continues to change with the rapid migration of logic, memory, and applications to the cloud, the evolution of the Internet of Things (IoT) to the Internet of Everything (IoE), the proliferation of smart devices everywhere, the rise of 5G, the increasing presence of microelectronics in wearables & health application, and in autonomous automotive, and the rapid advancement of AI.

The pace of innovation is simultaneously increasing to meet these challenges. The Heterogeneous Integration Roadmap will address the future directions of heterogeneous integration technologies and applications serving the future markets and applications.

The Heterogeneous Integration Roadmap Technical Working Groups are celebrating the completion of the 1st edition of the Heterogeneous Integration Roadmap. The Technical Working Groups will be reporting out their work products and on their plan for the next edition.

We like to invite all the ECTC & ITherm participants to attend this important working session for our profession and for our industry. Registration is not required.

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Sekisui Semiconductor Package & Assembly Materials

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2099 Gateway Place, Suite 310
San Jose, CA, 95110
inquiry@sekiisuproduxts.com
2019 SPECIAL SESSION
Transient Electronics: A Green Revolution for Packaging?
Tuesday, May 28, 2019
9:00 a.m. – 11:30 a.m.
Castellana 2, 3rd Floor

Chairs: W. Hong Yeo - Georgia Institute of Technology and Mikel Miller - EMD Performance Materials

Speakers:
1. John Rogers – Northwestern University
2. Matthew MacEwan – Washington University
3. Paul Kohl – Georgia Institute of Technology
4. Mihai Irimia-Vladiu – Joanneum Research Forschungsgesellschaft mbH

2019 PHOTONICS SPECIAL SESSION
Photonics on the Cutting-Edge of Technology Evolution
Tuesday, May 28, 2019
2:00 p.m. – 4:30 p.m.
Castellana 2, 3rd Floor

Chairs: Rena Huang - Rensselaer Polytechnic Institute and Soon Jang - ficonTEC (USA) Corporation

Speakers:
1. Bert Offrein – IBM Research GmbH-Zurich
2. Mark Thompson – PsiQuantum
3. Roy Meade – Ayar Labs

2019 ECTC PANEL SESSION
Future (Visions) of Electronic Packaging
Tuesday, May 28, 2019
7:45 p.m. – 9:15 p.m.
Mont-Royal 1 & 2, 4th Floor

Chairs: Avi Bar-Cohen, EPS President - Raytheon and Karheinz Bock - TU Dresden

Speakers:
1. Martin Schubert – TU Dresden
2. Shreya Dwarkanath – Georgia Institute of Technology
3. Chandrasekharan Nair – Georgia Institute of Technology
4. Siddharth Ravichandran – Georgia Institute of Technology
## Professional Development Courses

### Morning Courses 8:00 a.m. – 12:00 Noon

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<td>Achieving High Reliability of Lead-Free Solder Joints – Materials Considerations</td>
<td>Ning-Cheng Lee – Indium Corporation</td>
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<td>Nolita 1</td>
<td>2. Introduction to Fan-Out Wafer-Level Packaging</td>
<td>Beth Keser – Intel Corporation</td>
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<td>5. Polymers and Nanocomposites for Electronic and Photonic Packaging</td>
<td>C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation</td>
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<td>Mont-Royal 1</td>
<td>6. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers</td>
<td>Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM</td>
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<td>2. Introduction to Fan-Out Wafer-Level Packaging</td>
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<td>9. Integrated Thermal Packaging and Reliability of Power Electronics</td>
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### Afternoon Courses 1:30 p.m. – 5:30 p.m.

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### Refreshment Breaks
- 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
- Mont-Royal Commons, Belmont Commons 4 & 8, & Castellana 1
AWARDS FROM THE 68TH ECTC

BEST OF CONFERENCE PAPERS
The Electronic Components and Technology Conference is proud to announce the “Best of Conference” papers selected from the 68th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper
Session 27, Paper 5
Material Characterization of Advanced Cement-Based Encapsulation Systems for Efficient Power Electronics with Increased Power Density

Best Interactive Presentation Paper
Session 39, Paper 6
Correlated Model For Wafer Warpage Prediction of Arbitrarily Patterned Films
Gregory T. Ostrawicki, Siva Gumum and Amit Nangia – Texas Instruments, Inc.

INTEL BEST STUDENT PAPER
The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 68th ECTC.

Session 23, Paper 3
Miniaturized High-Performance Filters for 5G Small-Cell Applications

OUTSTANDING PAPERS
The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 68th ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper
Session 7, Paper 1
Laser Sintering of Dip-Based All-Copper Interconnects
Luca Del Carro, Thomas Brunschwiler – IBM Research, Zurich; Martin Kossatz, Lucas Schnackenberg, Matthias Fettke – PacTech – Packaging Technologies GmbH; and Ian Clark – Intrinsic Materials Ltd.

Outstanding Interactive Presentation
Session 37, Paper 20
Non-destructive Assessment of the Porosity in Silver (Ag) Sinter Joints using Acoustic Waves
Sebastian Brand, Bianca Böttge, Michael Kägel, Falk Naumann, Frank Altmann – Fraunhofer Institute for Microstructure of Materials and Systems (IMWS); Junian Zijl, Sebastiaan Kersjes – BEST Netherlands, B.V. and Thomas Behrens - Infineon Technologies AG

TEXAS INSTRUMENTS OUTSTANDING STUDENT INTERACTIVE PRESENTATION
The winning student receives a personalized plaque and a check for US $1,000. The following paper was selected based on the Texas Instruments Outstanding Student Interactive Presentation competition conducted at the 68th ECTC.

Session 39, Paper 10
Copper Transparent Antennas on Flexible Glass by Subtractive and Semi-Additive Fabrication for Automotive Applications
Jack P. Lombardi III, Robert E. Makay, Mark D. Poliks - Binghamton University; James H. Schaffner, Hyok Jae Song - HRL Laboratories, LLC, Ming-Huang Huang, Scott C. Pollard - Corning, Inc.; and Timothy Talty – General Motors

CORNING LEADERSHIP IN GLASS AWARD
The winning authors receive an engraved Steuben crystal Euclidean award and each receive a gift card for US $100. The following paper was selected from submissions to the 68th ECTC.

Session 38, Paper 18
A Novel Inorganic Substrate by Three Dimensionally Stacked Glass Core Technology
Toshiaki Iwai, Taiji Sakai, Daisuke Mizutani, Seiki Sakuyama - Fujitsu Laboratories Ltd.; Kenji Iida, Takayuki Inaba, Hidehiko Fujisaki, and Yoshinori Miyazawa - Fujitsu Interconnect Technologies Ltd.

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 28, 2019
8:00 a.m. – 5:00 p.m.
EPS Heterogeneous Integration Roadmap Workshop
Condesa 3, 2nd floor
9:00 a.m. – 10:30 p.m.
ECTC OPTO Committee Meeting
Jardins Boardroom, 2nd floor
9:00 a.m. – 10:30 p.m.
ECTC Interconnect Committee Meeting
Bellavista Boardroom, 2nd floor
Wednesday, May 29, 2019
7:00 a.m. – 8:00 a.m.
EPS Materials & Processes TC
Jardins Boardroom, 2nd floor
7:00 a.m. – 8:00 a.m.
EPS Power & Energy TC
Bellavista Boardroom, 2nd floor
4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs Meeting
Bellavista Boardroom, 2nd floor
6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair’s Suite (by invitation only)
Thursday, May 30, 2019
7:00 a.m. – 8:00 a.m.
EPS Region 8 Meeting
Condesa 5, 2nd floor
7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Bellavista Boardroom, 2nd floor
7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
Jardins Boardroom, 2nd floor
7:00 a.m. – 8:00 a.m.
EPS Electrical Design, Modeling & Simulation TC
Belmont 4, 4th floor
7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Condesa 6, 2nd floor
5:30 p.m. – 6:30 p.m.
ECTC 2020 Program Committee Meeting
Nolita 1, 4th floor
8:00 p.m.
69th ECTC Governing/Executive Committee Reception
General Chair’s Suite
Friday, May 31, 2019
7:00 a.m. – 8:00 a.m.
EPS Emerging Technologies TC
Jardins Boardroom, 2nd floor
7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
Condesa 5, 2nd floor
7:00 a.m. – 8:30 a.m.
EPS Transaction Editors TC / AE’s Meeting
Condesa 2, 2nd floor
1:30 p.m. – 4:30 p.m.
ECTC Executive Committee Meeting
Jardins Boardroom, 2nd floor
### Conference At A Glance

<table>
<thead>
<tr>
<th>Registration</th>
<th>Monday 3:00 p.m. - 5:00 p.m.</th>
<th>Tuesday 6:45 a.m. - 5:00 p.m.</th>
<th>Wednesday 6:45 a.m. - 4:00 p.m.</th>
<th>Thursday 7:30 a.m. - 4:00 p.m.</th>
<th>Friday 7:30 a.m. - 12:00 p.m.</th>
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<tbody>
<tr>
<td>Technology Corner</td>
<td>Exhibits</td>
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<td>Belmore Commons Foyer</td>
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<tr>
<td>Wednesday 9:00 a.m. - 12:00 p.m.</td>
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<td>1:30 p.m. - 6:30 p.m.</td>
<td>Reception - 5:30 p.m. - 6:30 p.m.</td>
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<tr>
<td>Speaker Preparation Room</td>
<td>Tuesday - Friday 7:00 a.m. - 5:00 p.m.</td>
<td>Yaletown 2</td>
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<tr>
<td>Tuesday</td>
<td>PDC Instructors and Proctors</td>
<td>Briefing &amp; Breakfast 7:00 a.m. - 7:45 a.m.</td>
<td>Belmont 3, 4th Floor</td>
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<tr>
<td>Professional Development Courses (PDCs)</td>
<td>8:00 a.m. - Noon</td>
<td>1:30 p.m. - 5:30 p.m.</td>
<td>See page 9 for locations</td>
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<tr>
<td>EPS Heterogeneous Integration Roadmap Workshop</td>
<td>8:00 a.m. - 5:00 p.m.</td>
<td>Condesa 3, 2nd Floor</td>
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<tr>
<td>Special Sessions:</td>
<td>ECTC Special Session 9:00 a.m. - 11:30 a.m.</td>
<td>Castellana 2, 3rd Floor</td>
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<tr>
<td>Photonics Special Session</td>
<td>2:00 p.m. - 4:30 p.m.</td>
<td>Castellana 2, 3rd Floor</td>
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<tr>
<td>Refreshment Breaks</td>
<td>10:00 a.m. - 10:20 a.m.</td>
<td>3:00 p.m. - 3:20 p.m.</td>
<td>Mont-Royal Commons, Belmont Commons 4 &amp; 8, &amp; Castellana</td>
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<tr>
<td>Lunch for PDCs</td>
<td>12 p.m. Noon</td>
<td>Belmont 3, 4th Floor</td>
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<tr>
<td>Technology Corner Set Up</td>
<td>1:00 p.m. - 5:00 p.m.</td>
<td>Belmont 1 &amp; 5, 4th Floor</td>
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<tr>
<td>ECTC Student Reception</td>
<td>5:00 p.m. - 6:00 p.m.</td>
<td>Mont-Royal Commons, 4th Floor</td>
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<tr>
<td>General Chair’s Speakers Reception</td>
<td>6:00 p.m. - 7:00 p.m.</td>
<td>OUTSIDE at the North Blvd. Pool (Rain Backup: Belmont 3, 4th Floor)</td>
<td>By invitation only</td>
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<tr>
<td>Young Professionals Networking Panel</td>
<td>7:00 p.m. - 7:45 p.m.</td>
<td>Nolita 1, 4th Floor</td>
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<tr>
<td>ECTC Panel Session</td>
<td>7:45 p.m. - 9:15 p.m.</td>
<td>Mont-Royal 1 &amp; 2, 4th Floor</td>
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<tr>
<td>Wednesday</td>
<td>Speakers Breakfast 7:00 a.m. - 7:45 a.m.</td>
<td>Belmont 3, 4th Floor</td>
<td>Sessions 1 - 12 8:00 a.m. - 11:40 a.m.</td>
<td>1:30 p.m. - 5:30 p.m.</td>
<td>See pages 12 - 15 for specifics</td>
</tr>
<tr>
<td>Interactive Presentations</td>
<td>Sessions 37 - 38</td>
<td>9:00 a.m. - 11:00 a.m. or 2:00 p.m. - 4:00 p.m.</td>
<td>see pages 24 - 25 for specifics</td>
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<tr>
<td>Refreshment Breaks</td>
<td>9:15 a.m. - 10:00 a.m.</td>
<td>2:45 p.m. - 3:30 p.m.</td>
<td>Belmont 1 &amp; 5, 4th Floor</td>
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<tr>
<td>Lunch</td>
<td>12 p.m. - 1:15 p.m.</td>
<td>Belmont 3, 4th Floor</td>
<td>Overflow: Castellana, 3rd Floor</td>
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<tr>
<td>ECTC/IHERM Panel &amp; Reception</td>
<td>6:30 p.m. - 7:30 p.m.</td>
<td>Nolita 1, 4th Floor</td>
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<tr>
<td>ECTC Plenary Session</td>
<td>7:30 p.m. - 9:00 p.m.</td>
<td>Mont-Royal 1 &amp; 2, 4th Floor</td>
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<tr>
<td>Thursday</td>
<td>Speakers Breakfast 7:00 a.m. - 7:45 a.m.</td>
<td>Belmont 3, 4th Floor</td>
<td>Sessions 13 - 24 8:00 a.m. - 11:40 a.m.</td>
<td>1:30 p.m. - 5:30 p.m.</td>
<td>See pages 16 - 19 for specifics</td>
</tr>
<tr>
<td>Interactive Presentations</td>
<td>Sessions 39 - 40</td>
<td>9:00 a.m. - 11:00 a.m. or 2:00 p.m. - 4:00 p.m.</td>
<td>see pages 25 - 26 for specifics</td>
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<tr>
<td>Refreshment Breaks</td>
<td>9:15 a.m. - 10:00 a.m.</td>
<td>2:45 p.m. - 3:30 p.m.</td>
<td>Belmont 1 &amp; 5, 4th Floor</td>
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<tr>
<td>Lunch</td>
<td>12 p.m. - 1:15 p.m.</td>
<td>Belmont 3, 4th Floor</td>
<td>Overflow: Castellana, 3rd Floor</td>
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<tr>
<td>69th ECTC Gala Reception</td>
<td>6:30 p.m. - 7:30 p.m.</td>
<td>Mont-Royal 1 &amp; 2, 4th Floor</td>
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<tr>
<td>Friday</td>
<td>Speakers Breakfast 7:00 a.m. - 7:45 a.m.</td>
<td>Belmont 3, 4th Floor</td>
<td>Sessions 25 - 36 8:00 a.m. - 11:40 a.m.</td>
<td>1:30 p.m. - 5:30 p.m.</td>
<td>See pages 20 - 23 for specifics</td>
</tr>
<tr>
<td>Interactive Presentations</td>
<td>Session 41</td>
<td>8:30 a.m. - 10:30 a.m.</td>
<td>see pages 26 - 27 for specifics</td>
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<td>Refreshment Breaks</td>
<td>9:15 a.m. - 10:00 a.m.</td>
<td>2:45 p.m. - 3:30 p.m.</td>
<td>Mont-Royal Commons</td>
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<tr>
<td>Lunch</td>
<td>12 p.m. - 1:15 p.m.</td>
<td>Belmont 3, 4th Floor</td>
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</table>
Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

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<tr>
<th>Session 1: Wafer-Level Fan-Out Process Integration</th>
<th>Session 2: Next-Generation Wirebonding and Die Attach</th>
<th>Session 3: RDL and Additive Manufacturing</th>
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<tbody>
<tr>
<td>Committee: Packaging Technologies</td>
<td>Committee: Interconnections</td>
<td>Committee: Packaging Technologies in conjunction with Emerging Technologies</td>
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<tr>
<td>Mont-Royal 1</td>
<td>Mont-Royal 2</td>
<td>Nolita 1</td>
</tr>
</tbody>
</table>

Session Co-Chairs:
- Bora Baloglu
- Amkor Technology
- Beth Rosen
- Intel Corporation

1. 8:00 a.m. - 3D-MiM (Must-in-Must) Technology for Advanced System Integration
   An-Jhih Su, Terry Ku, Chung-Hao Tsai, Kuo-Chung Yee, and Douglas Yu – Taiwan Semiconductor Manufacturing Company Ltd.

2. 8:25 a.m. - Construction on FO-MCM with C4 Bumps Built First Using Chip Last Assembly Technology
   Chih-Hsun Hsu, Wen-Yang Li, Chi-Jen Chen, Yih Jenn Jiang, Jui-Feng Tai, Chang-Fu Lin, and C. Key Chung – Siliconware Precision Industries Co., Ltd.

3. 8:50 a.m. - Feasibility Study of Fan-Out Panel-Level Packaging for Heterogeneous Integration
   Ching-Hsia Ko, Harry Yang, Cunnu Lin, Y.H. Chen – Umnicon Technology Corporation; John Liu, Ming Li, Penny Lo, R. So, Nelson Fan, Eric Kuan, Eric Ng, Y.F. Cheung – ASMT Pacific Technology; Cao Xi – Huawei Technologies Co. Ltd.; Iris Xu, Tony Chen, Zhang Li, Kim Hew, Te-Te Jiang; Chang Advanced Packaging Co. Ltd.; Zhin Lin, Chang, Jieh Yen Pan, Hong Hua Wu, Rozalia Beica and Marc Lin – Dow Chemical Company; Cao Pei Lin, N.C. Lee – Indium Corporation; Ming Taw, Jeffrey Lu, Rolly Lee – Hong Kong University of Science and Technology

4. 10:00 a.m. - Ultra-Thin FO Package-on-Panel Process for Mobile Application
   Hsiang-Tao Hsiao, Soon Wee Ho, Simon Siak Boon Lim, Leong Ching Wai, Ser Choong Chong, Pei Sang Sharon Lim, Yong Han, and Tai Chong Chai – Institute of Microelectronics A*STAR

5. 10:25 a.m. - Development of Wafer-Level Process for the Fabrication of Advanced Capacitive Fingerprint Sensor Using Embedded Silicon Fan-Out (eSiFO®) Technology
   Shuying Mu, Chengqian Wang, and Fengfeng Zheng – Huariant Technology (Kunshan) Electronics Co., Ltd.; Daquan Yu, Xiaobing Yang, Li Ma, Ma Li, and Wensong Liu – Huariant Technology (Xi’an) Electronics Co., Ltd.; Hong Xie – Rchip International; Jambu Yu, Jason Goodlett – Synapsis, USA

6. 10:50 a.m. - Three-Dimensional Integrated Circuit (3D-IC) Package Using Fan-Out Technology
   Jun Kyu Lee, Sang Yong Park, Young Ho Kim, Jae Cheon Lee, Sun Hyuk Lee, Chul Hyo Lee, Yong Tae Kwon, Chang Woo Lee, Jong Heon Kim, Nam Chul Kim, and Yun Hyun Sung – NEFES Corporation

7. 11:15 a.m. - Ultra-High-Density I/O Fan-Out Design Optimization with Signal and Power Integrity
   Chih-Yi Huang, Keng Tian Chang, Hung-Chun Kuo, Ming-Fong Jhong, Tsun-Lung Hsieh, Mi-Chun Hung, and Chen-Chao Wang – Advanced Semiconductor Engineering Inc.

Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5

<table>
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<tr>
<th>Session 4: RDL and Additive Manufacturing</th>
<th>Session 5: 3D Printed Substrates for the Design of Compact RF Systems</th>
<th>Session 6: Fully Additively Manufactured Tunable Active Frequency Selective Surfaces with Integrated On-Package Solar Cells for Smart Packaging Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Packaging Technologies in conjunction with Emerging Technologies</td>
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<tr>
<td>Mont-Royal 1</td>
<td>Mont-Royal 2</td>
<td>Nolita 1</td>
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</table>

Session Co-Chairs:
- Kuldeep Johal
- Atotech
- C. S. Pramachandran

1. 8:00 a.m. - Submicron-Scale Cu RDL Patternning Based on Semi-Additive Process for Heterogeneous Integration
   Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, and Miyuki Akazawa – Dai Nippon Printing Co., Ltd.

2. 8:25 a.m. - Smart Wire Bond Solutions for SIP and Memory Packages
   Basil Milton, Ashish Shah, Hui Xu, Odal Kwon, Gary Schulze, Ivy Qin – Kulicke and Soffa, USA; Nelson Wong – Kulicke and Soffa, Singapore

3. 8:50 a.m. - Preparation and Application of Cu-Ag Composite Solder Preforms for Power Electronic Packaging
   Li Liu, Shengfa Liu, Hu Xiang, and Dongqiao Zhang – Wuhan University of Technology; Zhaoxia Zhou, Stuart Robertson, Canyu Liu, and Changqing Liu – Loughborough University; Zhiwen Chen – Wuhan University

4. 10:00 a.m. - Au-Rich/Sn-Bi Interconnection in Chip-on-Module Package
   Jin Wang, Qian Wang, and Jin Cai – Tsinghua University; Xinnan Hou, Ke Du, and Lixin Zhao – GalaxyCore Inc.

5. 10:25 a.m. - The Properties of Cu Sinter Paste for Pressure Sintering at Low Temperature
   Jung-Lee Jo, Sinichi Yamauchi, Kei Anai, and Takahiko Sakaue – Mitsui Mining & Smelting Co., Ltd.

6. 10:50 a.m. - Low Temperature Sintering of Dendritic Cu Based Pastes for Power Semiconductor Device Interconnection
   Gang Li, Jie Fan, Suyan Liao, Pengli Zhu, Baoan Zhang, Tao Zhao, Rong Sun, and Ching-Fong Wong – Shenzhen Institutes of Advanced Technology

7. 11:15 a.m. - First Demonstration of a Low Cost/Customizable Chip Level 3D Printed Microjet Hotspot-Targeted Cooler for High Power Applications

8. 11:40 a.m. - New Development of Direct Bonding to Aluminum and Nickel Surfaces by Silver Sintering in Air Atmosphere
   Ly My Chew and Wolfgang Schmitt – Heraeus Deutschland GmbH & Co. KG; Tamira Stegmann, Erika Schwenk, and Monique Dubis – Hochschule Aschaffenburg University of Applied Sciences, Germany

9. 11:40 a.m. - Rapid Production of Customized 3D Electronics via Hybrid Additive Manufacturing Technology
   Ji Li, Yang Wang, Peeren Wang, Jiafeng He, Hanka Liu, and Gengzhao Xiang – Southeast University
Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

Session 1: Materials & Processing

Committee: Materials & Processing

1. 8:00 a.m. - Solid-Liquid InterDiffusion (SLID) Bonding, for Thermally Challenging Applications
   Knut E Aasmundtveit, Hoang-Vu Nguyen, and Andreas Larsson – University of South-Eastern Norway; Thi-Thuy Luu – Zimmer & Peacock; Torleif A Tollesen – TEGma

2. 8:25 a.m. - Fluxless Bonding Technique of Diamond to Copper Using Silver-Indium Multilayer Structure
   Roozbeh Sheikh, Yongjun Huo, and Chin C. Lee – University of California, Irvine

3. 8:50 a.m. - Formulation and Processing of Conductive Polysulfide Sealants for Automotive and Aerospace Applications
   Bo Song, Fan Wu, Kyoung-Sik Moon, and C.P. Wong – Georgia Institute of Technology

Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5

4. 10:00 a.m. - Challenges and Approaches to Developing Automotive Grade 1/0 FCBBGA Package Capability
   Rajen Chai, Mike Kelly, Devnaran Balaraman - Amkor Technology, Inc. USA; Hideaki Shoji and Tomio Shirawan – J-Devices Corporation, Japan; KwangSeok Oh and Joon Young Park - Amkor Technology, Korea

5. 10:25 a.m. - Advanced Substrates for GaN-Based HEMTs Devices
   Anthony Cibié, Julie Widel, René Escoffier, Denis Blacher, Kremena Vladimirova, Jean-Philippe Colonna, Paul-Henri Haumesser, Stéphane Bécu, Perceval Coudrain, William Vandendaele, Jerome Bocarrat, Charlotte Gilot, Matthew Charles, Lea Di Ciocco – CEA-LETI

6. 10:50 a.m. - A New Reliable, Corrosion Resistant Gold-Palladium Coated Copper Wire Material
   Sandy Klenge, Robert Klenge, Jan Schichka, Tino Stephan, and Matthias Petzold – Fraunhofer IMWS; Motoki Eto, Nontoshi Araki, and Takashi Yamada – Nippon Micrometal Corporation

7. 11:15 a.m. - Ultrasonic-Accelerated Intermetallic Joint Formation with Composite Solder for High-Temperature Power Device Packaging
   Hongjun Ji, Mingyu Li, Weimei Zhao, and Wenwu Zhang – Harbin Institute of Technology

Session 2: Bonding Manufacturing Technologies

Committee: Assembly & Manufacturing Technology

1. 8:00 a.m. - Comprehensive Study of Copper Nano-Paste for Cu-Cu Bonding
   Ser Choong Chong and Pei Sung Lim Sharon – Institute of Microelectronics A*STAR

2. 8:25 a.m. - Enhanced Performance of Laser-Assisted Compression Bonding (LACB) Compared with Thermal Compression Bonding (TCB) Technology
   Kwang Seong Choi, Yong-Sung Eom, Seok Hwan Moon, Jiho Joo, and Iesseul Jeong – Electronics and Telecommunications Research Institute; Kwangsoo Lee, Jung Hak Kim, and Ju hyeon Kim – LG Chem; Gi Sang Yoon – RITECH; Kwang-Ho Lee and Chul-Hoon Lee – Inha University, Geun-Sik Ahn, and Moo-Sup Shim - Protec

3. 8:50 a.m. - A Study of 3D Packaging Interconnection Performance Affected by Thermal Diffusivity and Pressure Transmission
   Jin-San Jung, Hyeong Gi Lee, Ji-Min Kim, Yong-Jin Park, Ji-Ui Yu, Yong Sung Park, Jun Su Lim, Hyun-Seok Choi, Sung-Il Cho, Dong wook Kim, and Sang-Ho An – Samsung Electronics Company, Ltd.

4. 10:00 a.m. - Vertical Laser Assisted Bonding for Advanced “3.5D” Chip-Packaging
   Andrej Kolbassow, Matthias Fetske and Georg Friedrich – Pac Tech GmbH; Timo Kubisch and Thorsten Teutsch – Pac Tech USA

5. 10:25 a.m. - Optimization of a BEOL Aluminum Deposition Process Enabling Wafer Level AI-Thermo-Compression Bonding
   Sebastian Schulze, Matthias Wiestruck, Mirko Frischke, and Mehmet Kaynak – Innovations for High Performance Microelectronics; Peter Keregesi, Helmut Kurz, and Bernhard Rehban – EV Group, Inc.

6. 10:50 a.m. - Self-Assembly Process for 3D Die-to-Wafer Using Direct Bonding: A Step Forward Toward Process Automatisation
   Amandine Jouve, Loïc Sanchez, Clément Gastan, Maxence Laugier, Emmanuel Rolland, Brigitte Monmayeur, Rémi Franasi, Frank Fourmel, and Severine Chermay – CEA-LETI

7. 11:15 a.m. - A Single Bonding Process for Diverse Organic-Inorganic Integration in IoT Devices
   Tito H. Yang, Yu-Shan Chiu, Hai-Yang Yu, and C. Robert Kao – National Taiwan University; Akitsu Shigetou – National Institute for Materials Science

Session 3: Emerging Flexible Hybrid Electronics

Committee: Emerging Technologies

1. 8:00 a.m. - Stretchable and Printable Medical Dry Electrode Arrays on Textile for Electrophysiological Monitoring
   Yougen Hu, Hui Wang, Yaoxu Xieng, Han Gu, Pengli Zhu, Guangli Li, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ommeaymen Sheikhnejad – ACZT Research GmbH; Ching-Ping Wong – Georgia Institute of Technology

2. 8:25 a.m. - Screen-Printed Flexible Coplanar Waveguide Transmission Lines: Multi-Physics Modeling and Measurement

3. 8:50 a.m. - Inkjet-Printed Filtering Antenna on a Textile for Wearable Applications
   Hisan-Ling Lee and Chun-Hsiang Chang – Chang Gung University; Cheng-Lin Cho – National Tsing Hua University

4. 10:00 a.m. - Mechanical and Electrical Characterization of FOWLP-Based Flexible Hybrid Electronics (FHE) for Biomedical Sensor Application
   Yuki Suzuki, Qian Zhengyang, Aiselle Jacquemond, Noriyuki Takahashi, Hisashi Kno, Tetsu Tanaka, and Takafumi Fukushima – Tohoku University

5. 10:25 a.m. - A Wearable Fingernail Deformation Sensing System and Three-Dimensional Finite Element Model of Fingertip
   Katsuyuki Sakuma, Bucknell Webb, Rajeev Narayanan, Avner Abrami, Jeff Rogers, John Knickerbocker, and Stephen J. Hesig – IBM Thomas J. Watson Research Center

6. 10:50 a.m. - Heterogeneous Integration of a Fan-Out Wafer-Level Packaging Based Foldable Display on Elastomeric Substrate

7. 11:15 a.m. - A Study on the Flexible Chip-on-Fabric (COF) Assembly Using Anisotropic Conductive Films (ACFs) Materials
   Seung-Yoon Jung and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology
Session 7: Advances in Flip Chip Packaging

Committee: Packaging Technologies

Mont-Royal 1

Session Co-Chairs: Mike Gallagher
DuPont Electronics & Imaging
Daniel Baldwin – H.B. Fuller Company

1. 1:30 p.m. - Laser Releasable Temporary Bonding Film with High Thermal Stability
Yong-suk Yang, Kyo-sung Hwang, and Robin Gorrell – 3M

2. 1:55 p.m. - Ultra Large Area SIPs and Integrated mmWave Antenna Array Module for 5G mmWave Outdoor Applications
Pouya Taleb Baydokhti, Siddarth Dalma, Trang Thai, Raanan Sover, Sharon Tal – Intel Corporation

3. 2:20 p.m. - Hybrid Approach for Large Size FC-BGA to Enhance Thermal and Electrical Performance Including Power Delivery
Heeseok Lee, Yunheok Im, Junghwa Kim, Jisoo Hwang, James Jeong, Youngsang Cho, Heejung Choi, and Youngm Shin – Samsung Electronics Company, Ltd.

4. 3:30 p.m. - Package-on-Package Micro-BGA Microstructure Interaction with Bond and Assembly Parameter
Pascale Gagnon and Clément Fortin – IBM Canada Limited; Thomas Weis – IBM Systems

5. 3:55 p.m. - Low-Cost Flip-Chip Stack for Partitioning Processing and Memory
Andy Heing and Fabian Hopsch – Fraunhofer IIS/EAS

6. 4:20 p.m. - High-Density Ultra-Thin Organic Substrate for Advanced Flip-Chip Package

7. 4:45 p.m. - Impact of Low Temperature solder on Electronic package Dynamic Warpage Behavior and Requirement
Wei Keat Loh – Intel Corporation; Ron W. Kulterman – Flex Ltd.; Haley Fu – INEMI; Chih Chung Hsu – CoreTech System (Moldex3D)

Session 8: Material and Process Trends in FOWLP and PLP

Committee: Materials & Processing

Mont-Royal 2

Session Co-Chairs: Tanja Braun
Fraunhofer IZM
Yi Li – Intel Corporation

1. 1:30 p.m. - Laser Releasable Temporary Bonding Film with High Thermal Stability
Yong-suk Yang, Kyo-sung Hwang, and Robin Gorrell – 3M

2. 1:55 p.m. - Design and Demonstration of 1um Low Resistance RDL Using Panel Scale Processes for High-Performance Computing Applications
Bartien DeFrutos, Chandrasekharan Nair, Varun Rajagopal, Jeneta Kannan, Emanuel Surles, Fuhan Lu, Mohanraj Gangam, Katherinormal, and Raul Tumala – 3D Systems Packaging Research Center, Georgia Institute of Technology, Aya Morozawa and Atsushi Kato – Tokyo Ohka Kogyo Co., Ltd.

3. 2:20 p.m. - Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-Up

4. 3:30 p.m. - Development of Novel Low-Temperature Curable Positive-Tone Photosensitive Dielectric Materials with High-Reliability
Yutaro Koyama, Yu Shoji, Keika Hashimoto, Yuki Masuda, Hitoshi Araki, and Masao Tomikawa – Toray Industries, Inc.

5. 3:55 p.m. - Highly Reliable Photosensitive Negative-Tone Polyimide with Low Cure Shrinkage
Daisaku Matsukawa, Hiroko Yotsuyanagi, Shiori Sakaihara, Noryuki Yamazaki, Tetsuya Enomoto, and Takeharu Motobe – Hitachi Chemical DuPont MicroSystems, Ltd., Japan

6. 4:20 p.m. - High Rate and Low Damage Etching Method as Pre Treatment of Seed Layer Sputtering for Fan Out Panel Level Packaging
Tetsushi Fujinaga – ULVAC, Inc.

7. 4:45 p.m. - Investigating and Methods Using Various Release and Thermoplastics Bonding Materials to Reduce Die Shift and Wafer Warpage for eWLB Chip-First Processes
Michelle Fowler and John P. Massey – Brewer Science, Inc.; Tanja Braun, Steve Voges, Robert Gershhardt, and Markus Wohrmann – Fraunhofer Institute IZM

Session 9: Wearables and Thin-Package Reliability and Chip Package Interaction

Committee: Thermal/Mechanical Simulation & Characterization

Nolita 1

Session Co-Chairs: Przemyslaw Greielska
Robert Bosch GmbH
Yong Liu – ON Semiconductor

1. 1:30 p.m. - Effect of Charging Cycle Elevated Temperature Storage and Thermal Cycling on Thin Flexible Batteries in Wearable Applications
Pradeep Lall and Amrit Abrol – Auburn University; Ben Leever – US AFRL; Scott Miller – NextFlex Manufacturing Institute

2. 1:55 p.m. - Bladder Inflation Stretch Test Method for Reliability Characterization of Wearable Electronics
Benjamin G. Stewart and Suresh K. Sitaraman – Georgia Institute of Technology

3. 2:20 p.m. - Study of BEOL Failure Mode in Flip-Chip Packages at High-Temperature Conditions
Wei Wang, Yangyang Sun, Xuefeng Zhang, Lejun Wang, Lily Zhao, Mark Schwarz, Bill Stone, and Ahmer Syed – Qualcomms Technologies, Inc.

4. 3:30 p.m. - A Novel Metal Scheme and Bump Array Design Configuration to Enhance Advanced Si Packages CPI Reliability Performance by Using Finite Element Modeling Technique
Kuo-Chin Chang, Ming-Ji Lui, Steven Hsu, Hao-Chun Liu, Yen-Kun Lai, Sheng-Han Tsai, and Chieh-Hao Hsu – Taiwan Semiconductor Manufacturing Company Ltd.

5. 3:55 p.m. - Assessment of CMP Fill Pattern Effect on the Thermal Performance of Interconnects in Integrated Circuits BEOL
Assaad Helou and Peter Raad – Southern Methodist University; Archana Venugopal – Texas Instruments, Inc.

6. 4:20 p.m. - Three-Dimensional Simulation of the Thermo-Mechanical Interaction Between the Micro-Bump Joints and Cu Protrusion in Cu-Filled TSVs of the High Bandwidth Memory (HBM) Structure
Je-Ying Zhou, Shu-Biao Liang, Cheng Wei, Wen-Kai Le, Chang-Bo Ke, Min-Bo Zhou, Xiao Ma, and Xin-Ping Zhang – South China University of Technology
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<tr>
<td>Session 10: Dicing and Encapsulation Technologies</td>
<td>Nolita 2</td>
<td>1:30 p.m. - A More Than Moore Enabling Wafer Dicing Technology</td>
<td>Jeroen van Borkulo, Roger Evertsen, and Richard van der Stam – ASM Pacific Technologies Inc.</td>
</tr>
<tr>
<td>Session 11: Automotive and Harsh-Environment Reliability</td>
<td>Nolita 3</td>
<td>1:30 p.m. - Effect of Substrate Preheating Treatment on Thermal Reliability and Micro-Structure of Ag Paste Sintering on Au Surface Finish</td>
<td>Zheng Zhang, Chuantong Chen, and Katsuaki Suganuma – Osaka University; Seigo Kurosaka – C. Uyemura &amp; Co., Ltd.</td>
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<tr>
<td>Session 12: Advanced Photonic Devices and Packaging</td>
<td>Yaletown 1</td>
<td>1:30 p.m. - Micro-Fabricated SERF Atomic Magnetometer for Weak Gradient Magnetic Field Detection</td>
<td>Xiang Yue, Jintang Shang, and Chen Ye – Southeast University</td>
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<tr>
<td>Session Co-Chairs: Garry Cunningham</td>
<td>Session Co-Chairs: Sandy Klongel</td>
<td>Session Co-Chairs: Philipp Bernabe</td>
<td>JHU/APL; Fraunhofer Institute for Microstructure of Materials and Systems; CEA Leti</td>
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<td>Texas Instruments</td>
<td>Texas Instruments, Inc.</td>
<td>Texas Instruments, Inc.</td>
<td>Gordon Eigner; Technische Hochschule Ingolstadt</td>
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<tr>
<td>4. 3:30 p.m. - Active Control of NCF Fillet Shape for 3D CoW by Multi Beam Laser Bander</td>
<td>4. 3:30 p.m. - Reliability Investigation of Extremely Large Ratio Fan-Out Wafer-Level Package With Low Ball Density for Ultra-Short-Range Radar</td>
<td>4. 3:30 p.m. - Integration and Characterization of InP Die on Silicon Interconnect Fabric</td>
<td>Keku Ueno, Kaotaka Honda, Tsuboshi Ogawa, and Toshitsa Nonaka – Hitachi Chemical Company, Ltd.</td>
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<tr>
<td>6. 4:20 p.m. - Reliability and Benchmark of 2.5D Non-Molding and Molding Technologies</td>
<td>6. 4:20 p.m. - Prognostication of Accrued Damage and Impending Failure Under Temperature-Vibration in Lead Free Electronics</td>
<td>6. 4:20 p.m. - Vertically Stacked and Directionally Coupled Cavity-Resonator-Integrated Grating Couplers for Integrated-Optic Beam Steering</td>
<td>Yu-Hsiang Hsiou, Che-Ming Hsu, Yi-Sheng Lin, and Chien-Lin Chang Chen – Advanced Semiconductor Corporation; Deschamps, Alexi Bedoin, and David Henry – CEA Leti</td>
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<tr>
<td>Yu-Hsiang Hsiou, Che-Ming Hsu, Yi-Sheng Lin, and Chien-Lin Chang Chen – Advanced Semiconductor Corporation; Group, Inc.</td>
<td>Pradeep Lall, Tony Thomas, and Jeff Suhling – Auburn University; Ken Blecker – US Army ARDEC</td>
<td>Shogo Ura and Junishi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology</td>
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<tr>
<td>7. 4:45 p.m. - Laser-Induced Trench Design, Optimisation and Validation for Restricting Capillary Underfill Spread in Advanced Packaging Configurations</td>
<td>7. 4:45 p.m. - Electrochemical Impedance Spectroscopy (EIS) for Monitoring the Water Load on PCBAs under Cycling Condensing Conditions to Predict Electrochemical Migration Under DC Loads</td>
<td>7. 4:45 p.m. - CIB(Chip-in-Board) Optical Engine Module Using Advanced Fan-Out Package Technology</td>
<td>Gu Li and David Danovitch – Université de Sherbrooke; Eric Turcotte – IBM Canada Ltd.</td>
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<tr>
<td>Gu Li and David Danovitch – Université de Sherbrooke; Eric Turcotte – IBM Canada Ltd.</td>
<td>Simone Lauser and Theresia Richter – Robert Bosch GmbH; Verdingovas Vadimas and Rajan Ambat – Technical University of Denmark</td>
<td>Sang Yong Park, JU Hyun Nam, Ji Ni Shim, Jun Kyu Lee, Yong Tae Kwon, Chang Wook Lee, Jong Heon Kim, and Nam Chul Kim – NEPES Corporation</td>
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<td>Session Co-Chairs:</td>
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<td>Peng Su</td>
<td>Nanyang Technological University</td>
<td>Florida International University</td>
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<td>Juniper Networks</td>
<td>Tom Gregorisch</td>
<td>Amit P. Agrawal</td>
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<td>Subhash L. Shinde</td>
<td>Zeiss Semiconductor Manufacturing Technology</td>
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<td>University of Notre Dame</td>
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### Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

#### Session 13: Technologies Enabling 3D and Heterogeneous Integration
- **Peng Su**
- **Juniper Networks**
- **Subhash L. Shinde**
- **University of Notre Dame**

#### Session 14: Fine-Pitch Solderless Bonding
- **Chuan Song Tan**
- **Nanyang Technological University**
- **Tom Gregorisch**
- **Zeiss Semiconductor Manufacturing Technology**

#### Session 15: High-Bandwidth Packaging
- **Chuan Song Tan**
- **Nanyang Technological University**
- **Tom Gregorisch**
- **Zeiss Semiconductor Manufacturing Technology**

### Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5

#### Session 4: 10:00 a.m. - System on Integrated Chips (SoIC (TM)) for 3D Heterogeneous Integration
- **Ming-Fa Chen**
- **Fang-Cheng Chen**
- **Amit P. Agrawal**
- **Siliconware Precision Industries Co., Ltd.**

#### Session 5: 10:25 a.m. - Die-to-Wafer (D2W) Processing and Reliability for 3D Packaging of Advanced Node Logic
- **Luke England**
- **Daniel Fisher**
- **Kate Rivera**
- **Bill Guthrie**
- **GLOBALFOUNDRIES**
- **Ping-Jui Kuo**
- **Chang-Chi Lee**
- **Che-Ming Hsu**
- **Fan-Yu Min**
- **Kuo-Chang Kang**
- **Chen-Yuan Weng**
- **Taiwan Semiconductor Manufacturing Company Ltd.**

#### Session 6: 10:50 a.m. - Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems
- **Alvin Phommahaxay**
- **Samuel Suhard**
- **Peng Su**
- **Texas Instruments Inc.**

#### Session 7: 11:15 a.m. - Making Sense of the Novel System-on-Package Technology (ICE-SIP) for Mobile and 3D High-End Packages
- **Taejo Hwang**
- **DanKyoung Suk**
- **Junjie Li**
- **Eric Beyer**
- **IMEC**

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**Committee:** Packaging Technologies

**Committee:** Interconnections

**Committee:** High-Speed, Wireless & Components
Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

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<th>Session 16: Advanced Materials for High-Speed Electronics</th>
<th>Session 17: Materials and Design for Reliability of Next-Generation Packages</th>
<th>Session 18: Warpage and Material Performance</th>
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<td>Committee: Thermal/Mechanical Simulation &amp; Characterization</td>
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<tr>
<td>Session Co-Chairs: Yoichi Taira Keio University</td>
<td>Session Co-Chairs: Varugheese Mathew NXP Semiconductors Lakshmi R. Ramanathan Microsoft Corporation</td>
<td>Session Co-Chairs: Pradeep Lall Auburn University Karsten Meier Technische Universität Dresden</td>
</tr>
<tr>
<td>1. 8:00 a.m. - Low-Loss Glass Substrates Formulated With a Variety of Dielectric Characteristics for mm Wave Applications Kazutaka Hayashi, Nobutaka Kidera, and Yochoro Sato – AQC Inc.</td>
<td>1. 8:00 a.m. - Highly (1 1 1)-Oriented Nanotwinned Cu for High Fatigue Resistance in Fan-Out Wafer-Level Packaging Yu-Jin Li, Chih-Han Theng, I-Hsin Tseng, and Chih Chen – National Chiao Tung University; Benson Lin and Chia-Cheng Chang – MediaTek Inc.</td>
<td>1. 8:00 a.m. - Improved Finite Element Modeling of Moisture Diffusion Considering Discontinuity at Material Interfaces in Electronic Packages Lulu Ma and Xuejun Fan – Lamar University; Rahul Joshi and Keith Newman – Advanced Micro Devices, Inc.</td>
</tr>
<tr>
<td>4. 10:00 a.m. - The Highly Effective EMI Shielding Materials for Electric and Magnetic Fields Over the Wide Range of Frequency in Near-Field Region Yoon-Hyun Kim, Kisu Joo, Kyu Jae Lee, Jung Woo Hwang, Se Young Jeong Seung Jae Lee, and Hyun Ho Park – Ntrium Inc.</td>
<td>4. 10:00 a.m. - The How and Why of Biased Humidity Tests with Copper Wire Amar Mavinkurve, Rene Rongen, Leon Goumans, Mark Luke Farnuga, Erik van Olst, Olfa O’Halloran, and Michel van Soestbergen – NXP Semiconductors</td>
<td>4. 10:00 a.m. - Peridynamics for Predicting Thermal Expansion Coefficient of Graphene Ergodan Madenog, Atila Barut, and Mehmet Dorduncu – The University of Arizona</td>
</tr>
<tr>
<td>5. 10:25 a.m. - Low-Loss NCF Material for High-Frequency Device Kazutaka Honda, Keiko Ueno, Tsuyoshi Ogawa, and Toshihisa Nonaka – Hitachi Chemical Company, Ltd.</td>
<td>5. 10:25 a.m. - Twist Testing for Flexible Electronics Justin Chow and Suresh Sitaraman – Georgia Institute of Technology; Jeffrey Meth – DuPont</td>
<td>5. 10:25 a.m. - Machine Learning Approach to Improve Accuracy of Warpage Simulations Cheryl Selvanayagam, Pham Luu Trung Duong, and Nagarajan Raghavan – Singapore University of Technology and Design; Rathin Mandal – Advanced Micro Devices Inc.</td>
</tr>
<tr>
<td>6. 10:50 a.m. - In-Situ Redox Nanowelding of Copper Nanowires with Surficial Oxide Layer as Solder for Flexible Transparent Electromagnetic Interference Shielding Xiawen Liang, Jiawei Zhou, Gang Li, Tao Zhao, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ching-Ping Wong – Georgia Institute of Technology</td>
<td>6. 10:50 a.m. - Mechanical Properties and Microstructural Fatigue Damage Evolution in Cyclically Loaded Lead-Free Solder Joints Sian Su, Mohd Amirul Hoque, Md Mahmudur Chowdhury, Si’i’d Hamada, Jeffrey C. Suhling, John L. Evans, and Pradeep Lall – Auburn University</td>
<td>6. 10:50 a.m. - Study on Warpage of Fan-Out Panel Level Packaging (FO-PLP) Using Gen-3 Panel Fa Xing Che, Kazunori Yamamoto, Vempati Srinivasa Rao and Vasarla Nagendra Sekhar – Institute of Microelectronics A*STAR</td>
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<td>7. 11:15 a.m. - Compartamental EMI Shielding Material with Jet-Dispensed Material Technology Xuan Hong, Qizhuo Zhuo Zhuo, Xinpei Cao, Dan Maslyk, Noah Ekstrom, Juliet Sanchez, Selene Hernandez, and Jinu Choi – Henkel Corporation</td>
<td>7. 11:15 a.m. - Reliability Studies of Silicon Interconnect Fabric Nilofar Shakoorzadeh, Sva Chandra Jangam, Pranav Ambhore, Amir Hanna, and Subramanian Iyer – University of California, Los Angeles; Kayzar Rahim – Global Foundries; Han Chien – National Chiao Tung University</td>
<td>7. 11:15 a.m. - Mechanical Properties of Intermetallic Compounds at Elevated Temperature by Nanoindentation Fan Yang, Sheng Liu, and Zhiren Chen – Wuhan University; Zhaoxia Zhou, Canyu Liu, and Changqing Liu – Loughborough University; Li Liu – Wuhan University of Technology</td>
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<tr>
<td>Session 19: MEMS, Sensors, and IoT</td>
<td>Session 20: Fan-Out and Heterogeneous Integration</td>
<td>Session 21: 5G, mm-Wave, and Antenna-in-Package</td>
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<td><strong>Committee:</strong> Packaging Technologies</td>
<td><strong>Committee:</strong> Interconnections</td>
<td><strong>Committee:</strong> High-Speed, Wireless &amp; Components</td>
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<td>Mont-Royal 1</td>
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<td>Nolita 1</td>
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</table>

### Session 1: 1:30 p.m. - A MEMS Microphone in a FOWLP


### Session 2: 1:55 p.m. - Fan-Out Wafer Level Packaging - A Platform for Advanced Sensor Packaging

Tanja Braun, Karl-Friedrich Becker, Ole Hoelck, Steve Voges, Ruben Kahle, Pascal Graup, Markus Wollhorn, and Rolf Aschenbrener – Fraunhofer IZM; Marc Dressigacker, Martin Schneider-Ramelow, and Klaus-Dieter Lang – Technical University Berlin

### Session 3: 2:20 p.m. - 3D-MID Evaluation and Validation for Space Applications

Etienne Hirt and Klaus Ruszka – Art of Technology AG; Benedikt Wigget, Maximilian Barth, Rafat Saleh, and Florian Janek – Hahn Schickard; Ernst Müller – Universität Stuttgart Institute of Microintegration

### Session 4: 3:30 p.m. - High-Temperature Pressure Sensor Package and Characterization of Thermal Stress in the Assembly up to 500 °C

Nivazhagan Subbiah, Qingming Feng, and Juergen Wilde – University of Freiburg; Gudrun Bruckner – CTR AG, Austria

### Session 5: 3:55 p.m. - Development of 3D WL CSP with Black Shielding for Optical Finger Print Sensor for the Application of Full Screen Smart Phone

Daquan Yu, Yichao Zou, Xinu Xiu, Aihua Shi, Xiaobing Yang and Zhiyi Xiao – Huanian Technology (Kunshan) Electronics Co., Ltd.

### Session 6: 4:20 p.m. - Micro Fountain-Like Resonators

Jianfeng Zhang, Jintang Shang, Bin Luo, and Zhaoxi Su – Southeast University

### Session 7: 4:45 p.m. - Novel Additively Manufactured Packaging Approaches for 5G/mm-Wave Wireless Modules

Tong-Hong Lin, Aline Eid, Jimmy Hester, Bijan Tehrani, and Manos Tentzeris – Georgia Institute of Technology; Jo Bito – Texas Instruments, Inc.
# Program Sessions: Thursday, May 30, 1:30 p.m. - 5:30 p.m.

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<td>Committee: Photonics in conjunction with Interconnections</td>
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<td>Session Co-Chairs:</td>
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<td>Kimberly Yass</td>
<td>Takaaki Isigure</td>
<td>Scott Savage</td>
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<td>Brewer Science</td>
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<td>Mikul Mito</td>
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<td>EMD Performance Materials</td>
<td>Broadcom Inc.</td>
<td>Taiwan Semiconductor Manufacturing Company, Ltd.</td>
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1. 1:30 p.m. - Temporary SiC-SiC Wafer Bonding Compatible With High Temperature Annealing  
Fengwen Mu and Tadatomo Suga – The University of Tokyo; Myuki Uomoto and Takehito Shimatsu – Tohoku University

1. 1:30 p.m. - A Highly Reliable 1.4um Pitch Via-last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems  
Stefaan Van Huylenbroeck, Joeri De Vos, Zaid El-Mekki, Geraldine Jameson, Nina Tutunyan, Kartik Muga, Michele Succhi, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC

1. 1:30 p.m. - Effects of In and Zn Double Addition on Eutectic Sn-38Bi Alloy  
Shiq Zhou, Yu-An Shen, and Hiroshi Nishikawa – Osaka University; Tiffani Uresti, Vasanth Shunmugasamy, and Bilal Mansoor – Texas A&M University at Qatar

2. 1:55 p.m. - Ultrathin Glass to Ultrathin Glass Bonding Using Laser Sealing Approach  
Messoud Bedjaoui, Johnny Amiran, and Jean Brun – CEA-LETI

2. 1:55 p.m. - Nanoscale Topography Characterization for Direct Bond Interconnect  
Bongsu Lee, Pawel Mrozek, Gill Fountain, John Posthill, Jeremy Theil, Guilian Gao, Rajesh Katkar, and Laura Mirkarmi – Xerox Corporation

2. 1:55 p.m. - Microstructural Evolution in SAC+X Solders Subjected to Aging  
Jing Wu, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

3. 2:20 p.m. - Development of Resins for Bumpless Interconnects and Wafer-on-Wafer (WOW) Integration  
Naoki Araki and Shinya Maetani – Dacel Corporation; Kim Young Suk and Shoichi Kodama – Disco Corporation; Takayuki Ohba – Tokyo Institute of Technology

3. 2:20 p.m. - Fully-Filled, Highly-Reliable Fine-Pitch Interconnects With TSV Aspect Ratio >10 for Future 3D-LSI/IC Packaging  

3. 2:20 p.m. - Microstructure Signature Evolution in Solder Joints, Solder Bumps, and Micro-Bumps Interconnection in a Large 3.5D FCGBGA Package During Thermo-Mechanical Cycling  
Arman Ahan, Andy Hsiao, Tae-Kyu Lee, and Greg Baty – Portland State University; Peng Su – Juniper Networks

4. 3:30 p.m. - Development of Novel Photosensitive Dielectric Material for Reliable 2.1D Package  

4. 3:30 p.m. - 3D Silicon Photonics Interposer for Tb/s Optical Interconnections in Data Centers With Double-Side Assembled Active Components and Integrated Optical and Electrical Through Silicon Via on SOI  
Bogdan Sirbu, Yann Edrichammer, Hermann Oppermann, and Tidja Tekei – Fraunhofer IZM; Victor Sidobor and Jochen Kraft – AMS AG; Xin Yin and Johan Baetens – IMEC; Christin Neumeier – VERTILAS GmbH; Francisco Soares – Fraunhofer HHI

4. 3:30 p.m. - Long-Term Reliability of Solder Joints in 3D ICs Under Near-Application Conditions  
Omar Ahmed, Golareh Jalkivand, Hector Fernandez, and Tingfei Jiang – University of Central Florida; Peng Su – Juniper Networks; Tae-Kyu Lee – Portland State University

5. 3:55 p.m. - High Reliability Solder Resist With Strong Adhesion and High Resolution for High Density Packaging  

5. 3:55 p.m. - Flip-Chip III-V-to-Silicon Photonics Interconnects for Optical Sensor  
Yves Martin, Jason Orcutt, Chi Xiong, Laurent Schares, Tymon Barwicz, Martin Glodde, Swetha Kamalpurkar, Eric J. Zhang, and William M.J. Green – IBM Corporation; Victor Dolores-Calzada, Martin Moelvik, and Ariane Sigmund – Fraunhofer HHI

5. 3:55 p.m. - Experimental Investigation of the Correlation between a Load-Based Metric and Solder Joint Reliability of BGA Assemblies on System Level  
Fabian Schemp, Marc Dressler, Daniel Kraetschmer, and Friederike Loerke – Robert Bosch GmbH; Juergen Wilde – University of Freiburg, IMTEK

6. 4:20 p.m. - Method for Mitigating the Warpage of Ultra-thin FC-CSPs by Controlling of EMC Properties  
Chika Arayama, Takahiro Akihisa, Yasunari Tomita, and Naoaki Kanagawa – Panasonic Corporation

6. 4:20 p.m. - Extremely Low-Profile Single Mode Fiber Array Coupler Suitable for Silicon Photonics  

6. 4:20 p.m. - Fatigue Life Predictive Model Development for Decoupling Capacitors  
Krishna Tunga, Joseph Ross, Kamal Sikka, and Bakul Parikh – IBM Corporation

7. 4:45 p.m. - Innovative Socketable and Surface-Mountable BGA Interconnections  
Omkar Gupte, Kristie Teoh, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Gregorio Murtagian – Intel Corporation

7. 4:45 p.m. - Micro-Lens Array Assembly for Optical Organic Substrates  

7. 4:45 p.m. - A Study of Substrate Models and Its Effect on Package Warpage Prediction  
Van Lai Pham, Jiefeng Xu, Jing Wang, Huyuan Wang and Seungbae Park – Binghamton University; Charandeep Singh – Coming, Inc.
## Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

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<th>Session 25: Wafer Level Packaging and Fan-In/Fan-Out Structures &amp; Materials</th>
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<th>Session 27: Advanced Biosensors and Bioelectronics</th>
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<td>Committee: Emerging Technologies</td>
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<td>Mont-Royal 2</td>
<td>Nolita 1</td>
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</table>

### Session Co-Chairs:
- Albert Lan: Applied Materials
- Andrew Kim: Intel Corporation
- Civit Tzau: Ford Motor Company
- Vivian Chu: Intel Corporation
- Ted Keppler: Texas Instruments
- Jeongik Chung: Samsung Electronics
- Yifan Huang: Amphenol ICC
- Stephen Smith: Amphenol ICC

### Session 1: 8:00 a.m. - 3D Fan-Out Package Technology with Photosensitive Through Mold Interconnects
Kantaro Morii, Soichi Yamashita, Takaumnu Fukuda, Masahiro Sekiguchi, Hirokazu Ezawa, and Shuzo Akejima – Toshiba Corporation

### Session 2: 8:25 a.m. - Effects of the Materials Properties of Epoxy Molding Films (EMFs) on Fan-Out Packages (FOPs) Characteristics

### Session 3: 8:50 a.m. - Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP)
Lin Bu, F.X. Che, Vempati Srinivasa Rao, and Xiaowu Zhang – Institute of Microelectronics A*STAR

### Session 4: 10:00 a.m. - Open CAPI Memory Interface Signal Integrity Study for High-Speed DRAM/DfM Channel with Standard Loss FR-4 Material and SNIA SST-TA-1002 Connector
Biao Cai, Jose Hejase, Kyle Giesen, Junyan Tang, Brian Connolly, Kyu Hyoun Kim, and Daniel Dreps – IBM Corporation; Zhiheng Fan, Rocky Huang, Luoyin Yi, Qiaoli Chen, Yifan Huang, and Stephen Smith - Amphenol ICC

### Session 5: 10:25 a.m. - Study of Board Level Reliability of eWLB (Embedded Wafer-Level BGA) for 0.35mm Ball Pitch

### Session 6: 10:50 a.m. - Board Level Reliability Study of Fan-Out Single Die Package with 350um Bump Pitch
Cheh Lung Lai, Gu Yan Lin, Tz-Yuan Chao, Yih-Sin Chen, and Feng-Lung Chien – Siliconware Precision Industries Co., Ltd.

### Session 7: 11:15 a.m. - Direct Heterogeneous Bonding of SiC to Si, SiO2, and Glass for High-Performance Power Electronics and Bio-MEMS
Jikai Xu, Chenxi Wang, Qishu Kang, Shicheng Zhou, and Yanhong Tian – Harbin Institute of Technology

### Refreshment Break: 9:15 a.m. - 10:00 a.m. Mont-Royal Commons

### Session 4: 10:00 a.m. - Study of the Board Level Reliability Performance of a Large 0.3 mm Pitch Wafer-Level Package
Bernd Waithas, Jan Proschwitz, Christoph Pietrzyga, Thomas Wagner, and Beth Kezer – Intel Deutschland GmbH

### Session 5: 10:25 a.m. - Study of Board Level Reliability of eWLB (Embedded Wafer-Level BGA) for 0.35mm Ball Pitch

### Session 6: 10:50 a.m. - Board Level Reliability Study of Fan-Out Single Die Package with 350um Bump Pitch
Cheh Lung Lai, Gu Yan Lin, Tz-Yuan Chao, Yih-Sin Chen, and Feng-Lung Chien – Siliconware Precision Industries Co., Ltd.

### Session 7: 11:15 a.m. - System Co-Design of a 600V GaN FET Power Stage with Integrated Driver in a QFN System-in-Package (QFN-SIP)
Jie Chen, Yong Xie, Django Trombley, and Rajen Murugan – Texas Instruments, Inc.

### Session 8: 11:40 a.m. - Open CAPI Memory Interface Signal Integrity Study for High-Speed DDR5 and Processes for Micro-TCB (Thin Film Battery) to Enable Miniaturized Healthcare Internet-of-Things (IoT) Devices
<table>
<thead>
<tr>
<th>Session Co-Chairs:</th>
<th>Nimish Bajaj</th>
<th>Akihisa Iwata</th>
<th>T. Susumu</th>
<th>Toshihiro Fukao</th>
<th>Tatsuhiko Hara</th>
<th>Takaaki Uemoto</th>
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<td>Session</td>
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<td>8:00 a.m.</td>
<td>Development of Flexible Hybrid Electronics Using Reflow Assembly With Stretchable Film</td>
<td>Welfeng Liu, William Uy, Alex Chan, and Dongkai Shangguan – Flex, Ltd.; Andy Behr, Takatoshi Abe, and Fukao Tomohiro – Panasonic Corporation</td>
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<td>8:25 a.m.</td>
<td>Highly Compact RF Transceiver Module Using High Resistive Silicon Interposer with Embedded Inductors and Heterogeneous Dies Integration</td>
<td>Gabriel Pare, Jean-Philippe Michel, Edoardo Deschaseaux, Pierre Ferris, Ayssar Serhan, and Alexandre Giry – CEA-LETI</td>
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<td>8:50 a.m.</td>
<td>Process Induced Wafer Warpage Optimization for Multi-Chip Integration on Wafer Level Molded Wafer</td>
<td>Chen-Yu Huang, Daniel Ng, Hung-Ho Lee, Vito Lin, Chang Fu Lin, and C. Key Chung – Siliconware Precision Industries Co., Ltd.</td>
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<tr>
<td>9:05 a.m.</td>
<td>3D Packaging with Embedded High-Power-Density Passives for Integrated Voltage Regulators</td>
<td>Teng Sun, Robert Spumey, Atom Watanabe, Pulugurtha Mandayakara, Himani Sharma, Rao Tummala, and – Georgia Institute of Technology; Furukawa Yoshinori – NTT Denko Corporation</td>
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<td>9:35 a.m.</td>
<td>Assessment of Accelerometer Versus LASER for Board Level Vibration Measurements</td>
<td>Varun Thukral, Malee Cahu, Jeroen Zaal, Jeroen Jalink, Romuald Roucou, and Rene Rongen – NXP Semiconductors</td>
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<td>9:50 a.m.</td>
<td>Effect of Process Parameters on the Long-Run Print Consistency and Material Properties of Additively Printed Electronics</td>
<td>Pradeep Lal, Amrit Abrol, Nakul Kothari, Jeff Suhling, and Susan Ahmed – Auburn University; Ben Leever – US AFRL; Scott Miller – NextFlex Manufacturing Institute</td>
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<tr>
<td>10:20 a.m.</td>
<td>Effect of Process Parameters on the Long-Run Print Consistency and Material Properties of Additively Printed Electronics</td>
<td>Pradeep Lal, Amrit Abrol, Nakul Kothari, Jeff Suhling, and Susan Ahmed – Auburn University; Ben Leever – US AFRL; Scott Miller – NextFlex Manufacturing Institute</td>
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<td>10:35 a.m.</td>
<td>Chiplet Microassembly Printer</td>
<td>Brad Rupp, Anne Plochowitz, Sara S. Crawford, Matthew Shreve, Sourabh Raychaudhuri, Sergey Buzlykov, Yunda Wang, Ping Mei, Qian Wang, Jamie Kalb and Yu Wang, Eugene M. Chow and Jing Ping Lu – Palo Alto Research Center Inc.</td>
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<td>10:50 a.m.</td>
<td>A Viscoelastic-Based Fatigue Reliability Model for the Polyimide Dielectric Thin-Film</td>
<td>Yu-Chen Chang and Tz-Cheng Chiu – National Cheng Kung University; Yu-Ting Yang, Yi-Hsu Tseng, and Xi-Hong Chen – Advanced Semiconductor Engineering Group, Inc.</td>
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<td>11:05 a.m.</td>
<td>Comprehensive Investigation on Warpage Management of FBGA With Multi-Embedded Ring Designs</td>
<td>Chang-Chun Lee, Yan-Yu Liou, and Pei-Chen Huang – National Tsing Hua University; Fussen Hsu, Puru Bruce Lin, Cheng-Ta Ko, and Yu-Hua Chen – Unimicron Technology Corporation</td>
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<tr>
<td>1. 1:30 p.m.</td>
<td>Development of High Power and High Junction Temperature SiC Based Power Packages</td>
<td>Gonguee Tang, Leong Ching Wai, Teck Guan Lim, Yong Liang Ye, Ravinder Pai Singh, Lin Bu, Boon Long Lau, Tai Chong Chai, Kazunori Yamamoto, and Xiaowu Zhang – Institute of Microelectronics A*STAR</td>
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<td>2. 1:55 p.m.</td>
<td>New Developments of Copper Plating Technology for Embedded Power Chip Packages Challenges</td>
<td>Yung-Da Chiu, Shu-Chih Wang, David Ho, B.H. Ma, Jensen Tsai, and Yu-Po Wang – Silicone Precision Industries Co., Ltd.</td>
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<td>3. 2:20 p.m.</td>
<td>Innovative Flip Chip Package Solutions for Automotive Applications</td>
<td>Tom Tang, Bo-Siang Fang, David Ho, B.H. Ma, Jensen Tsai, and Yu-Po Wang – Silicone Precision Industries Co., Ltd.</td>
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<td>4. 3:30 p.m.</td>
<td>Reliability of Laminated Bond Structure Using (Cu,Ni)/Sn TLP Bonding with AI Interlayer for High-Temperature Power Electronics Packaging</td>
<td>Yangthe Liu, Shalesh Joshi, and Ercan M. Dede – Toyota Research Institute North America</td>
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<td>5. 3:55 p.m.</td>
<td>Silver Sintering on Organic Substrates for the Embedding of Power Semiconductor Devices</td>
<td>Alexander Schifflacker, Lorenz Litzenberger, and Juergen Wilde – IMTEK University of Freiburg; Till Huegen and Vladimir Polezhaev – Kempston University of Applied Sciences</td>
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<td>7. 4:45 p.m.</td>
<td>Pb-Free, High Thermal and Electrical Performance Driven Die Attach Material Development for Power Packages</td>
<td>Byong Jin Kim, DongSu Ryu, Hyeong Il Jeon, Weng Tuck Chin, Jinn Young Khim, and Muhammad Hadiham Hazellah – Amkor Technology, Inc.</td>
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<td>8. 4:45 p.m.</td>
<td>- Fan-Out, Flip Chip, and WLCSP</td>
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## Program Sessions: Friday, May 31, 1:30 p.m. - 5:30 p.m.

<table>
<thead>
<tr>
<th>Session 34: Emerging Materials and Processing</th>
<th>Session 35: New Interconnects for Package Scaling</th>
<th>Session 36: RF and Power Components and Modules</th>
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<tbody>
<tr>
<td>Committee: Materials &amp; Processing in conjunction with Applied Reliability</td>
<td>Committee: Interconnections</td>
<td>Committee: High-Speed, Wireless &amp; Components</td>
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<tr>
<td><strong>Session Co-Chairs:</strong> Ziyin Lin, Intel Corporation Dwayne Shirley Inphi</td>
<td><strong>Session Co-Chairs:</strong> David Dunovitch University of Sherbrooke Katsumi Sakuma IBM Corporation</td>
<td><strong>Session Co-Chairs:</strong> Yong-Kyu Yoon University of Florida Craig Gau NXF Semiconductor</td>
</tr>
<tr>
<td>1. 1:30 p.m. - <strong>Flexible Graphene-Glass Fiber Composite Film With Ultrahigh Thermal Conductivity and Mechanical Strength as Highly Efficient Thermal Interface Materials</strong> Xiaoqiang Zhang, Linlin Ren, and Rong Sun – Shenzhen Institutes of Advanced Technology; Jianbin Xu – The Chinese University of Hong Kong; Ching-Ping Wong – Georgia Institute of Technology</td>
<td>1. 1:30 p.m. - <strong>Development of 2.3D High Density Organic Package Using Low Temperature Bonding Process With Sn-Bi Solder</strong> Shota Miiki, Hiroshi Taneda, Naoki Kobayashi, Kyoshi Oi, Koji Nagai, and Toshinori Koyama – Shinko Electric Industries Co. Ltd.</td>
<td>1. 1:30 p.m. - <strong>Multilayer Decoupling Capacitor Using Stacked Layers of BST and LNO</strong> Todd Schumann, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida; Jongmin Yook and Dongsu Kim – Korea Electronics Technology Institute</td>
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<tr>
<td>2. 1:55 p.m. - <strong>Highly Thermal Conductive and Electrically Insulated Graphene Based Thermal Interface Material With Long-Term Reliability</strong> Ya Liu and Johan Liu – Chalmers University of Technology; Shujing Chen – Shanghai University; Lilei Ye and Nan Wang – SHT Smart High Tech AB</td>
<td>2. 1:55 p.m. - <strong>PowerTherm Attach Process for Power Delivery and Heat Extraction in the Silicon-Interconnect Fabric Using Thermocompression Bonding</strong> Pranav Ambhoore, Boris Vaistband, Unmesha Mogera, Ujash Shah, Timothy Fisher, Mark Goosky, and Subramaniam S. Iyer – University of California, Los Angeles</td>
<td>2. 1:55 p.m. - <strong>System Co-Design of a High Current (40A) Synchronous Step-Down Converter in an Innovative Multi-chip Module (MCM) in LQFN-Type Packaging Technology</strong> Todd Lawson, Jie Chen, and Rajen Murugan – Texas Instruments, Inc.</td>
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<tr>
<td>4. 3:30 p.m. - <strong>Wafer-Level Integration of Thin Silicon Bare Dies Within Flexible Label</strong> Jean-Charles Sourrou, Ahmad Ithawi, and Laetitia Castagné – CEA-LETI</td>
<td>4. 3:30 p.m. - <strong>Ultra-Wide Micro Bumps Interconnection Matrix for Particle Detection: Process and Assembly</strong> Jean Charbonnier, Myrann Assous, Thierry Mourier, Celine Ribière, Stéphane Minoret, Sophie Verrun, Pierre Tissier, Remi Coquand, Mehmet Bicer, Fabienne Allain, Rémi Franziat, Gabriel Paras – CEA-LETI</td>
<td>4. 3:30 p.m. - <strong>A Zero Height Small Size Low Cost RF Interconnect Substrate Technology for RF Front Ends for M.2 Modules and Sip Swath V. Vajjakumar, Karthika Nalagaram, Sidharth Dalma, and Posyud Talebneyderkhe – Intel Corporation</strong></td>
</tr>
<tr>
<td>5. 3:55 p.m. - <strong>Laser Sintering of Aerosol Jet Printed Conductive Interconnects on Paper Substrates</strong> Mohammed Alhendi, Darshana Weerawarne, Jack Lombardi, Rajesh S. Sivasubramony, Peter Borgesen, and Mark Poliks – Binghamton University; Azar Alizadeh – GE Global Research</td>
<td>5. 3:55 p.m. - <strong>Low-Temperature Transient Liquid Phase (TLP) Bonding Using Eutectic Sn-In Solder Anisotropic Conductive Films (ACFs) for Flexible Transducers</strong> Jae-Hyong Park and Kyung-Wook Pak – Korea Advanced Institute of Science and Technology; Jongchul Park – National NanoFab Center</td>
<td>5. 3:55 p.m. - <strong>Open and Closed Loop Inductors for High-Efficiency System-on-Package Integrated Voltage Regulators</strong> Claudio Alvarez, Mohamed Bellarejad, and Madhavan Swaminathan – Georgia Institute of Technology</td>
</tr>
<tr>
<td>6. 4:20 p.m. - <strong>In-Situ Investigation of Organic Additive Interactions in Copper Electroplating Solutions With Surface Enhanced Raman Spectroscopy (SERS)</strong> Nitin Nudimathakady, Bartlet DeProspe, Himani Sharma, Nasrin Hooshmand, Saajal Pankajpannal, and Rao Tummala – Georgia Institute of Technology; Rahul Maneppali and Sashi Kandurud – Intel Corporation</td>
<td>6. 4:20 p.m. - <strong>Development of a No Reflow Cu Pillar Bump to Improve Chip/Package Interconnections (CPI) Process and Reliability Performance</strong> Kuei Hisao (Frank) Kuo, Yen Neng Wang, Feng Lung Chien, Rick Lee, and Jiunn Jie Wang – Silicone Precision Industries Co., Ltd.</td>
<td>6. 4:20 p.m. - <strong>RF Inductors Integrated in Organic Packaging</strong> Denis Mercier, Jean-Philippe Michel, Christine Raynaud, and Christophe Billard – CEA-LETI</td>
</tr>
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</table>
Wednesday, May 29, 2019

Session 37: Interactive Presentations 1
9:00 AM - 11:00 AM

Room: Belmont Commons

Co-Chairs:
Nam Pham
IBM Corporation

Pavel Roy Paladin
IBM Corporation

1. Comprehensive Solution for Micro Bump Coplanarity Control

2. Structural Enhancement for a CMOS-MEMS Microphone Under Thermal Loading by Taguchi Method
Chun-Lin Lu and Meng-Kao Yeh – National Tsing Hua University

3. A Methodology to Correct In-Fixture Measurement of Impedance by a Machine Learning Model
Bo-Sang Fang, Cha-Chu Lai, Ying-Wei Lu, Kuan-Ta Chen, Mike Tsai, and Don-Son Jiang – Siliconware Precision Industries Co., Ltd.


5. The Microstructure and Mechanical Property of the High Entropy Alloy as a Low Temperature Solder
Yingxia Liu, Xiuchen Zhao, Zhuangzhuang Hou, and JY On – Advanced Semiconductor Engineering Inc.

6. A Versatile Fan-Out Infrastructure Based on Die-Stencil Substrate Promoted by an Advanced Multifunctional Temporary Bonding Material
Xiao Liu, Baron Huang, Hong Zhang, Lisa Kirchner, Arthur Southard, Rama Puligadda, and Tony Faim – Brewer Science, Inc.

7. Low Temperature and Pressureless Microfluidic Electroless Bonding Process for Vertical Interconnections
Han-Tang Hung, S. Yang, I. A. Weng, and C. R. Kao – National Taiwan University; Y. H. Chen – Unimicron Technology Corporation

8. 3D Integration of CMOS-Compatible Surface Electrode Ion Trap and Silicon Photonics for Scalable Quantum Computing
Jing Tao, Yu Dian Lim, Nam Pau Chew, Peng Zhao, and Chuan Seng Tan – Nanyang Technological University; Hong Yu Li, Anak Agung Ali Atriyana, and Lin Bu – Institute of Microelectronics, Agency for Science, Technology and Research A*STAR; Luca Guidoni – University Paris Diderot and Chuan Seng Tan-Nanyang Technological University

9. Integrated RTD Sensors for Maintaining Thermal Uniformity During TCB Process
Salwa Ben Jemaa and Julien Sylvestre – University de Sherbrooke; Pascale Gagnon – IBM Canada, Ltd.

10. Wireless Transfer of Power and Data via a Single Resonant Inductive Link
Lih-Tyng Hwang, Yi-Chen Hsieh, Chin-Wei Chan, I-Fang Lo, Hsiu Suryanono, and Shiang-Hwua Yu – National Sun Yat-Sen University

11. Adaptive Patternning of Optical and Electrical Fan-Out for Photonic Chip Packaging
Ahmed Elmoji, Andres Desmet, Jeroen Missinne, Hannes Ramon, Jons Lambrecht, Johan Bauwelink, and Geert Van Steenberge – Ghent University; Peter De Heyn, Marianne Pantouvaki, and Joris Van Campenhout – IMEC

12. Low Surface Reflectance at Near Infrared Wavelength Thermoplastic Optical Lens Without AR Coating

13. A Novel Design of a Bandwidth Enhanced Dual-Band Impedance Matching Network with Coupled Line Wave Sloping
Deepayan Banerjee and Antra Saxena – Indraprastha Institute of Information Technology, Delhi; Mohammad Hashimi – Nazarbaye University

14. Effects of Electromigration on Microstructural Evolution and Mechanical Properties of Preferential Growth Intermetallic Compound Interconnects for 3D Packaging
Minghui Huang and Lin Zou – Dalian University of Technology

15. Telemetry for Implantable Biosensors
Ryan Green and Erdem Topсалaka – Virginia Commonwealth University

Ayad Ghanaim – 3DS Technologies; Niek van Haare and Sebastjan Kersjes – Besi Nl; Julian Bravin and Elisabeth Brandl – EV Group; Birgit Brandstätter, Hannes Kingler, and Benedikt Auer – Besi AT; Philippe Meunier – NXP Semiconductors

17. Low-Cost Non-TSV Based 3D Packaging Using Glass Panel Embedding (GPE) for Power-Efficient, High-Bandwidth Heterogeneous Integration
Siddharth Ravichandran, Fuhan Liu, Vanessa Smet, Mohanalingam Kathaperumal, and Rao Tummala – Georgia Institute of Technology; Shuhei Yamada – Murata Manufacturing Co., Ltd.

18. Polyhedral Integration of 2.5D and 3D Chiplets Using Interconnect Stitching
Paul Jo, Ting Zheng, and Muhammad Bakir – Georgia Institute of Technology

19. Characterization of the Current Mechanisms and Improved Leakage Current in Silver Doped Barium Strontium Titanate
Todd Schumann, Kyoung Tae Kim, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida

20. High-Temperature Aging Effects in SAC and SAC-X Lead-Free Solders
Mohammad Alam, KPI Rafidh Hassan, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

Wednesday, May 29, 2019

Session 38: Interactive Presentations 2
2:00 PM - 4:00 PM

Room: Belmont Commons

Co-Chairs:
Patrick Thompson
Texas Instruments, Inc.

Rao Bonda
Amkor Technology

1. Laundering Reliability of Electrically Conductive Fabrics for E-Textile Applications
Jeffrey Lee, Chang-Ho Lo, and Cheng-Chih Chen – Integrated Service Technology; Weifeng Liu – Flex, Ltd.

2. Preconditioning Technologies for Sputtered Seed Layers in FOPLP
Johannes Weichart, Jürgen Weichart, and Andreas Erhart – Evatec Corporation; Kay Vehwege – Fraunhofer IZM, Berlin

3. Impact of Thermal Boundary Resistance on the Thermal Design of GaN-on-Diamond HEMTs
Huaixin Guo, Yuechan Kong, and Tangsheng Chen – Nanojit Electronic Devices Institute

4. Measuring the Electric Properties of Thin Film Shape Memory Polymers in Simulated Physiological Conditions
Daniel Del Nero, Alexandra Joshi-Imre, and Walter Voit – The University of Texas at Dallas

5. Evaluation of WLP Dielectrics for High-Voltage Applications
Markus Woehmann, Marcus Paeck, and Michael Toepfer – Fraunhofer IZM; Klaus-Dieter Lang – TU Berlin

6. Mitigating the Effects of Microvortices in High-Re Deterministic Lateral Displacement by Using Symmetric Airfoil-Shaped Pillars
Jong-Hoon Kim, Kawkab Ahasan, and Brian Dincau – Washington State University

7. Plasma Dry Process Technology Development of Glass-Epoxy Film on the Silicon Substrate to Fabricate RDL for Future GPU/AI Application
Takahide Murayama, Muneyuki Sato, Akiyoshi Suzuki, Atsuhito Itoh, Tetsushi Fujinaga, and Yasuhiro Monkawa – ULVAC, Inc.

8. Fully Solid-State Integrated Capacitors Based on Carbon Nanofibers and Dielectrics with Specific Capacitances Higher than 200 nF/mm²
Amin Saleem, Rickard Andersson, Maria Bylund, Gulhem Pacot, Shafiq Kabir, and Vincent Desmaris – Smoltek AB; Charlotte Goemare – Smoltek AB

Wei-Yuan Cheng, Chen-Tsaì Yang, Shau-Fei Cheng, Wei-Han Chen, Han-Cheng Lai, Tai-Jui Wang, and Yuh-Zheng Lee – Industrial Technology Research Institute (ITRI)

10. Structuring of Laser Activated Polymers for Sensor Applications
Kevin Cromwell, Sebastian Bengsch, Aue, and Marc Wurst – Leibniz University Hanover

Wednesday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Belmont 1 & 5
1. A Deep Learning Approach for Volterra Kernel Extraction for Time Domain Simulation of Weakly Nonlinear Circuits
Thong Nguyen, Xinping Yang, Xu Chen, and Jose Schutt-Aine – University of Illinois

2. 24G Package Interconnect Study Based on Artificial Neural Network Modeling Approach
Hui Liu, Qian Ding, and Penglin Liu – Intel Corporation

3. Enhanced Reliability of a RF-SIP With Mold Encapsulation and EMI Shielding
Chen-Yuan Lu, Kuo-Hsien Liao, Yu-Chou Tseng, Dao-Long Chen, Alex Chan, Mengkai Shih, Mark Gerber, and Jason Chen – Advanced Semiconductor Engineering Inc.

4. Study of the Effect and Mechanism of a Cop Layer in Controlling the Statistical Variation of Via Extrusion
Golareh Javaljand and Tengfei Jiang – University of Central Florida

Chih-Sung Chen, Nicholas Kao, Poyu Liao, Ssu-Cheng Lai, and Don Son Jiang – SiliconWise Precision Industries Co., Ltd.

6. Three-Dimensional Copper Foam-Filled Elastic Conductive Composites With Simultaneously Enhanced Mechanical, Electrical, Thermal and Electromagnetic Interference (EMI) Shielding Properties
Yugen Hu, Han Gu, Tao Zhao, Tan Li, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology; Cheng-Ping Wong – Georgia Institute of Technology

7. Vertical Interconnect Technology for Enlarging Capacity on Micro Solid Thin Film Rechargeable Battery
Akihiro Horibe, Keniake Sueoka, Risa Miyazawa, Takahiro Mori, and Hiroyuki Mori – IBM Corporation

8. Characterization of Fine Pitch Hybrid Bonding Pads Using Electrical Mislallocation Test Vehicles
Imed Jadi, Diederick Lattard, Pascal Vivet, Edith Beigné, and Lucile Arnaud – CEA-LETI; Alexis Farcy, Joris Imed Jani, Didier Lattard, Pascal Vivet, Edith Beigné, and Lucile Arnaud – CEA-LETI; Alexis Farcy, Joris Jani, Didier Lattard, Pascal Vivet, Edith Beigné, and Lucile Arnaud – CEA-LETI

9. Characterization of Coated Silver Wire Mold Encapsulation and EMI Shielding
Masatoshi Tsunoda and Toshiaki Michihiro – Kyocera

10. Characterization of Coated Silver Wire Bond Interface Using TEM
Murali Sarangapani, Eric Tan Swee Seng, and Jason Wong Chin Yeung – Heraeus Holding GmbH

11. Characterization of Coated Silver Wire Bond Interface Using TEM
Murali Sarangapani, Eric Tan Swee Seng, and Jason Wong Chin Yeung – Heraeus Holding GmbH

Lianyuan Liu, Tao Lu, Daqun Luo, and Hui Xiao – China Electronic Product Reliability and Environmental Testing Research Institute

Gunvinder Singh Khinda, Maan Z. Kokaah, Mohanned Alhendi, M. Y. Nadler, Jack P. Lombardi, Danhara L. Weerawarne, Mark D. Polkis, and Peter Borgesen – Binghamton University; Nancy C. Stoffel – GE Global Research

14. Effects of Oven and Laser Sintering Parameters on the Electrical Resistance of IJP Nano-Silver Traces on Mesoporous PET Before and During Fatigue Cycling
Gunvinder Singh Khinda, Maan Z. Kokaah, Mohanned Alhendi, M. Y. Nadler, Jack P. Lombardi, Danhara L. Weerawarne, Mark D. Polkis, and Peter Borgesen – Binghamton University; Nancy C. Stoffel – GE Global Research

15. Multilayer Glass Substrate With High-Density Via Structure for All Inorganic Multi-Chip Module
Toshiki Iwai, Taiji Sakai, Daiseuke Muztani, and Seiki Saksyama – Fujitsu Laboratories, Ltd.; Kenji lida, Takayuki Inaba, Hidehiko Fujisaki, Akira Tamura, and Yosihon Miyazawa – Fujitsu Interconnect Technologies Limited

16. Three-Poisson’s Ratio of Lead-Free Solder – The Often Forgotten but Important Material Property
KPI Rafidah Hassan, Mohammad Alam, Jeffrey C. Suhling, and Pradepend Lai – Auburn University

17. Modeling and Design of Power Accelerator Laboratory
Christopher Kenney and Julie Segal – SLAC National Accelerator Laboratory

18. 24G Package Interconnect Study Based on Artificial Neural Network Modeling Approach
Hui Liu, Qian Ding, and Penglin Liu – Intel Corporation

19. Dynamic Characteristics Evaluation on Test Vehicles
Tatsuo Nagamatsu, and Junichi Kaneko – Dexerials Ltd.; Hidekazu Yagi, Ryoji Kojima, Daichi Mori, Chenhsiu, Toru Maeda, and Doug Day – Shinkawa

20. Study of Electrical and Mechanical Interference (EMI) Shielding Properties
Yugen Hu, Han Gu, Tao Zhao, Tan Li, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology; Cheng-Ping Wong – Georgia Institute of Technology

21. Study of the Effect and Mechanism of a Cop Layer in Controlling the Statistical Variation of Via Extrusion
Golareh Javaljand and Tengfei Jiang – University of Central Florida

Oscar Chuang, Chang-Chun Lee, and Chia-Ping Hsieh – National Tsing Hua University; Wei-Yuan Cheng and Steve Chiu – Industrial Technology Research Institute

23. The Poisson’s Ratio of Lead-Free Solder – The Often Forgotten but Important Material Property
KPI Rafidah Hassan, Mohammad Alam, Jeffrey C. Suhling, and Pradepend Lai – Auburn University

24. Additive Metal Deposition onto Silicon for Enhanced Microelectronics Cooling
Arad Aziz, Matthias Daeumer, Jacob C. Simmons, Bahgat G. Sammakia, Bruce T. Murray, and Scott Schiffrin – Binghamton University

Jinho Hah, Michael Suliks, Chao Ren, Kyung-Sk (Jack) Moon, Samuel Graham, and C. P. Wong – Georgia Institute of Technology

Thursday, May 30, 2019
Session 39: Interactive Presentations 3 9:00 AM - 11:00 AM

Committee: Interactive Presentations Room: Belmont Commons
Session Co-Chairs:
Michael Mayer
University of Waterloo

Alan Huffman
Micross Advanced Interconnect Technology

1. Modeling and Design of Power Distribution Network for a Heterogeneous Integrated Active Interposer With Neuromorphic Computing Circuits
Min Miao, Tianfang Chen, Jincan Zhang, Na Li, Kunkun Li, and Liyuan Wang – Beijing Information Science and Technology University; Yangqing Chen – IBM Corporation

2. PCB Microstrip Line Far-End Crosstalk Mitigation by Surface Mount Capacitors
Zhaqing Chen – IBM Corporation

3. New Cost-Effective Via-Last Approach on Artificial Neural Network Modeling Approach
Huan Liu – Peking University; Yang Yang, Xiaole Cui, Li, and Liyuan Wang – Beijing Information Science and Technology University; Yang Yang, Xiaole Cui, Li, and Liyuan Wang – Beijing Information Science and Technology University

4. Electromigration-Induced Sn Grain Rotation in Lead-Free Flip Chip Solder Bumps
Mingliang Huang, Jiameng Kuang, and Hongyu Sun – Dalan University of Technology

5. Low-Cost MT-Ferrule-Compatible Optical Connector for Co-Packaged Optics Using Single-Mode Polymer Waveguide
Akihiro Noriki and Takeru Amano – National Institute of Advanced Industrial Science and Technology; Masatoshi Tsunoda and Toshiaki Michihiro – Kyocera Corporation

6. Characterization of Coated Silver Wire Bond Interface Using TEM
Murali Sarangapani, Eric Tan Swee Seng, and Jason Wong Chin Yeung – Heraeus Holding GmbH

7. Research on Applied Reliability of BGA Solder Balls in Extreme Marine Environment
Lianyuan Liu, Tao Lu, Daqun Luo, and Hui Xiao – China Electronic Product Reliability and Environmental Testing Research Institute

8. Influence of Single/Double Sweeping Modes and Sweeping Voltage Increment/Polarity on Measurement of TSV Leakage Current
Qinghua Zeng, Jing Chen, and Yufeng Jin – Peking University

9. Improving the Solder Wettability via Atmospheric Plasma Technology
Sagun Kang, Yee-Wen Yen, and Yu-Lin Kuo – National Taiwan University of Science and Technology; Wallace Chuang and Eckart Schellkes – Robert Bosch Taiwan Co., Ltd.

10. Simulation and Experimental Validations of EM/TM/SM Physical Reliability for Interconnects Utilized in Stretchable and Foldable Electronics
Oscar Chuang, Chang-Chun Lee, and Chia-Ping Hsieh – National Tsing Hua University; Wei-Yuan Cheng and Steve Chiu – Industrial Technology Research Institute

11. A Deep Learning Approach for Volterra Kernel Extraction for Time Domain Simulation of Weakly Nonlinear Circuits
Thong Nguyen, Xinping Yang, Xu Chen, and Jose Schutt-Aine – University of Illinois

Lianyuan Liu, Tao Lu, Daqun Luo, and Hui Xiao – China Electronic Product Reliability and Environmental Testing Research Institute

13. Influence of Single/Double Sweeping Modes and Sweeping Voltage Increment/Polarity on Measurement of TSV Leakage Current
Qinghua Zeng, Jing Chen, and Yufeng Jin – Peking University

14. Improving the Solder Wettability via Atmospheric Plasma Technology
Sagun Kang, Yee-Wen Yen, and Yu-Lin Kuo – National Taiwan University of Science and Technology; Wallace Chuang and Eckart Schellkes – Robert Bosch Taiwan Co., Ltd.

15. Orthogonal Quilt Packaging 3D Integration for High Energy Particle Detectors
Jason Kulick, Tian Lu, Carlos Ortega, Gary Bernstein, and Edit Varga – Indiana Integrated Circuits, LLC; Christopher Kenney and Julie Segal – SLAC National Accelerator Laboratory

Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Belmont 1 & 5
16. Carbonized Electrodes for Electrochemical Sensing
Mohammad Aminul Haque and Nicole McFarlane – The University of Tennessee, Knoxville; Nickolay V. Lavinik and Dale Hensley – Oak Ridge National Laboratory

17. Moldability Challenges Associated With the Assembly of Thicker IC Packages for High Voltage and Power Applications
Sadia Naseem, Jack Chang, Megan Chang, Bob Lee, and Jason Chien – Texas Instruments, Inc.

18. Highly Compact, Multiband Composite-Right-Handed (CRLH) Transmission Line Based Stub for GPS Applications
Hae-In Kim, Seheee Hwangbo, Renuka Bowrothu, and Yong-Kyu Yoon – University of Florida

Thursday, May 30, 2019
Session 40: Interactive Presentations 4
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Belmont Commons
Session Co-Chairs:
Mark Eblen
Kyoercer International SC
Jeffrey Lee
IST-Integrated Service Technology Inc.

1. Die Thickness Optimization for Preventing Electro-Thermal Fails Induced by Solder Voids in Power Devices
Dario Visello, Andrea Albernetti, and Marco Rovitto – STMicroelectronics

2. 3-T (8-7) Decoupling Capacitors for Improved PDN in LPDDR4/4X3 System
Sunil Gupta – Qualcomm Technologies, Inc.

3. Improved Correlation Between Accelerated Board Level Reliability (BLR) Testing and Customer BLR Results Using a Hybrid Closed-Form/Finite Element Methodology
Maxim Serebrenik, Natalie Hernandez, Gil Sharon, Nathan Blattau, and Craig Hillman – DFR Solutions; Ken Symonds – Western Digital Corporation

4. Fabrication and Reliability Demonstration of 3 µm Diameter Photo Vias at 15 µm Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications

5. Pre-Cure Modification of Electrically Conductive Adhesive for Low Temperature Interconnection
Jintao George and David Danovitch – University of California, Los Angeles

6. RDL-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging

7. Epoxy Composites with Surface Modified Silicon Carbide Filler for High-Temperature Molding Compounds
Fan Wu, Nicholas C Mitchell, Bo Song, Kyongsik Moon, and C.P. Wong – Georgia Institute of Technology

8. Ultra Low Resistivity and High Electrical Stability SiIoy-2 ECAs Produced from Curing Chemistry Optimization for Flexible Electronics
Xueqiao Wang, Kyongsik Moon, Bo Song, and C.P. Wong – Georgia Institute of Technology

9. Physics of Failure Based Simulation and Experimental Testing of Quad Flat No-Lead Package
Jia-Shen Lan and Mei-Ling Wu – National Sun Yat-Sen University

10. An Assessment of Electromigration in 2.5D Packaging
Jiefeng Xu, Huayuan Wang, Jing Wang, VanLai Pham, Stephen R. Cain, and S.B. Park – Binghamton University; Scott McCann and Gamal Refai-Ahmed – Xinlin, Inc.

11. Diffusion Enhanced Drive Sub 100 °C Wafer Level Fine-Pitch Cu-Cu Thermocompression Bonding for 3D IC Integration
Asiya Kumar Panigrahy, Satish Bonam, Tamal Ghosh, Sva Rama Krishna Vanjari, and Shiv Govind Singh – Indian Institute of Technology, Hyderabad

12. Development of Sheet Type Molding Compounds for Panel-Level Package
Kenichi Ueno, Kazuhiro Dohi, Yui Suzuki, Masakazu Hirose, and Akira Nakao – Sanyu Rec Co., Ltd.

Huan Liu, Runu Feng, Yufeng Jin, and Yang Yang – Peking University; Min Miao – Beijing Information Science & Technology University

Rahil Khazaka, Donatien Martineau, Tony Youssef, Thanh Long Le, and Stephane Azzopardi – Safran R&D

15. Server CPU Package Design Using PoINT Architecture

16. Highly Reliable Die Attach Silver Joint with Pressure-Less Sintering Process
Shai Chen, Christine LaBarbera, and Ning-Cheng Lee – Indium Corporation; William Shambach and Jordan Palmer – Rochester Institute of Technology; Xuanyi Ding – Cornell University

17. 3D Power Packaged Device Thermomechanical Modeling and Stress Analysis after Reliability Trials
Lucrezia Guarino – STMicroelectronics; Lucia Zullino, Fumihiro Inoue, Patrick Verdonck, Soon-Wook Kim, Erik Steedk, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC

18. Direct Bonding of Low-Temperature Heterogeneous Dielectrics
Serena Iacovo, Lan Peng, Alain Phommahaaxay, Fumihiro Inoue, Patrick Verdonck, Soon-Wook Kim, Erik Steedk, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC

19. Millimeter Wave Dual Polarization Design Using Frequency Selective Surface (FSS) for 5G Base-Station Applications
Li-Ting Hwang, Chung-Yi Hsu, and Chi-Hau Yang – National Sun Yat-Sen University

Friday, May 31, 2019
Session 41: Student Interactive Presentations
8:30 AM - 10:30 AM
Room: Belmont Commons
Session Co-Chairs:
Kristina Young-Fisher
GLOBALFOUNDRIES
Ibrahim Guven
Virginia Commonwealth University

1. Room-Temperature Wire Bonding with Pd Coated Cu Wire on Al Pods: Ball Bond Optimization with 2-Stage Methodology
Nicholas Kam, Michael Hook, and Michael Meyer – University of Waterloo; Celal Con and Karim Karm – KA Imaging Inc.

2. On-Chip ESD Monitor
Kannan Kalappurakkal Thakkanp, Boris Vaibasd, and Subramanian S. Iyer – University of California, Los Angeles

3. Preparation and Characterization of Electroplated Cu/Graphene Composite
Xin Wang, Qian Wang, Jian Cai, Changming Song, and Yang Hu – Tsinghua University; Yang Zhao and Yu Pei – University of Science and Technology of China

4. Quantifying the Impact of RF Probing Variability on TRL Calibration for LTCC Substrates
Omer Faruk Yildiz, David Dahl, and Christian Schuster – Hamburg University of Technology

5. Effects of NCF and UBMs Materials on Electromigration Reliabilities of Sn-Ag Microbumps for Advanced 3D Packaging
Kirir Son, Gahui Kim, Hydongs Ryu, YoungCheon Kim, Jeong Sam Han, and Young-Bae Park – Andong National University; Gyu-Tae Park – Amkor Technology, Inc.; Ho-Young Son and Nam-Seong Kim – SK hynix Inc.; Cheol Wooong Yang – Sungkyunkwan University

6. Ag Diffusion Control Through Sn on a Sequential Plating-Based Bumping Process
Abderrahim El Amrani, Etienne Paradis, David Danovitch, and Dominique Drouin – Université de Sherbrooke

7. Mechanical Reliability Assessment of Cu65Sn35 Intermetallic Compound and Multilayer Structures in Cu/Sn Interconnects for 3D IC Applications
Jui-Yang Wu and C. Robert Kao – National Taiwan University; Jenn-Ming Yang – University of California, Los Angeles

Da-Jin Yoon and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology
Ji-Hye Kim, Dal-Jin Yoon, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

10. Effects of the Curing Properties and Viscosities of Non-Conductive Films (NCFs) on Sn-Ag Flip Chip Solder Bump Joint Morphology and Reliability
HanMin Lee, SeYong Lee, SangMyung Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Taejin Choi and SooIn Park – Doosan Corporation Electro-Materials BG

11. Experimental Investigations on Vertical Ultrasonic Assisted Low Temperature Sintering Process
Henning Seefisch and Jens Twiefel – Leibniz University Hanover

12. Pressureless Transient Liquid Phase Sintering Bonding of Sn-58Bi with Ni Particles for High-Temperature Packaging Applications
Kyung Deuk Min, Kwang-Ho Jung, Choong-Jae Lee, and Seung-Boo Jung – Sungkyunkwan University

13. Epoxy/Triazine Copolymer Resin System for High Temperature Encapsulant Applications
Jiaxiong Li, Chao Ren, Kyoung-Sik Moon, and CP Wong – Georgia Institute of Technology

14. Low-Temperature Ag-Ag Direct Bonding Technology for Advanced Chip-Package Interconnection
Jiaqi Wu and Chin C. Lee – University of California, Irvine

15. Reliability of Micro-Alloyed SnAgCu Based Solder Interconnections for Various Harsh Applications
Sihan Su, Francy Akkara, Anto Raj, Seth Gordon, Sharath Sridhar, Sivasubramanian Thirugnanasambandam, Sa’d Hamasha, Jeffery Suhling, and John Evans – Auburn University; Cong Zhao – Apple Inc.

16. A Novel Approach of Copper-Ceramic-Joints Manufactured by Selective Laser Melting
Thomas Stoll and Matthias Kirstein – Institute for Factory Automation and Production Systems; Joerg Franke

17. Automatic Transient Thermal Impedance Tester for Quality Inspection of Soldered and Sintered Power Electronic Devices on Panel and Tile Level

18. Time 0 Void Evolution and Effect on Electromigration
Jiefeng Xu, Van Lai Pham, Huayan Wang, Stephen R. Cain, and S.B. Park – Binghamton University; Scott McCann, Ho Hyung Lee, and Gamal Refai-Ahmed – Xilinx, Inc.

19. Quintuple Band lambda/4 Stub by Using Unbalanced Bridged CRLH Transmission Lines
Renuka Bowrothu, Sehee Hwangbo, Yong-Kyu Yoon, and Hein Kim – University of Florida

20. Product Level Design Optimization for 2.5D Package Pad Cratering Reliability during Drop Impact
Huayan Wang, Jing Wang, Jiefeng Xu, Vanlai Pham, Ke Pan, and Seungbae Park – Binghamton University; Hohyung Lee and Gamal Refai-Ahmed – Xilinx, Inc.

Jinho Hah, Yongja Kim, Patxi Fernandez-Zelaia, Sangil Lee, Shreyes Melkote, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology; Leroy Christie – ASM Pacific Assembly Products, Inc.; Paul Houston – Engent Inc.

22. Reduction of Ag Corrosion Rate During Decapsulation of Ag Wire Bond Packages
Jinho Hah, Kyoung Sik (Jack) Moon, and C. P. Wong – Georgia Institute of Technology; Yong Ja Kim – Samsung Electronics Company, Ltd.

Interactive Presentations: Friday, May 31, 8:30 a.m. - 10:30 a.m.

Friday Refreshment Break: 9:15 a.m. - 10:00 a.m. in Mont-Royal Commons
2019 TECHNOLOGY CORNER EXHIBITS AND INTERACTIVE PRESENTATIONS

Technology Corner Exhibits
Wednesday, May 29
9:00 a.m. - 12:00 Noon / 1:30 p.m. - 6:30 p.m.
Thursday, May 30
9:00 a.m. - 12:00 Noon / 1:30 p.m. - 4:00 p.m.
Belmont 1 & 5

Interactive Presentation Sessions
Wednesday, May 29
Session 37: 9:00 a.m. - 11:00 a.m. / Session 38: 2:00 p.m. - 4:00 p.m.
Thursday, May 30
Session 39: 9:00 a.m. - 11:00 a.m. / Session 40: 2:00 p.m. - 4:00 p.m.
Friday, May 31
Session 41: 8:30 a.m. - 10:30 a.m.
Belmont Commons
Booth 323
3D Systems Packaging Research Center (PRC)
Georgia Institute of Technology
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Phone: +1-404-894-9097
Fax: +1-404-894-3842
www.prc.gatech.edu
Email: gptrc@prc.gatech.edu
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Small Scale Systems Integration and Packaging (S3IP) Center
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Contact: Steve Czarnecki
Email: czar@binghamton.edu
The S3IP is a research and development organization that addresses research challenges in electronics packaging system design, process development, prototyping, and manufacturing for academia and the microelectronics industry. Located at Binghamton University, the Center brings together partners from government, industry and academia, providing opportunities for collaborations that will advance microelectronics research and development, with particular focus on electronics packaging design and manufacturing technology; thermal analysis and management for electronics; characterization of materials, surfaces, and physical interfaces for electronics devices and assemblies; and failure analysis and reliability improvement for electronics. Subject areas addressed include packaging of microelectronics, 2.5D/3D chip assemblies, power electronics, and integrated photonics.

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Canon USA Industrial Products Division provides advanced wafer & panel process equipment for applications including semiconductor, advanced packaging, power device & display. Canon provides cost-effective processing solutions including l-line & KrF optical lithography, nanoimprint lithography & Canon ANELVA deposition & etch equipment. Canon products supporting Compound Semiconductor applications include FPA-30305+ & FPA-3030EX6 lithography systems & BC7000 permanent wafer bonding systems.

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CEA-LETI is an institute providing R&D and Prototyping services in the field of Micro and Nanotechnologies. Capabilities include 8" and 12" wafer process flows for advanced CMOS, 3D stacking, MEMS and Silicon Photonics. Based in Grenoble, France, CEA-LETI has offices in the US and Japan. Over the past ten years CEA-LETI has developed a wide range of expertise in the fields of silicon interposers and high density interconnects to address the needs of the semiconductor industry in market segments such as mobile telephones and low power computing. Leti is working on hybrid bonding, wafer-to-wafer or chip-to-wafer integration. Pitch of few microns is envisioned, without underfill, room temperature and ambient pressure bonding. Self-alignment using capillary force is also developed for high precision, high throughput chip-to-wafer bonding. With the support of its internal IC design teams LETI provides industrial partners with a unique environment for validating new concepts through models, new design tools, test vehicles and implementing fully functional demonstrators such as wide I/O memory standard, 60 GHz RF SOCs for video data transfer or photonic interposers. Recently CEA-LETI has developed CoolCube, an original technique for stacking transistors sequentially in the same process flow for 3D-VLSI. The technology is designed to allow a connection of the stacked active layers on a nanometric scale, with a very high density, due to their alignment by a standard lithographic process. CEA-LETI is embedded in a dynamic and international ecosystem that include European and Global leaders.

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CMP offers, at very attractive prices, a set of advanced packaging solutions for 3D IC prototyping. Both active and passive Silicon interposer solutions are now available to designer as well as wafer-level or die–level post-processing for process modules integration (such as TSV and μ-pillars), enabling Silicon to Silicon assemblies for 3D-IC applications. Since 1981, CMP is a Multi-Project Wafer service organization in ICs, Photonic ICs, Smart Power and MEMS for prototyping and low volume production. CMP enables prototypes fabrication on industrial processes at very attractive costs and offers technical expertise and support in providing MPW and related services for researchers from Industrial companies Research Labs and Universities, and More than 600 Institutions from 70 countries have been served, 8100 projects have been prototyped, 74 different technologies have been interfaced. This year CMP will also promote advanced packaging solutions from NEXTS-Europractice consortium, with a focus on silicon photonics packaging.

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CPS Technologies Corporation is the worldwide leader in the design and high-volume production of AlSiC (aluminum silicon carbide) for high thermal conductivity (up to 1000 W/mK with embedded Pyrolytic Graphite) and device compatible thermal expansion. AlSiC thermal management components manufactured by CPS include hermetic electronic packages, heat sinks, microprocessor & flip chip heat spreader lids, Thermal substrates, IGBT base plates, cooler baseplates, Pin Fin baseplates for hybrid electric vehicles, microwave & optoelectronic housings.

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Fraunhofer IMWS-CAM is a leading service provider of failure diagnostics and material assessment for industry including semiconductor technologies, microelectronic components, microsystems and nanostructured materials. We consider the entire work flow from non-destructive defect localization over high precision target preparation to cutting edge nanoanalytics supplemented by micro-mechanical testing, finite element modeling and numerical simulation. Our goal is to support cooperation partners in introducing innovative materials and technologies, improving manufacturing process steps, securing reliable field use of components, analyzing field returns, and consequently optimizing manufacturing yield, product quality, reliability, and cost efficiency. In addition, we are collaborating with suppliers of microstructure diagnostics and material testing equipment in developing innovative failure analysis methods and instrumentation, problem-adapted work flows for quality and reliability control, and new industry-compatible applications for future markets.
Thick Package IC's enabling a new evolution in electronics. Semiconductor-on-Polymer™ (SoP) technology is set to rise to prominence for thin Flexible Hybrid Electronics (FHE) by 2020 as consumers seek revolutionary experiences.

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At IBM Assembly and Test Facility in Bromont, we have asserted our proposition in several key areas providing solutions for high current and high thermal dissipation applications in computing electronics market and developing specialized areas with attractive know- how in RF, Antennas, SIP and advanced opto electronic packaging for communication and wireless markets. Beyond our technical orientation, our experienced engineering team takes pride in using its design, assembly and test expertise to provide tailor-made solutions for our client’s needs and bring forth designs, prototypes and fast manufacturing ramp ups that are key to our client’s success. Several fruitful collaborations have been enacted in the past months and we already have received feedback that it provides high value to the customers that have chosen us as their development and manufacturing OSAT solution. Clients also see value in our supply chain management proposition. Clearly beyond the customer-supplier relationship, we value true partnerships for mutual growth. We have an exciting 2019 roadmap, some of the highlights include deploying high density interconnect laminates, pursuing integration and optimization of SiP packages and also deploying technical milestones to prepare for dense optical integration which is highly anticipated by several key players of the communications market in the years ahead.

**Booth 57**

**Integrated Service Technology (IST)**

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Founded in 1994 in Taiwan, IST began its business from IC circuit debugging and modification and gradually expanded its scope of operations, including Failure Analysis, Reliability Verification, Material Analysis, Automotive Electronic Verification Platforms and Signal Integrity Testing Services. IST has offered full-scope verification and analysis services to the IC engineering industry, its customers cover the whole spectrum of the electronics industry from IC design to end products. In response to IST’s mission of providing integrated solutions to customers, IST not only focuses on its core laboratory services but also enters the mass production services

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Interconnect Systems International, LLC (“ISI”), specializes in high-density module packaging, advanced interconnect and real-time signal processing hardware. ISI offers design, qualification, and testing, coupled with fully integrated in-house manufacturing. ISI’s system design capabilities include hardware, firmware and software and high-density PCB design. ISI’s additional capabilities include custom manufacturing process development, fine pitch SMT, flip chip, wire bond assembly, IC packaging, custom molding, over molding, and automated optical inspection.
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Group companies create continual improvements in photonics assembly product lines. These Nagase modules, disk drive, printed electronics and negative photoresist for semiconductor, circuit technology focus on electronic materials and for Pb-free. Engineered Materials Systems, Inc. Paste (NCP) for Fine pitch FC-PKG, Underfill for FOWLP, 2.5D, 3D, SiP, Non-Conductive semiconductor encapsulant of epoxy resin, Nagase ChemteX is a leading company for www.nagasechemtex.co.jp/en/ Fax: +1-408-567-9729 Phone: +1-408-567-9728 Santa Clara, CA 95054 Nagase America Corporation Booth 406 2880 Lakeside Drive, Suite 320 Santa Clara, CA 95054 Phone: +1-408-567-9728 Fax: +1-408-567-9729 www.nagasechemtex.co.jp/en/ Contact: Ippei Yamai Email: ippei.yamai@nagase-nam.com Nagase Chemtex is a leading company for semiconductor encapsulant of epoxy resin, especially Liquid Molding Compound (LMC) for FOWLP, 2.5D, 3D, SIP, Non-Conductive Paste (NCP) for Fine pitch FC-PKG, Underfill for Pb-free. Engineered Materials Systems, Inc. technology focus on electronic materials and negative photoresist for semiconductor, circuit assembly, photovoltaic, printer head, camera module, disk drive, printed electronics and photonics assembly product lines. These Nagase Group companies create continual improvements guiding its customers into the future.

Booth 205 NAMICS Technologies, Inc. 2055 Gateway Place, Suite 480 San Jose, CA 95110 Phone: +1-408-516-4611 Fax: +1-408-516-4617 www.namics.co.jp/e Contact: Tony Ruscigno Email: sales@namics-usa.com NAMICS is a global technology leader for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells with over 70 years of experience and expertise. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China, NAMICS serves its worldwide customers with enabling products for leading edge applications. We build more than products; we build relationships setting the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application. NAMICS CORPORATION is a leading source for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea and China, NAMICS serves its worldwide customers with enabling products for leading edge applications.

Booth: 111 nepes Corporation 9605 Scranton Road, Suite 402 San Diego, CA 92121 Phone: +1-858-429-6703 Cell: +1-669-264-6385 www.nepes.us Contact: Masayuki Oe Email: sales@nepes.us nepes is a leading-edge provider of Wafer Level Packaging, Panel Level Packaging and turnkey assembly solutions including testing and DPP services. Since 2001, nepes has been providing OSAT services in partnership with Fabless and IDM customers worldwide. With ISO/TS 16949, ISO 14001, OHSAS 18001 and AEO certified facilities located in South Korea and China, nepes provides an extensive range of packages: bump, wafer level package (WLP), fan-out wafer level package (FO-WLP), fan-out wafer level System in Package (FOWL-SIP) as well as 2 and 3D modules. Its PLP (Panel Level Package) has revolutionized the mass production of advanced semiconductor packages while providing price competitiveness by utilizing an innovative process and structure based on extensive touch screen panel (TSP) and LCD production experience. nepes is well positioned to support leading semiconductor companies, foundries and electronics IDMs with their advanced packaging requirements.

Booth 218 Neu Dynamics Corp. 110 Steamwhistle Dr. Ivyland, PA 18974 Phone: +1-215-355-2460 Fax: +1-215-355-7365 www.neudynamics.com Contact: Don Johnson Email: sales@neudynamics.com Neu Dynamics/NDC International, is a distributor of a wide range of back-end semiconductor assembly packaging equipment and materials for microelectronics including the following companies. Our portfolio includes Hamni Semiconductor, Boschman Advanced Packaging Technology, ATi, Micro Point Pro, Pink, Kulicke & Soffa, Master Machinery Corp, Haacker Automation, FA Systems Automation. We also supply automatic and semi-automatic trim and form dies and systems supplied with trim presses (both Servo and Hydraulic driven). Neu Dynamics further offers contract transfer molding services. Our fully equipped molding lab allows for mold tryouts, pilot runs and low to medium volume production. Neu Dynamics is also capable of building high precision injection molds specializing in insert and over-molding applications.

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Booth 414 Nitto Inc. Bayside Business Park 48500 Fremont Blvd. Fremont, CA 94538 Phone: +1-510-445-5400 Fax: +1-510-445-5480 www.nitto.com Contact: Yasuko Ferris Email: yasuko.ferris@nitto.com Nitto is a global supplier of materials and equipment for semiconductor manufacturing, represented by the following products: ELEP holder tapes for back-grinding and dicing; high temperature resistant masking tape; NEL machines (Taper/Detaper/ Wafer Mounter with or without peeling function/ UV machine) for thin wafer application; ELEPMOUNT (2-in-1:...
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Nordson DAGE manufacturers wire pull, ball and die shear test systems along with X-Ray inspection systems that are recognized as the industry standard. The 4800 bondtester brings the latest developments in automated wafer testing technology to users testing wafers from 200mm upwards. When combined with an integrated wafer handling device the 4800-INTEGRA™ can test multiple wafers consecutively. Automation on non-wafer samples can also be conducted on the 4000Plus which performs shear tests up to 200kg, pull tests up to 100kg and push tests up to 50kg. The 4000HS high speed bond tester is used for pull and shear testing of solder spheres to identify brittle fractures at speeds up to 4mm/sec in shear and 1.3mm/sec pull. Technologies such as TSV, PoP, 2.5D and 3D integration demand a new level of metrology. The XM8000 intelligent X-ray metrology system delivers fully automated, non-destructive, radiation safe defect detection of all complex devices.

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EMI shielding paste for spraying method / EMI shielding Film / EMI absorber / Conductive Bonding Film for camera module / Thermal Interface Material(TIM) / Conductive Particles for Elastomer Test Socket / Conductive Beads for Anisotropic Conductive Film(ACF). Do you have the interested with our products or technology? Please visit our booth or contact us.

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Palomar Technologies makes the connected world possible by delivering a Total Process Solution™ for advanced photonic and microelectronic device assembly processes utilized in today’s smart, connected devices. With a focus on flexibility, speed and accuracy, Palomar’s Total Process Solution includes Palomar die bonders, Palomar wire and wedge bonders, SST vacuum reflow systems, along with Innovation Centers for outsourced manufacturing and assembly, and Customer Support services, that together deliver improved production quality and yield, reduced assembly times, and rapid ROI. With its deep industry expertise, Palomar equips customers to become leaders in the development of complex, digital technologies that are the foundation of the connected world and the transmission of data generated by billions of connected devices. Palomar solutions are utilized by the world’s leading companies providing solutions for datacom, 5G, electric vehicle power modules, autonomous vehicles/LiDAR, enhanced mobile broadband, Internet of Things, SMART technology, and mission critical services.
Plasma-Therm’s products have been meeting the requirements of both R&D and volume applications. Manufacturers, academic and government institutions depend on Plasma-Therm equipment, designed with “lab-to-fab” flexibility to meet the requirements of both R&D and volume production. Plasma-Therm’s products have been adopted globally and have earned their reputation for value, reliability, and world-class support.

Plasma-Therm is a U.S. manufacturer of advanced plasma-processing equipment, providing etch, deposition, and plasma dicing technologies used in semiconductor packaging, solid-state lighting, power, data storage, renewable energy, MEMS, nanotechnology, photonics, and wireless communication markets. Plasma-Therm’s VERSALINE® platform is the workhorse for a variety of applications in specialty semiconductor markets. The platform’s modular design allows flexible configuration of substrate handling and technologies that address the wide range of customer requirements. Plasma-Therm’s SINGULATOR® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with “lab-to-fab” flexibility to meet the requirements of both R&D and volume production. Plasma-Therm’s products have been adopted globally and have earned their reputation for value, reliability, and world-class support.

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Shin-Etsu MicroSi, Inc. is a wholly owned subsidiary of Shin-Etsu Chemical Company. Shin-Etsu MicroSi is a world class supplier of packaging materials for the semiconductor industry. With a global support network- Sales Engineers, R&D, Manufacturing, Quality Assurance, and Logistics- we are able to quickly develop and provide new technologies to benefit our customers. This allows our clients to meet their ever changing technical, commercial and environmental needs by implementing Shin-Etsu MicroSi’s technology. Shin-Etsu MicroSi is known for supplying high performance Thermal Interface Materials, Underfills, Molding Compounds, High Purity Silicone Encapsulants, and Die Attach Materials.

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SPTS Technologies, an Orbotech company, designs, manufactures, sells, and supports advanced etch, PVD, CVD, and MVD® wafer processing equipment and solutions for the global semiconductor and micro-device industries, with focus on the Advanced Packaging, MEMS, high speed RF device, power management and LED markets. SPTS also offers Additive Printing solutions for 3D structural printing of dams and isolating layers for IC packaging and package marking. SPTS has manufacturing facilities in Newport, Wales and Allentown, Pennsylvania, and operates across 19 countries in Europe, North America and Asia-Pacific.

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