Don't miss out on the industry's premier event!

ECTC 2011

The 61st Electronic Components and Technology Conference

May 31 - June 3, 2011

Walt Disney World
Swan and Dolphin Resort
Lake Buena Vista, Florida USA

Sponsored by: CPMT, IEEE

Supported by: ECA, EIA

Welcome from the Mayor of Orlando

CITY OF ORLANDO

WELCOME TO THE GREAT
CITY OF ORLANDO!

On behalf of the residents of Orlando, it's my pleasure to welcome you to our Central Florida community. We are honored to host the 61st Electronic Component and Technology Conference and hope your stay is a memorable one.

Orlando is a City on the rise.

In addition to our world-class attractions, I invite you to experience all of the things that make Orlando one of the fastest growing, most business-friendly and quality of life-centered cities in the world.

Underneath a skyline that has doubled in just the last five years, Orlando offers fine dining, exciting night life, fabulous shopping, year-round outdoor activities, professional sports, arts and culture, abundant parks, nature trails and the chance to see some of Florida's unique wildlife up close.

Our vibrant and diverse culture is evidenced by the many distinctive neighborhoods that dot our city. I invite you to walk our red brick, tree lined streets, visit our revitalized downtown or see our medical or digital entertainment "clusters" and find out for yourself why Orlando is quickly becoming one of the next great American Cities of the new century.

I hope you enjoy your time here… and I hope you visit Orlando again soon.

Sincerely,

Buddy Dyer
Mayor

OFFICE OF THE MAYOR
CITY HALL • POST OFFICE BOX 4990 • ORLANDO, FLORIDA 32802-4990
PHONE 407-246-2221 • FAX 407-246-2842 • http://www.ci.orlando.fl.us

WELCOME FROM ECTC GENERAL AND PROGRAM CHAIRS

The Executive and Program Committees of the Electronic Components and Technology Conference (ECTC) welcome you to our 61st meeting at the Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida. This premier international conference is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT). ECTC provides a dynamic environment for learning, discussion, and technical exchange.

ECTC consists of three major parts: the technical program, the professional development courses, and the technology exhibition corner. Over 300 high-quality technical papers will be presented in 36 oral sessions and five poster sessions, including a student poster session. Contributions from more than 20 countries make ECTC a truly global conference. The papers cover a wide spectrum of topics, including advanced packaging technologies, all types and levels of interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, electronic components and simulation.

The program also includes 8 technical sessions on 3D Packaging and TSV (Through-Silicon-Via) to address exciting new developments and applications in this quickly expanding field.

In addition to the technical sessions during the day, a Tuesday morning and three evening panel sessions focusing on various special topics will be held. In Tuesday morning's special session titled "The Impact of Manufacturing Limitations on Electronic Packaging Performance and Reliability," session chair Lei Shan will gather a panel of experts to present and discuss the effect manufacturing errors and tolerances can have on system design, performance and reliability. A panel discussion on Tuesday evening, 7:30pm, chaired by Rolf Aschenbrenner and Prof. Bi titled "ECTC Spotlight on China" will analyze the position, direction and impact of packaging development and manufacturing in China. In the plenary session, chaired by Henning Braunisch, on "Power Efficiency Challenges and Solutions: From Outer Space to Inside the Human Body," industry experts will look at the power efficiency problem from different angles and at different scales (Wednesday, 7:00pm). Thursday evening starts with the Gala Reception at 6:30pm and is followed at 8:00pm by a CPMT Seminar on "Printed Devices and Large Area Interconnect Technologies for New Electronics," chaired by Kishio Yokouchi and Yoshitaka Fukuoka, which will focus on advanced and unique materials and process technologies for realizing printed-electronics in Japan.

The Professional Development Courses, chaired by Kitty Pearsall, will be on Tuesday (8am-5:15pm). World-class experts in their fields offer 16 courses on different topics. Participants can catch up with new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the technical exhibition corner. Leading companies primarily in the electronics components, materials, and packaging fields exhibit their latest technologies and products. Exhibit hours are 9:00am to noon and 1:30pm to 6:30pm on Wednesday, and 9:00am to noon and 1:30pm to 4:00pm on Thursday. The exhibitors invite you to their reception on Wednesday at 5:30pm. Along with our luncheons and morning and afternoon coffee breaks, this is another great opportunity to network and discuss technical and business matters. These social arrangements bring a lot of value to the conference, taking it beyond information exchange into the human side of business and technology.

The ECTC luncheon speaker is Dr. Nasser Grayeli, Vice President of the Technology and Manufacturing Group and Director of Intel's Corporate Quality Network. Dr. Grayeli will give us a presentation on "Challenges and Opportunities Ahead… Are we ready for the future digital world?"

This year we are trying new ways to promote our sponsors to help us to defray some of the increasing costs of running a large conference. We will be using large screen TVs in the conference entrance area and other areas to promote the products/services of our sponsors. We appreciate your feedback and ideas. If your company/affiliation is interested in this promotion medium for next year's ECTC, please let us know.

Finally, we would like to take this opportunity to thank our sponsors, exhibitors, authors and speakers, instructors, session chairs, committee members, and arrangement, publication, and publicity chairs, as well as all the volunteers for their support and hard work. Without the great effort from these many people ECTC would not be what it is. Special thanks to the Gala Reception sponsors and the corporate refreshments break sponsors. We also thank all conference attendees for making ECTC a success. We hope you will like the program and enjoy the conference, and we are grateful for your feedback. Let us have a great ECTC.

Rajen Dias
General Chair
Intel Corporation

Wolfgang Sauter
Program Chair
IBM Corporation

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Components, Packaging and Manufacturing Technology Society (CPMT), I welcome you to the 61st Electronic Components and Technology Conference (ECTC 2011).

I'm pleased to note that ECTC 2011 marks the first year in which the Conference will have a single sponsor – IEEE CPMT. Over its long history, ECTC was co-sponsored by the IEEE CPMT Society and the Electronic Components Association (ECA). That partnership produced an event that is recognized as the premier technology conference on electronics packaging, components, and microelectronic systems science, technology and education.

And as ECTC 2011 demonstrates, the Conference continues as the leading international event in its field – presenting more than 300 quality papers by authors from nearly 20 countries, as well as a special Panel Session "ECTC Spotlight on China," professional development courses, and other opportunities to learn the latest in our technologies.

Of course none of this could happen without the commitment of our dedicated volunteers – many of them IEEE CPMT Members – and our participants, who travel from around the world to spend long days and nights listening to presentations, networking with colleagues and developing new relationships. It's a sign of ECTC's ongoing success that these professionals return year after year

I hope you'll take advantage of all the opportunities that this year's ECTC has to offer.

Rolf Aschenbrenner
President, IEEE CPMT Society

CONFERENCE POLICIES AND GUIDELINES

Badges

Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits and all conference sponsored social functions.

Medical Services

For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property

The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelery. If there is a mini-safe in your room, you should consider using it.

Smoking Policy

The Walt Disney World Swan & Dolphin Resort does not allow smoking on it premise. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, or seminars. Thank you for your consideration and cooperation.

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Speaker

Wednesday, June 1, 2011 • Noon - Northern Hemisphere Ballrooms D – E (5th Level)

Challenges and Opportunities Ahead… Are we ready for the future digital world?

Presenter: Dr. Nasser Grayeli
Vice President of the Technology and Manufacturing Group and
Director of Intel's Corporate Quality Network

Nasser Grayeli is Vice President of the Technology and Manufacturing Group and Director of Intel's Corporate Quality Network. He leads a company-wide network for quality and reliability organizations responsible for product reliability, customer satisfaction and quality business practices.

Previously, Nasser managed Assembly & Test Technology Development, and was responsible for assembly test board, materials and equipment technology development. Nasser received his PhD in Materials Science & Engineering from Stanford University in 1981 and was a post-doctoral fellow at Stanford through 1983.

He participates in several industry associations and university advisory boards. He is currently Chairman of the Board of Directors of International Electronic Manufacturing Initiative (iNEMI), Intel Senior Sponsor of Stanford University, and Advisory Board member of the Materials Science & Engineering department at Stanford University.

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk in the foyer area of Australia 3 (Lobby Level), Walt Disney World DOLPHIN Resort as follows:

Monday, May 30, 2011 – 3:00 p.m. - 5:00 p.m.
(PD Courses & Conference)

Tuesday, May 31, 2011 – 6:45 a.m. - 8:15 a.m.
(AM PD Courses & Special Session Only)

Tuesday, May 31, 2011 – 11:00 a.m. - 1:15 p.m.
(PM PD Courses Only)

Tuesday, May 31, 2011 – 1:15 p.m. - 5:00 p.m.
(Conference)

Wednesday, June 1, 2011 – 6:45 a.m. - 4:00 p.m.

Thursday, June 2, 2011 – 7:30 a.m. - 4:00 p.m.

Friday, June 3, 2011 – 7:30 a.m. - 12:00 p.m.

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses.

Door Registration Fees

Door Registration with Proceedings on USB drive

Non-Member	$840
IEEE Member	$700
One Day	$450
Speaker/Session Chair	$600
Speaker/One Day	$325
Student	$200
Student Speaker	$200
Exhibits Only	$20
Tuesday AM or PM Course with luncheon	$475
Tuesday All-Day Courses with luncheon	$675
Tuesday Student All-Day Courses with luncheon	$125
Extra Luncheon Tickets for each day	$50
Extra Proceedings with registration	$100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

6:30 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Asia 1 / Lobby Level)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows XP and MS Office 2003.

7:00 a.m. Wednesday thru Friday
(Room Location: Northern Hemisphere Ballroom E 3 – 4 / 5th Level)

Speaker Prep Room

Speakers should prepare and review their digital presentations as follows: 7:00 a.m. – 5:00 p.m., Tuesday – Friday (Room Location: Europe 2 / Lobby Level)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

Companion Hospitality Room

8:00 a.m. - 4:00 p.m. Wednesday
(Room Location: Europe 1 / Lobby Level)

8:00 a.m. - 4:00 p.m. Thursday
(Room Location: Europe 3 / Lobby Level)

8:00 a.m. - 12:00 p.m. Friday
(Room Location: Europe 5 / Lobby Level)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to any show or restaurant, or give suggestions for that special night out. The Concierge can help to make your visit to Walt Disney World and the greater Orlando, FL area more exciting.

Message Center
Please use the hotel switchboard or the ECTC Registration Desk (Australia 3 Foyer / Lobby Level) to leave and pickup messages. The hotel number is +1-407-934-4000.

Press Room
Press Interviews will be scheduled on an as-requested basis. Check at the ECTC Registration Desk (Australia 3 Foyer) to schedule an interview while onsite. You may also coordinate an interview with conference leadership or presenting technical experts by contacting Jacqulyn Hampton at jhampton@pcgpr.com or +1-202-379-6616 (cell).

LUNCHEONS

Tuesday, May 31, 2011
Noon (Southern II, 5th Level)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, June 1, 2011
Noon (Northern Hemisphere Ballrooms D-E, 5th Level)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Dr. Nasser Grayeli of Intel Corporation.

Thursday, June 2, 2011
Noon (Northern Hemisphere Ballrooms D-E, 5th Level)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, June 3, 2011
Noon (Northern Hemisphere Ballrooms D-E, 5th Level)
The ECTC Program Chair will sponsor a luncheon for conference attendees.

There will be a raffle for attendees.

PANEL SESSION, PLENARY SESSION, CPMT SEMINAR AND RFID SPECIAL SESSION

ECTC Panel Session

ECTC Spotlight on China

Tuesday, May 31, 2011 • 7:30 - 9:00 p.m.

Southern Hemisphere Ballroom III (5th Level)

Chair: Rolf Aschenbrenner – President, CPMT

Co-Chair: Keyun Bi – President, Electronic Manufacturing and Packaging Technology Society of China, China

China has been leading the world in electronic products manufacturing with emphasis in consumer products. As such, it is a major consumer of Integrated Circuits Products eclipsing Japan, Europe, the Americas and the ASEAN regions. While much of the electronic products manufactured in China are exported to the rest of the world, with the GDP growing at 9 percent, China is now also becoming a major end-market for electronic products for consumer, automotive, and industrial applications. There is general consensus that in China the domestic electronic industry will grow to serve and compete in the worldwide market. There has been significant investment in China by multinational companies, domestic companies, as well as government. Advanced R&D programs that are heavily funded by the government at national and state levels are ongoing at top domestic packaging companies, universities and research institutes. How will the industry supply chain develop? What are the major directions for future innovation? How are the fruits of research and development in China being implemented in domestic industry? What is the impact of emerging Chinese packaging companies on the world's semiconductor industry? We have a distinguished panel of experts to look into their crystal balls and provide answers.

1. **China's Impact on the Semiconductor Industry - 2010 Update**
   C.E. (Ed) Pausa, PwC, USA
2. **Perspectives on Semiconductor Assembly Manufacturing in China**
   Bill Chen, ASE Group, USA
3. **An Overview of Electronic Packaging R&D in China**
   Ricky Lee, Hong Kong University of Science and Technology
4. **Innovation and Technology Development of the Chinese IC Packaging Industry**
   Bill Li, Jiangsu Changjiang Electronics Technology Co., Ltd., China
5. **Western China: Opportunities for Electronic Packaging Industry**
   Wenhui Zhu, TianShuiHuaTian Technology Co., Ltd, China

ECTC Plenary Session

Power Efficiency Challenges and Solutions: From Outer Space to Inside the Human Body

Wednesday, June 1, 2011 • 7:00 - 9:00 p.m.

Southern Hemisphere Ballroom III (5th Level)

Chair: Henning Braunisch – Intel Corporation

Power or energy per time consumed is a fundamental physical quantity ultimately limiting many of the microelectronic devices and systems employed at all levels of human activity. In deep space exploration a combination of battery life and radio efficiency may determine the maximum distance reachable from Earth. High-performance computing, in its quest for reaching exascale supercomputer performance within a practical power envelope, is struggling to improve energy per compute operation and bit of information exchanged between nodes. For the planners of the datacenters forming the backbone of the modern and future Internet, power efficiency is a key economical consideration with environmental implications as well. In consumer electronics power challenges lead to unique thermal issues. In the area of medical devices such as implants improved power efficiency contributes to extending human life itself. This year's Plenary Session looks at the power efficiency problem from various angles and at different scales. Be inspired by expert views and ideas and explore contributions of microelectronic packaging to the associated major societal challenges.

1. **Space Exploration**
   Greg Cardell, Power Systems Engineering Group Supervisor, JPL
2. **Supercomputing**
   Hans Jacobson, Research Staff Member, IBM Corporation
3. **Datacenters**
   Randy Mooney, Intel Fellow & Director I/O Research, Intel Corporation
4. **Consumer Electronics**
   Raj Master, General Manager, IC Packaging, Quality and Reliability, Microsoft Corporation
5. **Medical Implants**
   Sayfe Kiaei, Associate Dean of Research, School of ECEE, Arizona State University

CPMT Seminar

Printed Devices and Large Area Interconnect Technologies for New Electronics

Thursday, June 2, 2011 • 8:00 PM - 10:00 PM

Southern Hemisphere Ballroom III (5th Level)

Chair: Kishio Yokouchi - Fujitsu Interconnect Technologies Ltd.
Co-Chair: Yoshitaka Fukuoka – WEISTI

Printed electronics is a set of printing methods used to create electrical devices with large area and three-dimensional interconnection. Printed electronics is expected to facilitate widespread, very low-cost, and high-volume electronics for applications such as flexible displays, concomitant formation of sensors and transistors, smart labels, and active clothing. This seminar focuses on several kinds of advanced and unique materials and process technologies for realizing printed electronics.

1. **Printed Electronics: Low Temperature and Stretchable Wiring with Ag Inks**
   Katsuaki Suganuma, Osaka University
2. **Active-Matrix Backplane on Flexible Substrates for Printed Electronics**
   Hiroki Maeda, Dai Nippon Printing Co., Ltd.
3. **Printed Organic Transistors for Ultraflexible and Stretchable Electronics**
   Tsuyoshi Sekitani, The University of Tokyo
4. **Low Temperature Printing Techniques for High-performance Flexible Device Fabrication**
   Tatsuo Hasegawa, National Institute of Advanced Industrial Science and Technology
5. **Carbon Nanotube Thin Film Transistors on Plastic Films for Printed Electronics**
   Shinichi Yorozu, NEC Corporation

Special Session

The Impact of Manufacturing Limitations on Electronic Packaging Performance and Reliability

Tuesday, May 31, 2011 • 9:30 AM – Noon

Southern Hemisphere Ballroom I (5th Level)

Chair: Lei Shan – IBM Corporation

The increasing demands in system performance and functionality have been driving electronic packaging to their electrical, thermal, mechanical, material, and process limitations. Due to the ever shrinking design margins, not only design precision needs to be improved, but meanwhile, manufacturing errors/tolerance has to be taken into consideration and controlled accordingly to prevent unexpected failures during system evolutions. However, to date, the understanding of the effects of manufacturing errors/tolerance are quite limited, and therefore specifications are not in accord with the requirement of system reliability. This special session will provide a forum for experts in electrical, thermal, mechanical, material, and process fields covering various packaging levels from chip to substrate, PCB, and connectors/sockets. The presentations and discussions range from existing manufacturing capability to future trends in dealing with manufacturing errors/limitations such as material uniformity, dimension control, process variation, and manufacturing redundant features, etc.

1. **Manufacturing Limitations for 3D Electronic Die Stacking and Packaging using Through-Silicon-Vias (TSV)**
   John Knickerbocker, IBM Corporation
2. **Organic Package Evolution for High Performance Substrate Application**
   Koichi Nonomura, Kyocera Corporation
3. **PWB Technology/Materials Demands for Super Computing**
   Voya Markovich, Endicott Interconnect Technologies, Inc.
4. **Strategies for High Density Interconnect for Increasing Data Rates/Frequencies**
   Tom McCarthy, Taconic Advanced Dielectric Division
5. **Managing Fields in Complex Transmissions Structures**
   Rich Benson, Molex Connector Corporation

Attendees are encouraged to register as well for afternoon Professional Development Courses (PDCs).

Note: Lunch is not included for special session attendees who do not attend PDC courses.

These sessions/seminars are open to all conference attendees.

PROFESSIONAL DEVELOPMENT COURSES • TUESDAY, MAY 31, 2011

All Meeting Rooms Are Located on The 5th Level

Morning Courses 8:00 a.m. – Noon	Afternoon Courses 1:15 – 5:15 p.m.
Northern Hemisphere Ballroom E1 **1. Achieving High Reliability of Lead-Free Soldering – Materials Consideration** Course Leader: NingCheng Lee – Indium Corporation	**Northern Hemisphere Ballroom E1** **9. Solder Joint Reliability Testing and Life Prediction** Course Leader: Ahmer Syed – Amkor Technology
Northern Hemisphere Ballroom E2 **2. Electronics, Energy, and the Environment** Course Leader: Harry Charles, Jr. – The Johns Hopkins University, Applied Physics Laboratory	**Northern Hemisphere Ballroom E2** **10. On-Chip Thermal Management of Nano-Electronic Components** Course Leaders: Avram Bar-Cohen – University of Maryland; Karl J. L. Geisler – 3M
Northern Hemisphere Ballroom E3 **3. Wafer Level-Chip Scale Packaging (WLCSP)** Course Leader: Luu Nguyen – National Semiconductor Corporation	**Northern Hemisphere Ballroom E3** **11. Technology Advances in 3D-TSV Integration and Packaging of Micro-Nano Systems** Course Leader: James J.Q. Lu – Rensselaer Polytechnic Institute
Northern Hemisphere Ballroom E4 **4. 3D IC Integration: An Emerging System Level Architecture** Course Leader: Philip Garrou – Microelectronic Consultants of NC	**Northern Hemisphere Ballroom E4** **12. TSV and other Key Enabling Technologies for 3D IC Integration and WLP** Course Leader: John Lau – Industrial Technology Research Institute
Southern Hemisphere Ballroom III **5. Polymers and Nano-Composites for Electronic and Photonic Packaging: Recent Advances** Course Leaders: C.P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation	**Southern Hemisphere Ballroom III** **13. Polymers for Semiconductor Packaging** Course Leader: Jeffrey Gotro – InnoCentrix, LLC
Southern Hemisphere Ballroom IV **6. Analog and Power Electronic Packaging** Course Leader: Yong Liu – Fairchild Semiconductor Corporation	**Southern Hemisphere Ballroom IV** **14. Flip Chip Fabrication and Interconnection** Course Leader: Eric Perfecto – IBM Corporation
Southern Hemisphere Ballroom V **7. Fundamentals and Applications of Package Reliability Predictions** Course Leaders: Shubhada Sahasrabudhe, Alan Lucero – Intel Corporation	**Southern Hemisphere Ballroom V** **15. Moisture Related Reliability in Electronic Packaging** Course Leader: Xuejun Fan – Lamar University
Americas Seminar **8. IC Package Cost Reduction Using Supply Chain Modeling** Course Leaders: Chet Palesko – SavanSys Solutions LLC; Jan Vardaman – TechSearch International, Inc.	**Americas Seminar** **16. Packaging of High Brightness (HB) LED for Solid State Lighting** Course Leaders: Ricky Lee – HKUST; Sheng Liu – Huazhong University of Science and Technology

REFRESHMENT BREAKS – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
SOUTHERN HEMISPHERE BALLROOM FOYER (5TH LEVEL)

ECTC STUDENT RECEPTION

Tuesday, May 31, 2011
5:00 - 6:00 p.m.
Cabana Deck
(Near Pool & Cabana Bar Outside)
Rain Backup: Asia I (Lobby Level)
Host: Eric Perfecto – IBM Corporation

Students, have you ever wondered how the ECTC technical committees review and select papers? Or, just what subjects, content and paper organization make a standout ECTC paper? Then please come to the ECTC Student Reception. You'll have a chance to enjoy some good food and meet with representatives of each technical subcommittee. Don't miss this chance for an inside view of technical subcommittee operations. Sponsored by the IBM Corporation.

GENERAL CHAIR'S SPEAKERS RECEPTION

Tuesday, May 31, 2011
6:00 - 7:00 p.m.
Crescent Terrace (outside on SWAN property) / Rain Backup: Southern Hemisphere Ballroom I (5th Level)

Invited session chairs and speakers are requested to attend a reception on the Crescent Terrace located outside on the Swan Property. The rain backup will be Southern I (5th Level) inside the Dolphin property.

TECHNOLOGY CORNER RECEPTION

Wednesday, June 1, 2011
5:30 - 6:30 p.m.

An Exhibitor Sponsored Reception will be held in Atlantic Hall B (1st Level). All attendees and guests are invited.

61ST ECTC GALA RECEPTION

Thursday, June 2, 2011
6:30 p.m.

All badged attendees and guests are invited to attend a reception outside on the Lake Terrace on the Swan Property. The rain backup will be Northern Hemisphere D – E (5th level) inside the Dolphin Property.

CONTINUING EDUCATION UNITS

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 61st ECTC.

CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the "IEEE CPMT Professional Development Certificate." Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Courses CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.

2010 ECTC PAPER AWARDS

Best of Conference Papers – 2010

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 60th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Poster Paper share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

(Session 34, Paper 1)

Reduction of Lead-Free Solder Aging Effects Using Doped SAC Alloys

Zijie Cai, Yifei Zhang, Jeffrey C. Suhling, Pradeep Lall, R. Wayne Johnson, and Michael J. Bozack – Auburn University

Best Poster Paper

(Session 38, Paper 16)

Acceleration Factor Study of Lead-Free Solder Joints under Wide Range Thermal Cycling Conditions

Hongtao Ma, Mudasir Ahmad, and KuoChuan Liu – Cisco Systems, Inc.

Outstanding Papers – 2010

The winning authors for Conference Outstanding Session and Poster Papers receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

(Session 24, Paper 3)

Self-Assembly Technology for Reconfigured Wafer-to-Wafer 3D Integration

Takafumi Fukushima, Eiji Iwata, Kang-Wook Lee, Tetsu Tanaka, and Mitsumasa Koyanagi – Tohoku University

Outstanding Poster Paper

(Session 40, Paper 2)

Nondestructive Evaluation of the Delamination of Fine Bumps in Three-Dimensionally Stacked Flip Chip Structures

Yuki Sato, Naokazu Murata, Kinji Tamakawa, Ken Suzuki, and Hideo Miura – Tohoku University

Intel Best Student Paper – 2010

The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at 60th ECTC:

(Session 13, Paper 4)

Through-Package-Via Formation and Metallization of Glass Interposers

Vijay Sukumaran, Qiao Chen, Fuhan Liu, Nitesh Kumbhat, Tapobrata Bandyopadhyay, Hunter Chan, Sunghwan Min, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Christian Nopper – STMicroelectronics

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 31, 2011

7:30 a.m. – 12:00 p.m.
INEMI Meeting
Asia 2 (Lobby Level)

1:00 p.m. – 5:00 p.m.
INEMI Research Meeting
Asia 2 (Lobby Level)

7:30 a.m. – 4:00 p.m.
ITRS Assemblies & Packaging Technology Committee
Europe 4 (Lobby Level)

9:00 p.m. – 10:30 p.m.
ECTC Opto Committee
Americas Seminar Room (5th Level)

Wednesday, June 1, 2011

7:00 a.m. – 8:00 a.m.
CPMT Materials TC
Europe 3 (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT High-Density Board Packaging TC
Europe 4 (Lobby Level)

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, June 2, 2011

6:45 a.m. – 7:45 a.m.
CPMT Transactions Editors / AEs
Europe 3 (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT Education TC
Asia 1 (Lobby Level)

5:30 p.m. – 6:30 p.m.
CPMT Publications Workshop I
Asia 1 (Lobby Level)

5:30 p.m. – 6:30 p.m.
ECTC 2012 Program Committee Meeting
Southern Hemisphere Ballroom IV (5th Level)

8:00 p.m.
61st ECTC Governing/ Executive Committee Reception
General Chair's Suite

Friday, June 3, 2011

7:00 a.m. – 8:00 a.m.
CPMT and Your Career
All Welcome
Northern Hemisphere Ballroom E-1 (5th Level)

7:00 a.m. – 8:00 a.m.
CPMT RF & Wireless TC
Asia 1 (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT Nano Packaging TC
Europe 3 (Lobby Level)

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Europe 3 (Lobby Level)

Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 1: 3D Interconnections	Session 2: Embedded and Wafer Level Packaging	Session 3: Lead Free Solder
Committee: Interconnections	**Committee: Advanced Packaging**	**Committee: Materials & Processing**
Southern Hemisphere III (5th Level)	**Southern Hemisphere II (5th Level)**	**Southern Hemisphere I (5th Level)**
Session Co-Chairs: **James E. Morris – Portland State University** **Gilles Poupon – CEA LETI - MINATEC**	**Session Co-Chairs:** **Sam Karikalan – Broadcom Corporation** **S. W. Ricky Lee – Hong Kong Univ. of Science & Tech.**	**Session Co-Chairs:** **Yoichi Taira – IBM Japan** **Mikel Miller – Draper Laboratory**
1. *8:00 a.m. – Chip-to-Wafer (C2W) 3D Integration with Well-Controlled Template Alignment and Wafer-Level Bonding* Qianwen Chen – Tsinghua University, Rensselaer Polytechnic Institute (RPI); Dingyou Zhang and James Jian-Qiang Lu – Rensselaer Polytechnic Institute (RPI); Zheyao Wang and Litian Liu – Tsinghua University	1. *8:00 a.m. – Low Cost, Chip-Last Embedded ICs in Thin Organic Cores* Nitesh Kumbhat, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Georg Meyer-Berg – Georgia Institute of Technology, Infineon Technologies AG	1. *8:00 a.m. – Minor Alloying Effects of Ni or Zn on Microstructure and Microhardness of Pb-Free Solders* Sun-Kyoung Seo and Moon Gi Cho – Samsung Electronics; Sung K. Kang – IBM T.J. Watson Research Center; Jaewon Chang and Hyuck Mo Lee – KAIST
2. *8:25 a.m. – Fluxless Bonding for Fine-Pitch and Low-Volume Solder 3-D Interconnections* K. Sakuma, H. Noma, K. Toriyama, K. Sueoka, and Y. Orii – IBM Corporation; N. Unami, J. Mizuno, and S. Shoji – Waseda University	2. *8:25 a.m. – Through Mold Vias for Stacking of Mold Embedded Packages* T. Braun, K.-F. Becker, V. Bader, J. Bauer, K. Piefke, and R. Aschenbrenner – Fraunhofer IZM; S. Voges, T. Thomas, R. Kahle, R. Krüger, and K.D. Lang – TU Berlin	2. *8:25 a.m. – Solidification Processes in the Sn-Rich Part of the SnCu System* Iuliana Panchenko, Maik Mueller, and Klaus-Juergen Wolter – TU Dresden; Steffen Wiese – Saarland University; Sebastian Schindler – Fraunhofer Center for Silicon-Photovoltaics
3. *8:50 a.m. – Development of Fluxless Chip-On-Wafer Bonding Process for 3DIC Chip Stacking with 30µm Pitch Lead-Free Solder Micro Bumps and Reliability Characterization* Chau-Jie Zhan, Jing-Ye Juang, Yu-Min Lin, Yu-Wei Huang, Kuo-Shu Kao, Tsung-Fu Yang, Su-Tsai Lu, John H. Lau, Tai-Hong Chen, Robert Lo, and M.J. Kao – Industrial Technology Research Institute (ITRI)	3. *8:50 a.m. – Embedded Package Wafer Bow Elimination Techniques* J. Thompson, G. Tepolt, L. Racz, A. Mueller, T. Langdo, D. Gauthier, and B. Smith – Charles Stark Draper Laboratory	3. *8:50 a.m. – Diffusion Kinetics and Mechanical Behavior Lead-Free Microbump Solder Joints in 3D Packaging Applications* B.S.S. Chandra Rao – National University of Singapore, Institute of Microelectronics, A*STAR; V. Kripesh – Institute of Microelectronics, A*STAR; K.Y. Zeng – National University of Singapore
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Atlantic Hall B / 1st Level)		
4. *10:00 a.m. – Thermal Reliability of Fine Pitch Cu-Cu Bonding with Self-Assembled Monolayer (SAM) Passivation for Wafer-on-Wafer 3D-Stacking* L. Peng – Institute of Microelectronics, A*STAR, Nanyang Technological University; H.Y. Li and S. Gao – Institute of Microelectronics, A*STAR; D.F. Lim and C.S. Tan – Nanyang Technological University	4. *10:00 a.m. – System in Wafer-Level Package Technology with RDL-First Process* Norikazu Motohashi, Takehiro Kimura, Kazuyuki Mineo, Yusuke Yamada, Tomohiro Nishiyama, Koujiro Shibuya, Hiroaki Kobayashi, Yoichiro Kurita, and Masaya Kawano – Renesas Electronics Corporation	4. *10:00 a.m. – Ni/Cu/Sn Bumping Scheme for Fine-Pitch Micro-Bump Connections* W. Zhang, B. Dimcic, P. Limaye, A.L. Manna, P. Soussan, and E. Beyne – IMEC
5. *10:25 a.m. – High Density 20µm Pitch CuSn Microbump Process for High-End 3D Applications* J. De Vos, A. Jourdain, M.A. Erismis, W. Zhang, K. De Munck, A. La Manna, D.S. Tezcan, and P. Soussan – IMEC	5. *10:25 a.m. – Lithography Technique to Reduce the Alignment Errors from Die Placement in Fan-Out Wafer Level Packaging Applications* Warren Flack, Robert Hsieh, Gareth Kenyon, Khiem Nguyen, and Manish Ranjan – Ultratech Inc. Nuno Silva, Paulo Cardoso, and Eoin O. Toole – Nanium S.A.; Rainer Leuschner, Werner Robl, and Thorsten Meyer – Infineon Technology AG	5. *10:25 a.m. – Electromigration-Induced Accelerated Consumption of Cu Pad in Flip Chip Sn2.6Ag Solder Joints* W.J. Deng, K.L. Lin, and Y.T. Chiu – National Cheng Kung University; Y.S. Lai – Advanced Semiconductor Engineering, Inc.
6. *10:50 a.m. – Homo/Heterogeneous Bonding of Cu, SiO2, and Polyimide by Low Temperature Vapor-Assisted Surface Activation Method* Akitsu Shigetou – National Institute for Materials Science (NIMS); Tadatomo Suga – University of Tokyo	6. *10:50 a.m. – Reliability Evaluation on Low-k Wafer Level Packages* Praveen Yadav, Shantanu Kalchuri, Beth Keser, Ricky Zang, Mark Schwarz, and Bill Stone – Qualcomm, Inc.	6. *10:50 a.m. – Bonding of Bi2Te3 Chips to Alumina Using Ag-In System for High Temperature Applications* Wen P. Lin and Chin C. Lee – University of California, Irvine
7. *11:15 a.m. – High Resolution Acoustical Imaging of High-Density-Interconnects for 3D-Integration* Sebastian Brand and Matthias Petzold – Fraunhofer IWM; Peter Czurratis – PVA TePla Analytical Systems GmbH; Jason D. Reed, Matthew Lueck, Chris Gregory, Alan Huffman, John M. Lannon Jr., and Dorota S. Temple – RTI International	7. *11:15 a.m. – Process and Reliability Assessment of 200µm-Thin Embedded Wafer Level Packages (EMWLPs)* Hyoung Joon Kim, Ser Choong Chong, David Soon Wee Ho, Eric Woon Yik Yong, Chee Houe Khong, Calvin Wei Liang Teo, Daniel Moses Fernandez, Guan Kian Lau, Nagendra Sekhar Vasarla, Vincent Wen Sheng Lee, Srinivasa Rao Vempati, and Khan O.K. Navas – Institute of Microelectronics, A*STAR	7. *11:15 a.m. – Dependence of SnAgCu Solder Joint Properties on Solder Microstructure* B. Arfaei, T. Tashtoush, N. Kim, L. Wentlent, E. Cotts, and P. Borgesen – Binghamton University

Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 4: Metamaterials and Integrated Components

Committee:
Electronic Components & RF

Americas Seminar (5th Level)

Session Co-Chairs:
Rockwell Hsu – Wilinx Corporation
Andrea Paganini – IBM Corporation

1. *8:00 a.m. – Design Acceleration of Embedded RF Inductors on a Multilayer Flip Chip Package Substrate*
   Telesphor Kamgaing and Valluri Rao – Intel Corporation; Adel Elsherbini – University of Michigan

2. *8:25 a.m. – Integrated Balun Bandpass Filter Design with an Optimal Common Mode Rejection Ratio*
   Chien-Hsun Chen, Chien-Hsiang Huang, and Tzyy-Sheng Horng – National Sun Yat-Sen University; Sung-Mao Wu – National University of Kaohsiung; Jian-Yu Li and Cheng-Chung Chen – Industrial Technology and Research Institute (ITRI); Chi-Tsung Chiu and Chih-Pin Hung – Advanced Semiconductor Engineering Inc.

3. *8:50 a.m. – Design and Modeling Methodology of Embedded Passives Substrate in a Compact Wireless Connectivity Module*
   Chi-Tsung Chiu, Pao-Nan Lee, Chi-Han Chen, Yuan-Hung Lin, Yei-Shen Wu, Ying-Te Ou, and Chih-Jing Hsu – Advanced Semiconductor Engineering, Inc.

4. *10:00 a.m. – Chip-Package Electrical Interaction in Organic Packages with Embedded Actives*
   Nithya Sankaran, Hunter Chan, Madhavan Swaminathan, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Telesphor Kamgaing and Vijay K. Nair – Intel Corporation

5. *10:25 a.m. – An Investigation of Stiction in Poly-SiGe Micromirror*
   F.Z. Ling, J.P. Celis, and I. De Wolf – IMEC, KU Leuven; J. De Coster and A. Witvrouw – IMEC; R. Beernaert – Ghent University

6. *10:50 a.m. – High Quality Factor RF Inductors Using Low Loss Conductor Featured with Skin Effect Suppression for Standard CMOS/BiCMOS*
   I. Iramnaaz, T. Sandoval, and Y. Zhuang – Wright State University; H. Schellevis – TU Delft; B. Rejaei – Sharif University of Technology

7. *11:15 a.m. – A New Metamaterial Unit Cell for Compact Microstrip Circuit Designs*
   Nophadon Wiwatcharagoses, Kyoung Youl Park, and Prem Chahal – Michigan State University

Session 5: High-Speed Interconnects

Committee:
Modeling & Simulation

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
Bruce Kim – The University of Alabama
Madhavan Swaminathan – Georgia Institute of Technology

1. *8:00 a.m. – System-Level Exhaustive Link Simulation Needed for PCB Co-Design*
   Kevin J. Buchs, Michael J. Degerstrom, Bart O. McCoy, Erik S. Daniel, and Barry K. Gilbert – Mayo Clinic

2. *8:25 a.m. – Modeling and Characterization of High Speed Interfaces in Blade and Rack Servers Using Response Surface Model*
   Bhyrav Mutnury, Frank Paglia, Minchuan Wang, and Girish K. Singh – Dell Inc.; Antonio Ciccomancini Scogna – CST of America, Inc.

3. *8:50 a.m. – A Study of the Roughness Propagation Effects in Waveguides with the Mode Matching Technique Combined with the Method of Moments*
   Ruihua Ding and Leung Tsang – University of Washington; Henning Braunisch – Intel Corporation

4. *10:00 a.m. – Equivalent Model for Shielded Microstrip Transmission Lines over Lossy Layered Substrates*
   Sidharath Jain and Jiming Song – Iowa State University; Telesphor Kamgaing and Yidnekachew Mekonnen – Intel Corporation

5. *10:25 a.m. – Active Crosstalk Cancellation for Next-Generation Single-Ended Memory Interfaces*
   John Wilson and Dan Oh – Rambus, Inc.

6. *10:50 a.m. – Decision Feedback Equalizer (DFE) Behavioral Macro Model for Packaging System Eye Diagram Transient Simulations*
   Zhaoqing Chen – IBM Corporation

7. *11:15 a.m. – Ultra-High I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications*
   Gokul Kumar, Tapobrata Bandyopadhyay, Vijay Sukumaran, Venky Sundaram, Sung Kyu Lim, and Rao Tummala – Georgia Institute of Technology

Session 6: Emerging Packaging

Committee:
Emerging Technologies

Southern Hemisphere V (5th Level)

Session Co-Chairs:
John Cunningham – Oracle
Vasudeva P. Atluri – Renavitas Technologies

1. *8:00 a.m. – A Novel MCM Package Enabling Proximity Communication I-O*
   I. Shubin, A. Chow, D. Popovich, H. Thacker, M. Giere, R. Hopkins, A.V. Krishnamoorthy, J.G. Mitchell, and J.E. Cunningham – Oracle

2. *8:25 a.m. – MEMS Optical Acoustic Sensors Manufactured in Laminates*
   Yang Zhang, Jonas Tsai, G.P. Li, and Mark Bachman – University of California, Irvine

3. *8:50 a.m. – Surface Engineering of Graphene for High Performance Supercapacitors*
   Ziyin Lin, Yan Liu, Yagang Yao, Owen J. Hildreth, Zhuo Li, Kyoungsik Moon, and Joshua C. Agar – Georgia Institute of Technology; Chingping Wong – Georgia Institute of Technology, Chinese University of Hong Kong

4. *10:00 a.m. – Enhancement of Light Extraction Efficiency of Multi-Chips Light-Emitting Diode Array Packaging with Various Microstructure Arrays*
   Dan Wu, Kai Wang, and Sheng Liu – Huazhong University of Science & Technology (HUST), Wuhan National Laboratory for Optoelectronics

5. *10:25 a.m. – Novel Anisotropic Conductive Adhesive for 3D Stacking and Lead-Free PCB Packaging–A Review*
   S. Manian Ramkumar – Rochester Institute of Technology; Hari Venugopalan and Kumar Khanna – SunRay Scientific

6. *10:50 a.m. – Low Temperature Glass-Thin-Films for Use in Power Applications*
   Juergen Leib, Oliver Gyenge, Ulli Hansen, and Simon Maus – MSG Lithoglas AG; Karin Hauck, Ivan Ndip, and Michael Toepper – Fraunhofer IZM

7. *11:15 a.m. – MEMS in Laminates*
   Mark Bachman and G.P. Li – University of California, Irvine

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Atlantic Hall B / 1st Level)

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:10 p.m.

Session 7: 3D Integration

Committee:
Advanced Packaging

Southern Hemisphere III (5th Level)

Session Co-Chairs:
Rozalia Beica – Applied Materials
John Knickerbocker – IBM Corporation

1. ***1:30 p.m. – 3D Chip Stacking with 50 um Pitch Lead-Free Micro-C4 Interconnections***
J. Maria, B. Dang, S.L. Wright, C.K. Tsang, P. Andry, R. Polastre, Y. Liu, L. Wiggins, and J.U. Knickerbocker – IBM T.J. Watson Research Center

2. ***1:55 p.m. – Development of Super Thin TSV PoP***
Seung Wook Yoon, Shariff Dzafir, Meenakshi Prashant, Pandi Chelvam Marimuthu, and Flynn Carson – STATS ChipPAC; Kazuo Ishibashi – Nokia Japan Co., Ltd.

3. ***2:20 p.m. – Design, Simulation and Process Optimization of AuInSn Low Temperature TLP Bonding for 3D IC Stacking***
Ling Xie, Won Kyoung Choi, C.S. Premachandran, Cheryl S. Selvanayagam, Siong Chiew Ong, Ebin Liao, Ahmad Khairyanto, V.N. Sekhar, and Serene Thew – Institute of Microelectronics, A*STAR; Ke Wu Bai and Ying Zhi Zeng – Institute of High Performance Computing, A*STAR

4. ***3:30 p.m. – Advanced Reliability Study of TSV Interposers and Interconnects for the 28nm Technology FPGA***
Bahareh Banijamali, Suresh Ramalingam, Kumar Nagarajan, and Raghu Chaware – Xilinx, Inc.

5. ***3:55 p.m. – A Study on Wafer Level Molding for Realizing 3-D Integration***
C.S. Lee, E.K. Choi, U.B. Kang, M.O. Na, H.C. Kim, H.J. Song, J.S. Lee, M.S. Yoon, J.H. Hwang, T.J. Cho, and S.Y. Kang – Samsung Electronics Company, Ltd.

6. ***4:20 p.m. – Through Silicon Via Stacking & Numerical Characterization for Multi-Die Interconnections Using Full Array & Very Fine Pitch Micro C4 Bumps***
K.Y. Au, J.D. Beleran, Y.B. Yang, Y.F. Zhang, S.L. Kriangsak, P.L. Ong Wilson, Y.S. Koh Drake, C.H. Toh, and C. Surasit – United Test and Assembly Center Ltd. (UTAC)

7. ***4:45 p.m. – Process Integration and Reliability Test for 3D Chip Stacking with Thin Wafer Handling Technology***
H.H. Chang – Industrial Technology Research Institute (ITRI), National Tsing Hua University; J.H. Huang, C.W. Chiang, Z.C. Hsiao, H.C. Fu, C.H. Chien, Y.H. Chen, and W.C. Lo – Industrial Technology Research Institute (ITRI); K.N. Chiang – National Tsin

Session 8: Electromigration

Committee:
Interconnections

Southern Hemisphere II (5th Level)

Session Co-Chairs:
Li Li – Cisco Systems, Inc.
Voya Markovich – Endicott Interconnect Technologies, Inc.

1. ***1:30 p.m. – Outperformance of Cu Pillar Flip Chip Bumps in Electromigration Testing***
Riet Labie, Tomas Webers, Christophe Winters, Vladimir Cherman, Eric Beyne, and Bart Vandevelde – IMEC; Franck Dosseul – STMicroelectronics

2. ***1:55 p.m. – Electromigration Behavior of Interconnects between Chip and Board for Embedded Wafer Level Ball Grid Array (eWLB)***
Robert Bauer, Armin H. Fischer, Christian Birzer, and Lars Alexa – Infineon Technologies AG

3. ***2:20 p.m. – Electromigration Reliability of Redistribution Lines in Wafer-Level Chip-Scale Packages***
Yi-Shao Lai, Chin-Li Kao, and Ying-Ta Chiu – Advanced Semiconductor Engineering, Inc. Bernd K. Appelt – Advanced Semiconductor Engineering, Inc.

4. ***3:30 p.m. – Cu Pillar and μ-Bump Electromigration Reliability and Comparison with High Pb, SnPb, and SnAg Bumps***
Ahmer Syed, Karthikeyan Dhandapani, Robert Moody, Lou Nicholls, and Mike Kelly – Amkor Technology

5. ***3:55 p.m. – Electromigration Analysis of Peripheral Ultra Fine Pitch C2 Flip Chip Interconnection with Solder Capped Cu Pillar Bump***
Yasumitsu Orii, Kazushige Toriyama, Sayuri Kohara, Hirokazu Noma, and Keishi Okamoto – IBM Research Tokyo; Daisuke Toyoshima and Keisuke Uenishi – Osaka University

6. ***4:20 p.m. – Electromigration Study of Micro Bumps at Si/Si Interface in 3DIC Package for 28nm Technology and Beyond***
T.H. Lin, R.D. Wang, M.F. Chen, C.C. Chiu, S.Y. Chen, T.C. Yeh, Larry C. Lin, S.Y. Hou, J.C. Lin, K.H. Chen, S.P. Jeng, and Douglas C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

7. ***4:45 p.m. – Electromigration in Ni/Sn Intermetallic Micro Bump Joint for 3D IC Chip Stacking***
Yu-Min Lin, Chau-Jie Zhan, Jing-Ye Juang, John H. Lau, Tai-Hong Chen, Robert Lo, and M. Kao – Industrial Technology Research Institute (ITRI); Tian Tian and King-Ning Tu – University of California, Los Angeles

Session 9: Underfills, Mold Compounds, and Dielectrics

Committee:
Materials & Processing

Southern Hemisphere I (5th Level)

Session Co-Chairs:
Don Frye – Henkel Corporation
Lejun Wang – Medtronic, Inc.

1. ***1:30 p.m. – Novel Preparation of Functionalized Graphene Oxide for Large Scale, Low-Cost, and Self-Cleaning Coatings of Electronic Devices***
Ziyin Lin, Yan Liu, and Zhou Li – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology, Chinese University of Hong Kong

2. ***1:55 p.m. – An Evaluation of Effects of Molding Compound Properties on Reliability of Cu Wire Components***
Peng Su – Cisco Systems, Inc.; Hidetoshi Seki, Chen Ping, Shin-ichi Zenbutsu, and Shingo Itoh – Sumitomo Bakelite; Louie Huang, Nicholas Liao, Bill Liu, Curtis Chen, Winnie Tai, and Andy Tseng – Advanced Semiconductor Engineering Group

3. ***2:20 p.m. – High Performance Wafer Level Underfill Material with High Filler Loading***
Satoru Katsurayama and Hiroshi Suzuki – Sumitomo Bakelite Co., Ltd.; Jae-Woong Nah – IBM T.J. Watson Research Center; Michael Gaynes and Claudius Feger – IBM T J. Watson Research Center

4. ***3:30 p.m. – In-Situ Characterization of Moisture Absorption-Desorption and Hygroscopic Swelling Behavior of an Underfill Material***
Yi He – Intel Corporation

5. ***3:55 p.m. – New Fine Line Fabrication Technology on Glass-Cloth Prepreg without Insulating Films for PKG Substrate***
Daisuke Fujimoto, Kunpei Yamada, Nobuyuki Ogawa, Hikari Murai, Hiroyuki Fukai, Youichi Kaneko, and Makoto Kato – Hitachi Chemical Co., Ltd.

6. ***4:20 p.m. – Low Temperature Cure of BCB and the Influence on the Mechanical Stress***
M. Woehrmann, M. Toepper, H. Walter, and K.D. Lang – Fraunhofer IZM, TU Berlin

7. ***4:45 p.m. – Characterization of Material Properties of Low Temperature Curing Polymer Dielectrics***
Alan Huffman, Marianne Butler, and Jeffrey Piascik – RTI International; Philip Garrou – Microelectronic Consultants of North Carolina; Jay Im – University of Texas, Austin

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Atlantic Hall B / 1st Level)

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:10 p.m.

Session 10: Thermomechanical Reliability

Committee:
Applied Reliability

Americas Seminar (5th Level)

Session Co-Chairs:
S.B. Park – Binghamton University
Tim Chaudhry – Broadcom Corporation

1. ***1:30 p.m. – Squeezing the Chip: The Buildup of Compressive Stress in a Microprocessor Chip by Packaging and Heat Sink Clamping***
   Jordan C. Roberts, Mohammad Motalab, Safina Hussain, Jeffrey C. Suhling, Richard C. Jaeger, and Pradeep Lall – Auburn University

2. ***1:55 p.m. – Cooling Rate, Pad Finish Effects on Mechanical Behavior of SnAgCu Alloys***
   S. Chavali, Y. Singh, and G Subbarayan – Purdue University; A. Bansal and M. Ahmad – Cisco Systems Inc.

3. ***2:20 p.m. – Characterization of Fine-Pitch Solder Bump Joint and Package Warpage for Low K High-Pin Count Flip-Chip BGA through Shadow Moiré and Micro Moiré Technique***
   An-Hong Liu, David W. Wang, and Hsiang-Ming Huang – ChipMOS Technologies, Inc.; Ming Sun, Muh-Ren Lin, and Chonghua Zhong – Broadcom Corporation; Sheng-Jye Hwang and Hsuan-Heng Lu – National Cheng Kung University

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Atlantic Hall B / 1st Level)

4. ***3:30 p.m. – Mechanical Characterization of Next Generation eWLB (Embedded Wafer Level BGA) Packaging***
   S.W. Yoon, Yoajian Lin, Sharma Gaurav, and Pandi C. Marimuthu – STATS ChipPAC, Ltd.; Yonggang Jin and Xavier Baraton – STMicroelectronics; V.P. Ganesh – Infineon Technologies Asia Pacific Pte. Ltd.; Thorsten Meyer and Andreas Bahr – Intel Mobile Communications

5. ***3:55 p.m. – Effects of Shock Impact Repetition Frequency on the Reliability of Component Boards***
   J. Hokka, T.T. Mattila, and M. Paulasto-Kröckel – Aalto University

6. ***4:20 p.m. – Comparison of LED Package Reliability under Thermal Cycling and Thermal Shock Conditions by Experimental Testing and Finite Element Simulation***
   Zhaohui Chen – Shanghai Jiao Tong University; Qin Zhang, Run Chen, Feng Jiao, Mingxiang Chen, and Xiaobing Luo – Huazhong University of Science & Technology (HUST); Sheng Liu – Shanghai Jiao Tong University, Huazhong University of Science & Technology

7. ***4:45 p.m. – The Study on the Thermal Cycle and Drop Test Reliability of System-in-Packages with an Embedded Die***
   Seon Young Yu – Institute of Microelectronics, A*STAR; Yong-Min Kwon and Kyung-Wook Paik – KAIST; Jinsu Kim, Taesung Jeong, and Seogmoon Choi – Samsung Electro-Mechanics

Session 11: Electrical Modeling and Measurements

Committee:
Modeling & Simulation

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
Zhaoqing Chen – IBM Corporation
Tawfik Rahal-Arabi – Intel Corporation

1. ***1:30 p.m. – Techniques for De-Embedding a High Port Count Connector to PCB Via Interposer***
   Yan Ding – Institute of Microelectronics, A*STAR Polytechnique of Montreal; Young H. Kwark, Lei Shan, and Christian Baks – IBM T.J. Watson Research Center; Ke Wu – École Polytechnique of Montreal

2. ***1:55 p.m. – Asymmetrical Differential Signaling for Notchy Wireline Channels***
   Farshid Aryanfar – Institute of Microelectronics, A*STAR; Aliazam Abbasfar – Rambus, Inc.

3. ***2:20 p.m. – An Effective Modeling Method for Multi-Scale and Multilayered Power/Ground Plane Structures***
   Jae Young Choi and Madhavan Swaminathan – Georgia Institute of Technology

4. ***3:30 p.m. – An Accurate and Fast 3D Numerical Approach to Power/Signal and Thermal Co-Simulation***
   Xin Ai, An-Yu Kuo, Mazen Baida, and Yun Chase – Sigrity, Inc.

5. ***3:55 p.m. – Techniques and Considerations for Verification of Model Causality***
   Matt Doyle, Rohan Mandrekar, and Jason Morsey – IBM Corporation

6. ***4:20 p.m. – Multi-Objective Optimization of Microprocessor Package Vertical Interconnects***
   Ying Li and Vikram Jandhyala – University of Washington; Henning Braunisch – Intel Corporation

7. ***4:45 p.m. – Automating Pin Field Modeling for SerDes Channel Simulations***
   Michael J. Degerstrom, Sharon K.. Zahn, Bart O. McCoy, Erik S. Daniel, and Barry K. Gilbert – Mayo Clinic

Session 12: Assembly Challenges and Solutions

Committee:
Assembly & Manufacturing Technology

Southern Hemisphere V (5th Level)

Session Co-Chairs:
Shawn Shi – Medtronic Corporation
Hirofumi Nakajima – Renesas Electronics Corporation

1. ***1:30 p.m. – Chip Cracks During Assembly: Finding and Eliminating the Critical Defect***
   Wolfgang Sauter, Steffen Kaldor, Jennifer Clark, Stephane Laforte, Clare McCarthy, Darryl Restaino, Jon Casey, and David Questad – IBM Corporation

2. ***1:55 p.m. – Thin-Core MCM Assembly Development for High-Performance Server Microprocessor***
   Sean S. Too, Mohammad Khan, Kevin Lim, Mike Loo, W.C. Lau, Azlina Nayan, S.F. Ng, B.L. Peh, and Edwin Goh – Advanced Micro Devices

3. ***2:20 p.m. – Advanced Laminate Carrier Module Warpage Considerations for 32nm Pb-Free, FC PBGA Package Design and Assembly***
   Edmund Blackshear, Thomas Lombardi, Frank Pompeo, and Jean Audet – IBM Corporation; KyungMoon Kim, YongHyuk Jeong, and JoonYoung Choi – STATS ChipPAC, Inc.; JoonYeob Lee and ChangWoo Park – Amkor Technology, Inc.; Kyoji Kondo, Shunichiro Matsumoto, and Yoichi Miyazawa – Shinko Electric Industries Company, Ltd.

4. ***3:30 p.m. – High-Speed Flex-On-Board Assembly Method Using Anisotropic Conductive Films (ACFs) Combined with Room Temperature Ultrasonic (U/S) Bonding for High-Density Module Interconnection in Mobile Phones***
   Kiwon Lee – Institute of Microelectronics, A*STAR; Sangmin Oh, Ilkka J. Saarinen, and Lasse Pykari – Nokia Corporation; Kyung-Wook Paik – KAIST

5. ***3:55 p.m. – High Speed and Low Cost FOB (Film-on-Board) Direct Bonding Using Laser Soldering Technology***
   Soon-Min Hong, Won Choi, Ja-Myeng Koo, Sea-Gwang Choi, and Young-Jun Moon – Samsung Electronics Company, Ltd.

6. ***4:20 p.m. – Phenomenological Understanding of Sn Migration in Ceramic-Chip Capacitors***
   Arun Raman, Shubhada Sahasrabudhe, Lyndell Dietz, and Mohammad Hossain – Intel Corporation

7. ***4:45 p.m. – Impact of Isothermal Aging on Sn-Ag-Cu Solder Interconnect Board Level High G Mechanical Shock Performance***
   Tae-Kyu Lee, Weidong Xie and Kuo-Chuan Liu – Cisco Systems, Inc.

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 13: TSV: Interposers and Applications

Committee:
Interconnections

Southern Hemisphere III (5th Level)

Session Co-Chairs:
Tom Gregorich – MediaTek
Alan Huffman – RTI International

1. *8:00 a.m.* – ***Low-Profile 3D Silicon-on-Silicon Multi-Chip Assembly***
P. Andry, B. Dang, and J. Knickerbocker – IBM T.J. Watson Research Center; K. Tamura and N. Taneichi – Tokyo Ohka Kogyo Co. Ltd.

2. *8:25 a.m.* – ***3D Sensor Application with Open Through Silicon Via Technology***
J. Kraft, F. Schrank, J. Teva, J. Siegert, G. Koppitsch, C. Cassidy, and E. Wachmann – Austriamicrosystems AG; F. Altmann, S. Brand, C. Schmidt, and M. Petzold – Fraunhofer IWM

3. *8:50 a.m.* – ***Reliability Study of 3D-WLP Through Silicon Via with Innovative Polymer Filling Integration***
M. Bouchoucha – STMicroelectronics, Universités Paul Cézanne; P. Chausse, S. Moreau, and N. Sillon – CEA, LETI; L.L. Chapelon – STMicroelectronics; O. Thomas – Universités Paul Cézanne

Session 14: Flip Chip and Advanced Substrates

Committee:
Advanced Packaging

Southern Hemisphere II (5th Level)

Session Co-Chairs:
Altaf Hasan – Intel Corporation
Young-Gon Kim – IDT

1. *8:00 a.m.* – ***Advanced Coreless Flip-Chip BGA Package with High Dielectric Constant Thin Film Embedded Decoupling Capacitor***
GaWon Kim, SeungJae Lee, JiHeon Yu, Gyulck Jung, JinYoung Kim, Nozard Karim, HeeYeoul Yoo, and ChoonHeung Lee – Amkor Technology Korea

2. *8:25 a.m.* – ***CuBOL (Cu-Column on BOL) Technology: A Low Cost Flip Chip Solution Scalable to High I/O Density, Fine Bump Pitch and Advanced Si Nodes***
S. Movva, S. Bezuk, O. Bchir, and M. Shah – Qualcomm, Inc. M. Joshi, R. Pendse, E. Ouyang, Y.C. Kim, S.W. Park, H.T. Lee, S.S. Kim, and H.I. Bae – STATS ChipPAC, Inc.

3. *8:50 a.m.* – ***Reliability of 20μm Micro Bump Interconnects***
Ha-Young You, Yoon-Soo Lee, Sang-Keun Lee, and Ju-Seong Kang – Samsung Electronics

Session 15: Adhesives and Adhesion

Committee:
Materials & Processing

Southern Hemisphere I (5th Level)

Session Co-Chairs:
Daniel D. Lu – Henkel Corporation
Myung Jin Yim – Global Foundries

1. *8:00 a.m.* – ***Temperature Dependence of Mechanical Properties of Isotropic Conductive Adhesive Filled with Metal Coated Polymer Spheres***
Hoang-Vu Nguyen, Nils Hoivik, and Knut Aasmundtveit – HiVe-Vestfold University College; Helge Kristiansen – Conpart AS; Rolf Johannessen – GE Vingmed Ultrasound AS; Erik Andreassen – HiVe-Vestfold University College, SINTEF Materials and Chemistry; Anreas Larsson – SINTEF ICT

2. *8:25 a.m.* – ***Investigations of the Water-Borne Isotropically Conductive Adhesives***
Cheng Yang, Matthew M.F. Yuen, Guohua Chen, and Zhongyu Li – Hong Kong University of Science & Technology (HKUST); C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong

3. *8:50 a.m.* – ***Cu/Epoxy Interfacial Adhesion Improvement by Thiol-Based Self Assembled Structures of Different Chain Lengths***
Peng He and Matthew M.F. Yuen – Hong Kong University of Science & Technology (HKUST)

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Atlantic Hall B / 1st Level)

4. *10:00 a.m.* – ***Ceramics vs. Low-CTE Organic Packaging of TSV Silicon Interposers***
Bahareh Banijamali, Suresh Ramalingam, Namhoon Kim, and Chris Wyland – Xilinx, Inc.

5. *10:25 a.m.* – ***Through Silicon Via Interposer for Millimetre Wave Applications***
Teck Guan Lim, Yee Mong Khoo, Cheryl Sharmani Selvanayagam, David Soon Wee Ho, Rui Li, Xiaowu Zhang, Gao Shan, and Xiong Yong Zhong – Institute of Microelectronics, A*STAR

6. *10:50 a.m.* – ***Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package-Vias***
Vijay Sukumaran, Tapobrata Bandyopadhyay, Qiao Chen, Nitesh Kumbhat, Fuhan Liu, and Ragh Pucha – Georgia Institute of Technology; Yoichiro Sato, Mitsuru Watanabe, Kenji Kitaoka, and Motoshi Ono – Asahi Glass Inc.; Yuya Suzuki – Zeon Corporation; Choukri Karoui and Christian Nopper – STMicroelectronics

7. *11:15 a.m.* – ***A Novel Inter-Package Connection for Advanced PoP Enabling***
Bok Eng Cheah, Jackson Kong, Shanggar Periaman, and Kooi Chi Ooi – Intel Corporation

4. *10:00 a.m.* – ***Next Generation Fine Pitch Cu Pillar Technology – Enabling Next Generation Silicon Nodes***
Mark Gerber, Craig Beddingfield, and Shawn O'Connor – Texas Instruments, Inc.; Min Yoo, MinJae Lee, DaeByoung Kang, SungSu Park, Curtis Zwenger, Robert Darveaux, Robert Lanzone, and KyungRok Park – Amkor Technology

5. *10:25 a.m.* – ***Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for High End Electronics***
Rabindra N. Das, Frank D. Egitto, Barry Bonitz, Mark D. Poliks, and Voya R. Markovich – Endicott Interconnect Technologies, Inc.

6. *10:50 a.m.* – ***Glass Panel Processing for Electrical and Optical Packaging***
Henning Schröder and Lars Brusberg – Fraunhofer IZM; Norbert Arndt-Staufenbiel, Jens Hofmann, and Sebastian Marx – TU Berlin

7. *11:15 a.m.* – ***Study of the Thermo-Mechanical Behavior of Glass Interposer for Flip Chip Packaging Applications***
Y.J. Lin, C.C. Hsieh, C.H. Yu, C.H. Tung, and Doug C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

4. *10:00 a.m.* – ***Nanofiber Anisotropic Conductive Adhesives (ACAs) for Ultra Fine Pitch Chip-on-Film (COF) Packaging***
Kyoung-Lim Suk, Chang-Kyu Chung, and Kyung-Wook Paik – KAIST

5. *10:25 a.m.* – ***Kinetically Controlled Assembly of Terpheny-4,4"-dithiol Self-Assembled Monolayers (SAMs) for Highly Conductive Anisotropically Conductive Adhesives (ACA)***
Joshua C. Agar, Jessica Durden, Daniela Staiculescu, and C.P. Wong – Georgia Institute of Technology; Rongwei Zhang – Georgia Institure of Technology

6. *10:50 a.m.* – ***Enhancement of Thermal Conductivity of Die Attach Adhesives (DAAs) Using Nanomaterials for High Brightness Light-Emitting Diode (HBLED)***
Dong Lu, Chenmin Liu, Xianxin Lang, Bo Wang, Zhiying Li, and W.M. Peter Lee – Nano and Advanced Materials Institute Limited (NAMI); S.W. Ricky Lee – Hong Kong University of Science & Technology (HKUST)

7. *11:15 a.m.* – ***Development and Characterisation of Nanofiber Films with High Adhesion***
Xin Tang, Hui Wang Cui, Xiu Zhen Lu, Qiong Fan, Zhichao Yuan, and Lilei Ye – Shanghai University; Johan Liu – Shanghai University, Chalmers of University of Technology

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 16: Solder Material Characterization

Committee:
Applied Reliability

Americas Seminar (5th Level)

Session Co-Chairs:
Dongming He – Intel Corporation
Deepak Goyal – Intel Corporation

1. ***8:00 a.m. – Reliability of Mixed Alloy Ball Grid Arrays Using Impact Bend Test and Drop Shock Test***
   Ranjit Pandher, Ashok Pachamuthu, and Rahul Raut – Cookson Electronics

2. ***8:25 a.m. – High Strain-Rate Mechanical Properties of SnAgCu Leadfree Alloys***
   Pradeep Lall, Sandeep Shantaram, Mandar Kulkarni, Geeta Limaye, and Jeff Suhling – Auburn University

3. ***8:50 a.m. – Aging Aware Constitutive Models for SnAgCu Solder Alloys***
   S. Chavali, Y. Singh, and G. Subbarayan – Purdue University; P. Kumar and I. Dutta – Washington State University; D.R. Edwards – Texas Instruments

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Atlantic Hall B / 1st Level)

4. ***10:00 a.m. – Comparison of the Electromigration Behaviors between Micro-Bumps and C4 Solder Bumps***
   C.C. Wei, C.H. Yu, C.H. Tung, R.Y. Huang, C.C. Hsieh, C.C. Chiu, T.C. Yeh, Larry C. Lin, and Doug C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.; H.Y. Hsiao, Y.W. Chang, C.K. Lin, Y.C. Liang, and C. Chen – National Chiao Tung University

5. ***10:25 a.m. – Effect of Sn Grain Structure on Electromigration Reliability of Pb-Free Solders***
   Yiwei Wang, Kuan H. Lu, Jay Im, and Paul S. Ho – University of Texas, Austin; Vikas Gupta, Leon Stiborek, and Dwayne Shirley – Texas Instruments, Inc.

6. ***10:50 a.m. – Electromigration Studies of Lead-Free Solder Balls Used for Wafer-Level Packaging***
   Christine Hau-Riege, Ricky Zang, You-Wen Yau, Praveen Yadav, Beth Keser, and Jong-Kai Lin – Qualcomm

7. ***11:15 a.m. – On the Evolution of the Properties and Microstructure of Backward Compatible Solder Joints During Cycling and Aging***
   Younis Jaradat, Awni Qasaimeh, Babak Arfaei, and Peter Borgesen – State University of New York, Binghamton; Pericles Kondos – Universal Instruments Corporation

Session 17: Thermomechanical Modeling

Committee:
Modeling & Simulation

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
Andrew A. O. Tay – National University of Singapore
L. J. Ernst – Delft University of Technology

1. ***8:00 a.m. – Modeling Characterization and Reliability Analysis of a Power System in Package***
   Yumin Liu, Bill Newberry, Yong Liu, and Stephen Martin – Fairchild Semiconductor Corporation

2. ***8:25 a.m. – A New Thermomechanical Fracture Analysis Approach for 3D Integration Technology***
   Abigail Agwai, Ibrahim Guven, and Erdogan Madenci – University of Arizona

3. ***8:50 a.m. – A Fast Simulation Framework for Full-Chip Thermo-Mechanical Stress and Reliability Analysis of Through-Silicon-Via Based 3D ICs***
   Joydeep Mitra, Suk-Kyu Ryu, Rui Huang, and David Z. Pan – University of Texas, Austin; Moongon Jung and Sung Kyu Lim – Georgia Institute of Technology

4. ***10:00 a.m. – Reliability Enhancement of Wafer Level Packages with Nano-Column-Like Hollow Solder Ball Structures***
   Ronak Varia and Xuejun Fan – Lamar University

5. ***10:25 a.m. – Exploration of the Design Space of Wafer Level Packaging through Numerical Simulation***
   Zhongping Bao, James Burrell, Beth Keser, Praveen Yadav, Shantanu Kalchuri, and Ricky Zang – Qualcomm, Inc.

6. ***10:50 a.m. – Issues in Fatigue Life Prediction Model for Underfilled Flip Chip Bump***
   Nokibul Islam, Ahmer Syed, TaeKyeong Hwang, YunHyeon Ka, and WonJoon Kang – Amkor Technology

7. ***11:15 a.m. – Interrogation of Accrued Damage and Remaining Life in Field-Deployed Electronics Subjected to Multiple Thermal Environments of Thermal Aging and Thermal Cycling***
   Pradeep Lall, Mahendra Harsha, Krishan Kumar, and Jeff Suhling – Auburn University; Kai Goebel – NASA Ames Research Center; Jim Jones – Oracle

Session 18: Board Level Optical Interconnects

Committee:
Optoelectronics

Southern Hemisphere V (5th Level)

Session Co-Chairs:
Ping Zhou – LDX Optronics, Inc.
Andrew Shapiro – JPL

1. ***8:00 a.m. – Terabit/Sec-Class Board-Level Optical Interconnects through Polymer Waveguides Using 24-Channel Bidirectional Transceiver Modules***
   Fuad E. Doany, Clint L. Schow, Benjamin G. Lee, Russell Budd, Christian Baks, Roger Dangel, Richard John, Frank Libsch, and Jeffrey A. Kash – IBM T.J. Watson Research Center; Benson Chan, How Lin, and Chase Carver – Endicott Interconnect Technologies

2. ***8:25 a.m. – Cost-Effective Optical Transceiver Subassembly with Lens-Integrated High-k, Low-Tg Glass for Optical Interconnection***
   Takashi Shiraishi, Takatoshi Yagisawa, Tadashi Ikeuchi, Satoshi Ide, and Kazuhiro Tanaka – Fujitsu Laboratories, Ltd.

3. ***8:50 a.m. – Chip-to-Chip Communication by Optical Routing Inside a Thin Glass Substrate***
   Lars Brusberg, Norbert Schlepple, and Henning Schröder – Fraunhofer IZM

4. ***10:00 a.m. – Dual-Layer WDM Routing for Wafer-Scale Packaging of Photonically-Interconnected Computing Systems***
   Daniel C. Lee, Dazeng Feng, Cheng-Chih Kung, Joan Fong, and Wei Qian – Kotura, Inc.; Xuezhe Zheng, Jin Yao, Guoliang Li, Kannan Raj, John E. Cunningham, and Ashok V. Krishnamoorthy – Oracle; Mehdi Asghari – Kotura, Inc.

5. ***10:25 a.m. – High-Bandwidth Density Optical I/O for High-Speed Logic Chip on Waveguide-Integrated Organic Carrier***
   Masao Tokunari, Yutaka Tsukada, Kazushige Toriyama, Hirokazu Noma, and Shigeru Nakagawa – IBM Research

6. ***10:50 a.m. – Planar Assembled Flexible Interconnect Link with Hybrid Optical/Electrical Data Transmission for Mobile Device Applications***
   Chris Keller, Zhenhua Shao, Yoshitsugu Wakazono, Masataka Ito, and Dongdong Wang – Ibiden USA R&D, Inc.

7. ***11:15 a.m. – Hybrid Integration of Silicon Nanophotonics with 40nm-CMOS VLSI Drivers and Receivers***
   Hiren D. Thacker, Ivan Shubin, Ying Luo, Joannes Costa, Jon Lexau, Xuezhe Zheng, Guoliang Li, Jin Yao, Jieda Li, Frankie Liu, and Ron Ho – Oracle; Dinesh Patil – Rambus

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:10 p.m.

Session 19: Interposers and TSVs

Committee:
Advanced Packaging

Southern Hemisphere III (5th Level)

Session Co-Chairs:
Christopher Bower – Semprius, Inc.
Subhash L. Shinde – Sandia National Laboratory

1. *1:30 p.m.* – ***TSV Based Silicon Interposer Technology for Wafer Level Fabrication of 3D SiP Modules***
   K. Zoschke, J. Wolf, C. Lopper, I. Kuna, N. Jürgensen, V. Glaw, K. Samulewicz, M. Wilke, M. Klein, and M. von Suchodoletz – Fraunhofer IZM; J. Röder and O. Wünsch – TU Berlin

2. *1:55 p.m.* – ***Integration of Fine-Pitched Through Silicon Vias and Integrated Passive Devices***
   Dzafir Shariff, Pandi Chelvam Marimuthu, Ken Hsiao, Lily Asoy, Chia Lai Yee, and Aung Kyaw Oo – STATS ChipPAC Ltd.; Keith Buchanan, Kath Crook, Tony Wilby, and Steve Burgess – SPTS Ltd.

3. *2:20 p.m.* – ***Development of Si Interposer with Low Inductance Decoupling Capacitor***
   Akihito Takano, Masahiro Sunohara, and Mitsutoshi Higashi – Shinko Electric Industries Co., Ltd.; Ichiro Hayakawa, Ken-ichi Ohta, and Yuichi Sasajima – Taiyo Yuden Co., Ltd.

4. *3:30 p.m.* – ***Design and Demonstration of Low Cost, Panel-Based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs)***
   Qiao Chen, Tapobrata Bandyopadhyay, Fuhan Liu, Venky Sundaram, Raghuram Pucha, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology; Yuya Suzuki – Georgia Institute of Technology, Zeon Corporation

5. *3:55 p.m.* – ***Characterization of the Thermal Impact of Cu-Cu Bonds Achieved Using TSVs on Hot Spot Dissipation in 3D Stacked Ics***
   H. Oprins, V. Cherman, B. Vandevelde, M. Stucchi, G. Van der Plas, P. Marchal, and E. Beyne – IMEC; C. Torregiani – Qualcomm, Inc.

6. *4:20 p.m.* – ***A Millimeter-Wave Wideband High-Gain Antenna and Its 3D System-in-Package Solution in a TSV-Compatible Technology***
   Sanming Hu, Yong-Zhong Xiong, Lei Wang, Rui Li, and Teck Guan Lim – Institute of Microelectronics, A*STAR

7. *4:45 p.m.* – ***Realization of Virtual 126-Core System with Thermal Sensor-Network Using Metallic Thermal Skeletons***
   Jui-Hung Chien, Kun-Ju Tsai, Ting-Sheng Chen, Yung-Fa Chou, and Ding-Ming Kwai – Industrial Technology Research Institute (ITRI); Chiao-Ling Lung – Industrial Technology Research Institute (ITRI), National Tsing Hua University; Chin-Chih Hsu and Ping-Hei Chen – National Taiwan University; Shih-Chieh Chang – National Tsing Hua University

Session 20: Flip Chip

Committee:
Interconnections

Southern Hemisphere II (5th Level)

Session Co-Chairs:
Bernd Ebersberger – Intel Mobile Communications GmbH
Matthew Yao – Rockwell Collins

1. *1:30 p.m.* – ***Development of Inclined Conductive Bump (ICB) for Flip-Chip Interconnection***
   Ah-Young Park, Sun-Rak Kim, Choong D. Yoo, and Taek-Soo Kim – KAIST

2. *1:55 p.m.* – ***Failure Mechanism of 20 µm Pitch Microjoint within a Chip Stacking Architecture***
   Shin-Yi Huang, Tao-Chih Chang, Ren-Shin Cheng, Jing-Yao Chang, Chia-Wen Fan, Chau-Jie Zhan, John H. Lau, Tai-Hong Chen, Wei-Chung Lo, and Ming-Jer Kao – Industrial Technology Research Institute (ITRI)

3. *2:20 p.m.* – ***Processing and Reliability Analysis of Flip-Chips with Solder Bumps Down to 30 µm Diameter***
   Jörg Franke, Florian Schüßler, and Stefan Härter – University of Erlangen-Nuremberg; Rainer Dohle and Thomas Friedrich – Micro Systems Engineering GmbH; Thomas Oppert – Pac Tech Packaging Technologies GmbH

4. *3:30 p.m.* – ***Optimization of Interconnections Structure in the Fine Pitch FCCSP for Low-k Dielectric Reliability***
   Seunghyun Cho – Dongyang Mirae University; Youngbae Ko – Korea Institute of Industrial Technology; Seongbo Shim, Kido Chun, Hyuksoo Lee, and Woong Kim – LG Innotek Co., Ltd.

5. *3:55 p.m.* – ***Thin Gold to Gold Bonding for Flip-Chip Applications***
   Lauren E.S. Rohwer and Dahwey Chu – Sandia National Laboratories

6. *4:20 p.m.* – ***15µm Silver Flip–Chip Technology with Solid-State Bonding***
   Chu-Hsuan Sha and Chin C. Lee – University of California, Irvine

7. *4:45 p.m.* – ***Co-W As an Advanced Barrier for Intermetallics and Electromigration in Fine-Pitch Flipchip Interconnections***
   Dibyajat Mishra, P. Markondeya Raj, Sadia Khan, Nitesh Kumbhat, Yushu Wang, Suman Addya, Raghuram V. Pucha, Abhishek Choudhury, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

Session 21: Solder Joint Reliability

Committee:
Applied Reliability

Southern Hemisphere I (5th Level)

Session Co-Chairs:
Darvin R. Edwards – Texas Instruments, Inc.
Sridhar Canumalla – Microsoft Corporation

1. *1:30 p.m.* – ***Second-Level Interconnects Reliability for Large-Die Flip Chip Lead-Free BGA Package in Power Cycling and Thermal Cycling Tests***
   Larry Lin, Yu-Ling Tsai, Tulip Chou, Ray Su, Gary Lu, Max K.C. Wu, H.Y. Pan, H.P. Pu, Roger Hsieh, and Kenneth Wu – Taiwan Semiconductor Manufacturing Company, Ltd.

2. *1:55 p.m.* – ***The Effects of Aging on the Cyclic Stress-Strain Behavior and Hysteresis Loop Evolution of Lead Free Solders***
   Muhannad Mustafa, Zijie Cai, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

3. *2:20 p.m.* – ***Crack Initiation and Growth in WLCSP Solder Joints***
   Robert Darveaux, Sabira Enayet, Corey Reichman, Christopher J. Berry, and Nabeel Zafar – Amkor Technology, Inc.

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Atlantic Hall B / 1st Level)

4. *3:30 p.m.* – ***Thermal Cycling Reliability, Microstructural Characterization, and Assembly Challenges with Backward Compatible Soldering of a Large, High Density Ball Grid Array***
   Vasu Vasudevan, Raiyo Aspandiar, Steve Tisdale, and Gary Long – Intel Corporation; Richard Coyle – Alcatel-Lucent; Robert Kinyanjui – Sanmina-SCI Corporation

5. *3:55 p.m.* – ***Reliability of Cu Pillar on Substrate Interconnects in High Performance Flip Chip Packages***
   Rajesh Katkar, Michael Huynh, and Laura Mirkarimi – Tessera

6. *4:20 p.m.* – ***Effect of Interfacial Strength between Cu6Sn5 and Cu3Sn Intermetallics on the Brittle Fracture Failure of Lead-Free Solder Joints with OSP Pad Finish***
   Chaoran Yang, Fubin Song, and S.W. Ricky Lee – Hong Kong University of Science & Technology (HKUST)

7. *4:45 p.m.* – ***Effects of Multiple Rework on the Reliability of Lead-Free Ball Grid Array Assemblies***
   Hongtao Ma, Weidong Xie, Guhan Subbarayan, and Kuo-Chuan Liu – Cisco Systems, Inc.

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:10 p.m.

Session 22: Manufacturing Challenges of Wafer Thinning and Flip Chip Processing

Committee:
Assembly & Manufacturing Technology

Americas Seminar (5th Level)

Session Co-Chairs:
Paul Houston – Engent
Sylvain Ouimet – IBM Corporation

1. *1:30 p.m.* – ***Processing of Ultrathin 300 mm Wafers with Carrierless Technology***
Sven Spiller and Froilan Molina – Doublecheck Semiconductors; Jürgen M. Wolf, Jürgen Grafe, and Andreas Schenke – Fraunhofer IZM; Dietrich Toennies and Marc Hennemeyer – Suss MicroTec; Tomotaka Tabuchi – Disco HiTech Europe GmbH; Hans Auer – OC Oerlikon Balzers Ltd.

2. *1:55 p.m.* – ***How to Select Adhesive Materials for Temporary Bonding and De-Bonding of 200mm and 300mm Thin-Wafer Handling in 3D IC Integration?***
W.L. Tsai, H.H. Chang, C.H. Chien, J.H. Lau, H.C. Fu, C.W. Chiang, T.Y. Kuo, Y.H. Chen, R. Lo, and M.J. Kao – Industrial Technology Research Institute (ITRI)

3. *2:20 p.m.* – ***Metrology and Inspection for Process Control During Bonding and Thinning of Stacked Wafers for Manufacturing 3D SIC's***
Sandip Halder, Anne Jourdain, Martine Claes, Ingrid de Wolf, Youssef Travaly, Eric Beyne, and Bart Swinnen – IMEC; Valery Pepper, Pierre-Yves Guittet, Greg Savage, and Lars Markwort – Nanda Tech Gmbh

4. *3:30 p.m.* – ***Vacuum Underfill Technology for Advanced Packaging***
A. Horibe, M.-C. Paquet, M. Gaynes, C. Feger, K. Sakuma, J.U. Knickerbocker, and Y. Orii – IBM Corporation; M. Hoshiyama, M. Hasegawa, T. Sato, H. Yoshii, K. Kotaka, T. Nagasaka, and O. Suzuki – Namics Corporation; K. Terada, K. Ishikawa, Y. Hirayama – Toray-Engineering Corporation

5. *3:55 p.m.* – ***Self-Aligned Positioning Technology to Connect Ultra-Small RFID Powder-Chip to an Antenna***
Hideyuki Noda, Mitsuo Usami, and Akira Sato – Hitachi, Ltd.; Satoshi Terasaki and Hironori Ishizaka – Hitachi Chemical Co., Ltd.

6. *4:20 p.m.* – ***Development of Wafer Level Underfill Materials and Assembly Processes for Fine Pitch Pb-Free Solder Flip Chip Packaging***
Jae-Woong Nah, Michael A. Gaynes, and Claudius Feger – IBM T.J. Watson Research Center; Satoru Katsurayama and Hiroshi Suzuki – Sumitomo Bakelite Co. Ltd.

7. *4:45 p.m.* – ***A Manufacturing Approach to Reducing Underfill Voiding on Large Die (> 18 mm) Flip Chip Organic Laminate Packaging***
Isabel de Sousa, Luc Bélanger, Catherine Dufort, and Simon D.L. Chénier – IBM Canada

Session 23: Components: RF and Bio Applications

Committee:
Electronic Components & RF

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
Craig Gaw – Freescale Semiconductor, Inc.
Albert F. Puttlitz – Mechanical Eng. Consultant

1. *1:30 p.m.* – ***Graphene Based RF/Microwave Impedance Sensing of DNA***
I. Iramnaaz, Y. Xing, K. Xue, and Y. Zhuang – Wright State University; R. Fitch – Air Force Research Laboratory

2. *1:55 p.m.* – ***Design and Test of Wide-Band Terahertz Dielectric Sub-Wavelength Focusing Probes***
Jose A. Hejase, Brian Schulte, and Prem Chahal – Michigan State University

3. *2:20 p.m.* – ***Compact Self-Packaged Active Folded Patch Antenna with Omni-Directional Radiation Pattern***
Xiaoyu Cheng, Jun Shi, Jungkwun Kim, Cheolbok Kim, David E. Senior, and Yong-Kyu Yoon – University of Florida

4. *3:30 p.m.* – ***On-Chip High Performance Slow Wave Transmission Lines Using 3D Steps for Compact Millimeter Wave Applications***
Guoan Wang, Wayne Woods, Jason Xu, and Essam Mina – IBM Corporation

5. *3:55 p.m.* – ***New Microstrip-to-CPS Transition for Millimeter-Wave Application***
Kyu Hwan Han, Benjamin Lacroix, John Papapolymerou, and Madhavan Swaminathan – Georgia Institute of Technology

6. *4:20 p.m.* – ***Temperature Dependence of SiC Thin Film Metal-Insulator-Metal (MIM) Capacitors on Alumina over a Temperature Range from 25 to 500°C***
Maximilian C. Scardelletti, George E. Ponchak, Jennifer L. Jordan, Nicholas C. Varaljay, and Elizabeth A. McQuaid – NASA Glenn Research Center; Christian A. Zorman – Case Western Reserve University

7. *4:45 p.m.* – ***The Design of Broadband 3D Si-Based Directional Couplers for Millimeter-Wave/THz Applications***
Jiankang Li – Nanjing University of Science and Technology, Instiute of Microelectronics, A*STAR, Nanyang Technological University; Yong-Zhong Xiong, Debin Hou, Teck Guan Lim, and Tang Min – Instiute of Microelectronics, A*STAR; Wang Lin Goh – Nanyang University of Science and Technology

Session 24: Fracture and Warpage in Packages

Committee:
Modeling & Simulation

Southern Hemisphere V (5th Level)

Session Co-Chairs:
Xuejun Fan – Lamar University
Yong Liu – Fairchild Semiconductor Corporation

1. *1:30 p.m.* – ***Considerations in Solution Stabilization for Thermal Fatigue Modeling of Lead-Free Solder Joints***
Y. Sing Chan and S.W. Ricky Lee – Hong Kong University of Science & Technology (HKUST)

2. *1:55 p.m.* – ***Experimental Contact Angle Determination and Characterisation of Interfacial Energies by Molecular Modelling of Chip to Epoxy Interfaces***
O. Hölck – Fraunhofer IZM, Chemnitz University of Technology; J. Bauer and O. Wittler – Fraunhofer IZM; K.D. Lang – TU Berlin; B. Michel – Fraunhofer ENAS; B. Wunderle – Fraunhofer IZM, Fraunhofer ENAS, Chemnitz University of Technology

3. *2:20 p.m.* – ***Quantification of the Leadframe Roughness Effect on Adhesion Properties***
S.P.M. Noijen – Philips Research, Delft University of Technology; O. van der Sluis and P.H.M. Timmermans – Philips Research; G.Q. Zhang – Delft University of Technology

4. *3:30 p.m.* – ***Establishing the Critical Fracture Properties of the Die Backside-to-Molding Compound Interface***
G. Schlottig – Delft University of Technology, Infineon Technologies AG, Fraunhofer IZM; H. Pape – Infineon Technologies AG; B. Wunderle – Fraunhofer IZM, Chemnitz University of Technology, Fraunhofer ENAS; L.J. Ernst – Delft University of Technology

5. *3:55 p.m.* – ***Particle Filter Models and Phase Sensitive Detection for Prognostication and Health Monitoring of Leadfree Electronics under Shock and Vibration***
Pradeep Lall and Ryan Lowe – Auburn University; Kai Goebel – NASA Ames Research Center

6. *4:20 p.m.* – ***Modeling of Separation Behavior of Epoxy/Cu Interface Using Molecular Dynamics Simulation***
Shaorui Yang, Feng Gao, and Jianmin Qu – Northwestern University

7. *4:45 p.m.* – ***A Numerical Analysis of Penny-Shaped Delaminations in an Encapsulated Silicon Module***
Siow Ling Ho and Andrew A.O. Tay – National University of Singapore

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Atlantic Hall B / 1st Level)

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 25: Manufacturing Aspects of 3D/TSV

Committee: Assembly & Manufacturing Technology

Southern Hemisphere III (5th Level)

Session Co-Chairs:
Andy Tseng – Advanced Semiconductor Engineering, Inc.
Sharad Bhatt – Shanta Systems, Inc.

1. *8:00 a.m.* – ***Integration of TSVs, Wafer Thinning and Backside Passivation on Full 300mm CMOS Wafers for 3D Applications***
   Anne Jourdain, Thibault Buisson, Alain Phommahaxay, Augusto Redolfi, Sarasvathi Thangaraju, Youssef Travaly, Eric Beyne, and Bart Swinnen – IMEC

2. *8:25 a.m.* – ***A Study on the 3D-TSV Interconnection Using Wafer-Level Non-Conductive Adhesives(NCAs)***
   Yongwon Choi, Jiwon Shin, and Kyung-Wook Paik – KAIST

3. *8:50 a.m.* – ***Effects of Etch Rate on Scallop of Through-Silicon Vias (TSVs) in 200mm and 300mm Wafers***
   Yu-Chen Hsin, Chien-Chou Chen, John H. Lau, Pei-Jer Tzeng, Shang-Hung Shen, Yi-Feng Hsu, Shang-Chun Chen, Chien-Ying Wn, Jui-Chin Chen, Tzu-Kun Ku, and Ming-Jer Kao – Industrial Technology Research Institute (ITRI)

Refreshment Break: 9:15 a.m. - 10:00 a.m. (Southern Hemisphere Ballroom Foyer / 5th Level)

4. *10:00 a.m.* – ***Development on Ultra High Density Memory Package with PoP Structure***
   Ji Cheng Lin, Jeter Yu, Brian Chung, Ken Chang, and David Fang – Powertech Technology Inc.

5. *10:25 a.m.* – ***Ultra Thin POP Top Package Using Compression Mold: Its Warpage Control***
   Myung Jin Yim, Richard Strode, Jason Brand, Ravikumar Adimula, James Jian Zhang, and Chan Yoo – Micron Technology

6. *10:50 a.m.* – ***Solder/Adhesive Bonding Using Simple Planarization Technique for 3D Integration***
   Masatsugu Nimura, Jun Mizuno, and Shuichi Shoji – Waseda University; Katsuyuki Sakuma – IBM Research-Tokyo

7. *11:15 a.m.* – ***Surface-Tension-Driven Multi-Chip Self-Alignment Techniques for Heterogeneous 3D Integration***
   Fengda Sun and Yusuf Leblebici – École Polytechnique Fédérale de Lausanne; Thomas Brunschwiler – IBM Research–Zurich

Session 26: TSV Design and Modeling

Committees: Interconnections / Modeling & Simulation

Southern Hemisphere II (5th Level)

Session Co-Chairs:
James Lu – Rensselaer Polytechnic Institute
Pradeep Lall – Auburn University

1. *8:00 a.m.* – ***Interposer Design Optimization for High Frequency Signal Transmission in Passive and Active Interposer Using Through Silicon Via (TSV)***
   Namhoon Kim, Daniel Wu, Dongwook Kim, Arif Rahman, and Paul Wu – Xilinx, Inc.

2. *8:25 a.m.* – ***3-D Copper Based TSV for 60-GHz Applications***
   Sukeshwar Kannan, Sai Shravan Evana, Anurag Gupta, and Bruce Kim – University of Alabama; Li Li – Cisco Systems, Inc.

3. *8:50 a.m.* – ***Electrical Characterization and Impact on Signal Integrity of New Basic Interconnection Elements Inside 3D Integrated Circuits***
   J. Roullard, S. Capraro, T. Lacrevaz, C. Bermond, and B. Flechet – University of Savoie; A. Farcy – STMicroelectronics; P. Leduc, J. Charbonnier, C. Ferrandon, and C. Fuchs – CEA-LETI-MINATEC

4. *10:00 a.m.* – ***Expert Advisor for Integrated Virtual Manufacturing and Reliability for TSV/SiP Based Modules***
   Zhaohui Chen and Shengiun Zhou – Shanghai Jiao Tong University; Zhicheng Lv, Chuan Liu, Xing Chen, Xiao Jia, Ke Zeng, Bin Song, Fulong Zhu, Mingxiang Chen, Xuefang Wang, and Honghai Zhang – Huazhong University of Science & Technology (HUST)

5. *10:25 a.m.* – ***Thermo-Mechanical Behavior of Through Silicon Vias in a 3D Integrated Package with Inter-Chip Microbumps***
   Xi Liu, Qiao Chen, Venkatesh Sundaram, Rao R. Tummala, and Suresh K. Sitaraman – Georgia Institute of Technology; Margaret Simmons-Matthews and Kurt P. Wachtler – Texas Instruments

6. *10:50 a.m.* – ***Wafer Level Warpage Modeling Methodology and Characterization of TSV Wafers***
   F.X. Che, H.Y. Li, Xiaowu Zhang, S. Gao, and K.H. Teo – Institute of Microelectronics, A*STAR

7. *11:15 a.m.* – ***A Thermal Performance Measurement Method for Blind Through Silicon Vias (TSVs) in a 300mm Wafer***
   Heng-Chieh Chien, Yu-Lin Chao, John H. Lau, Ra-Min Tain, Ming-Ji Dai, Pei-Jer Tzeng, Cha-Hsin Lin, Yu-Chen Hsin, Shang-Chun Chen, Jui-Chin Chen, Chein-Chou Chen, and Chi-Hon Ho – Industrial Technology Research Institute (ITRI)

Session 27: Novel Materials and Processing

Committee: Materials & Processing

Southern Hemisphere I (5th Level)

Session Co-Chairs:
Rajen Chanchani – Sandia National Laboratory
Tieyu Zheng – Intel Corporation

1. *8:00 a.m.* – ***Aerosol Jet Printing on Rapid Prototyping Materials for Fine Pitch Electronic Applications***
   Christian Goth, Sonja Putzo, and Joerg Franke – University of Erlangen-Nuremberg

2. *8:25 a.m.* – ***Gravure Printed Hydrophobic Templates onto PET Films for Guiding the Assembly of Nanowires: Towards the Ultralow-Cost Transparent Conductive Electrodes***
   Wayman N.M. Wong, Cheng Yang, and Matthew M.F. Yuen – Hong Kong University of Science and Technology (HKUST)

3. *8:50 a.m.* – ***A Novel Micromachined Loudspeaker Topology***
   F. Neri – ST-Ericsson; F. Di Fazio, R. Crescenzi, and M. Balucani – Sapienza University of Rome

4. *10:00 a.m.* – ***Nano and Micro Materials in a Pb-Free World***
   Rabindra N. Das, John M. Lauffer, Kevin Knadle, Michael Vincent, Mark D. Poliks, and Voya R. Markovich – Endicott Interconnect Technologies, Inc.

5. *10:25 a.m.* – ***Carbon Metal Composite Film Deposited Using Novel Filtered Cathodic Vacuum Arc Technique***
   Nai Yun Xu, Hang Tong Teo, and Beng Kang Tay – Nanyang Technological University; Xin Cai Wang – Singapore Institute of Manufacturing Technology (SIMTech); An Yan Du and Chee Mang Ng – Global Foundries Singapore Pte. Ltd.

6. *10:50 a.m.* – ***Synthesis of High-Quality, Closely-Packed, Vertically-Aligned Carbon Nanotube Array and a Quantitative Study of the Influence of Packing Density on the Collective Thermal Conductivity***
   Wentian Gu, Wei Lin, and Yagang Yao – Georgia Institute of Technology; Chingping Wong – Georgia Institute of Technology, Chinese University of Hong Kong

7. *11:15 a.m.* – ***Novel Nanomagnetic Materials for High-Frequency RF Applications***
   P. Markondeya Raj, Himani Sharma, G. Prashant Reddy, Nevin Altunyurt, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology; David Reid – Georgia Tech Research Insitute; Vijay Nair – Intel Corporation

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 28: Characterization Methods of Interfaces and Interconnections

Committee:
Applied Reliability

Americas Seminar (5th Level)

Session Co-Chairs:
Lakshmi N. Ramanathan – Microsoft Corporation
Dongji Xie – nVidia Corp

1. *8:00 a.m.* – ***Drop Reliability of Glass Panel for LCD***
   Soon-Wan Chung, Jae-Woo Jeong, Seunghee Oh, Young-Jun Moon, In-Youl Baek, and Dong-Sool Hong – Samsung Electronics Company, Ltd.

2. *8:25 a.m.* – ***Method for Early Detection of PCB Bending Induced Pad Cratering***
   Anurag Bansal, Gnyaneshwar Ramakrishna, and Kuo-Chuan Liu – Cisco Systems, Inc.

3. *8:50 a.m.* – ***Detection and Characterization of Defects in Microelectronic Packages and Boards by Means of High-Resolution X-Ray Computed Tomography (CT)***
   Mario Pacheco and Deepak Goyal – Intel Corporation

Refreshment Break: 9:15 a.m. - 10:00 a.m. (Southern Hemisphere Ballroom Foyer / 5th Level)

4. *10:00 a.m.* – ***Delamination Prediction in Lead Frame Packages Using Adhesion Measurements and Interfacial Fracture Modeling***
   Venkat Srinivasan, Mikel Miller, Siva Gurrum, Jie-Hua Zhao, Darvin Edwards, and Masood Murtuza – Texas Instruments, Inc.

5. *10:25 a.m.* – ***Application of Piezoresistive Stress Sensor in Wafer Bumping and Drop Impact Test of Embedded Ultra Thin Device***
   Xiaowu Zhang, Ranjan Rajoo, Cheryl S Selvanayagam, Aditya Kumar, Srinivasa Rao Vempati, Navas Khan, V. Kripesh, John H. Lau, and D.-L. Kwong – Institute of Microelectronics, A*STAR; V. Sundaram and Rao R. Tummula – Georgia Institute of Technology

6. *10:50 a.m.* – ***Crack Evolution and Rapid Life Assessment for Lead Free Solder Joints***
   Awni Qasaimeh, Susan Lu, and Peter Borgesen – State University of New York, Binghamton

7. *11:15 a.m.* – ***Knowledge-Based Reliability Qualification and an Acceleration Model for Lead-Free Solder Joint***
   Yuchul Hwang, Hwan-Ki Jeon, Young-Gyun Ryu, and Juseong Kang – Samsung Electronics Company, Ltd.

Session 29: Biosensing and Packaging

Committee:
Emerging Technologies

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
Bernd Appelt – ASE Group
Allison Xiao – Henkel Corporation

1. *8:00 a.m.* – ***Acoustic Impediography: Imaging Surface Acoustic Impedance Using 1-3 Piezo-Composite for Integrated Fingerprinting***
   Rainer M. Schmitt and Justin Owen – Sonavation Inc.

2. *8:25 a.m.* – ***Silicon Micro Heater Based Tagging Module and the Biocompatible Packaging for Capsule Endoscope***
   Ruiqi Lim, Jayakrishnan Chandrappan, Kripesh Vaidyanathan, and Sin Win Shwe – Institute of Microelectronics, A*STAR

3. *8:50 a.m.* – ***High-Density Electrical Interconnections in Liquid Crystal Polymer (LCP) Substrates for Retinal and Neural Prosthesis Applications***
   Venky Sundaram, Vijay Sukumaran, Michael E. Cato, Fuhan Liu, and Rao Tummala – Georgia Institute of Technology; Patrick J. Nasiatka, James D. Weiland, and Armand R. Tanguay, Jr. – University of Southern California

4. *10:00 a.m.* – ***Multiphoton Angiogenesis and Tumor Biomarker Imaging***
   Kevin D. Belfield – University of Central Florida

5. *10:25 a.m.* – ***Technology and Design of Innovative Flexible Electrode for Biomedical Applications***
   M. Balucani, P. Nenzi, C. Crescenzi, P. Marracino, F. Apollonio, M. Liberti, A. Densi, and C. Colizzi – Sapienza University of Rome

6. *10:50 a.m.* – ***Embedded Discrete Passives Technology for Bandage-Type Medical Sensors of E-Healthcare System***
   Baik-Woo Lee, Seong Woon Booh, and Kunsoo Shin – Samsung Advanced Institute of Technology

7. *11:15 a.m.* – ***RFDNA: A Wireless Authentication System On Flexible Substrates***
   Gerald DeJean and Darko Kirovski – Microsoft Corporation; Vasileios Lakafosis, Anya Traille, Hoseon Lee, Edward Gebara, and Manos Tentzeris – Georgia Institute of Technology

Session 30: Embedded GHz Systems Packaging

Committee:
Electronic Components & RF

Southern Hemisphere V (5th Level)

Session Co-Chairs:
Nanju Na – IBM Corporation
Amit P. Agrawal – Cisco Systems, Inc.

1. *8:00 a.m.* – ***Packaging of Ka-Band Patch Antenna and Optoelectronic Components for Dual-Mode Indoor Wireless Communication***
   Jun Liao, Pengfei Wu, and Z. Rena Huang – Rensselaer Polytechnic Institute; Ali Mirvakili and Valencia Joyner – Tufts University

2. *8:25 a.m.* – ***Design of a Miniaturized Single Package Radio Solution for Dual Band Wi-MAX Module***
   Arun Chandra Kundu, Yasser Hussein, Pouya Talebbeydokhti, and Mohamed Megahed – Intel Corporation

3. *8:50 a.m.* – ***Design Study of Electronically Steerable Half-Width Microstrip Leaky Wave Antennas***
   Jose A. Hejase, Joshua Myers, Leo Kempel, and Prem Chahal – Michigan State University

4. *10:00 a.m.* – ***A Novel Compact Antenna with a Low Profile Demonstrated on Embedded Wafer Level Packaging (EMWLP) Technology***
   Ying Ying Lim, Soon Wee David Ho, Ser Choong Chong, Ei Pa Pa Myo, and Teck Guan Lim – Institute of Microelectronics, A*STAR

5. *10:25 a.m.* – ***High-Q Embedded Inductors in Fan-Out eWLB for 6 GHz CMOS VCO***
   M. Wojnowski, V. Issakov, G. Knoblinger, K. Pressel, and G. Sommer – Infineon Technologies AG; R. Weigel – University of Erlangen-Nuremberg

6. *10:50 a.m.* – ***Ultra-Miniaturized WLAN RF Receiver with Chip-Last GaAs Embedded Active***
   Vivek Sridharan, Abhilash Goyal, Srikrishna Sitaraman, Nitesh Kumbhat, Nithya Sankaran, Hunter Chan, Fuhan Liu, Debasis Dawn, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Vijay Nair and Telesphor Kamgaing – Intel Corporation; Frank Juskey – TriQuint Semiconductor

7. *11:15 a.m.* – ***Warpage and Electrical Performance of Embedded Device Package, MCeP***
   Kouichi Tanaka, Nobuyuki Kurashima, Hajime Iizuka, Kiyoshi Ooi, Yoshihiro Machida, and Tetsuya Koyama – Shinko Electric Industries Co., Ltd.

Program Sessions: Friday, June 3, 1:30 p.m. - 5:10 p.m.

Session 31: Emerging Materials and Processing for 3D

Committees: Materials & Processing / Emerging Technologies

Southern Hemisphere III (5th Level)

Session Co-Chairs:
Bing Dang – IBM Corporation
Rabindra Das – Endicott Interconect Technologies

1. ***1:30 p.m. – Implementation of an Industry Compliant, 5x50µm, Via-Middle TSV Technology on 30 mm Wafers***
A. Redolfi, D. Velenis, S. Thangaraju, P. Nolmans, P. Jaenen, M. Kostermans, U. Baier, E. Van Besien, H. Dekkers, T. Witters, N. Jourdan, and A. Van Ammel – IMEC

2. ***1:55 p.m. – Impact of Slurry in Cu CMP (Chemical Mechanical Polishing) on Cu Topography of Through Silicon Vias (TSVs), Re-Distributed Layers, and Cu Exposure***
J.C. Chen, P.J. Tzeng, S.C. Chen, C.Y. Wu, C.C. Chen, Y.C. Hsin, J.H. Lau, Y.F. Hsu, S.H. Shen, S.C. Liao, C.H. Ho, and C.H. Lin – Industrial Technology Research Institute (ITRI)

3. ***2:20 p.m. – Novel Thinning/Backside Passivation for Substrate Coupling Depression of 3D IC***
Woonseong Kwon, Jaesik Lee, Vincent Lee, Justin Seetoh, Yenchen Yeo, YeeMong Khoo, Nagarajan Ranganathan, Keng Hwa Teo, and Shan Gao – Institute of Microelectronics, A*STAR

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Southern Hemisphere Ballroom Foyer / 5th Level)

4. ***3:30 p.m. – A 10µm Pitch Interconnection Technology Using Micro Tube Insertion into Al-Cu for 3D Applications***
B. Goubault de Brugière, F. Marion, M. Fendler, V. Mandrillon, M. Volpert, and H. Ribot – CEA-LETI-MINATEC; A. Hazotte – Université Paul-Verlaine

5. ***3:55 p.m. – Cost-Effective Lithography for TSV-Structures***
Uwe Vogler and Reinhard Völkel – SUSS MicroOptics SA; Frank Windrich, Andreas Schenke, and Matthias Böttcher – Fraunhofer IZM; Ralph Zoberbier – SUSS MicroTec GmbH

6. ***4:20 p.m. – Embedded 3D BioMEMS for Multiplexed Label Free Detection***
Arvind Sai Sarathi Vasan, Ravi Doraiswami, and Michael Pecht – University of Maryland

7. ***4:45 p.m. – Modeling of Electromigration in Through-Silicon-Via Based 3D IC***
Jiwoo Pak and David Z. Pan – University of Texas, Austin; Mohit Pathak and Sung Kyu Lim – Georgia Institute of Technology

Session 32: 3D Package Reliability

Committee: Applied Reliability

Southern Hemisphere II (5th Level)

Session Co-Chairs:
Keith Newman – Oracle
Scott Savage – Medtronic Microelectronics Center

1. ***1:30 p.m. – Design and Reliability Analysis of Pyramidal Shape 3-Layer Stacked TSV Die Package***
F.X. Che, T.C. Chai, Sharon P.S. Lim, Ranjan Rajoo, and Xiaowu Zhang – Institute of Microelectronics, A*STAR

2. ***1:55 p.m. – Interfacial Reliability and Micropartial Stress Analysis between TSV and CPB through NIT and MSA***
Gyujei Lee, Yu-hwan Kim, Suk-woo Jeon, and Kwang-yoo Byun – Hynix Semiconductor, Inc.; Dongil Kwon – Seoul National University

3. ***2:20 p.m. – Electro- and Thermomigration in Micro Bump Interconnects for 3D Integration***
L. Meinshausen and K. Weide-Zaage – Leibniz University; M. Petzold – Fraunhofer IWM

4. ***3:30 p.m. – Characterization and Failure Analysis of TSV Interconnects: From Non-Destructive Defect Localization to Material Analysis with Nanometer Resolution***
M. Krause, F. Altmann, C. Schmidt, and M. Petzold – Fraunhofer IWM; D. Malta and D. Temple – RTI International

5. ***3:55 p.m. – Fracture-Mechanical Interface Characterisation for Thermo-Mechanical Co-Design – an Efficient and Comprehensive Method for Critical Mixed-Mode Data Extraction***
B. Wunderle – Chemnitz University of Technology, Fraunhofer ENAS, Fraunhofer IZM; M Schulz – Chemnitz University of Technology, Angewandte Micro-Messtechnik GmbH,; J. Keller – Angewandte Micro-Messtechnik GmbH,; G. Schlottig and H. Pape – Infineon Technologies AG; I Maus – Infineon Technologies AG, Fraunhofer ENAS; D. May and O. Hölck– Chemnitz University of Technology, Fraunhofer IZM; B. Michel– Fraunhofer ENAS

6. ***4:20 p.m. – Characterization and Reliability Assessment of Solder Microbumps and Assembly for 3D IC Integration***
Ching Kuan Lee, Tao-Chih Chang, Yu-Jiau Huang, Huan-Chun Fu, Jui-Hsiung Huang, Zhi-Cheng Hsiao, John H. Lau, Cheng-Ta Ko, Ren-Shin Cheng, Pei-Chen Chang, Kuo-Shu Kao, and Yu-Lan Lu – Industrial Technology Research Institute (ITRI)

7. ***4:45 p.m. – Temperature-Dependent Thermal Stress Determination for Through-Silicon-Vias (TSVs) by Combining Bending Beam Technique with Finite Element Analysis***
Kuan H. Lu, Suk-Kyu Ryu, Qiu Zhao, Jay Im, Rui Huang, and Paul S. Ho – University of Texas, Austin; Klaus Hummler – siXis Inc.

Session 33: Advanced Wirebonds

Committee: Interconnections

Southern Hemisphere I (5th Level)

Session Co-Chairs:
William Chen – ASE-US, Inc.
Prema Palaniappan – Texas Instruments, Inc.

1. ***1:30 p.m. – Growth of CuAl Intermetallic Compounds in Cu and Cu(Pd) Wire Bonding***
Y.H. Lu, Y.W. Wang, and C.R. Kao – National Taiwan University; B.K. Appelt and Y.S. Lai – Advanced Semiconductor Engineering, Inc.

2. ***1:55 p.m. – Wire Bonding of Cu and Pd Coated Cu Wire: Bondability, Reliability, and IMC Formation***
Ivy Qin, Horst Clauberg, Ray Cathcart, Bob Chylak, and Cuong Huynh – Kulicke and Soffa Industries, Inc.; Hui Xu and Viola L. Acoff – University of Alabama

3. ***2:20 p.m. – Over Pad Metallization for High Temperature Interconnections***
S. Qu, S. Athavale, A. Prabhu, A. Xu, L. Nguyen, A. Poddar, C.S. Lee, Y.C. How, and K.C. Ooi – National Semiconductor

4. ***3:30 p.m. – Die to Die Copper Wire Bonding Enabling Low Cost 3D Packaging***
Flynn Carson, Hun Teak Lee, Jae Hak Yee, Jeffrey Punzalan, and Edward Fontanilla – STATS ChipPAC

5. ***3:55 p.m. – Copper Wire Bonding on Low-k/ Copper Wafers with Bond Over Active (BOA) Structures for Automotive Customers***
Tu Anh Tran, Chu-Chung (Stephen) Lee, Varughese Mathew, and Leo Higgins – Freescale Semiconductor Inc.

6. ***4:20 p.m. – Free-Air Ball Formation and Deformability with Pd Coated Cu Wire***
A. Rezvani, M. Mayer, A. Shah, and N. Zhou – University of Waterloo; S.J. Hong and J.T. Moon – MK Electron Company Ltd.

7. ***4:45 p.m. – Effect of Heat Affected Zone on the Mechanical Properties of Copper Bonding Wire***
Dong Liu, Haibin Chen, and Jingshen Wu – Hong Kong University of Science & Technology (HKUST); Fei Wong, Kan Lee, and Ivan Shiu – NXP Semiconductors Hong Kong Ltd.

Program Sessions: Friday, June 3, 1:30 p.m. - 5:10 p.m.

Session 34: Novel Packaging Technologies

Committee:
Advanced Packaging

Americas Seminar (5th Level)

Session Co-Chairs:
Raj N. Master – Microsoft Corporation
Paul M. Harvey – IBM Corporation

1. *1:30 p.m.* – ***Package-Die Co-Optimization for Improved Performance and Lower Cost: A 32nm 10-Core Xeon CPU Case Study***
Srikanth Balasubramanian and David Ayers – Intel Corporation; Arun Chandrasekhar, Surya Prekke, Bhunesh Kshatri, and Srikrishnan Venkataraman – Intel India

2. *1:55 p.m.* – ***A Highly Reliable Measurement of Thermal Transport Properties of Vertically Aligned Carbon Nanotube Arrays***
Wei Lin – Georgia Institute of Technology; C.P. Wong – Chinese University of Hong Kong

3. *2:20 p.m.* – ***Si Microchannel Cooler Integrated with High Power Amplifiers for Base Station of Mobile Communication Systems***
Yoshihiro Mizuno, Ikuo Soga, Shinichi Hirose, Osamu Tsuboi, and Taisuke Iwai – Fujitsu Laboratories, Ltd.

4. *3:30 p.m.* – ***A Study on an Ultra Thin PoP Using Through Mold Via Technology***
Akito Yoshida, Shengmin Wen, and Wei Lin – Amkor Technology, Inc.; Jae Yun Kim – Amkor Technology, Korea; Kazuo Ishibashi – Nokia Japan Company, Ltd.

5. *3:55 p.m.* – ***Novel Low Temperature Hermetic Sealing of Micropackages***
Thomas F. Marinis and Joseph W. Soucy – Charles Stark Draper Laboratory

6. *4:20 p.m.* – ***Millimeter-Wave Multichip BGA Package for InP Circuits Utilizing a Laminated Ceramic and Organic Substrate***
Donald Schott – Agilent Technologies, Inc.

7. *4:45 p.m.* – ***Through Silicone Vias: Multilayer Interconnects for Stretchable Electronics***
Joshua C. Agar, Jessica Durden, Rongwei Zhang, Daniela Staiculescu, and C.P. Wong – Georgia Institute of Technology

Session 35: Microfluidics and MEMs

Committees: Advanced Packaging / Emerging Technologies

Southern Hemisphere IV (5th Level)

Session Co-Chairs:
James Jian Zhang – Micron Technology, Inc.
Nancy Stoffel – Infotonics Technology Center

1. *1:30 p.m.* – ***Polymer Opto-Electronic-Fluidic Detection Module on Plastic Film Substrates***
Anna Ohlander, Markus Burghart, Christof Strohhöfer, Dieter Bollmann, Christof Landesberger, and Gerhard Klink – Fraunhofer EMFT; Karlheinz Bock – Fraunhofer EMFT, University of Berlin

2. *1:55 p.m.* – ***Microfluidic Printed Circuit Boards***
Liang Li Wu, Sarkis Babikian, Guann-Pyng Li, and Mark Bachman – University of California, Irvine

3. *2:20 p.m.* – ***Stretchable Microfluidic Electric Circuit Applied for Radio Frequency Antenna***
Masahiro Kubo – NEC Corporation; Xiaofeng Li, Choongik Kim, Michinao Hashimoto, Benjamin J. Wiley, Donhee Ham, and George M. Whitesides – Harvard University

4. *3:30 p.m.* – ***Zero-Level Packaging for (RF-) MEMS Implementing TSVs and Metal Bonding***
Nga P. Pham, Vladimir Cherman, Bart Vandevelde, Paresh Limaye, Nina Tutunjyan, Roelof Jansen, Nele Van Hoovels, Deniz S. Tezcan, Philippe Soussan, Eric Beyne, and Harrie A.C Tilmans – IMEC

5. *3:55 p.m.* – ***Applications on MEMS Packaging and Micro-Reactors Using Wafer-Level Glass Cavities by a Low-Cost Glass Blowing Method***
Jintang Shang, Boyin Chen, Di Zhang, and Chao Xu – Southeast University; Wei Lin and Ching-Ping Wong – Georgia Institute of Technology

6. *4:20 p.m.* – ***A New Wafer-Level Packaging Technology for MEMS with Hermetic Micro-Environment***
Rajen Chanchani, Christopher D. Nordquist, Roy H. Olsson III, Tracy Peterson, Randy Shul, Catalina Ahlers, Thomas A. Plut, and Gary A. Patrizi – Sandia National Labs

7. *4:45 p.m.* – ***Gold-Tin Bonding for 200mm Wafer Level Hermetic MEMS Packaging***
A. Garnier, E. Lagoutte, X. Baillin, C. Gillot, and N. Sillon – CEA-LETI-MINATEC

Session 36: High Power LEDs and Lasers

Committee:
Optoelectronics

Southern Hemisphere V (5th Level)

Session Co-Chairs:
Fuad Doany – IBM Corporation
Kannan Raj – Sun Labs, Oracle

1. *1:30 p.m.* – ***LED Packaging Using Silicon Substrate with Cavities for Phosphor Printing and Copper-filled TSVs for 3D Interconnection***
Rong Zhang – Hong Kong University of Science & Technology (HKUST); S.W. Ricky Lee – Hong Kong University of Science and Technology (HKUST); David Guowei Xiao and Haiying Chen – Advanced Photoelectronic Packaging Ltd.

2. *1:55 p.m.* – ***Silicon-Based, Wafer-Level Packaging for Cost Reduction of High Brightness LEDs***
Thomas Uhrmann, Thorsten Matthias, and Paul Lindner – EV Group

3. *2:20 p.m.* – ***High Humidity Resistance of High-Power, White-Light-Emitting Diode Modules Employing Ce:YAG Doped Glass***
Chun-Chin Tsai, Jyun-Sian Liou, Wei-Chih Cheng, Cheng-Hsun Chung, Ming-Hung Chen, Jimmy Wang, and Wood-Hi Cheng – National Sun Yat-Sen University

4. *3:30 p.m.* – ***Performance of High-Brightness LEDs with VACNT-TIM on Aluminum Heat Spreaders***
Zhaoli Gao, Kai Zhang, and M.M.F. Yuen – Hong Kong University of Science and Technology (HKUST)

5. *3:55 p.m.* – ***Thermal Improvements for High Power UV LED Clusters***
Marc Schneider, Benjamin Leyrer, Christian Herbold, Klaus Trampert, and Jürgen J. Brandner – Karlsruhe Institute of Technology

6. *4:20 p.m.* – ***Wafer-Level Glass-Caps for Advanced Optical Applications***
Juergen Leib, Oliver Gyenge, Ulli Hansen, and Simon Maus – MSG Lithoglas AG; Karin Hauck, Kai Zoschke, and Michael Toepper – Fraunhofer IZM

7. *4:45 p.m.* – ***Inline Thermal Transient Testing of High Power LED Modules for Solder Joint Quality Control***
Gordon Elger, Reinhard Lauterbach, Kurt Dankwart, and Christopher Zilkens – Philips Technology GmbH

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Southern Hemisphere Ballroom Foyer / 5th Level)

Posters: Wednesday, June 1 and Thursday, June 2, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, June 1
Session 37: Posters 1
9:00 a.m. - 11:00 a.m.
Committee: Posters
Atlantic Hall B

Session Co-Chairs:
Nam Pham – IBM Corporation
Mark Eblen – Kyocera America, Inc.

1. ***Compact Thermal Model for Microchannel Substrate with High Temperature Uniformity Subjected to Multiple Heat Sources***
   Zhangming Mao, Xiaobing Luo, and Sheng Liu – Huazhong University of Science & Technology (HUST)
2. ***Pitfalls and Solutions of Replacing Gold Wire with Palladium Coated Copper Wire in IC Wire Bonding***
   Lei-Jun Tang and Yue-Jia Zhang – Institute of Microelectronics, A*STAR; Hong-Meng Ho – Semicon Fine Wire Pte. Ltd.; Wei Koh – Powertech Technology Inc.; Kay-Soon Goh – Semicon Fine Wire Pte Ltd.; Chun-Shu Huang and Yung-Tsan Yu – NiChing Industrial Corporation
3. ***Thermal Behaviours of Silicone Based Optical Interconnects with Mirror Optical Coupling***
   Dengke Cai and A. Neyer – TU Dortmund
4. ***Stress Analysis During Assembly and Packaging***
   Thomas Schreier-Alt and Frank Ansorge – Fraunhofer IZM; Katrin Unterhofer – TU Berlin; Klaus-Dieter Lang – Fraunhofer Institute IZM
5. ***Green Manufacturing Process for Solderless PCB Assembly Using Uniform Pressure Surface Interconnector and Anisotropic Conductive Film***
   Kyung-Woon Jang, Chang-Kyu Chung, Jiyoung Jang, Soon-Min Hong, Min-Young Park, and Youngjun Moon – Samsung Electronics Co., Ltd.; Seungbae Park – State University of New York, Binghamton
6. ***Correlation between Electrical and Mechanical Properties of Polymer Composite***
   I.B. Vendik, O.G. Vendik, V.P. Afanasjev, I.M. Sokolova, and D.A. Chigirev – St. Petersburg Electrotechnical University; R.A. Castro – Russian State Pedagogical University; K.M.B. Jansen and L.J. Ernst – Delft University of Technology; P. Timmermans – Philips Applied Technologies
7. ***Modeling and Optimization of Energy Harvesting-Systems under Non-Ideal Operating Temperatures with Regard to Availability of Power-Supply and Reduction of Environmental Impacts***
   Stephan Benecke, Andreas Middendorf, and Klaus-Dieter Lang – TU Berlin; Nils F. Nissen – Fraunhofer IZM
8. ***Ultra Low Cost Wafer Level Via Filling and Interconnection Using Conductive Polymer***
   D. Saint-Patrice, F. Jacquet, C. Bridoux, S. Bolis, R. Anciant, A. Pouydebasque, and A. Sillon – CEA-LETI-MINATEC; E. Vigier-Blanc – STMicroelectronics
9. ***Structure-Dependent Dielectric Constant in Thin Laminate Substrates***
   Hyun-Tai Kim, Yong-Taek Lee, Gwang Kim, and Billy Ahn – STATS ChipPAC, Inc.; Kai Liu – STATS ChipPAC, Ltd.; Robert C. Frye – RF Design Consulting, LLC
10. ***Critical New Issues Relating to Interfacial Reactions Arising from Low Solder Volume in 3D IC Packaging***
    H.Y. Chuang, W.M. Chen, W.L. Shih, and C.R. Kao – National Taiwan University; Y.S. Lai – Advanced Semiconductor Engineering, Inc.
11. ***Void Growth in Thermosonic Copper/Gold Wire Bonding on Aluminum Pads***
    H. Xu and V.L. Acoff – University of Alabama; C. Liu and V.V. Silberschmidt – Loughborough University; Z. Chen – Nanyang Technological University
12. ***Study on Microstructures and Tensile Properties of Active Solder Alloy***
    Mingxiang Chen, Cong Peng, Xing Chen, and Sheng Liu – Huazhong University of Science & Technology (HUST), Wuhan National Lab for Optoelectronics
13. ***Characterization of Intermetallic Compound (IMC) Growth in Cu Wire Ball Bonding on Al Pad Metallization***
    SeokHo Na, TaeKyeong Hwang, JungSoo Park, JinYoung Kim, HeeYeoul Yoo, and ChoonHeung Lee – Amkor Technology
14. ***Bumping and Stacking Processes for 3D IC Using Flux-Free Polymer***
    Kwang-Seong Choi, Ki-Jun Sung, Hyun-Cheol Bae, Jong-Tae Moon, and Yong-Sung Eom – Electronics and Telecommunications Research Institute (ETRI)
15. ***Co-Design of Flip Chip Interconnection with Anisotropic Conductive Adhesives and Inkjet-Printed Circuits for Paper-Based RFID Tags***
    Li Xie, Jue Shen, Jia Mao, Fredrik Jonsson, and Lirong Zheng – Royal Institute of Technology (KTH)
16. ***Process Development and Reliability Study with Anisotropic Conductive Film Bonding on Multiple Types of PCB Surface Finishes***
    Jenson Lee, David Geiger, and Dongkai Shangguan – Flextronics International
17. ***Design and Fabrication of a Test Chip for 3D Integration Process Evaluation***
    Chongshen Song – Chinese Academy of Sciences; Zheyao Wang and Litian Liu – Tsinghua University
18. ***Low-Temperature Bonding of LSI Chips to Polymer Substrate Using Au Cone Bump for Flexible Electronics***
    Takanori Shuto, Naoya Watanabe, Akihiro Ikeda, and Tanemasa Asano – Kyushu University
19. ***Effect of Blind Hole Depth and Shape of Solder Joint on the Reliability of Through Silicon Via (TSV)***
    Zhimin Wan, Xiaobing Luo, and Sheng Liu – Huazhong University of Science & Technology (HUST)

Wednesday, June 1
Session 38: Posters 2
2:00 p.m. - 4:00 p.m.
Committee: Posters
Atlantic Hall B

Session Co-Chairs:
Nam Pham – IBM Corporation
Mark Eblen – Kyocera America, Inc.

1. ***Recrystallization Behavior of Lead Free and Lead Containing Solder in Cycling***
   Awni Qasaimeh, Younis Jaradat, Luke Wentlent, Linlin Yang, Babak Arfaei, and Peter Borgesen – State University of New York, Binghamton; Liang Yin – Universal Instruments Corporation
2. ***Microstructures of Silver Films Plated on Different Substrates and Annealed at Different Conditions***
   Wen P. Lin, Chu-Hsuan Sha, Pin J. Wang, and Chin C. Lee – University of California, Irvine
3. ***Formation of Through Aluminum Via for Noble Metal PCB and Packaging Substrate***
   Jung Kyu Park, Seung Hwan Choi, and Myoung Soo Choi – Samsung LED; Young Ki Lee and Sang Hyun Shin – Samsung Electro-Mechanics
4. ***A Through-Silicon-Via to Active Device Noise Coupling Study for CMOS SOI Technology***
   Xiaomin Duan – IBM T.J. Watson Research Center, TU Hamburg-Harburg; Xiaoxiong Gu – IBM T.J. Watson Research Center; Jonghyun Cho and Joungho Kim – KAIST
5. ***Analysis of Thermo-Mechanical Behavior of ITO Layer on PET Substrate***
   Hyo-Soo Lee, Jae-Oh Bang, and Hai-Joong Lee – Korea Institute of Industrial Technology (KITECH); Gyu-Je Lee – Hynix Semiconductor; Kyung-Hoon Chai – LG Innotek Co. Ltd.; Seung-Boo Jung – Sungkyunkwan University
6. ***Development of a Non-Conductive, No-Flow, Wafer-Level Underfill***
   Chan-Lu Su, Kuo Yu Yeh, and Chang Chih Lin – Powertech Technology Inc.
7. ***Electrical and Aging Characterization of Organic Capacitive Substrate***
   Yun-Tien Chen, Shur-Fen Liu, Chin-Hsien Hung, and Meng-Huei Chen – Industrial Technology Research Institute (ITRI); Wei-Hsuan Wang – Taiwan Union Technology Corporation
8. ***Integrated Process for Silicon Wafer Thinning***
   Shengjun Zhou – Shanghai Jiao Tong University; Chuan Liu and Xiaobing Luo – Huazhong University of Science and Technology (HUST); Xuefang Wang – Huazhong University of Science & Technology (HUST); Sheng Liu – Shanghai Jiao Tong University, Huazhong University of Science & Technology (HUST)
9. ***Characterization of Thermo-Mechanical Stress and Reliability Issues for Cu-Filled TSVs***
   Dean Malta, Christopher Gregory, Matthew Lueck, and Dorota Temple – RTI International; Michael Krause, Frank Altmann, and Matthias Petzold – Fraunhofer IWM; Michael Weatherspoon and Joshua Miller – Harris Corporation
10. ***An Embedded Wi-Fi Front-End-Module in Printed-Circuit-Board by Employing Printed Lines***
    Jong-In Ryu, Se-Hoon Park, Dongsu Kim, and Jun-Chul Kim – Korea Electronics Technology Institute
11. ***Microstrip Antenna Tuning Using Variable Reactive Microelectromechanical Systems***
    Steven C. Yee, Christopher R. Anderson, Harry K. Charles, Samara L. Firebaugh, and Deborah M. Mechtel – United States Naval Academy
12. ***Silicon Microfilter Device Fabrication and Characterization for Diverse Microfluidics Applications***
    Bivragh Majeed, Lei Zhang, Deniz S. Tezcan, Philippe Soussan, and Paolo Fiorini – IMEC
13. ***Investigation of Various Photo-Patternable Adhesive Materials and Their Processing Conditions for MEMS Sensor Wafer Bonding***
    Jonghyun Kim – Institute of Microelectronics, A*STAR; Il Kim and Kyung-Wook Paik – KAIST
14. ***Maximum Channel Density in Multimode Optical Waveguides for Parallel Interconnections***
    Takaaki Ishigure, Ryota Ishiguro, Hisashi Uno, and Hsiang-Han Hsu – Keio University
15. ***Advanced Wafer Thinning and Handling for Through Silicon Via Technology***
    Jaesik Lee, Vincent Lee, Justin Seetoh, Serene Mei Ling Thew, Yen Chen Yeo, Hong Yu Li, Keng Hwa Teo, and Shan Gao – Institute of Microelectronics, A*STAR
16. ***Achievement of Low Temperature Chip Stacking by a Wafer-Applied Underfill Material***
    Ren-Shin Cheng, Kuo-Shu Kao, Jing-Yao Chang, Yin-Po Hung, Tsung-Fu Yang, Yu-Wei Huang, Su-Mei Chen, and Tao-Chih Chang – Industrial Technology Research Institute (ITRI); Qiaohong Huang, Rose Guino, Gina Hoang, and Jie Bai – Henkel Corporation
17. ***An Efficient Modeling of the Multi-Gigabit SSO Interference to the Pre-Driver in the Weak Power Supply System Based on the Charge Exchange Domain Partitioning Technique with Intentionally Utilizing High Power Supply Impedance***
    Ryuichi Oikawa – Renesas Electronics Corporation
18. ***Effect of Fine Solder Ball Diameters on Intermetallic Growth of Sn-Ag-Cu Solder at Cu and Ni Pad Finish Interfaces During Thermal Aging***
    Yong-Sung Park and Kyung-Wook Paik – KAIST; Jeong-Tak Moon, Young-Woo Lee, and Jae-Hong Lee – MK Electron Co., Ltd
19. ***An Efficient Edge Traces Technique for 3D Interconnection of Stack Chip***
    Sun-Rak Kim, Ah-Young Park, Choong D. Yoo, and Seung S. Lee – KAIST; Jae Hak Lee and Jun-Yeob Song – Korea Institute of Machinery and Materials

Thursday, June 2
Session 39: Posters 3
9:00 a.m. - 11:00 a.m.
Committee: Posters
Atlantic Hall B

Session Co-Chairs:
Nam Pham – IBM Corporation
Mark Eblen – Kyocera America, Inc.

1. ***Evaluation of the Use of a Rubber Buffer Layer to Protect Embedded SIP Devices from High Mechanical Forces***
   Amjad Alsakarneh, Liam Moore, and John Barrett – Cork Institute of Technology
2. ***Microwave Artificially Structured Periodic Media Microfluidic Sensor***
   Nophadon Wiwatcharagoses, Kyoung Youl Park, Jose A. Hejase, Lanea Williamson, and Prem Chahal – Michigan State University
3. ***Effect of Chemical Aging on Warpage for Encapsulated Packages – Characterization and Simulation***
   Tz-Cheng Chiu and Hong-Wei Huang – National Cheng Kung University; Yi-Shao Lai – Advanced Semiconductor Engineering, Inc.
4. ***Prospects and Limits in Wafer-Level-Packaging of Image Sensors***
   Martin Wilke, Kai Zoschke, Michael Toepper, Oswin Ehrmann, Herbert Reichl, and Klaus-Dieter Lang – Fraunhofer IZM; Frank Wippermann – Fraunhofer IOF
5. ***Evaluation of Additives and Current Mode on Copper Via Filling***
   Myung-Won Jung and Jae-Ho Lee – Hongik University; Young-Sik Song and Tae-Hong Yim – Korea Institute of Industrial Technology

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

6. ***Electropolishing and Electroless Plating of Copper and Tin to Replace CMP and Lithographic Processes in Cu/Sn Bump Fabrication***
Myung-Won Jung and Jae-Ho Lee – Hongik University; Seoung-Hun Kim and Yun-Sung Moon – LS-Nikko Company; Suk-Ei Lee and Yeong-Kwon Ko – Samsung Electronics Company
7. ***Effects of Bonding Parameters and ACF Material Properties on the ACF Joint Morphology in Ultrasonic Bonding***
Yoo-Sun Kim – Institute of Microelectronics, A*STAR; Kiwon Lee, Won-Chul Kim, and Kyuung-Wook Paik – KAIST
8. ***Miniature Detachable Photonic Turn Connector for Optical Module Interface***
Darrell Childers, Eric Childers, Joe Graham, Mike Hughes, Dirk Schoellner, and Alan Ugolini – US Conec, Ltd.
9. ***Conformal Atomic Layer Deposition (ALD) of Alumina on High Surface-Area Porous Copper Electrodes to Achieve Ultra-High Capacitance Density on Silicon Interposers***
Kanika Sethi, Himani Sharma, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology
10. ***Electromigration Prediction and Test for 0.18µm Power Technology in Wafer Level Reliability***
Jifa Hao, Yong Liu, and Mark Rioux – Fairchild Semiconductor Corporation; Yuanxiang Zhang and Lihua Liang – Zhejiang University of Technology
11. ***Novel Chip Stacking Process for 3D Integration***
Jaesik Lee, Daniel M. Fernandez, Myo Paing, Yen Chen Yeo, and Shan Gao – Institute of Microelectronics, A*STAR
12. ***Identification of Failure Modes in Portable Electronics Subjected to Mechanical-Shock Using Supervised Learning of Damage Progression***
Pradeep Lall and Prashant Gupta – Auburn University; Kai Goebel – NASA Ames Research Center
13. ***Thermal Modeling for Silicon-On-Sapphire (SOS) Based Power Amplifier Design in Wireless Communication***
John Zhiyuan Yang and Shing Lee – Peregrine Semiconductor
14. ***Compact 3D Integrable SU8 Embedded Microwave Bandpass Filters Using Complementary Split Ring Resonator Loaded Half Mode Substrate Integrated Waveguide***
D.E. Senior, X. Cheng, P. Jao, C. Kim, and Y.K. Yoon – University of Florida
15. ***Compact Electromagnetic-Bandgap Structures for Embedding into Si and Glass Interposers***
Koichi Takemura, Noriaki Ando, Hiroshi Toyao, Takashi Manako, and Tsuneo Tsukagoshi – NEC Corporation
16. ***Delamination Toughness of Cu-EMC Interfaces at Harsh Environment***
M. Sadeghinia, K.M.B Jansen, and L.J. Ernst – Delft University of Technology; G. Schlottig and H. Pape – Infineon Technologies AG
17. ***Study on TSV with New Filling Method and Alloy for Advanced 3D-SiP***
Akihiro Tsukada, Ryohei Sato, Yukihiro Sato, Yoshiharu Iwata, and Hidenori Murata – Osaka University; Shigenobu Sekine, Ryuji Kimura, and Keijiroh Kishi – Napura Co., Ltd.
18. ***Solution-Derived Electrodes and Dielectrics for Low-Cost and High-Capacitance Trench and Through-Silicon-Via (TSV) Capacitors***
Yushu Wang, Shu Xiang, P. Makondeya Raj, Himani Sharma, and Rao Tummala – Georgia Institute of Technology; Byron Williams – Texas Instruments

Thursday, June 2
Session 40: Posters 4
2:00 p.m. - 4:00 p.m.
Committee: Posters
Atlantic Hall B

Session Co-Chairs:
Nam Pham – IBM Corporation
Mark Eblen – Kyocera America, Inc.

1. ***Electrical, Optical, and Fluidic Through-Silicon Vias for Silicon Interposer Applications***
Mahavir S. Parekh, Paragkumar A. Thadesar, and Muhannad S. Bakir – Georgia Institute of Technology
2. ***Mechanical Characterization of Nickel Nanowires by Using a Customized Atomic Microscope in Scanning Electron Microscope***
Emrah Celik, Ibrahim Guven, and Erdogan Madenci – University of Arizona
3. ***Variation-Tolerant and Low-Power Clock Network Design for 3D ICs***
Xin Zhao, Saibal Mukhopadhyay, and Sung Kyu Lim – Georgia Institute of Technology
4. ***Reliability of Fine Pitch Halogen-Free Organic Substrates for Green Electronics***
Koushik Ramachandran, Fuhan Liu, Nitesh Kumbhat, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Mark Wilson – Dow Chemical Company
5. ***High Throughput and Fine Pitch Cu-Cu Interconnection Technology for Multichip Chip-Last Embedding***
Abhishek Choudhury, Nitesh Kumbhat, Sadia A. Khan, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Georg Meyer-Berg – Infineon Technologies AG
6. ***LSI Packaging Development for High-End CPU Built into Supercomputer***
Joji Fujimori – Fujitsu Semiconductor Limted; Masateru Koide – Fujitsu Advanced Technologies Limited
7. ***In-Plane/Out-of-Plane Mixed Probe Techniques to Obtain the RF Characteristics of the SMA Connectors***
Kuan-Chung Lu, Tzyy-Sheng Horng, and Lih-Tyng Hwang – National Sun Yat-Sen University
8. ***Coupled Electrical and Thermal 3D IC Centric Microfluidic Heat Sink Design and Technology***
Yue Zhang, Calvin R. King Jr., Jesal Zaveri, Yoon Jo Kim, Vivek Sahu, Yogenda Joshi, and Muhannd S. Bakir – Georgia Institute of Technology
9. ***Nanocomposite for Low Stress Underfill***
Ziyin Lin and Kyung-Sik Moon – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology, Chinese University of Hong Kong
10. ***Self-Assembly Technologies with High-Precision Chip Alignment and Fine-Pitch Microbump Bonding for Advanced Die-to-Wafer 3D Integration***
T. Fukushima, Y. Ohara, M. Murugesan, J.C. Bea, K.-W. Lee, T. Tanaka, and M. Koyanagi – Tohoku University
11. ***Analysis of CNT Based 3D TSV for Emerging RF Applications***
Anurag Gupta, Bruce C. Kim, Sukeshwar Kannan, and Sai Shravan Evana – University of Alabama; Li Li – Cisco Systems, Inc.
12. ***Tin-Bismuth Plating for Component Finishes***
Rui Zhang, Jaiwei Zhang, John Evans, and Wayne Johnson – Auburn University; Jan Vardaman – TechSearch International, Inc.; Issei Fujimura – Ishihara Chemical Co., Ltd.; Andy Tseng – Advanced Semiconductor Engineering, Inc. Jeff Knight – Endicott Interconnect
13. ***Impact of Board Configuration and Shock Loading Conditions for Board Level Drop Test***
Pradosh Guruprasad and James Pitarresi – Binghamton University; Brian Roggeman – Binghamton University, Universal Instruments Corp.
14. ***Enhancement of Dielectric Strength and Processibility of High Dielectric Constant Al Nanocomposite by Organic Molecule Treatment***
Zhuo Li, Kyoung-Sik Moon, and Saewon Kim – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
15. ***Low Temperature Cu-Cu Direct Bonding Using Formic Acid Vapor Pretreatment***
Wenhua Yang, Hiroyuki Shintani, Masatake Akaike, and Tadatomo Suga – University of Tokyo
16. ***Modeling, Optimization and Benchmarking of Chip-to-Chip Electrical Interconnects with Low Loss Air-Clad Dielectrics***
Vachan Kumar and Azad Naeemi – Georgia Institute of Technology; Rizwan Bashirullah – University of Florida
17. ***Advanced Solder TSV Filling Technology Developed with Vacuum and Wave Soldering***
Young-Ki Ko, Chang-Woo Lee, and Sehoon Yoo – Korea Institute of Industrial Technology (KITECH); Hiromichi T. Fujii and Yutaka S. Sato – Tohoku University

Friday, June 3
Session 41: Student Posters
8:30 a.m. - 10:30 a.m.
Committee: Posters
Northern Hemisphere Ballroom D-E Foyer

Session Co-Chairs:
Nam Pham – IBM Corporation
Mark Eblen – Kyocera America, Inc.

1. ***Ultra-Compact Dual-Band WLAN Filter Using Independent Band Stop Resonators***
Jun H. Park, Seong J. Cheon, and Jae Y. Park – Kwangwoon University; Jeong T. Lim – SGR Tech Co., Ltd.
2. ***The Development of Thin Film Barriers for Encapsulating Organic Electronics***
Yongjin Kim, Namsu Kim, Hyungchul Kim, and Samuel Graham – Georgia Institute of Technology
3. ***Metamaterial-Inspired Absorbers for Terahertz Packaging Applications***
Kyoung Youl Park, Jose A. Hejase, Collin S. Meierbachthol, Nophadon Wiwatcharagoses, and Prem Chahal – Michigan State University
4. ***Novel ZnO Nanowires/Silicon Hierarchical Structures for Superhydrophobic, Low Reflection, and High Efficiency Solar Cells***
Yan Liu, Ziyin Lin, and Kyoung Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
5. ***Micro Texture Dependence of the Mechanical and Electrical Reliability of Electroplated Copper Thin Film Interconnections***
Naokazu Murata, Naoki Saito, Fumiaki Endo, Kinji Tamakawa, Ken Suzuki, and Hideo Miura – Tohoku University
6. ***Characterization of the Mechanical Properties of Actual Solder Joints Using DIC***
Tung T. Nguyen and Seungbae Park – State University of New York, Binghamton
7. ***Vertical Interconnect Measurement Techniques Based on Double-Sided Probing System and Short-Open-Load-Reciprocal Calibration***
Kuan-Chung Lu, Yi-Chieh Lin, and Tzyy-Sheng Horng – National Sun Yat-Sen University; Sung-Mao Wu – National University of Kaohsiung; Chen-Chao Wang, Chi-Tsung Chiu, and Chih-Pin Hung – Advanced Semiconductor Engineering Group
8. ***Damage Prediction in Graphene Thermoplastics for Potential Electronic Packaging Applications***
Erkan Oterkus – National Institute of Aerospace; Erdogan Madenci – University of Arizona
9. ***Multi-Path Fan-Shaped Compliant Off-Chip Interconnects***
Robert E. Lee, Raphael Okereke, and Suresh K. Sitaraman – Georgia Institute of Technology
10. ***Air Cavity Low-Loss Transmission Lines for High Speed Serial Link Applications***
Jikai Chen, Yan Hu, and Rizwan Bashirullah – University of Florida; Yu-Chun Chen, Rajarshi Saha, and Paul Kohl – Georgia Institute of Technology
11. ***The Use of Implicit Mode Functions to Drop Impact Dynamics of Stacked Chip Scale Packaging***
Liangbiao Chen and Gang Sheng – University of Alaska; Cheng-fu Chen and Terrence Wilburn – University of Alaska Fairbanks
12. ***Large-Area Low-Cost Substrate Compatible CNT Schottky Diode for THz Detection***
Xianbo Yang and Prem Chahal – Michigan State University
13. ***Room Temperature SiO_2 Wafer Bonding by Adhesion Layer Method***
Ryuichi Kondou and Tadatomo Suga – University of Tokyo
14. ***Electromagnetic-SPICE Modeling and Analysis of 3D Power Network***
Zheng Xu – Rensselaer Polytechnic Institute (RPI); Jian-Qiang Lu – Rensselaer Polytechnic Institute; Bucknell C. Webb and John U. Knickerbocker – IBM T.J. Watson Research Center
15. ***Design and Characterization of Power Delivery System for Multi-Chip Package with Embedded Discrete Capacitors***
Hung-Hsiang Cheng and Chih-Wen Kuo – National Sun Yat-Sen University; Po-Chih Pan, Yi-Hua Chen, and Kuo-Hua Chen – Advanced Semiconductor Engineering, Inc.; Li Li, Ken Han, and Glenn Cooper – Cisco Systems, Inc.
16. ***Watt-Level Wireless Power Transfer Based on Stacked Flex Circuit Technology***
Xuehong Yu, Florian Herrault, Chang-Hyeon Ji, Seong-Hyok Kim, and Mark G. Allen – Georgia Institute of Technology; Gianpaolo Lisi, Luu Nguyen, and David I. Anderson – National Semiconductor Corporation
17. ***Assessment of Current Density Singularity in Electromigration of Solder Bumps***
Pridhvi Dandu and Xuejun Fan – Lamar University

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

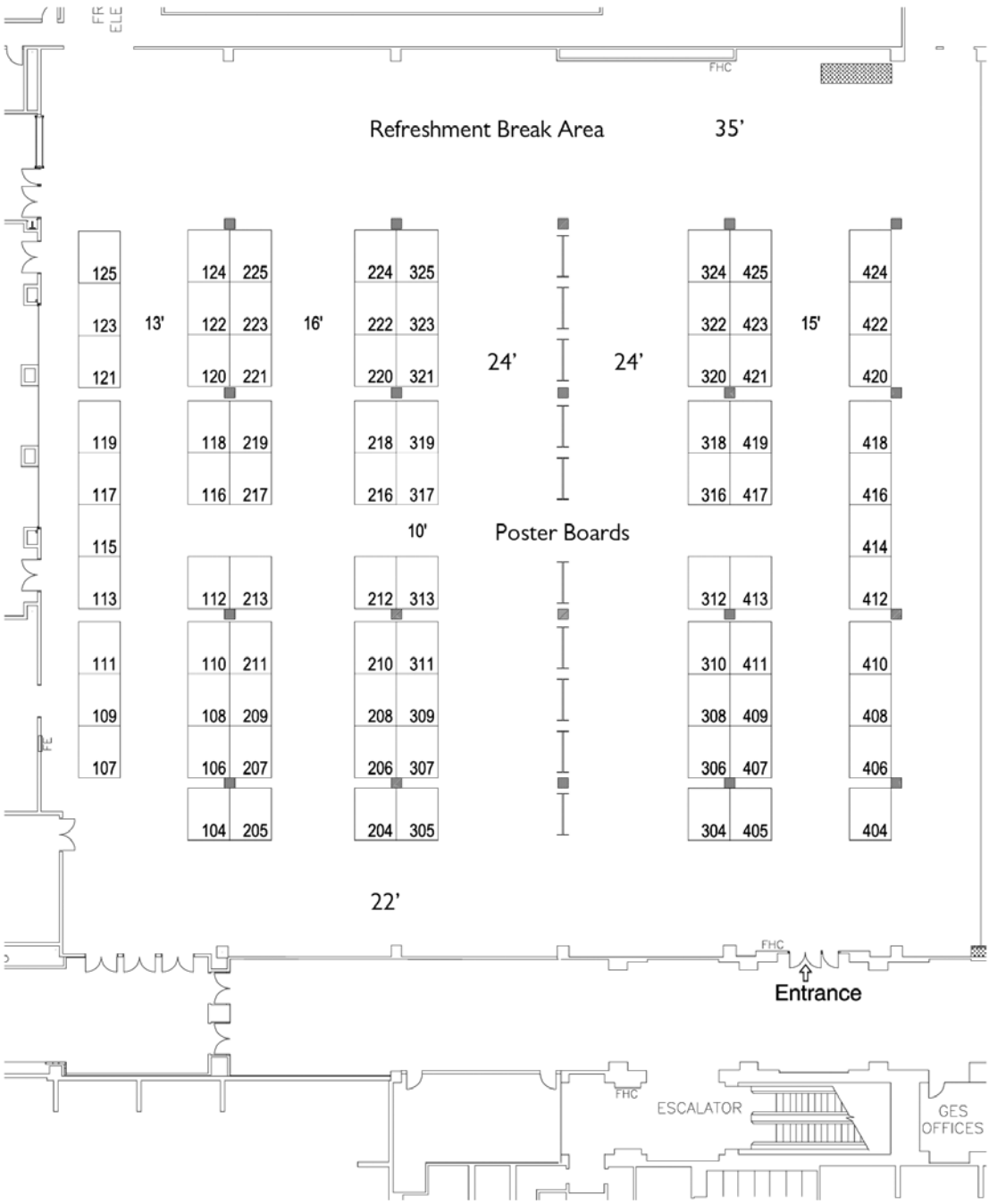
TECHNOLOGY CORNER BOOTH AND POSTER LAYOUT

Technology Corner Exhibits

Wednesday, June 1, 2011 • 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.
Thursday, June 2, 2011 • 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.
Atlantic Hall B (1st Level)

Poster Paper Sessions

Wednesday, June 1, 2011 morning posters • 9:00 a.m. - 11:00 a.m.
Wednesday, June 1, 2011 afternoon posters • 2:00 p.m. - 4:00 p.m.
Thursday, June 2, 2011 morning posters • 9:00 a.m. - 11:00 a.m.
Thursday, June 2, 2011 afternoon posters • 2:00 p.m. - 4:00 p.m.
Atlantic Hall B (1st Level)



TECHNOLOGY CORNER EXHIBITORS

3D Systems Packaging Research Center (PRC)
Georgia Institute of Technology
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Booth 324

The 3D Systems Packaging Research Center (PRC) at the Georgia Institute of Technology is a Global Academic Center dedicated to leading-edge research and education in the System-on-a-Package (SOP) concept to enable highly miniaturized, multi to mega-functional systems in a single package. Led by Prof. Rao Tummala, the PRC has developed a unique and integrated approach to research, education and industry partnership using its comprehensive 300 mm SOP panel facilities, research staff, faculty and students. The Center's research encompasses a full spectrum of the most advanced packaging technologies including; design and test; multi-functional 110GHz organic packages; glass and silicon interposers enabling lower cost 3D systems; thin film passives for power and signal conditioning applications; enabled by leading advances in materials and processes, interconnections, assembly, and reliability and thermal management. The PRC offers a variety of industry partnerships that include one-on-one contracts, and an extensive array of consortia research programs involving the entire supply chain of companies, including UnITE™ PAC – a global consortium for packaging information sharing and connectivity. Benefits include intellectual property rights, technology transfer, and access to students for recruiting, one-on-one company-faculty relationships, state-of-the-art R&D facilities, and more. For more information about the consortia and membership programs, research areas or other information, we invite you to visit our website at www.prc.gatech.edu.

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AI Technology is an ISO9001 certified facility and manufactures flexible "Stress-free" adhesives, films, pastes and thermal films, gels/grease. Products are available in syringes, jars, premixed & frozen or separated in Part A & Part B for ambient storage. Film based adhesives with tack for ease of use can be shipped in sheets or in performs. Adhesives are electrically conductive or insulating and applicable for die-attach, lid sealing, BGA, multichip modules, and wafer lamination. Solder-Sub™ and Chip-Coupler™ applications available.

Our Insulating Metal Substrate uses our proprietary flexible thermal dielectric insulating layer resulting in stress and warp-free thermal copper-clad laminates. We also have a variety of Thermal Insulating Materials which will improve performance. Both of these products have shown improvements in LED performance.

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ALLVIA, Inc. provides Silicon Interposer and Through-Silicon Via (TSV) foundry services to Semiconductor, Optoelectronics and MEMS industries meeting the demands of advanced vertical interconnects, 2.5D, 3D and System-in-Package (SiP) solutions. ALLVIA, a leader in TSV development, provides design and processing for frontside (filled) and backside (conformal plated) through silicon vias. With its full line of in-house processing equipment, ALLVIA offers services for prototyping as well as volume production runs.

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Amkor Technology, Inc. is one of the world's largest providers of advanced semiconductor assembly and test services. Founded in 1968, Amkor has become a strategic manufacturing partner for many of the world's leading semiconductor companies and electronics OEMs, providing a broad array of advanced package design, assembly and test solutions. Amkor's operational base encompasses more than 5 million square feet of manufacturing facilities, product development centers, and sales & support offices in Asia, Europe and the United States. Amkor offers a suite of services, including electroplated wafer bumping, probe, assembly and final test. Amkor is a leader in advanced copper pillar bump and packaging technologies which enables next generation flip chip interconnect.

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Technology Corner Reception

Wednesday, June 1, 2011
5:30 - 6:30 p.m.

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QualiTau offers a variety of reliability and parametric test equipment for the characterization and development of new materials used in the manufacture of Integrated Circuits. The DSPT 9012 (Desktop Semiconductor Parametric Tester) is a PC Controlled SMU test instrument built specifically for semiconductor device characterization and testing. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection, Dielectric Breakdown, Solder Bump at up to 8 Amps, and Electromigration at test temperatures up to 450C.

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Quik-Pak, a division of Delphon Industries, provides IC packaging and assembly services. The company's newest offering is its OmPP package. These pre-molded QFN packages are cost-effective, come in a variety of sizes and are ideal for prototype or production volume applications. Quik-Pak also specializes in a variety of services that together provide a full turn-key solution including wafer preparation, die/wire bonding, remolding and marking/branding. Custom assembly services are also offered for Flip Chip, Ceramic Packages, Chip-on-Board, Stacked Die, MEMS, etc

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RTI International's Center for Materials and Electronic Technologies is a world leader in advanced interconnect and packaging technologies. RTI provides access to state of the art wafer bumping and WLP technologies, supporting small and mid-volume customers as well as developmental applications. As a recognized leader in 3D integration, RTI has developed a comprehensive platform of technologies and works with commercial, government, and academic clients from around the world to develop and implement solutions. In addition to its focus on advanced interconnect technologies, RTI also conducts research and development in sensors and actuators, electronic material characterization, and novel device microfabrication. The Center is staffed with full time engineers and researchers developing new technologies and solutions in conjunction with our clients. Fully integrated fabrication and analytical facilities allow RTI to support a diverse project base, from process development, proof of concept and prototyping, to small-scale production.

RTI International is a non-profit research institute offering innovative research, technical expertise, and fabrication capabilities to governments and businesses worldwide.

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SET, Smart Equipment Technology (Former Suss MicroTec Device Bonder Division) is a world leading supplier of High Accuracy Assembly and Nano Imprint Lithography Solutions. SET joined Replisaurus Technologies in 2008. As a supplier of semiconductor equipment dedicated to high-end applications for over 30 years and with more than 300 Device Bonders installed worldwide, SET is globally renowned for the unsurpassed bonding accuracy (± 0.5 µm) and the high flexibility of its die and flip-chip bonders. SET's product portfolio ranges from manual loading versions to fully automated operation. The SET systems cover a wide range of bonding applications and offer the unique ability to handle both fragile and small components onto substrates up to 300mm.

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Shin-Etsu Microsi, Inc. is a wholly owned subsidiary of Shin-Etsu Chemical Ltd. Shin-Etsu MicroSi is a world class supplier of packaging materials for the semiconductor industry. With a global support network, which includes Sales Engineers, R&D, Manufacturing, Quality Assurance, and Logistics, we are able to quickly develop and provide new technologies to benefit our customers. This allows our clients to meet their ever changing technical, commercial and environmental needs by implementing Shin-Etsu MicroSi's technology. Shin-Etsu MicroSi is known for supplying high performance Thermal Interface Materials, Underfills, Molding Compounds, High Purity Silicone Encapsulants, and Die Attach Materials.

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SIGRITY provides software tools and technical services for power, ground and signal integrity analysis of high performance IC packages and printed circuit boards. SIGRITY analysis tools utilize a fast electromagnetic field solver that takes into account coupling between vias, reflection from edges, resonance, power and ground voltage fluctuations, and electromagnetic radiation. Sigrity's package physical design products provide eDriven capability and facilitate design reuse. Worldwide leading companies as well as high-tech start-ups have successfully adopted SIGRITY's software tools for applications in various pre- and post-layout power and signal integrity analyses.

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SIMULIA is the Dassault Systèmes brand that makes realistic simulation an integral business practice improving product performance, reducing physical prototypes, and driving innovation. SIMULIA solutions include Abaqus Unified Finite Element Analysis solutions, multiphysics solutions for insight into challenging engineering problems, and SIMULIA SLM for managing simulation data, processes, and intellectual property.

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Sonnet software is dedicated to the development of high-frequency electromagnetic analysis software. Sonnet's software is aimed at today's demanding design challenges involving predominately 3D planar circuits and antennas, including microstrip, stripline, co-planar waveguide, PCB (single and multiple layers) and RF packages incorporating any number of layers of metal traces embedded in stratified dielectric material. For more information on the Sonnet Suites visit www.sonnetsoftware.com

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SOURIAU PA&E, Inc. is an integrated manufacturing company, specializing in technically demanding ceramic and metal components and assemblies, hermetic connectors, advanced hermetic electronic packaging, EMI filters and explosively bonded metals for global leaders in the defense, space, medical and commercial industries.

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SPP Process Technology Systems (SPTS) is a leading manufacturer of plasma based etch , deposition and thermal systems serving the advanced semiconductor capital equipment and process technologies for the global semiconductor industry and related markets. These products are used in a variety of market segments, including R&D, MEMS and nanotechnology, advanced 3-D packaging, LEDs, and power integrated circuits for communications.

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STATS ChipPAC is a leading service provider of semiconductor packaging design, bump, probe, assembly, test and distribution solutions. A trusted partner to leading semiconductor companies worldwide, STATS ChipPAC provides fully integrated, multi-site, end-to-end packaging and testing solutions that bring products to market faster. With advanced process technology and a global manufacturing presence spanning Singapore, South Korea, China, Malaysia, Thailand and Taiwan, STATS ChipPAC offers a full range of backend turnkey services for a wide variety of electronics applications. STATS ChipPAC has a leadership position in advanced package technology such as fan-in and fan-out wafer level packaging, flip chip interconnect, 3D integration and Through Silicon Via to meet the increasing market demand for next generation devices with higher levels of integration, increased functionality and compact sizes.

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Tango Systems Inc. manufactures the Axcela, a PVD system for a variety of applications. The system is ideally suited for barrier and seed layers for Through-Silicon Vias, for Under-Bump Metallization, Arc Layers and Thick Metal Layers. Oxide and Nitride films can be deposited equally well. The system can be configured with one or two PVD chambers, each chamber can have 3 or even 4 different targets. The system is ideal for R&D and also for high volume production, up to 70 wafers per hour, and it can easily be changed for different wafer sizes, (100mm to 300 mm wafers). Our Service Lab can process up to 10,000 wafers per month for customers and we provide process development for specialized applications because we have most common targets in stock.

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TechSearch International, Inc. was founded in 1987 as a market research and consulting company specializing in emerging semiconductor packaging trends. Multi- and single-client services encompass market research, technology trends, strategic planning, and technology licensing. Research topics include wafer level packaging, flip chip interconnect, CSPs, BGAs, 3D integration with TSVs, manufacturing in China and India, multichip packages (MCPs) such as stacked die CSPs and System-in-Package (SiP), embedded components, microvia substrates, LED assembly, and Pb-free manufacturing. Market forecasts and trends in advanced semiconductor packages and materials are available. In conjunction with SavanSys Solutions, wire bond, flip chip and WLP trade-off cost models are offered. TechSearch International professionals have an extensive network of more than 15,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

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For over 50 years TOK has been supplying superior quality chemicals and equipment to the microelectronics and semiconductor manufacturers of the world. TOK is now offering materials and equipment to enable fabrication of 3DIC with TSVs. These products include photoresists for plating (Au, Ni, Cu, Pb/Sn, SN/Ag), photo definable insulators, and the "Zero Newton" system, an innovative turn-key solution for temporary wafer handling that can be tailored to meet the demanding needs of companies on the forefront of 3DIC packing technology. Please visit our booth to learn more about TOK's products and how TOK can help you solve your most challenging advanced packaging requirements.

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Toray Engineering Co., Ltd provides Flip Chip Bonding Equipment for Semiconductor Packaging (FC 2000), Optoelectronics (OF2000) and LCD devices (CL2000FW, OS2000). Also, Vacuum Encapsulation Equipment (VE500) and various Flexible substrates (TCP,interposer) manufacturing equipment such as resist coater, proximity exposer, etching, developing line are available.

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XYZTEC, a leading global supplier of bond test equipment, offers the most flexible bond testing platform on the market today! The Condor series features a single platform with multiple test capabilities allowing end-users the added flexibility of performing many types of tests all on one system. In addition to standard bond testing applications such as wire pull, ball shear, die shear, the Condor series has the capability to perform peel testing, push testing, high impact testing, fatigue testing, and creep testing.

XYZTEC is the only bond test supplier that offers a Revolving Measurement Unit, featuring four different measurement sensors to address 80% of your test requirements. The joysticks are ergonomically friendly, easily move the XY stage to the desired position, and feature 12 logically arranged buttons for increased operator efficiency. The Condor EZ software features onboard graphics and intelligent wizards, providing intuitive operator control as well as sophisticated SPC software thus ensuring complete documentation of the test protocol.

Check out our new web site at www.xyztec.com.

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Beginning in 1998 with Yole Développement, we have grown to become a group of companies providing market research, technology analysis, strategy consulting, media in addition to finance services. With a solid focus on emerging applications using silicon and/or micro manufacturing Yole Développement group has expanded to include more than 40 associates worldwide covering MEMS and microfluidics, Advanced Packaging, Compound Semiconductors, Power Electronics, LED, and Photovoltaic. The group supports companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

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Zeon Corporation, Japanese technology polymer company, and Zeon Chemicals L.P., USA have developed two innovative state of the art packaging materials: 1) "New Build-Up Film" used for Build-Up substrate for IC packages, GPU, WLP, Si Interposer and any application requiring superior electrical properties, and 2) "New PCB Materials" low loss laminate for both high k and low k applications such as milli-wave radars, high speed servers and circuits, and RF/mobile applications for technology leading devices.

1) "New Build-Up Film"
This film provides high density, high speed, and reliable IC or GPU packages with properties such as low CTE, 10/10um or less L/S, low dielectric constant, low loss tangent, and low moisture absorption. Its low shrinkage characteristic makes it an ideal choice for WLP applications with strong cost advantages over conventional liquid spin on materials. In addition to those properties, it allows forming very fine Copper lines on high smooth surfaces, with its Ra is around 70nm while maintaining superior peel strength performance.

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Adhesives and encapsulants for electronics and optoelectronics assembly. Products include electrically conductive, thermally conductive adhesives, ultra-low stress adhesives, anisotropically conductive adhesives, UV curable glob top encapsulants and underfill encapsulants for flip chips, CSP's and BGA's, including reworkable underfill encapsulants

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First Call For Papers

62nd Electronic Components and Technology Conference

www.ectc.net

To be held May 29th - June 1st, 2012, at the Sheraton San Diego Hotel & Marina, San Diego, California, USA.

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:

Design, development, fabrication, testing, and characterization of advanced packaging and novel component integration technologies involving electronics, photonics, MEMS and their innovative configurations for applications related to computing, sensing, imaging, photovoltaic, high power and bio-medical systems. Special emphasis will be on solutions for high performance, density, and thermal management related to systems involving 3D integration, through silicon vias (TSVs), flip-chip, and fine pitch and high lead count packaging in CSP, WLP, BGA, CGA, LGA and SMT packages for both Pb-based and Pb-free packages.

Applied Reliability:

Advances in reliability assessment and prediction at the system, PWB or package level, reliability testing and data analysis, reliability modeling of accelerated testing, reliability issues in emerging technologies, medical electronics and consumer electronics, reliability physics, reliability predictions, reliability test methods and failure analysis.

Assembly and Manufacturing Technology:

Advanced process and equipment improvement for volume production of emerging technology, including: Advanced packaging, system in package, package on package, bumping and flip chip, die thinning and stacking, low-K device, photonic device , MEMS and optoelectronics, product and system level assembly, electrical/mechanical/green performance and board level assembly.

Electronic Components & RF:

Discrete Passive Components; integrated and embedded passive and active components integration on silicon, ceramic, organic substrates; electronic components - design, materials, processing, test, characterization; new technology development for components - silicon through vias, wafer level RDL, nano materials and processes; tunable materials, structures, devices and switches; RFID/sensors, RF MEMS, integrated antennas, filters, baluns; components and modules for WLAN, UWB, mobile PC and multi-band radio applications.

Emerging Technologies:

Design, fabrication, modeling and performance aspects of materials, devices, systems and packaging in the areas of bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices; organic/printable electronics; portable power supplies such as fuel cells; and other novel packaging.

Interconnections:

Interconnect designs, structures, processes, and innovations at all levels of packaging. Topic areas include wire bonding, flip chip and wafer level package interconnects, solder- and nonsolder-based bump interconnects and bonding processes, under bump metallurgy, interconnects for 3D integration, through Si via connections, printed circuit board interconnect, electromigration, thermal performance of interconnects, conductive polymer, composite, and nanomaterial-based interconnects, novel enabling techniques, electrical performance, characterization and properties of interconnect materials, and reliability, cost, and environmental concerns.

Materials & Processing:

Materials and processes for traditional and advanced microelectronic systems, 3D packages, WLP and TSV, photonics, MEMS, solar and biomedical packaging that enhance mechanical, thermal, electrical and optical performance and cost effectiveness. This includes advances in adhesives, nano-materials, embedded active and passive components, flexible and printed electronics, magnetic, optical and thermal interface materials, Pb-free solders, alloys and assembly processes.

Modeling & Simulation:

Electrical, thermal, optical and mechanical modeling, simulation and characterization of packaging solutions including system-level applications. Example topics include assembly manufacture modeling, Cu low-K interconnects, drop impact models, embedded passives, equivalent circuit models, fullwave modeling, lead-free solders, macromodeling, measurements and thermo-mechanical reliability

Optoelectronics:

Packaging and technology for optoelectronic modules, components and devices including amplifiers, transmitters, receivers, integrated photonics, passive components, fiber optics, optical sensors, chip-chip, backplanes interconnect and storage. Special interest topics include high power lasers, high-brightness LEDs, thermal management and reliability, micro-optic packaging & manufacturing, silicon photonics, photovoltaics, integrated optical sensors, nano-optics, RF over fiber, optoelectronics for space applications and harsh environments, and advanced optoelectronic materials.

Posters:

Papers may be submitted on any of the listed major topics; presentation of papers in a poster format is highly encouraged at ECTC. Poster papers allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Papers not fitting into topic of an oral session or any submitted abstract or paper may be included in poster sessions at the discretion of the program committee.

You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

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Chander, Arizona
Phone: +1-480-552-4898
Email: spekin@msn.com

Abstracts must be received by October 15, 2011. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 15, 2011. If you have any questions, contact:

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62ND ELECTRONIC COMPONENTS & TECHNOLOGY CONFERENCE

Sheraton San Diego Hotel & Marina
San Diego, CA • May 29 - June 1, 2012

Nestled at the edge of spectacular San Diego Bay, the Sheraton San Diego Hotel & Marina enjoys panoramic views of the bay and the city skyline, yet is just 10 minutes from renowned attractions including the San Diego Zoo, Old Town and Balboa Park.

Dubbed by many as "the only area in the US with perfect weather," San Diego is the oldest port on the West Coast and the sixth-largest city in the nation. Long known as a naval base, the military, along with tourism, still dominates the economy. In addition to rolling mountains, beautiful deserts, and seventy miles of coastline featuring some of the world's best beaches, San Diego offers a wealth of attractions. Art lovers can choose from many fine museums or catch a Shakespearean play at the Old Globe Theater. With more championship golf courses, over 85, than any other US city, linksters will have no problem teeing off. The city also hosts the NFL's Chargers and Major League Baseball's Padres. And one last thing, don't forget to bring your passports as Tijuana, Mexico is only an hour away from sunny San Diego!

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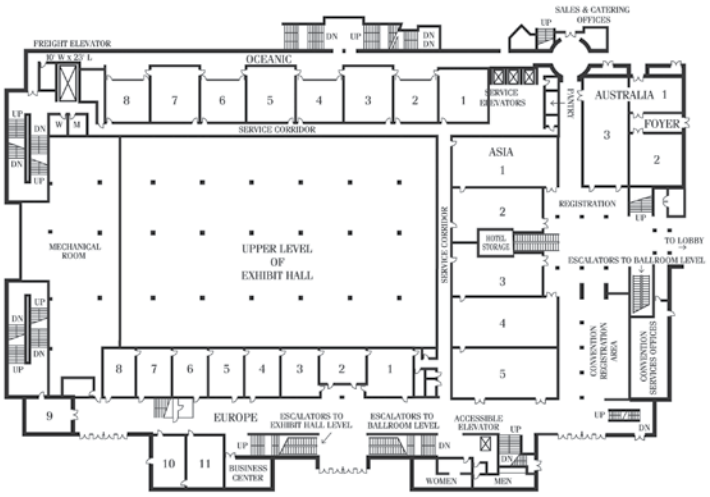
Dolphin Meeting Rooms
Lobby Level – 3rd Level
ECTC Registration



Dolphin Ballroom Level
Technical Sessions and Luncheons
5th Level

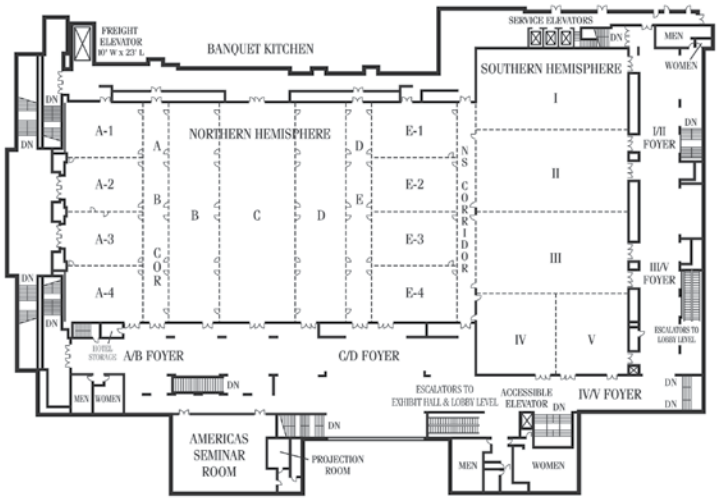
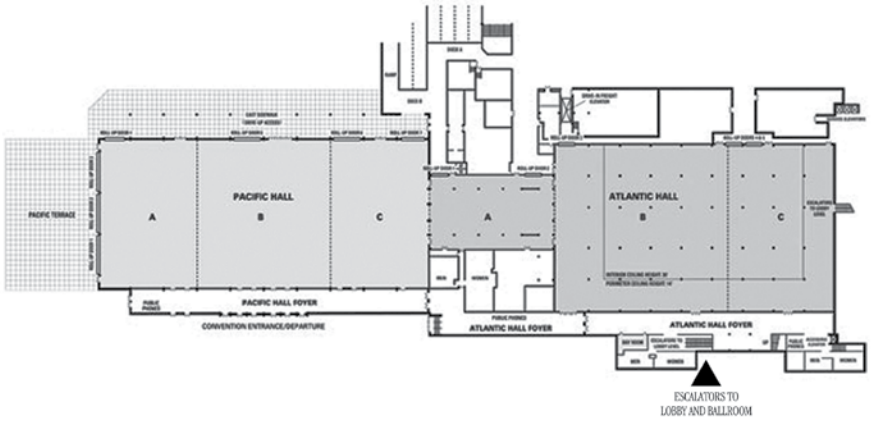


Exhibit Hall Level
ECTC Exhibits
Atlantic Hall B – 1st Level



Conference At A Glance

Monday, May 30, 2011

3:00 p.m. – 5:00 p.m.
Registration – Australia 3 Foyer (Lobby Level)

Tuesday, May 31, 2011

6:45 a.m. – 8:15 a.m.
AM PD Courses
Registration Only
Australia 3 Foyer (Lobby Level)

6:30 a.m. – 7:45 a.m.
PD Courses Instructor and Proctors Briefing & Breakfast
Asia I (Lobby Level)

7:00 a.m. – 5:00 p.m.
Speakers Prep – Europe 2 (Lobby Level)

8:00 a.m. – Noon
AM PD Courses
See page 8 for locations

9:30 a.m. – Noon
Manufacturing Limitations Special Session
Southern Hemisphere Ballroom I (5th Level)

10:00 a.m. – 10:20 a.m.
AM PD Course Break
Southern Hemisphere Ballroom Foyer (5th Level)

11:00 a.m. – 1:15 p.m.
Conference Registration
PM PD Courses Registration Only
Australia 3 Foyer (Lobby Level)

Noon
PD Courses Luncheon
Southern Hemisphere Ballroom II (5th Level)

1:00 p.m. – 5:00 p.m.
Technology Corner Set-up
Atlantic Hall B (First Level)

1:15 p.m. – 5:00 p.m.
Conference Registration
Australia 3 Foyer (Lobby Level)

1:15 p.m. – 5:15 p.m.
PD PM Courses
See page 8 for locations

3:00 p.m. – 3:20 p.m.
PM PD Course Break
Southern Hemisphere Ballroom Foyer (5th Level)

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Cabana Deck (Outside near Pool & Cabana Bar)
Rain Backup: Asia I (Lobby Level)

6:00 p.m. – 7:00 p.m.
General Chair's Speakers Reception (by Invitation)
Crescent Terrace
(Outside on SWAN property)
Rain Backup: Southern Hemisphere Ballroom I (5th Level)

7:30 p.m. – 9:00 p.m.
Panel Discussion
Southern Hemisphere Ballroom III (5th Level)

Wednesday, June 1, 2011

6:45 a.m. – 4:00 p.m.
Conference Registration
Australia 3 Foyer (Lobby Level)

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere Ballrooms E 3 – 4 (5th Level)

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2 (Lobby Level)

8:00 a.m. – 4:00 p.m.
Companion Hospitality Room
Europe I (Lobby Level)

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4 ,5, 6
See pages 10 thru 11 for Locations

9:00 a.m. – 11:00 a.m.
Session 37: Posters 1
Atlantic Hall B (First Level)

9:00 a.m. – Noon
Technology Corner Exhibits
Atlantic Hall B (First Level)

9:15 a.m. – 10:00 a.m.
Refreshment Break
Atlantic Hall B (First Level)

Noon
ECTC Luncheon
Northern Hemisphere Ballroom D – E (5th Level)

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Atlantic Hall B (First Level)

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12
See pages 12 thru 13 for Locations

2:00 p.m. – 4:00 p.m.
Session 38: Posters 2
Atlantic Hall B (First Level)

2:45 p.m. – 3:30 p.m.
Refreshment Break
Atlantic Hall B (First Level)

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Atlantic Hall B (First Level)

7:00 p.m. – 9:00 p.m.
Plenary Session
Southern Hemisphere Ballroom III (5th Level)

Thursday, June 2, 2011

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2 (Lobby Level)

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere Ballrooms E 3-4 (5th Level)

7:30 a.m. – 4:00 p.m.
Conference Registration
Australia 3 Foyer (Lobby Level)

8:00 a.m. – 4:00 p.m.
Companion Hospitality Room
Europe 3 (Lobby Level)

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14 thru 15 for Locations

9:00 a.m. – 11:00 a.m.
Session 39: Posters 3
Atlantic Hall B (First Level)

9:00 a.m. – Noon
Technology Corner Exhibits
Atlantic Hall B (First Level)

9:15 a.m. – 10:00 a.m.
Refreshment Break
Atlantic Hall B (First Level)

Noon
CPMT Luncheon
Northern Hemisphere Ballrooms D – E (5th Level)

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Atlantic Hall B (First Level)

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16 thru 17 for Locations

2:00 p.m. – 4:00 p.m.
Session 40: Posters 4
Atlantic Hall B (First Level)

2:45 p.m. – 3:30 p.m.
Refreshment Break
Atlantic Hall B (First Level)

6:30 p.m. – 7:30 p.m.
Gala Reception
Lake Terrace (Outside on the SWAN property)
Rain Backup: Northern Hemisphere Ballrooms D – E (5th Level)

8:00 p.m. – 10:00 p.m.
CPMT Seminar
Southern Hemisphere Ballroom III (5th Level)

Friday, June 3, 2011

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2 (Lobby Level)

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere Ballrooms E 3 – 4 (5th Level)

7:00 a.m. – 8:00 a.m.
CPMT and YOUR CAREER
Northern Hemisphere Ballroom E 1 (5th Level)

7:30 a.m. – Noon
Conference Registration
Australia 3 Foyer (Lobby Level)

8:00 a.m. – Noon
Companion Hospitality Room
Europe 5 (Lobby Level)

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18 thru 19 for Locations

8:30 a.m. – 10:30 a.m.
Student Poster Session
Northern Hemisphere D - E Foyer (5th Level)

9:15 a.m. – 10:00 a.m.
Refreshment Break
Southern Hemisphere Ballroom Foyer (5th Level)

Noon
Program Chair Luncheon
Northern Hemisphere Ballrooms D – E (5th Level)

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20 thru 21 for Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Southern Hemisphere Ballroom Foyer (5th Level)

All ECTC events will be taking place in the WDW Dolphin Resort unless otherwise specified

ECTC 2012

The 62nd Electronic Components and Technology Conference

May 29- June 1, 2012

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