High Density Packaging Needs for Next Generation Connected Markets

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Contents

• Industry Advanced Packaging
  • System integration and COO optimization
• eWLB as high density packaging platform
• Conclusion
System Integration Trends (1/5)

- Analog Wifi
- BB PMIC RF/RFFEM
- MEMS CIS Display Drivers
- Application Processors AP+BB AP+DRAM 5G Modules
- FPGA HPC Processors + Memories

Relationship between number of IOs and package size:

- Analog Wifi: 2x2
- BB PMIC RF/RFFEM: 5x5
- MEMS CIS Display Drivers: 10x10
- Application Processors AP+BB AP+DRAM 5G Modules: 15x15
- FPGA HPC Processors + Memories: >20x20

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System Integration Trends (2/5)
System Integration Trends (3/5)

- **LOW END**
  - QFN, P
  - WLCSP
  - FC-MIS
  - FOWLP
  - Multi-die FOWLP
  - Single side RFFEM

- **MIDDLE END**
  - Migration from QFN->WLP
  - Multi -die SIP
  - FOWLP
  - Low cost substrates & MIS

- **HIGH END**
  - FPGA
  - Large Processors
  - CPU + Memories
  - GPU, CPU
  - CPU + Memories
  - Application Processors
  - AP+BB
  - AP+DRAM
System Integration Trends (4/5)

- Higher density interposer - POP
- POP Module subsystem
- Double sided RFFEM
- Effective memory integration
- Antenna in package for 5G

- MLP, Interposer POP
- FOWLP-POP
- POP Module Subsystem
- Double side RFFEM
- 5G Module with antenna in package

- FPGA
- Large Processors + Memories

- Code, Power
- RF, RFFEM
- BB
- PMIC

- Package size
  - 2x2
  - 5x5
  - 10x10
  - 15x15
  - 20x20
  - >20x20
  - >>20x20

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System Integration Trends (5/5)

Large Body fcBGA
2.5D TSI- SIP
High Density Fan out
EMIB

Application Processors
AP+BB
AP+DRAM

Codec
Power
Wifi

BB
PMIC
RF/RFFEM

MEMS
CIS
Display Drivers

Package size

# of IOs

2x2
5x5
10x10
15x15
20x20
>20x20
>>20x20

5G Module with antenna in package for network
Packaging Technology Towards 4G+/5G

Increased functionality/performance

Decreased form factor

Time

SS MBGA w/Passive

SS MBGA SIP

SS MBGA SIP w/EDS

DS MBGA SIP

Embedded Antenna in Package

Discrete Antenna in Package
eWLB - high density packaging platform
High Density eWLB Package

eWLB and Fan out packages can serve as means of high density packaging
An Example is shown here

Package Configuration (3L RDL)

<table>
<thead>
<tr>
<th>Package Configuration (3L RDL)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die Size</strong></td>
<td>11.16 x 5.58 mm &amp; 11.16 x 5.58 mm</td>
</tr>
<tr>
<td><strong>PKG Size</strong></td>
<td>15x15mm</td>
</tr>
<tr>
<td><strong>Ball Composition</strong></td>
<td>SAC305</td>
</tr>
<tr>
<td><strong>Ball Pitch (Bottom / Top)</strong></td>
<td>400um / 200um</td>
</tr>
<tr>
<td><strong>Die Thickness (min)</strong></td>
<td>200um</td>
</tr>
<tr>
<td><strong>RDL Stack Thickness (nominal)</strong></td>
<td>39um</td>
</tr>
<tr>
<td><strong>Package ball height/size</strong></td>
<td>185um</td>
</tr>
<tr>
<td><strong>PKG Total Thickness (nominal)</strong></td>
<td>424um</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RDL Stack</th>
<th>39um +/- 10um</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSV1</td>
<td>4um +/- 1.0um</td>
</tr>
<tr>
<td>RDL1</td>
<td>3um +/- 1.0um</td>
</tr>
<tr>
<td>PSV2</td>
<td>5um +/- 1.0um</td>
</tr>
<tr>
<td>RDL2</td>
<td>4um +/- 1.0um</td>
</tr>
<tr>
<td>PSV3</td>
<td>6um +/- 1.5um</td>
</tr>
<tr>
<td>RDL3</td>
<td>8um +/- 1.5um</td>
</tr>
<tr>
<td>PSV4</td>
<td>9um +/- 1.5um</td>
</tr>
<tr>
<td>Bump Height (SAC305)</td>
<td>185um</td>
</tr>
</tbody>
</table>
# Technology: Fine Pitch RDL1 – Litho, Plating and etching

Fine Pitch RDL Development successfully completed

<table>
<thead>
<tr>
<th>RDL1 Litho (2um L/S)</th>
<th>RDL1 after Plating/Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>• BTM CD ~ 2.03um</td>
<td>• RDL1 thickness ~ 2.82 um</td>
</tr>
<tr>
<td>• Sidewall Angle ~ 85°</td>
<td>• BTM CD ~ 2.34um</td>
</tr>
<tr>
<td></td>
<td>• Sidewall Angle ≥ 85°</td>
</tr>
<tr>
<td></td>
<td>• No undercut</td>
</tr>
</tbody>
</table>

![Image showing RDL1 Litho and RDL1 after Plating/Etch](image-url)
**Technology: RDL2**

<table>
<thead>
<tr>
<th>RDL2 Litho (5um L/S)</th>
<th>RDL2 after Plating/Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>• BTM CD ~ 5.2um</td>
<td>• RDL thickness ~ 4.1 um</td>
</tr>
<tr>
<td>• Sidewall Angle ≥ 85°</td>
<td>• BTM CD ~ 5.0um</td>
</tr>
<tr>
<td></td>
<td>• Sidewall Angle ≥ 85°</td>
</tr>
<tr>
<td></td>
<td>• No undercut</td>
</tr>
</tbody>
</table>

- BTM CD: Bottom Metal CD
- L/S: Line/Space
- RDL: Redistribution Layer
- CD: Critical Dimension
- Sidewall Angle: The angle at which the sidewall meets the horizontal plane.
Technology: 3L RDL – PSV Via Stack and RDL Stack

- 3L RDL Stack
- Stacked Via
Technology: RDL 1 (2μ L/S)
Technology: RDL1 Connection – between Die 1, Die 2
Conclusion
Micro-Electronics Industry: Paradigm Changes

• Heterogeneous Integration is key enabler to solve the next decade’s system challenges
• Diverse packaging solutions will provide customers with cost-effective solutions
• Successful product introductions will be facilitated by partnership and collaboration across supply chain partners:
  • OEMs/system houses
  • Design houses
  • Foundries/OSATs
  • Materials suppliers
  • Component vendors