# Heterogeneous Integration at DARPA: Pathfinding and Progress in Assembly Approaches

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Presented by Jeffrey C. Demmin, Booz Allen Hamilton

68th IEEE Electronic Components and Technology Conference

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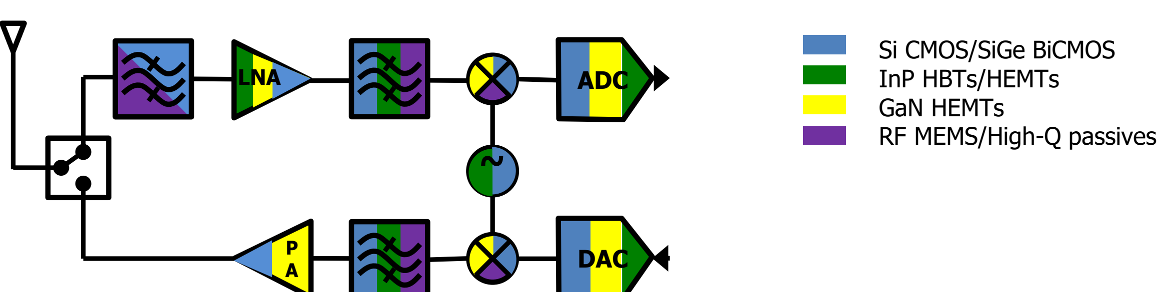
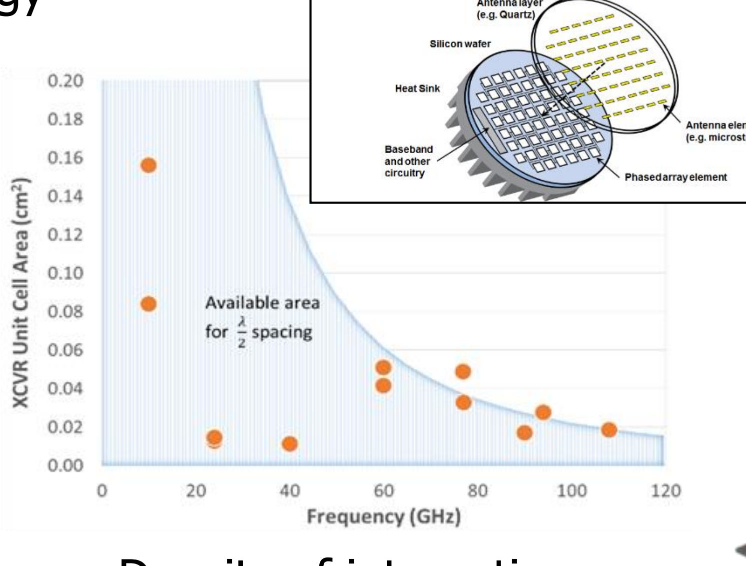
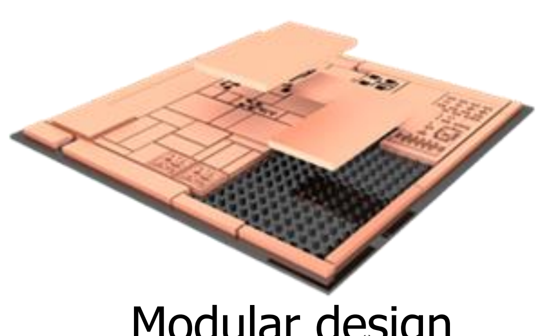
# Why Heterogeneous Integration?




Best of breed technology




Density of integration



Modular design

Sources: DARPA, UCSD

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# Civilian and defense needs overlap at the leading edge

Gbps
100
10
1
Mbps
100
10
1
kbps
100
10
1
bps
100
10

5G
WGS-DL
WGS-UL
5G
4G LTE
WiFi
TTNT
3G UMTS
EPLRS
Link 16
2G GSM
SINCGARS
Link 11
MILSTAR/AEHF-DL
MILSTAR/AEHF-UL
GPS

1 MHz
10 MHz
100 MHz
1 GHz
10 GHz
100 GHz

Frequency

Source: DARPA

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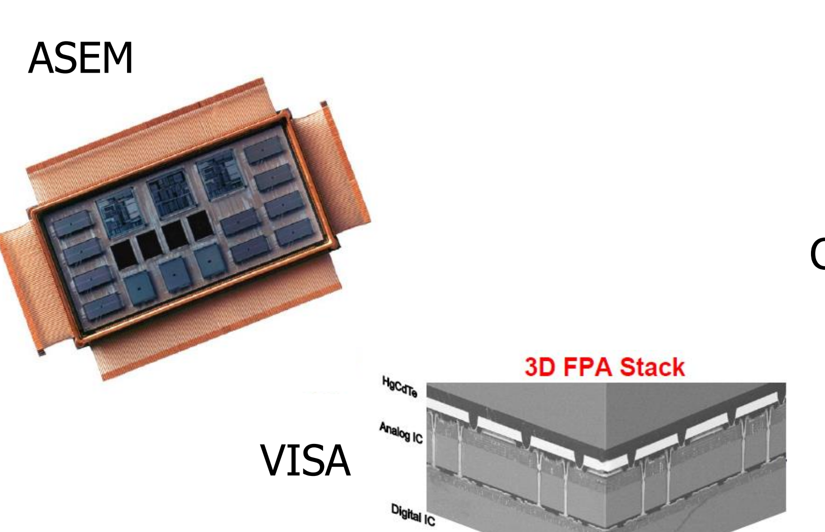
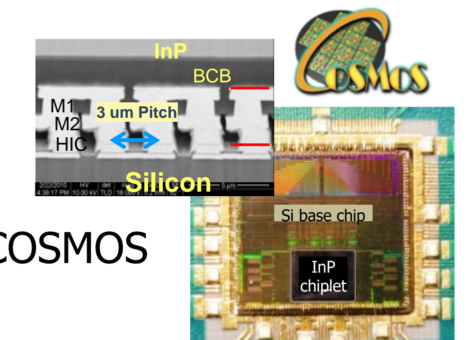
# DARPA's long history of innovation in integration

ASEM

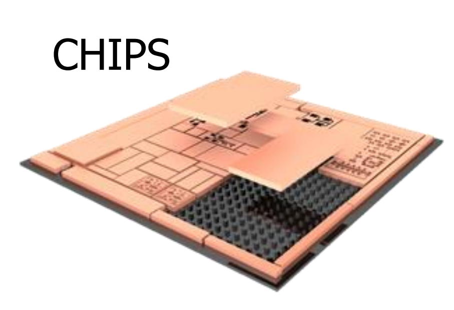



VISA




COSMOS

CHIPS



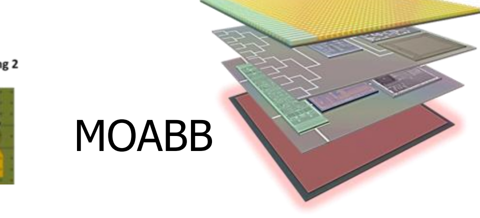
3D-IC

DAHI

E-PHI

Ring 1 Heater 1 Si III-V Gain 1 2 Heater 2 Ring 2

MOABB



ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s 2000s 2010s 2020s

Sources: DARPA, Smithsonion Chips

# What is heterogeneous integration?

CHIPS: modular design

Heterogeneous devices

Anode
p-Si
p-GaN
$Al_{0.82}Ga_{0.18}N$
Graded 100-200nm
AlN
AlGaN/AlGaN, QW/QB
AlN
Graded 100-200nm
$Al_{0.82}Ga_{0.18}N$
Cathode
Cathode
n-$Al_{0.82}Ga_{0.18}N$: Si
AlN substrate

DAHI: wafer scale

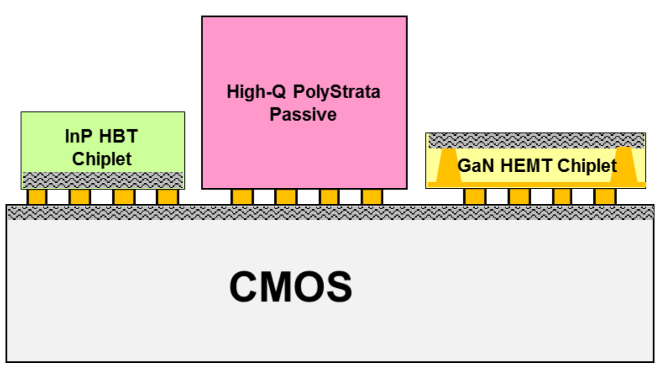
130 nm
Si CMOS
Cu/$SiO_2$
Bond
Interface
250 nm
InP HBT

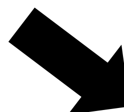
DAHI: RF power

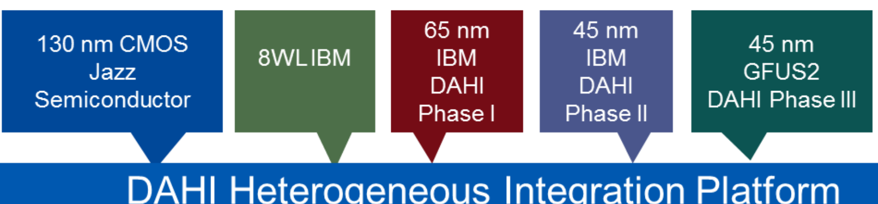
Si/SiGe
GaN
$Al_2O_3$/AlN

Source: DARPA

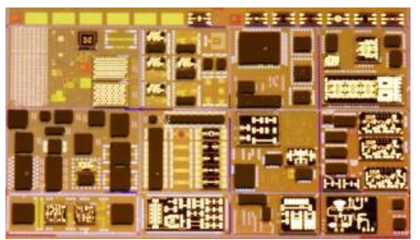
# DARPA's DAHI program:
# Diverse Accessible Heterogeneous Integration



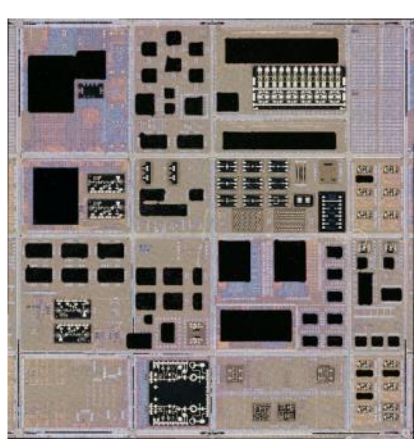





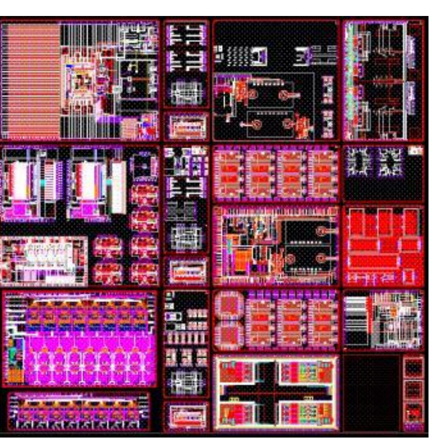

**Picture of MPW0 Reticle**



**Picture of MPW1 Reticle**



**MPW2**



**MPW3 in Fab**

Sources: DARPA, Northrop Grumman

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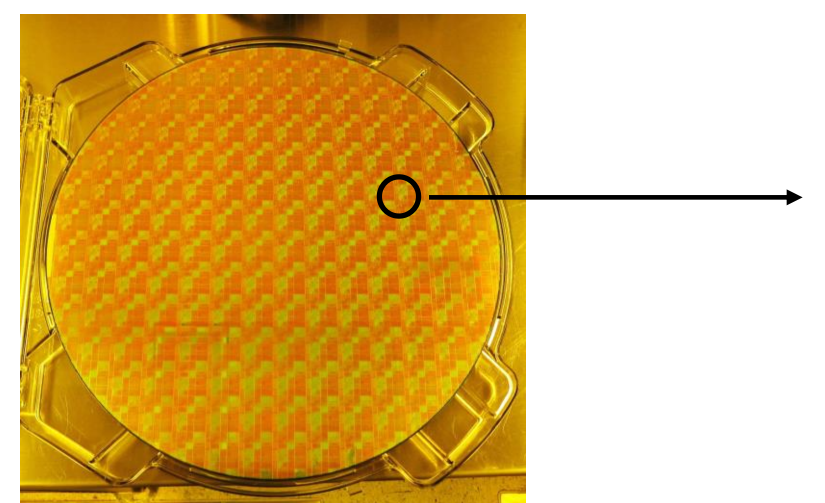
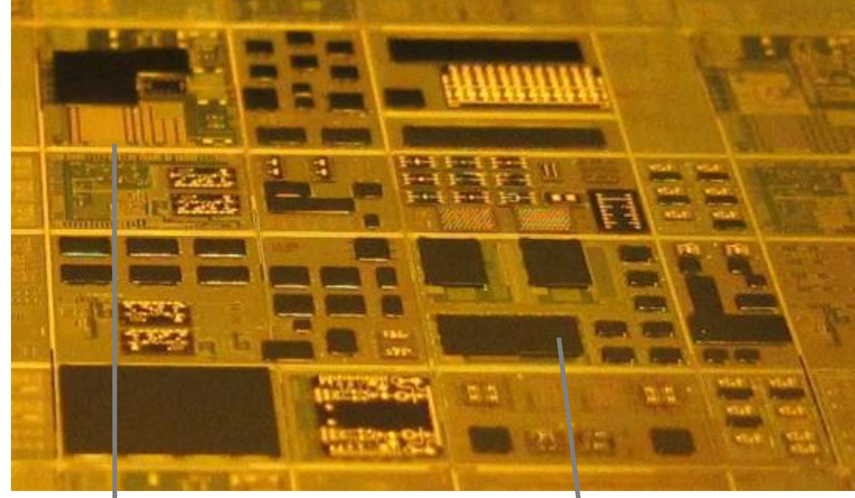
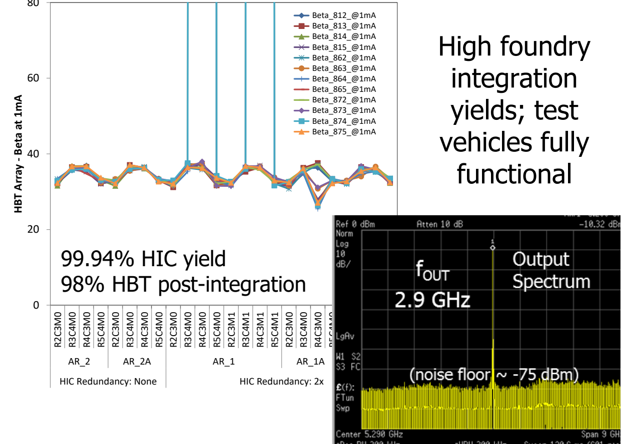
# DAHI snapshot: Excellent yield, demonstrated RF performance



300mm diameter Si CMOS wafer (45nm node)

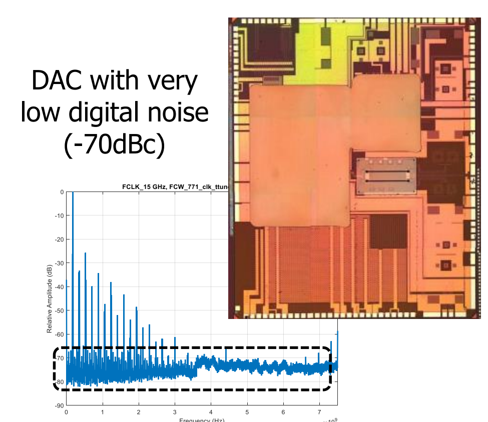


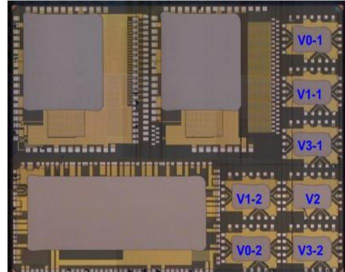
DAHI integration: Si (45nm), InP (TF5 HBT), GaN (GaN20 HEMT)




High foundry integration yields; test vehicles fully functional

DAC with very low digital noise (-70dBc)






Successful testing identified optimal S/H circuit for ADC (>65dB SFDR @ 2GHz)

Sources: DARPA, Northrop Grumman

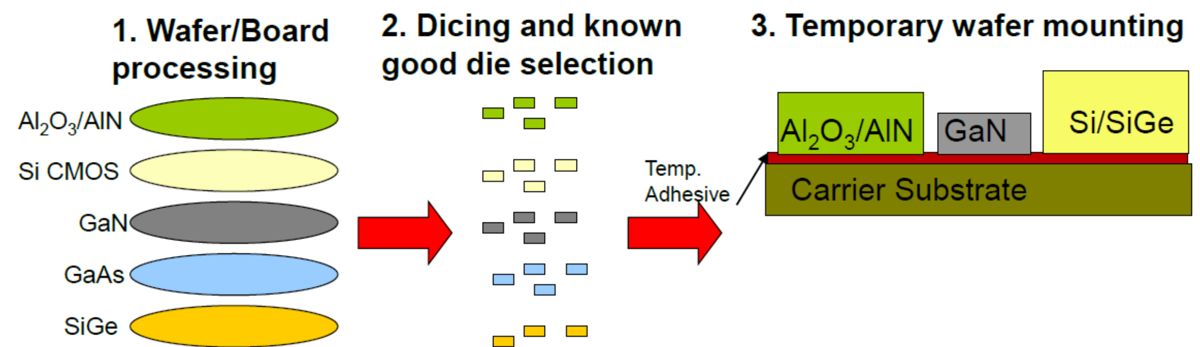
# DAHI simplicity enables rapid evolution

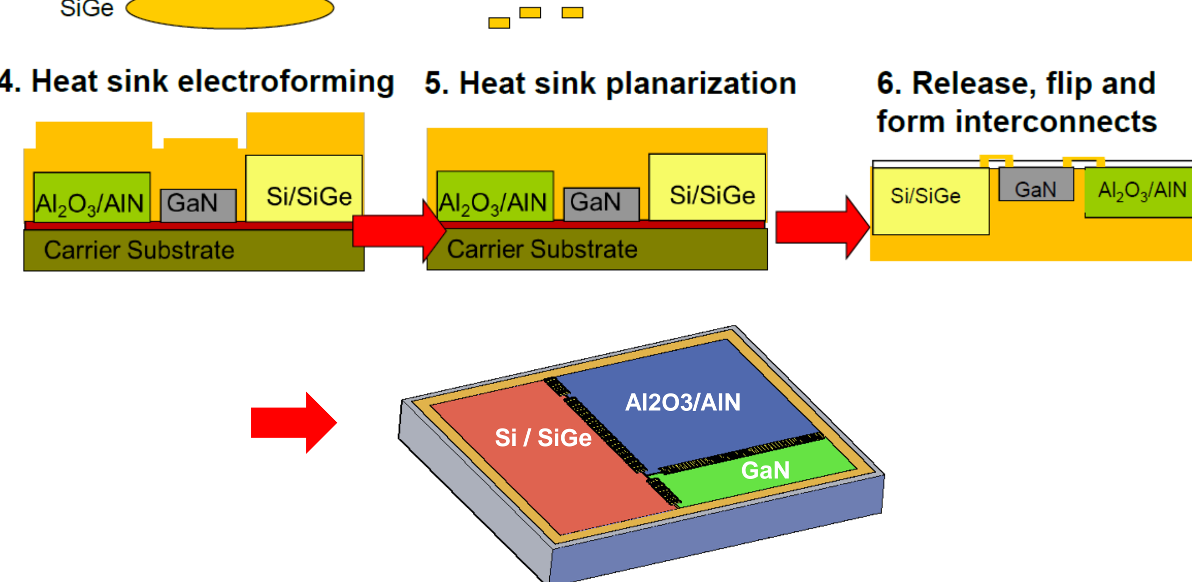
| Technology | MPW0 | MPW1 | MPW2 | MPW3 | Future MPWs |
|---|---|---|---|---|---|
| **CMOS** | IBM 65nm | GF 45 nm | GF 45 nm | GF 45 nm | GF 45 nm |
| **InP HBT** | TF4 (2 metals) | TF4 (3 metals) | TF4 (4 metals) | TF4 (4 metals) | TF4 (4 metals) |
| | | TF5 (3 metals) | TF5 (4 metals) | TF5 (4 metals) | TF5 (4 metals) |
| **InP Varactor Diode** | | | | | AD1 |
| **GaN HEMT** | GaN20 | GaN20 | GaN20 | GaN20 | GaN20 |
| | T3 (HRL) | T3 (HRL) | T3 (HRL) | T3 (HRL) | T3 (HRL) |
| **GaAs HEMT** | | | | P3K6 | P3K6 |
| **Passive Components** | | PolyStrata (Nuvotronics) | PolyStrata (Nuvotronics) | PolyStrata (Nuvotronics) | PolyStrata (Nuvotronics) |
| **Base Substrate** | CMOS | CMOS | CMOS | CMOS | CMOS |
| | | | | SiC Interposer (IWP5) | SiC Interposer (IWP5) |
| | | | | In fab | |

Sources: DARPA, Northrop Grumman

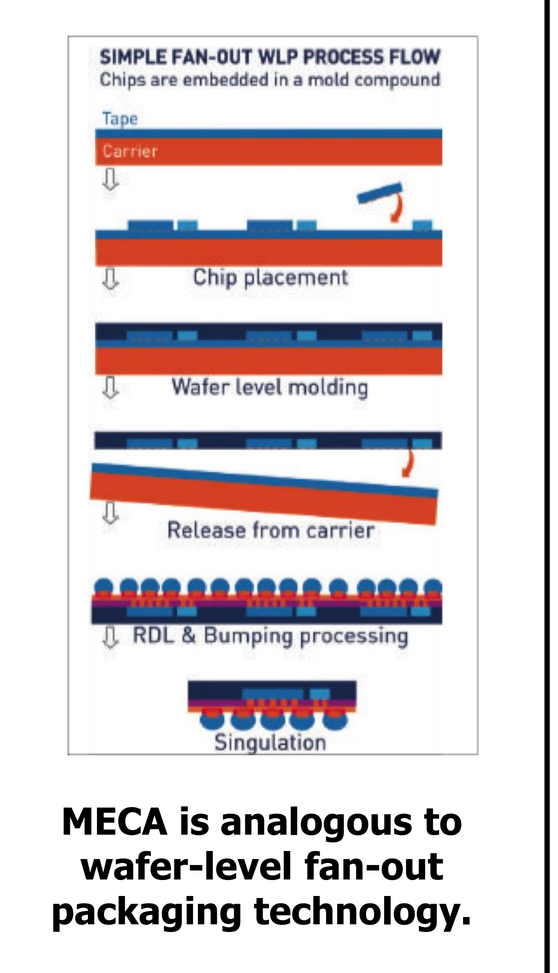
# Metal Embedded Chip Assembly (MECA)

**MECA enables heterogeneous integration with a metal interconnect platform for high-power requirements.**




**MECA-integrated heterogeneous module**

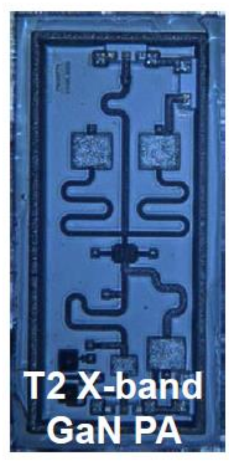


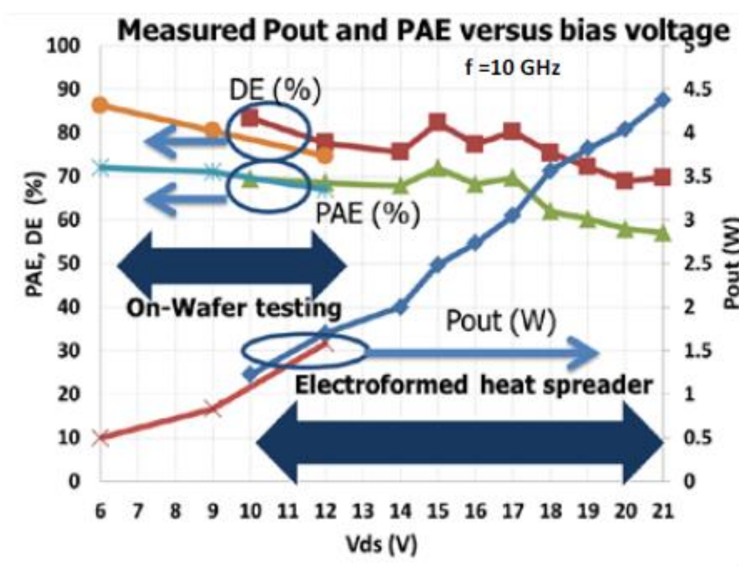

**MECA is analogous to wafer-level fan-out packaging technology.**

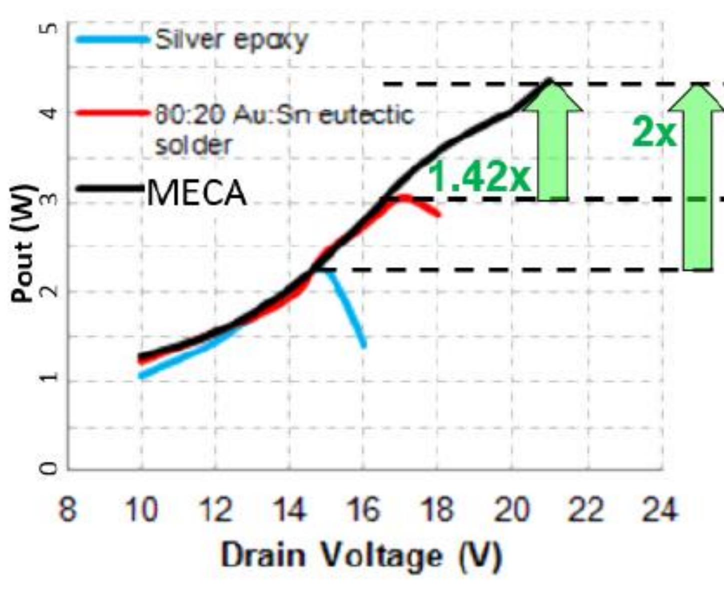
Sources: HRL, Solid State Technology

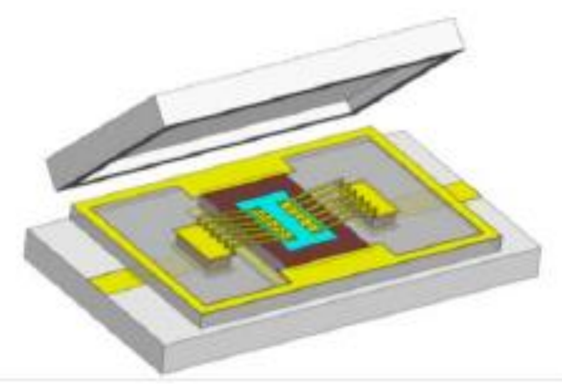
# MECA-enabled performance upgrade

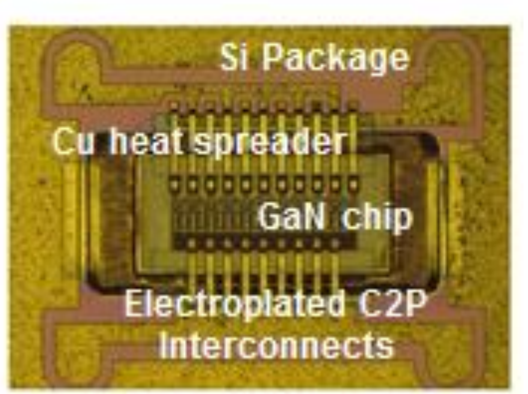
**Integration in electroformed heat spreader: 1.4-2x improvement in PA performance**






Source: HRL

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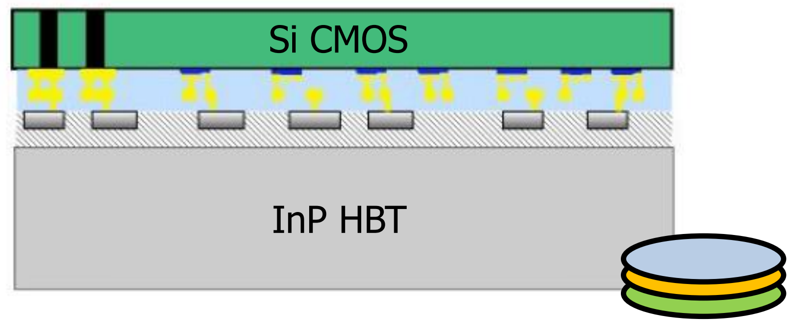
# DAHI chip-scale phased arrays

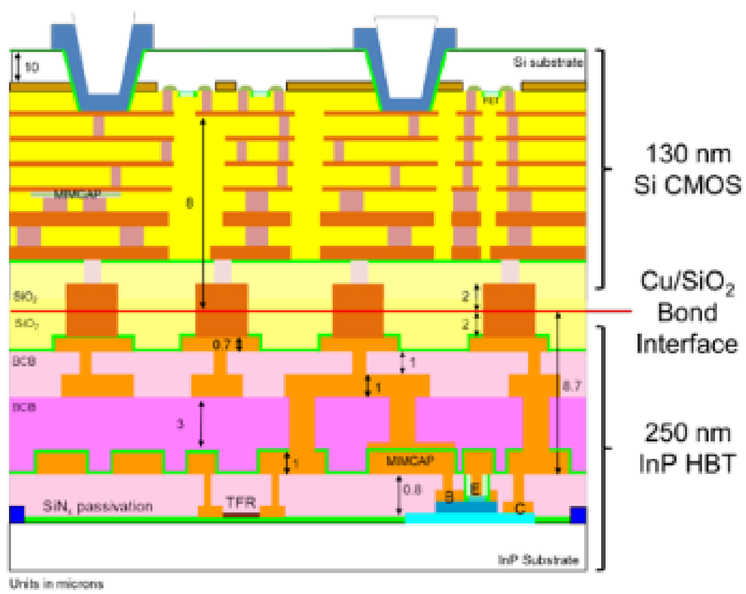
## Heterogeneous integration for mm-wave: Phased array beamformers

- Can maintain $\lambda/2$ channel spacing as frequencies increase
- CMOS control circuitry closely integrated with RF chain
- Improved channel performance and efficiency with addition of III-V devices
- Fully integrated beamformer channels demonstrated with integrated InP devices and Si control electronics
- >100mW Pout Tx channel, 4.5 dB NF Rx

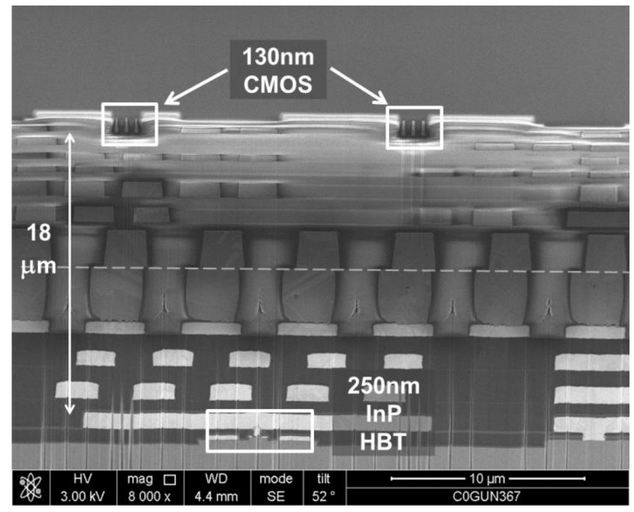
## Wafer-level heterogeneous integration




## Integration schematic




## InP/CMOS with DBI Process




DBI = Direct Bond Interconnect

Source: Teledyne

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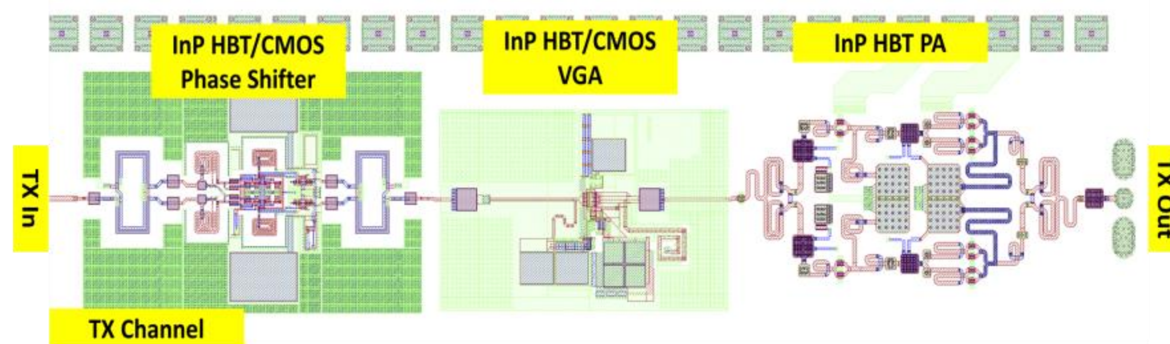
# DAHI InP/CMOS beamformer performance

**Q-band InP/CMOS Tx Channel Layout**

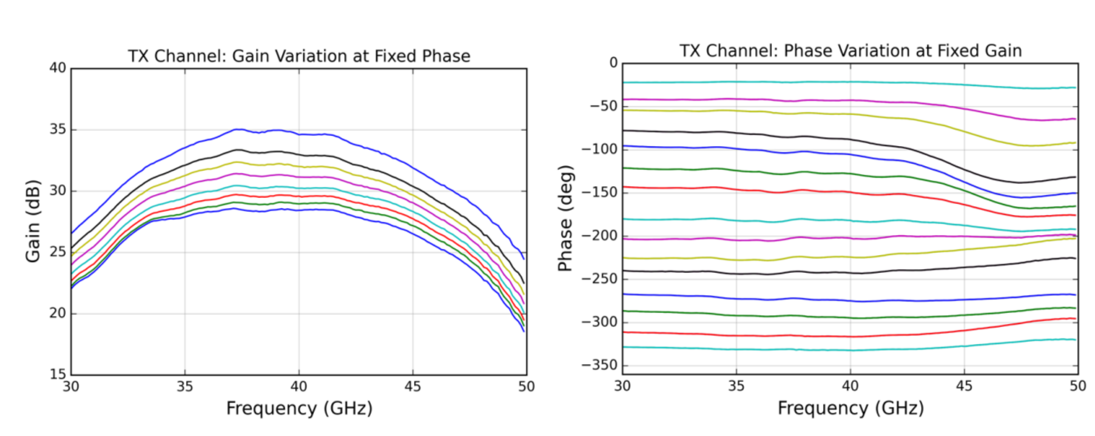



**Channel dimensions: 3.0x0.6mm²**

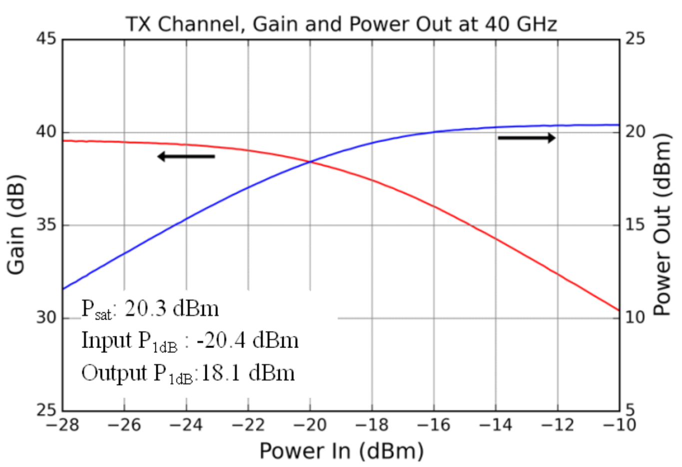
## Q-band Tx Channel

- 57 HBTs, 1704 CMOS gates, 76 HICs
- Pdiss ~ 1W
- 28-35 dB gain variation
- 5° RMS phase error at 40 GHz
- 20.3 dBm Psat, 18.1 dBm P1dB

**Measured Gain and Phase Variation**




**Measured Tx Channel Power**




Source: Teledyne

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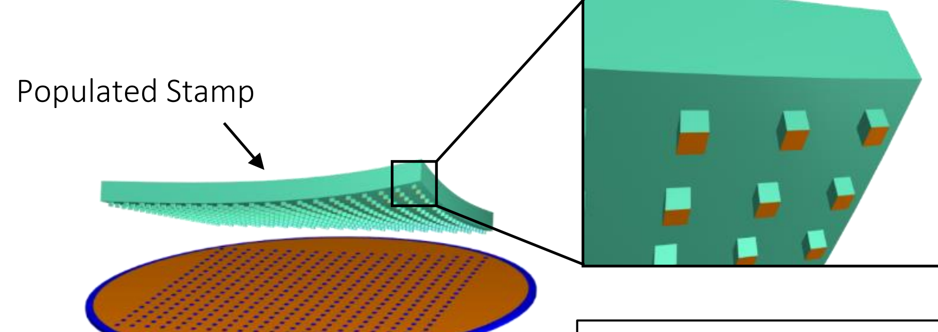
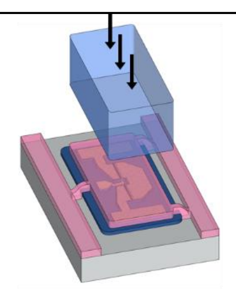
# Advancing integration to the device level

## Microtransfer Printing

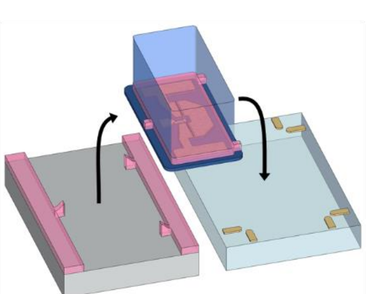


1. Fabricate GaN devices on $Nb_2N$ template on SiC substrate using standard fabrication processes.

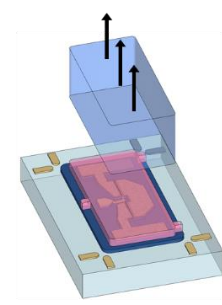
2. Mask known-good GaN devices for transfer and recess etch to gain access to $Nb_2N$ layer.



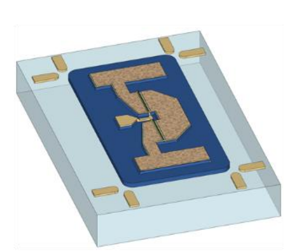
3. Pattern photoresist anchors and protective mask. Selectively etch $Nb_2N$ layer using $XeF_2$ reactive gas.



4. Transfer print GaN device to target substrate using polymer stamp and optional adhesive.



5. Release GaN device from polymer stamp.



6. Remove photoresist protective mask from transferred GaN device.

Source: Naval Research Laboratory

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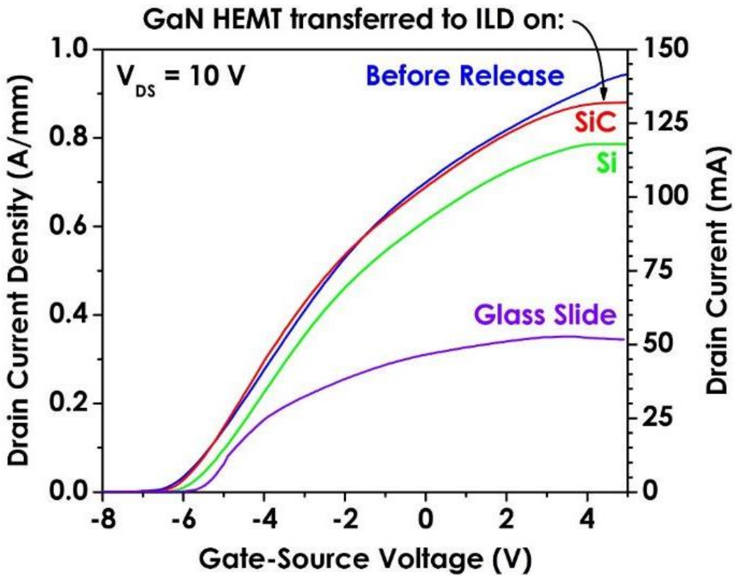
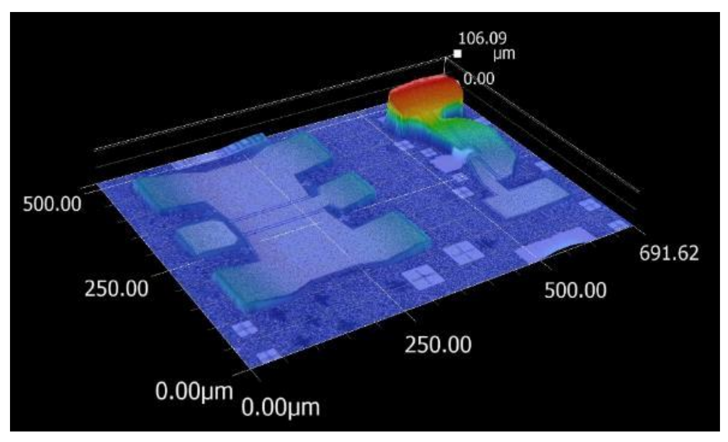
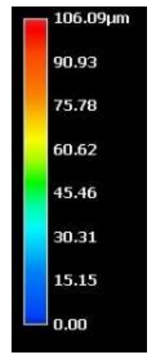
# Transferred device results

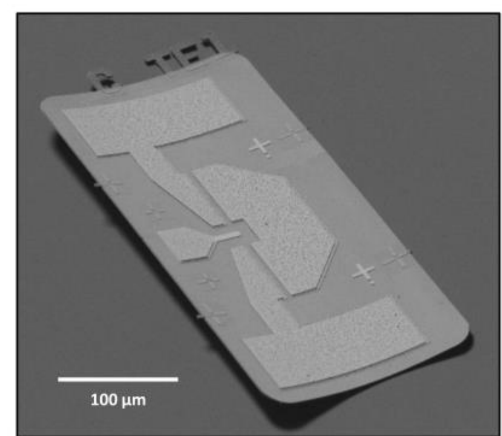
## Microtransfer Printing: GaN HEMT




## Challenges to managing thin-film strain




Source: Naval Research Laboratory

# Transfer printing to *create* a device

**Transfer printing can stack nano-membrane layers to create junctions and devices**

(a) Source wafers
p-Si mesa on i-Si SOI
P-Si
i-Si
p-Si NM release with PDMS
i-AlGaN QW on AlN subs.
p-Si NM print on i-AlGaN QWs
AlN substrate removal
n-Si SOI
n-Si
n-Si NM release with PDMS
n-Si/i-AlGaN/p-Si junction
n-Si NM
i-AlGaN
p-Si NM

Transfer printed
p-Si/i-AlGaN/n-Si junction
n-Si
i-AlN
i-AlGaN QW
i-AlN
i-Si
p-Si

SiNM
GaN

Sources: U. of Wisconsin, Michigan State U.

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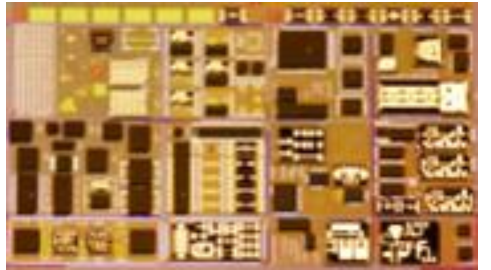
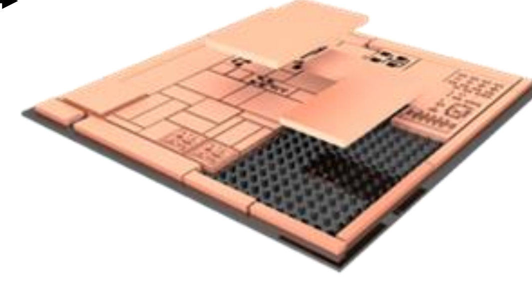
# Common Heterogeneous Integration and IP Reuse Strategies: The next step in heterogeneous integration



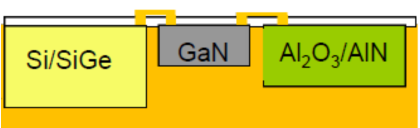
CHIPS: modular design

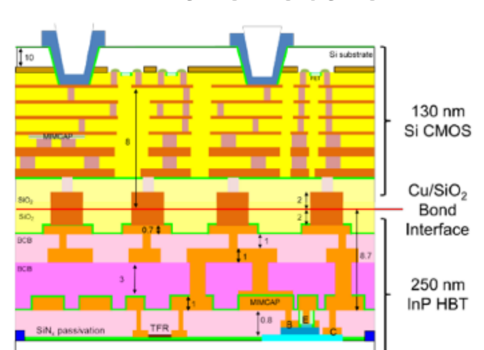


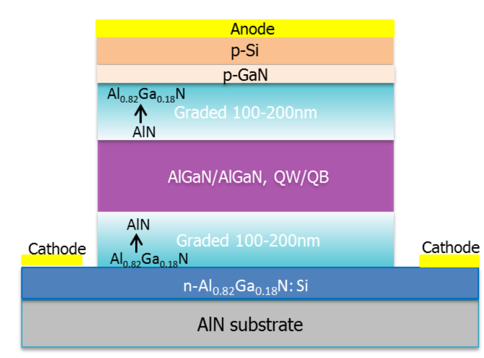
Integration technologies

Heterogeneous devices

DAHI: wafer scale




Source: DARPA

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# Integration impact driven by **Standards** and **Modularity**

Image: Intel

| Year | Milestone |
|---|---|
| 1936 | "Printed circuit board" invented by Paul Eisler. |
| 1941 | Early PCB demo in a radio. |
| 1943 | First HVM PCBs enable proximity fuze during WWII. |
| 1956 | Patent to US Army for PCB assembly. |
| 1957 | IPC (Institute for Printed Circuits) founded; standards follow. |
| 1960 | Multi-layer PCB invented. |
| 1980s | Surface Mount Technology on PCBs revolutionizes manufacturing. |
| 1995 | HDI / Microvia technology enables further integration. |
| 2006 | First package-on-package standard from JEDEC |

**DoD jump-start**

**PCB industry sees steady expansion with DoD origins, standardization, and technology development.**

Global PCB Revenue ($M)

$70,000 · $60,000 · $50,000 · $40,000 · $30,000 · $20,000 · $10,000 · $-

1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016

**Computers, smartphones, and tablet sales: 1975-2011**

Unit sales (thousands)

500,000 · 450,000 · 400,000 · 350,000 · 300,000 · 250,000 · 200,000 · 150,000 · 100,000 · 50,000 · 0

1975 1980 1985 1990 1995 2000 2005 2010

Smartphones

Computers

Tablets

Sources: Prismark, Arstechnica, USPTO, Wikipedia, IPC, SMTA

# End of Moore's Law?

## Moore's Law

Relative Manufacturing Cost/Component

$10^5$, $10^4$, $10^3$, $10^2$, 10, 1

1962
1965
1970

1, 10, $10^2$, $10^3$, $10^4$, $10^5$

Number of Components Per Integrated Circuit

The Economist

**Faith no Moore**

Selected predictions for the end of Moore's Law

Cited reason: Economic limits, Technical limits

*Prediction issued* — *Predicted end date*

1995 2000 2005 2010 2015 2020 2025 2030

| Predictor | Prediction issued | Predicted end date |
|---|---|---|
| **Gordon Moore**, Intel | 1995 | 2005 |
| **G. Dan Hutcheson**, VLSI Research | 1996 | 2003 |
| **Isaac Chuang**, IBM Research | 2000 | 2020 |
| **Paolo Gargani**, Intel | 2003 | 2021 |
| **Lawrence Krauss**, Case Western, and **Glenn Starkman**, CERN | 2004 | approx. 2600 |
| **Gordon Moore**, Intel | 2005 | 2015–25 |
| **Michio Kaku**, City College of NY | 2011 | 2021–22 |
| **Robert Colwell**, DARPA; (fmr) Intel | 2013 | 2020–22 |
| **Gordon Moore**, Intel | 2015 | 2025 |

Sources: Press reports; *The Economist*

Economist.com

**Changes in silicon industry will be felt by compound semiconductors**

Source: Electronics Magazine, Economist.com

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# Moore’s Law INCLUDES Heterogeneous Integration

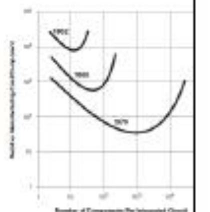
It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

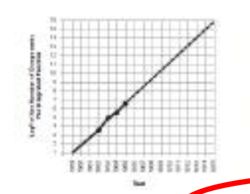
The experts look ahead

## Cramming more components onto integrated circuits

**With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip**

By Gordon E. Moore

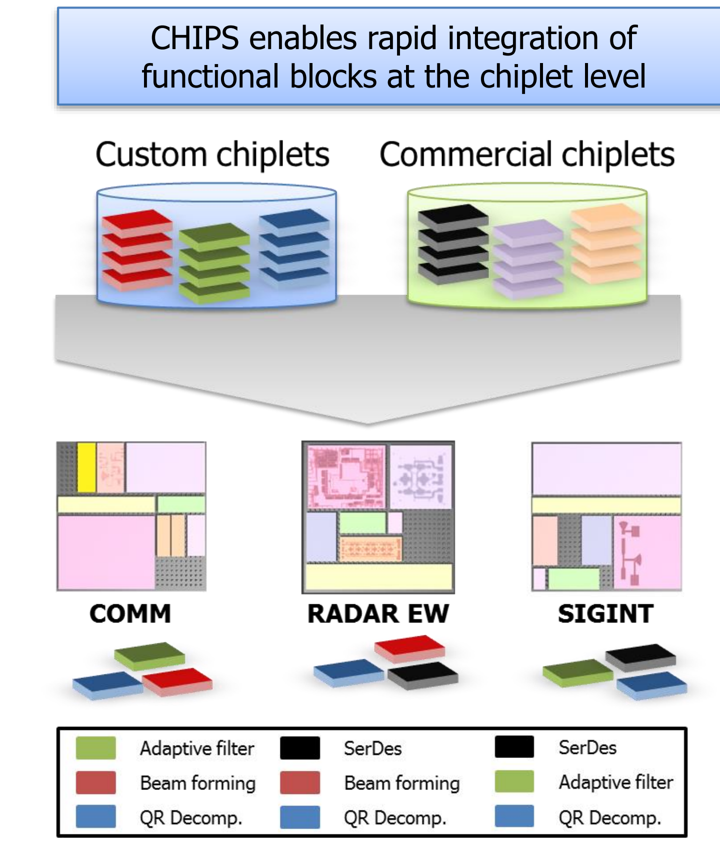




**G. E. Moore** is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

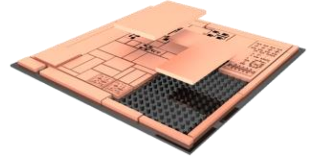
# What is CHIPS?

**CHIPS** will develop design tools, integration standards, and IP blocks required to demonstrate modular electronic systems that can leverage the best of DoD and commercial designs and technology.




Source: DARPA

# CHIPS developing interface standard



**CHIPS Target**

| CHIPS Program Interface Standard Metrics | |
|---|---|
| Data rate | 10 Gpbs |
| Energy efficiency | < 1 pJ/bit |
| Latency | < 5 ns |
| Bandwidth density | > 1000 Gbps/mm |

Bandwidth density / energy per bit (Gbps/mm) / (pJ/bit)

100,000
10,000
1,000
100
10
1

0.1
1
10
100
1000

Interconnect Length (mm)

Single-ended
EMIB
Ground ref.
Differential
HBM
SerDes
Co-ax

- 28nm SOI, Single-ended, Al on Si
- 28nm, ground-ref., single-ended, organic PCB
- 45nm SOI, differential, Cu on Si
- 32nm, differential, 32AWG cable
- EMIB
- 14nm SERDES, PCB
- 14nm HBM

Sources:
1. 2016 *JSSC*, Dehlaghi
2. 2013 *JSSC*, Poulton
3. 2012 *JSSC*, Dickson
4. 2013 *JSSC*, Mansuri
5. 2016 *ECTC*, Mahajan

**CHIPS interface is one of many possible routes for efficient interdie communications**

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# CHIPS program: structure and timing

| PHASE 1 | PHASE 2 | PHASE 3 |
|---|---|---|
| Interface and IP Block Demo | Module Demo with IP Blocks | Rapid Module Upgrade |
| Integration platform → Interface demo | Full system IP reuse demo | Reconfigured demo |



| | |
|---|---|
| TA1 | Modular Digital Systems |
| TA3 | Supporting Technologies |
| TA2 | Modular Analog Systems |

**Seeking CHIPS collaboration to help drive a common interface**

Source: DARPA

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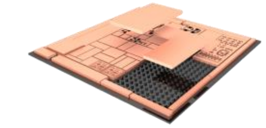
# CHIPS: August 2017 Kickoff



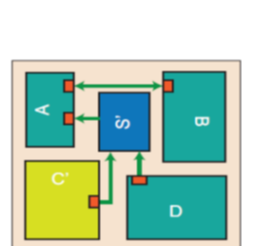
## CHIPS Team

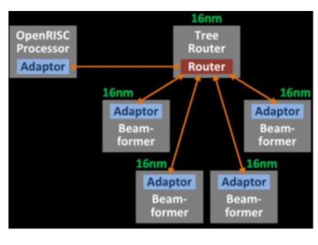
**Designs**
- Boeing
- Intel
- Lockheed Martin
- Northrop Grumman
- Univ. of Michigan

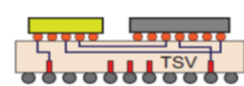
**Chiplets**
- Intrinsix
- Jariet
- Micron
- North Carolina State
- Synopsys

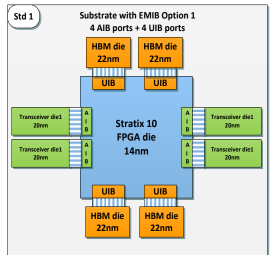
**Tools**
- Cadence
- Georgia Tech

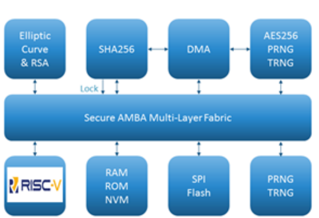
## CHIPS Approach
**Modularity**
**Standards**

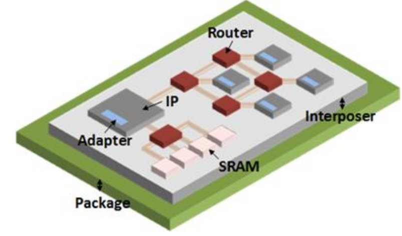



## CHIPS Results
**Fast**
**Cost-Effective**
**Best-in-Class**

Images sources:
Lockheed Martin, Boeing, Intel,
Intrinsix, Univ. of Michigan, 3GPP.org

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# What’s next?

# Electronics Resurgence Initiative

- ERI—creating an electronics capability that will provide a foundational contribution to national security
- Three thrust areas: Materials and Integration, Architectures, Designs

**2025 – 2030**
**NATIONAL ELECTRONICS CAPABILITY**

**$216 MILLION**
**TOTAL (FY18)**

**ERI**
**Electronics Resurgence Initiative**

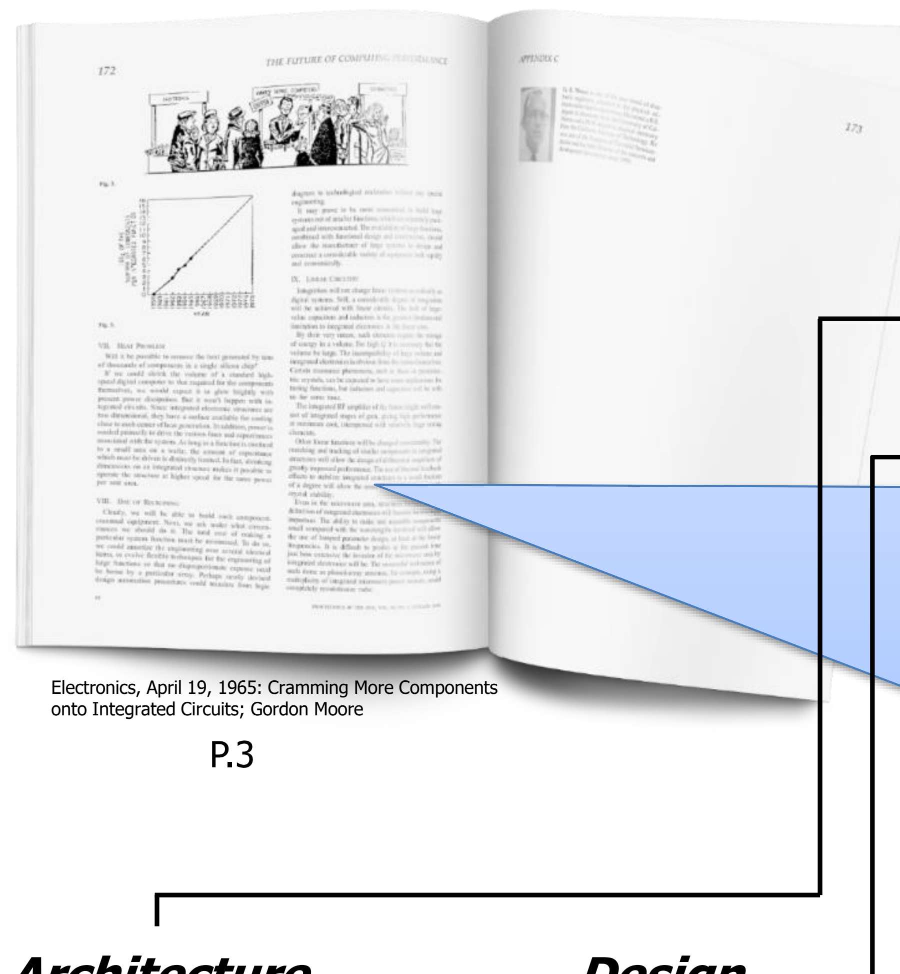
**Page 3 Investments**
$75 million
Of New Funding
(FY18)

$141 million in Current Efforts (FY18)

**MATERIALS** | **ARCHITECTURES** | **DESIGNS**

JUMP + Traditional Programs

# New investment based on "Page 3"



Electronics, April 19, 1965: Cramming More Components onto Integrated Circuits; Gordon Moore

P.3

## VIII. DAY OF RECKONING

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. **The total cost of making a particular system function must be minimized.** To do so, we could amortize the engineering over several identical items, or **evolve flexible techniques for the engineering of large functions** so that no disproportionate expense need be borne by a particular array. Perhaps **newly devised design automation procedures could translate from logic diagram to technological realization** without any special engineering.

It may prove to be **more economical to build large systems out of smaller functions, which are separately packaged** and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

### *Architecture*

Maximizing specialized functions

### *Design*

Quickly enabling specialization

### *Materials & Integration*

Adding separately packaged novel materials and using integration to provide specialized computing

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# Recent DARPA investments and momentum

2016 | 2017 | 2018 | 2019

- 11/2015 N-ZERO Kickoff
- 4/2016 CRAFT Kickoff
- 6/2016 CHIPS Approved
- 8/22/2016 JUMP Approved
- 1/2017 L2M Approved
- 4/2017 HIVE Kickoff
- 4/2017 SSITH BAA Released
- **ERI Launch**

**OTAs signed in 12 month period**

**Electronics Resurgence Initiative**

**JUMP**
*University Driven*

+

**Page 3 Investments**
*Industry Driven*

+

**Traditional Programs**
- N-ZERO
- CRAFT
- CHIPS
- L2M
- HIVE
- SSITH

Intel, Qualcomm, Cadence, Keysight Technologies, Rambus, NVIDIA, XILINX, Flexlogix Technologies, Inc, Micron

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# Investments inspired by Moore's "Page 3"

## Page 3 Investments

| Architectures | Designs | Materials & Integration |
|---|---|---|
| *Domain-Specific System on Chip* (**DSSoC**) – Thomas Rondeau | *Intelligent Design of Electronic Assets* (**IDEA**) – Andreas Olofsson | *Three Dimensional Monolithic System-on-a-Chip* (**3DSoC**) – Linton Salmon |
| *Software Defined Hardware* (**SDH**) – Wade Shen | *Posh Open Source Hardware* (**POSH**) – Andreas Olofsson | *Foundations Required for Novel Compute* (**FRANC**) – Daniel Green |

Heterogeneous Integration directly part of Materials and Integration thrust and indirectly part of Architectures and Design thrusts as well

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# The Challenge: Overcoming Memory Bottleneck

## Current von Neumann architecture spends more time moving data than processing it

| | Neural Programmer (LSTM) | ResNet-152 (CNN) | Alex Net (CNN) |
|---|---|---|---|
| Compute | 8% | 20% | 15% |
| Memory | 92% | 80% | 85% |

*Data from S. Mitra of Stanford*

Data for 7nm instantiation of a state-of-the-art Machine Learning accelerator

<u>Accelerators don’t help (enough) if using the same architecture</u>

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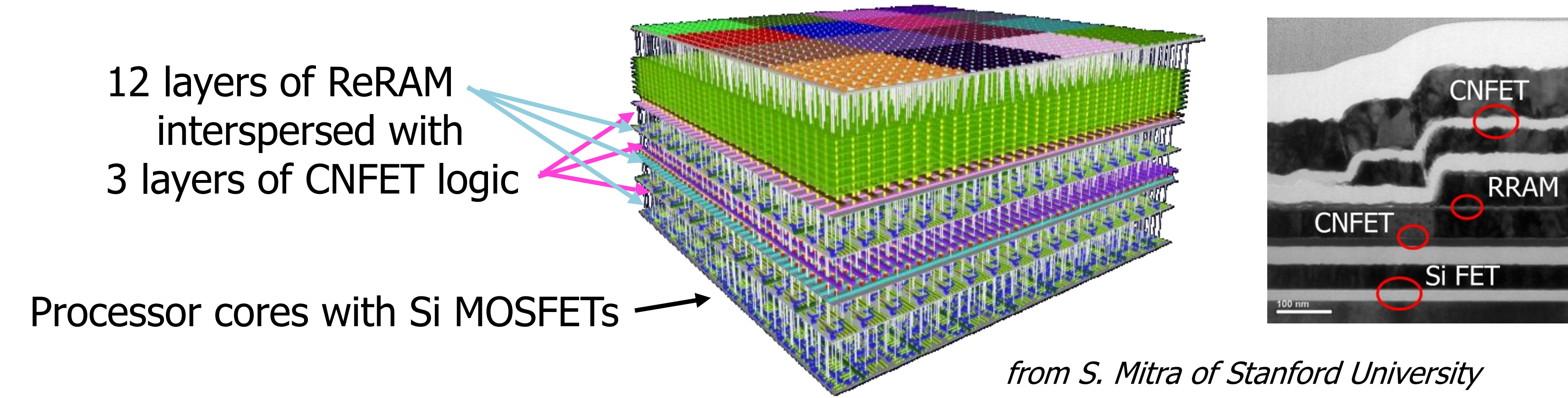
# An Integrated, Monolithic SoC (3DSoC) Solution

*An example of an integrated flow that fabricates 3D logic and memory on a single die*




*from S. Mitra of Stanford University*

*Note: This is an example only. Other technical approaches are expected.*

## **Critical characteristics for a monolithic solution**

- Must permit new architectures that leverage fast, configurable access to non-volatile main memory
- Stackable 3D logic and memory functions that allow new architectures
  - Low temperature formation
  - Logic AND memory
  - High density of memory – at least 4GB (Giga-Byte)/die
- Possible to fabricate in existing domestic, commercial, high-yielding infrastructure
  - 90nm on 200mm wafers
  - High yield on large SoCs

# FRANC leverages demonstrated benefits of beyond von Neumann topologies

Stacked Memory Layers

DRAM Banks

A Single Logic Layer

MC A

Crossbar

Acc. Controller

Acc. Controller

(To/From Processor)

From Memory or Crossbar

Input Buffer

To Memory Controller

Address Generation

Accelerator

Output Buffer

To Memory or Crossbar

U. Mich, UCSD

Near-memory processing provides dramatic performance and energy improvements

Xeon+HMC

NM Atom

External Acc. + HMC

NM Acc

Speedup

9 8 7 6 5 4 3 2 1 0

13x

13x

string matching (fgrep)

sort

memcpy

hash table lookup

- Xeon+HMC—Quad Xeon and Hybrid Memory Cube
- NM Atom—16 Intel Atom Cores
- External Acc—16 external accelerators, SerDES linked
- NM Acc—Near memory accelerator

Source: S.F. Yitbarek, et al., DATE 2016.

Performance Comparison (higher better)

Key result: near-memory processing provides dramatic performance improvements

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# Investments inspired by Moore's "Page 3"

**Page 3 Investments**

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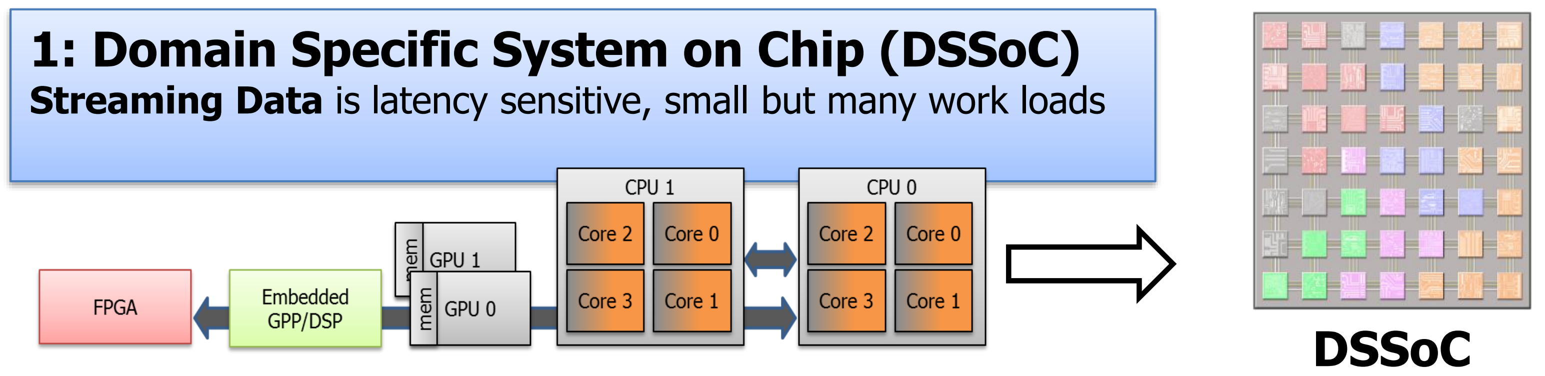
# ERI Page 3: Architectures

*Build new processors that solve the significant computing needs of today's and tomorrow's applications.*

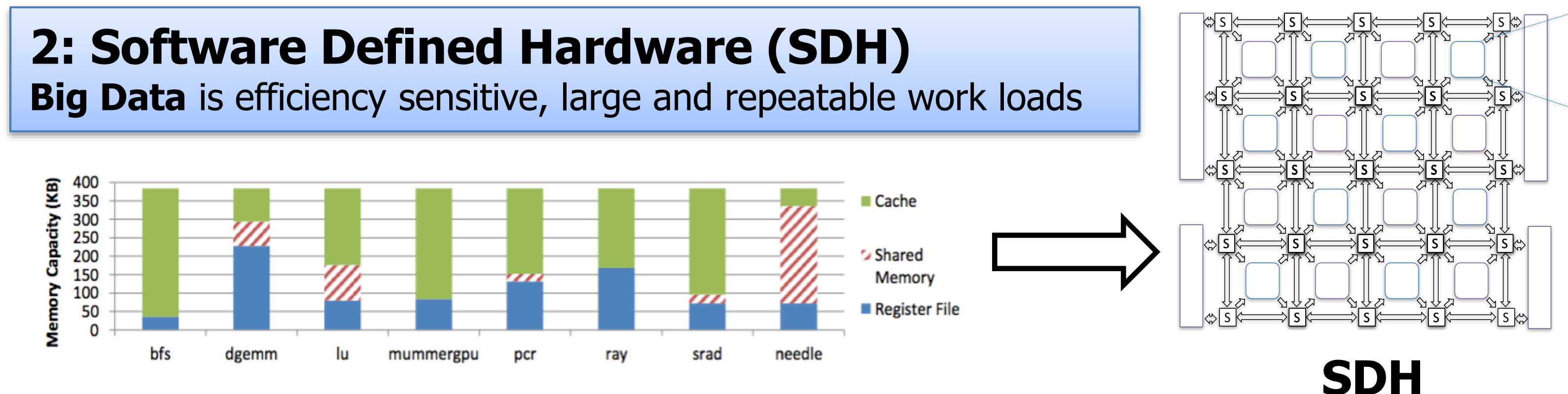
## 1: Domain Specific System on Chip (DSSoC)

**Streaming Data** is latency sensitive, small but many work loads




## 2: Software Defined Hardware (SDH)

**Big Data** is efficiency sensitive, large and repeatable work loads

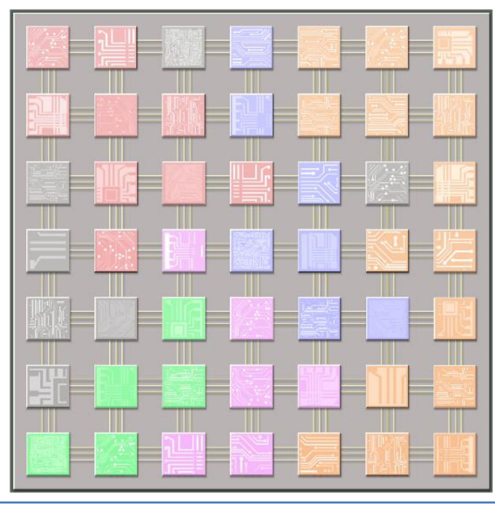


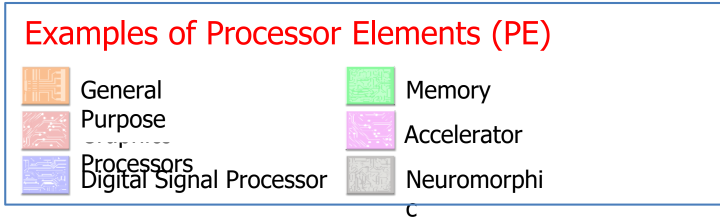
# DSSoC program will…

- Create a development ecosystem that takes advantage of the specialized hardware with no added burden to the programmer

- Design an intelligent scheduler for efficient data movement between DSSoC processor elements

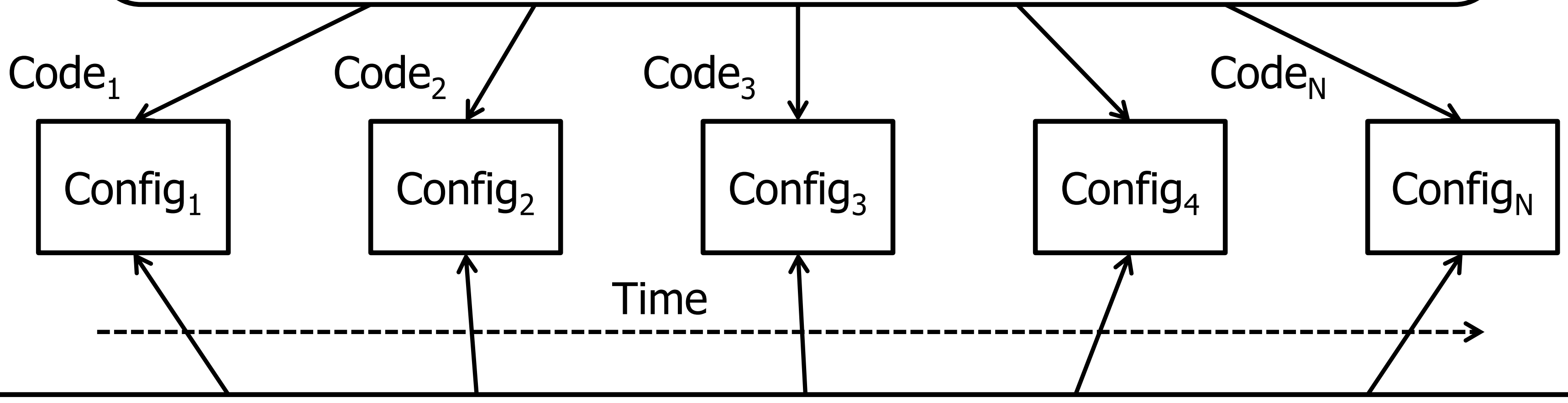
- Build a DSSoC of advanced, heterogeneous processors and accelerators for software radio






*DSSoC will enable rapid development of multi-application systems through a single programmable device*

# Software-defined hardware (SDH)




**Reconfigurable processors (TA1)**

**Properties:**

1. Reconfiguration times: 300 - 1,000 ns
2. Re-allocatable compute resources – i.e. ALUs for address computation or math
3. Re-allocatable memory resources – i.e. cache/register configuration to match data
4. Malleable external memory access – i.e. reconfigurable memory controller

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# Investments inspired by Moore's "Page 3"

**Page 3 Investments**

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# IDEA: High level objectives

**IDEA will completely automate the layout of electrical circuits and systems**

**Machine-generated chip and package layout**

**Machine-generated board layout**

**Intent-driven system generation**

Sources: Raspberry Pi

# A unified electrical circuit layout generator

## Today

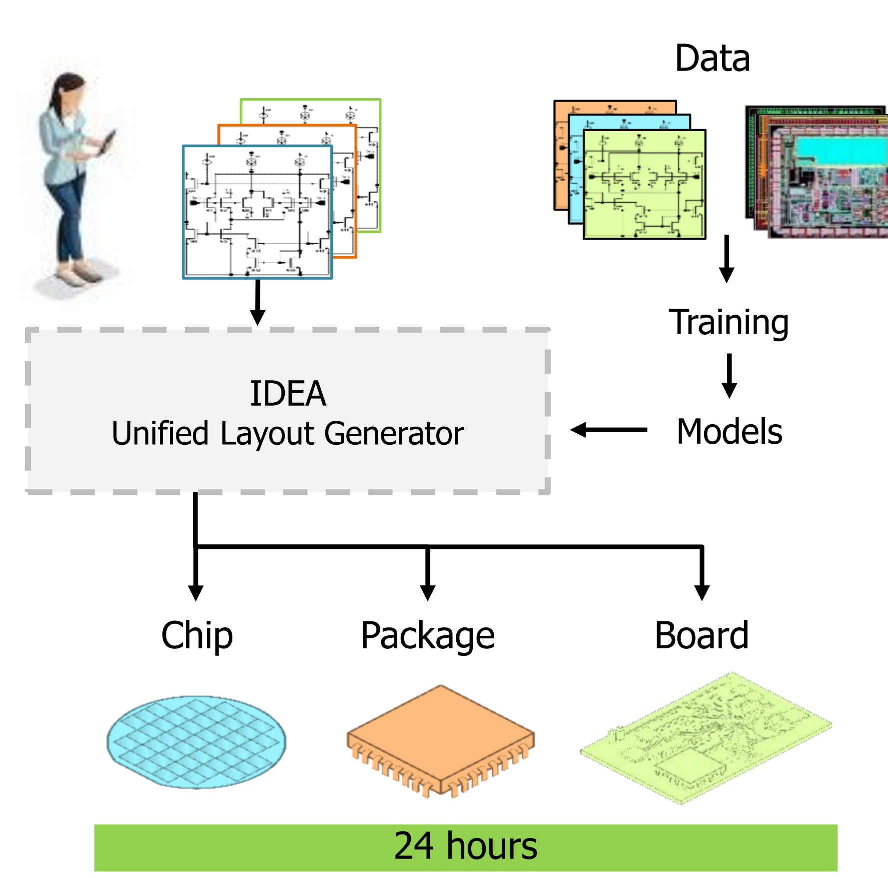
**Chip**
9 months

**Package**
3 months

**Board**
3 months

- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

## IDEA




- Knowledge embedded in software
- 100% automation
- 24 hour turnaround

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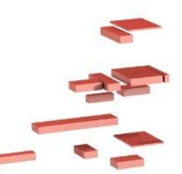
# Future of heterogeneous integration



Requires a lot of pieces coming together!

Source: DARPA

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www.darpa.mil

GIGAOM.com