Panel Fan-Out Manufacturing: Why, When, How?
The Jury Has Convened

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Example of FOWLPs in Smartphones

- FO=WLPs$n$many$ Smartphones$
  - Samsung'models'
  - Huawei'models'
  - Xiaomi'models'
- Parts$from$Qualcomm$ using$WLB$process$

Qualcomm RF transceiver
Package is 3.3 mm x 3.3 mm

Qualcomm PMIC
5.4 mm x 5.4 mm
part also found

Qualcomm Audio CODEC
Package is 4.25 mm x 3.90 mm

Source: ChipWorks.

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### Example of Scaling in Package Assemble

- Growth of Substrate Strips to Leverage Batch Processing Economics

<table>
<thead>
<tr>
<th>SAT</th>
<th></th>
<th>Low Density</th>
<th>High Density</th>
<th>Ultra High Density 2-Up</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>4-up</td>
<td>1-up</td>
<td>4-up</td>
</tr>
<tr>
<td>A</td>
<td>62x230mm</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>B</td>
<td>63.45x240mm</td>
<td>63.45x240mm</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>C</td>
<td>60x220mm</td>
<td>-</td>
<td>74x240mm</td>
<td>-</td>
</tr>
<tr>
<td>D</td>
<td>63x240mm</td>
<td>-</td>
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</tbody>
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Packages per batch operation increasing,
- Utilization of Panel Increasing
- Cost Advantage

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Wafer Processed Package Evolution

<table>
<thead>
<tr>
<th>Time</th>
<th>WLP</th>
<th>Face Down FOWLP</th>
<th>WLP with Sidewall Prot.</th>
<th>Face Up WLP/FOWLP (DECA)</th>
<th>Face Down FOWLP POP</th>
<th>Face Up FOWLP (InFO)</th>
</tr>
</thead>
</table>

**Features and Benefits**

**WLP**
- Lowest cost solution if applicable
- Finer pitch routing than substrates

**Face Down FOWLP**
- Cost effective for die requiring some fan out
- Lower parasitics
- Finer pitch routing than substrates

**WLP with Sidewall Prot.**
- More robust handling, Not prone to edge cracking

**Face Up WLP/FOWLP (DECA)**
- Flat surface to pattern RDL. Finer pitch possible
- Mold protection over die surface

**Face Down FOWLP POP**
- Thinner POP possible compared to substrate based

**Face Up FOWLP (InFO)**
- Flat surface for patterning RDL. Finer pitch Pillars for POP connection than solder balls

**Challenges**

**WLP**
- Rel limits die size
- Handling issues for EMS
- Low K challenged

**Face Down FOWLP**
- 2+ layers of RDL more expensive than substrate pkg.

**WLP with Sidewall Prot.**
- Increases cost over WLP

**Face Up WLP/FOWLP (DECA)**
- Requires growth of Cu pillar on die

**Face Down FOWLP POP**
- Cost For 2+ RDL

**Face Up FOWLP (InFO)**
- Cost for 2+ RDL
- Cost to grow Cu pillars for POP

**Applications**

**WLP**
- Devices that I/O boundary

**Face Down FOWLP**
- Alternative to FC for many apps
- Multi chip modules

**WLP with Sidewall Prot.**
- Same as WLP

**Face Up WLP/FOWLP (DECA)**
- Same as FOWLP, WLP, sidewall protected WLP

**Face Down FOWLP POP**
- Apps processor for high end phones

**Face Up FOWLP (InFO)**
- Apps processor for high end phones

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## 2.1/2.5D Advanced Packages for Multichip, Processors, GPUs and FPGA – Opportunities for FO Packaging

<table>
<thead>
<tr>
<th></th>
<th>2.5D</th>
<th>2.1D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TSI</strong></td>
<td>Fan Out Chip on Substrate</td>
<td>Photo-Defined Organic Interposer (POI)</td>
</tr>
<tr>
<td>CoWoS, CoW, CoS</td>
<td>SWIFT (Die last FO)</td>
<td>EMIB</td>
</tr>
<tr>
<td><strong>FOCoS</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>SWIFT</strong></td>
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<tr>
<td><strong>2.1D</strong></td>
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<tr>
<td><strong>Suppliers</strong></td>
<td>TSMC, Multiple OSATS</td>
<td>ASE</td>
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<tr>
<td><strong>Features</strong></td>
<td>Si Interposer</td>
<td>Die first face down FO construction</td>
</tr>
<tr>
<td></td>
<td>Glass Interposers for electrical</td>
<td>Leverages HVM processes of standard</td>
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<tr>
<td></td>
<td>performance by GaTech</td>
<td>FOWLP but fine pitch RDL</td>
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<tr>
<td></td>
<td>Die first or last assembly depending</td>
<td>In Dev.</td>
</tr>
<tr>
<td></td>
<td>on process flow</td>
<td>Panel possible</td>
</tr>
<tr>
<td></td>
<td>In LVM</td>
<td></td>
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<tr>
<td><strong>Assembly Complexity</strong></td>
<td>Si Interposer + Substrate Assembly</td>
<td>FO processes+ PKG to Substrate Assembly</td>
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**Notes:**
- TSMC: Taiwan Semiconductor Manufacturing Corporation
- OSATS: Outsourcing Services for Technologies
- ASE: American Science & Engineering
- Amkor: Advanced Micro-Engineering, Inc.
- Shinko: Shinko Electric Industry Company
- Intel: Intel Corporation
- LVM: Low Volume Manufacturing
- RDL: Routing and Distribution Layer
- PKG: Package
- AOI: Automated Optical Inspection
- PID: Process Integration Design
- SRO: Solder Resist over Interposer
- LQFP: Leadless Quad Flat Pack
- 300mm: 300mm wafer size
- LQFP: Leadless Quad Flat Pack

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FOWLP and the Quest for Smaller Form Factor, Higher Integration, and Larger Panels

- Eliminates die interconnect (bump & wire bonds) and substrate
  - Finer pitches than substrate based technology
  - 10-15um L/S common, 5/5um in HVM, ~2/2um L/S in LVM
  - Shorter interconnects = Lower parasitic
  - Eliminate interconnect stress and ELK crack delamination issues
  - Can improve thermal characteristics

- Batch packaging process like WLP
  - Can use KGD
  - Round panels can leverage WLP and FC bumping equipment
  - Square panels can leverage material and process understanding form WLP

- Potential SiP, Multi-die, 3D Solution

- Larger panel batch processing in development to lower cost
  - Challenges in patterning, sputtering, plating, and materials
  - Challenges with metrology over large format