Electronic Interconnect Convergence

... through large panel fan-out

Tim Olson  Founder & CTO

Deca Technologies
Remember when?  ... there were 3 distinct industries

Wafer Foundries
- Semiconductor Device
  - Nanometers

OSATs
- Packaging
  - 10's of Microns

EMS
- Electronic Systems
  - 100's of Microns
Remember when? … there were 3 distinct industries

**Wafer Foundries**
- Semiconductor Device
- Nanometers

**OSATs**
- Packaging
- 10’s of Microns

**EMS**
- Electronic Systems
- 100’s of Microns
Today, the lines are blurring
... while electronic interconnect cost remains quite different

### Device Level Electronic Interconnect

<table>
<thead>
<tr>
<th>Technology</th>
<th>Typical Geometries</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital processor</td>
<td>14 nm</td>
<td>6 ¢ per mm(^2)</td>
</tr>
<tr>
<td>Analog</td>
<td>40 to 150nm</td>
<td>3 ¢ per mm(^2)</td>
</tr>
<tr>
<td>RF</td>
<td>55 to 180nm</td>
<td>2 ¢ per mm(^2)</td>
</tr>
</tbody>
</table>

### Packaging - 1\(^{st}\) Level Elec. Interconnect

- Flip chip CSP packaging
  - Typical Cost: 0.7 ¢ per mm\(^2\)

### EMS - 2\(^{nd}\) Level Elec. Interconnect

- 10 layer Smartphone motherboard
  - Typical Cost: 0.5 ¢ per mm\(^2\)
Where does large panel fan-out fit?

Technology Cost Comparison
(Sales price to customers)

<table>
<thead>
<tr>
<th>Technology</th>
<th>Cents per mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adv Si</td>
<td>6</td>
</tr>
<tr>
<td>Analog Si</td>
<td>3</td>
</tr>
<tr>
<td>RF Si</td>
<td>2</td>
</tr>
<tr>
<td>FC CSP</td>
<td>0.7</td>
</tr>
<tr>
<td>OEM PCB</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Large Panel Fan-out Potential
The basics of cost for capacity

Large panel fan-out has the potential for >30% cost reduction

- Capital productivity
- Material efficiency
Breaking through the barriers

Wafer level capital cost breakthrough

Chip attach cost breakthrough

*Note: Multiple patents issued & pending

Adaptive Alignment*
Align the entire RDL pattern to the measured die position

Adaptive Patterning™

Adaptive Routing*
Dynamically adapt RDL routing to the measured die position

Enables high metal density designs
Precisely aligns inductors to the die

BGA array fixed to package outline
Enables multi-die fan-out
... the future is near

Initial Production

300mm round

M-Series Structure*

Future Production

(post chip attach)

(post mold & debond)

Large panel format M-Series*

*Note: Multiple patents issued & pending

... in cooperation with ASE
Thank You