Panel Fan-Out Manufacturing: Why, When, and How?

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Panel Level Packaging is not a geometrical extension

Silicon Scaling ≠ Package Scaling

Silicon Scaling

S. Iyer (UCLA), IEEE Trans CPMT 2016

Solution for SiP???? – Focus on system-level-scaling
Heterogeneous integration for SiP using *Embedding*

- **I/O Count**
  - High
  - Medium
  - Small

- **SiP Size**
  - Small
  - Medium
  - High

- **Examples**
  - **RF**
  - **Power/WiFi**
  - **MEMS/Images**
  - **ASIC**
  - **GPU, CPU + Memory, FPGA**
Panel Level is: The intelligent combination of Wafer Level Processing and PCB Processing

- I/O Count
  - high
  - medium
  - small

- SiP Size

Diagram: PL (Panel Level) and WL (Wafer Level) compared to different I/O counts and SiP sizes.
Fraunhofer IZM has formed a consortium for Panel Level Packaging

Goal is to drive Panel Level FO-WLP to a similar performance as WLP but at lower cost