Innovation and Technology Development of the Chinese IC Packaging Industry

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Jiangyin, Jiangsu, China
Chinese IC Packaging Industry Technology Innovation Strategic Alliance (PITISA)

- Established on December 30, 2009.
- Inauguration ceremony held in Beijing with the General Party Secretary and Deputy Minister of the Ministry of Science and Technology (MOST) as the honor speaker and guest.
- The first industry alliance under the umbrella of the 02 National Hi-Tech Program.
Charter of PITISA

1. To promote the domestic IC packaging equipment, materials, and manufacturing industry, education and research.

2. To facilitate the close collaboration among domestic IC packaging industry, research institutions and universities.

3. To advance the domestic packaging technology innovation and accelerate the adoption of advanced technology.

4. To establish a platform for information exchange, communications, industry and technology roadmapping.

5. To liaison with and advise to various government bodies on IC packaging industrial policy, planning and incentives.

6. To coordinate various government and industrial programs and activities in packaging and test manufacturing, equipment, materials, research, development and education.
PITISA is hosted by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) and supported by Nantong Fujitsu Microelectronics (NFME). Chairman of the Board is Mr. Xinchao Wang, CEO of JCET and General Secretary is Mr. Xiekang Yu, Vice Chairman of JCET. 25 members in the Alliance, representing the majority of packaging assembly and test industry, research and development and education in China.

**Organization Structure of PITISA**

- **Board of Directors**
  - Expert Advisory Committee

- **Working Committee**
  - Admin.
  - IP Management
  - Project Management
    - Member 1
    - Member 2
    - Member 3
    - Member 4

- Coordinator
- Patent Library
# Current Membership

<table>
<thead>
<tr>
<th>Company</th>
<th>Industry</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jiansu Changjiang Electronics Technology Co., Ltd. (JCET)</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>Nantong Fujitsu Microelectronics Co., Ltd. (NFME)</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>Beijing Zhong Dian Ke Electronics Equipment Co.</td>
<td>Equipment</td>
</tr>
<tr>
<td>CETC No.2 Institute</td>
<td>Equipment</td>
</tr>
<tr>
<td>Wuxi Anst Co.</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>Tianshui Huatian Co.</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>Ningbo Kangqiang Co.</td>
<td>Materials</td>
</tr>
<tr>
<td>Shennan Circuits Co. (SCC)</td>
<td>Materials</td>
</tr>
<tr>
<td>Microelectronics Research Institute of CAS</td>
<td>Research</td>
</tr>
<tr>
<td>Microsystems and Information Technology Research Institute of CAS</td>
<td>Research</td>
</tr>
<tr>
<td>CETC No.13 Institute</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>CETC No.58 Institute</td>
<td>Assembly &amp; Test</td>
</tr>
<tr>
<td>Tsinghua University</td>
<td>Research &amp; Education</td>
</tr>
<tr>
<td>Fudan University</td>
<td>Research &amp; Education</td>
</tr>
<tr>
<td>Huazhong University of Science and Technology</td>
<td>Research &amp; Education</td>
</tr>
<tr>
<td>Shanghai Microelectronics Equipment Co.</td>
<td>Equipment</td>
</tr>
<tr>
<td>Shenyang Kingsemi Microelectronics Systems</td>
<td>Equipment</td>
</tr>
<tr>
<td>Shenzhen Grand Technology</td>
<td>Equipment</td>
</tr>
<tr>
<td>Trinity Electronics Co.</td>
<td>Equipment</td>
</tr>
<tr>
<td>Jiangyin Glory Technology Co.</td>
<td>Equipment</td>
</tr>
<tr>
<td>Dalian Jiafeng Electronic Co.</td>
<td>Equipment</td>
</tr>
<tr>
<td>Shanghai Singyang Semiconductor Materials Co.</td>
<td>Materials</td>
</tr>
<tr>
<td>Runma Electronics Chenical Co.</td>
<td>Materials</td>
</tr>
<tr>
<td>Jiangsu Zhongpeng Electronic Co.</td>
<td>Materials</td>
</tr>
<tr>
<td>Yixin Electronic Component Factory</td>
<td>Assembly &amp; Test</td>
</tr>
</tbody>
</table>
Major Achievements

• Established and Enhanced the Operations
  o Staffed up the Working Committee
  o Produced a recommendation for packaging assembly and test equipment and materials development and market strategy to better service the domestic demand and localize the supply.
  o Recommended the members to further invest in management system and attract overseas talents to improve management, operations and market research to narrow the gap with the international leading players

• Coordinated the programs in the “Eleventh 5-Year Plan” (11.5)
  o The Alliance performed audit, review and tracking of all the IC packaging and test projects in the “Applied Engineering Program of Key Packaging and Test Equipment and Materials” during the 11.5 period.

• Organized the Draft of IC Packaging and Test Part for the “Twelfth 5-Year Plan” (12.5)
  o By the directives of the Office of Special Program Management of the Ministry of Science and Technology and under the leadership of the Special Program Taskforce, The Alliance organized the draft of the Guidelines No.4 – Packaging and Test Equipment, Processes and Materials as part of the 2011 National Hi-Tech Program “ULSI Manufacturing Equipment and Complete Processes”.

• Promoted the IP and Patent Awareness and Development
  o Enacted the Alliance’s “IP Management Guidelines” and “Patent Management Method”. Encouraged members of the Alliance and 02 Hi-Tech Program participants to effectively manage their IP resources and convert R&D results into patents for better protection of technologies. Under the Program, 10 key technologies were developed and 127 patents were granted.
Awards and Recognitions

- The Alliance was praised in the “2011 National Science and Technology Working Conference”

- JCET was recognized as the “Excellent Execution Team of 11.5 Hi-Tech Project”

- Mr. Xiekang Yu, General Secretary of PITISA was awarded the “Outstanding Organizer of 11.5 National Science and Technology Program”
JCET Profile

- Founded: Dec. 1972
- Location: Jiangyin City, Jiangsu Province
- Chairman: Mr. Wang Xinchao
- General Manager: Mr. He Zhiwen
- Registered Capital: USD 111 Million
- Total Land Area: 325,008 Sqm.
  - Total Building Area: 96,212 Sqm.
  - Clean Room: 29,540 Sqm. (Class 10K)
  - Clean Room: 12,380 Sqm. (Class 100K)
- Employees: 8000
- Publicly Listed on SSE: June, 2003
### 2009 World Wide SATS Ranking

<table>
<thead>
<tr>
<th>2009 Ranking</th>
<th>2008 Ranking</th>
<th>Company</th>
<th>Headquarters Country</th>
<th>2008 Revenue ($M)</th>
<th>2009 Revenue ($M)</th>
<th>2009 Growth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>ASE</td>
<td>Taiwan</td>
<td>2,952</td>
<td>2,597</td>
<td>-12.0</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Amkor Technology</td>
<td>United States</td>
<td>2,658</td>
<td>2,179</td>
<td>-18.0</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>SPIL</td>
<td>Taiwan</td>
<td>1,918</td>
<td>1,722</td>
<td>-10.2</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>STATS ChipPAC</td>
<td>Singapore</td>
<td>1,658</td>
<td>1,326</td>
<td>-20.0</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>Powertech Technology</td>
<td>Taiwan</td>
<td>994</td>
<td>982</td>
<td>-1.2</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>UTAC</td>
<td>Singapore</td>
<td>711</td>
<td>600</td>
<td>-15.6</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>ChipMOS Technology</td>
<td>Taiwan</td>
<td>519</td>
<td>368</td>
<td>-29.1</td>
</tr>
<tr>
<td>8</td>
<td>11</td>
<td>JCET</td>
<td>China</td>
<td>349</td>
<td>342</td>
<td>-2.0</td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td>King Yuan Electronics</td>
<td>Taiwan</td>
<td>413</td>
<td>319</td>
<td>-22.8</td>
</tr>
<tr>
<td>10</td>
<td>9</td>
<td>Unisem</td>
<td>Malaysia</td>
<td>373</td>
<td>300</td>
<td>-19.6</td>
</tr>
</tbody>
</table>

**Total Top 10**

<table>
<thead>
<tr>
<th></th>
<th>2008 Revenue ($M)</th>
<th>2009 Revenue ($M)</th>
<th>2009 Growth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Top 10</td>
<td>12,545</td>
<td>10,735</td>
<td>-14.4</td>
</tr>
<tr>
<td>Others</td>
<td>7,556</td>
<td>6,452</td>
<td>-14.6</td>
</tr>
<tr>
<td>Total Market</td>
<td>20,101</td>
<td>17,187</td>
<td>-14.5</td>
</tr>
</tbody>
</table>

Top 10 SATS Companies’ Revenues, 2009. (Source: Gartner, February 2010)
JCET Overall Product Roadmap

- IC package
- TR package
- SiP package

Stacked die technical

TCP/COG
TO220/263
SOT523
SOT23/323
DPAK, IPA
TO94/126
TO92

WLCSP
TO247/TO3P
SOD523/723
SOD123/323

8” Bumping

MSOP/TSSOP
SOT59/89/223

FDIP
PSOP/HSOP

PDIP/SIP

LGA
TSOT

SiP BGA
FLIP CHIP BGA
STACKED DIE BGA
W-BGA

LQFP/HTSOP
DFN/QFN

TQFP
FBP

3D PKG
MCM PKG
Flip Chip LGA/Technical
MEMS(BGA LGA)
BGA

1999-2000
1996-1998
1993-1995
1992
1991
1990

1999-2000
1996-1998
1993-1995
1992
1991
1990

1999-2000
1996-1998
1993-1995
1992
1991
1990
Thank You!

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