7. Flip Chip Technologies

Course Leaders: Shengmin Wen – JCET and Eric Perfecto – IBM Research

Course Objective:

This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various type of wafer bumping technologies, solder joint formation, substrate selection, underfill type and selection, and reliability evaluation. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. Plenty of examples are presented to show the versatile flip-chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form interconnection such as wire bond / flip chip mixed integration. Major flip chip assembly packages are discussed, such as the BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages that uses Si or organic interposers, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization and its consequence on packaging, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their project's success. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today's flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

Course Outline

1. Introduction to Flip-Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Waver Lever Fan-Out; and Panel Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-Bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend:

The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical

issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

BIO: Dr. Shengmin Wen is vice president and general manager of Design Service Business Unit at JCET. He has more than 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. Recent years, he focused on advanced package and integration methods, organic RDL for 2.5D and 3D chiplet based integration, in addition to development of panel-based packaging that uses chip last flip chip methodologies. He has extensive and unique experiences in flip chip assembly technologies that use fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, advanced fine pitch flip chip assembly process, and reliability. He previously worked at Synaptics Inc as the principal packaging architect, and Amkor Technology where he was a director of 3D CSP Product Group. Dr. Wen received his Ph.D. from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science-based fatigue theory. Dr. Wen has been actively participating and contributing to industry technical conferences to learn, to share, and to contribute.

Eric Perfecto has over 38 years of experience working in the development and implementation of C4 and advanced Si packages at IBM and GLOBALFOUNDRIES. Responsibilities included UBM and Pb-free solder definition for C4 and u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College. Eric has published over seventy-five external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards and an IBM Outstanding Contribution Award for the Development of 3D Wafer Finishing Process (2014). Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. Eric is an IEEE Fellow and has achieved senior member status from IMAPS and Society of Plastic Engineers. He is an EPS Distinguish Lecturer and the Awards Program Director of the Electronics Packaging Society of IEEE.