6. Avoiding inelastic strains in solder joint interconnections of IC packages

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Course Description and Outline: The following three important questions associated with predicting and improving the reliability of solder joint interconnections (SJI) of IC packages are addressed in this short course:

1. Could inelastic strains in the solder material be avoided by a rational physical design, and if not, could the sizes of the inelastic strain areas be predicted and, if possible, minimized? **Motivation**: SJIs are the most vulnerable structural elements in today's IC packages. That is mostly because the solder material experiences at the peripheral portions of an IC assembly, where the interfacial thermal stresses are the highest, inelastic strains, and suffers, because of that, from low cycle fatigue conditions; as the consequence of that, its fatigue lifetime is often shorter than required for many applications. There is an obvious incentive therefore to consider and explore ways to bring down the induced stresses and strains in the solder material, even, if possible, to an extent that the inelastic strains in it are avoided; then the material will perform within the elastic range, and, owing to that, its fatigue lifetime will be significantly longer. If avoiding inelastic strains is impossible, the size of the inelastic zones at the assembly ends could be, desirably, predicted, minimized and considered in the SJI lifetime evaluations.

2. Considering that the difference between a highly reliable and an insufficiently reliable product is "merely" in the level of their never-zero probability of failure, and that SJIs are usually the most vulnerable structural elements in an IC package design, could this probability be assessed at the design stage? **Motivation:** The era in materials science, when creating a new material "we heat, we beat and we pray," and when its performance in the field is not "ours to see," has gone. In today's electronic materials science, when the behavior and performance of a material is critical, ability to predict/quantify its reliability is imperative, and, because of various inevitable unpredictable intervening factors, such a prediction should be done on the probabilistic basis. The recently suggested probabilistic design-for-reliability (PDfR) concept enables assessing the never-zero probability of the operational failure of an IC material by using predictive analytical ("mathematical") modeling that determines this probability from the highly focused, highly cost-effective, carefully designed and thoroughly conducted failure-oriented-accelerated testing (FOAT) .Highly flexible and highly physically meaningful Boltzmann-Arrhenius-Zhurkov (BAZ) model could be applied to predict this probability from the FOAT data.

3. Should temperature cycling accelerated testing for SJIs be replaced with a more physically meaningful, less costly, less time- and labor- consuming and, most importantly, less misleading accelerated test vehicle? **Motivation:** Temperature cycling, the most widespread accelerated test today, is costly, time- and labor consuming, and, most importantly, can result in misleading information, because electronic materials' properties are temperature dependent, and testing is done in a temperature range, which is much wider than what the material will encounter in actual operation. Thus, a clear motivation exists for finding a test vehicle that would be less costly, less time and labor consuming and, most importantly, more physically meaningful, and trustworthy. Since the highest stresses occur in SJIs at low temperature conditions and crack propagation is effectively accelerated by random vibrations, a low-temperature/random-vibrations bias is suggested as an attractive substitute for temperature cycling,

especially for applications, when such a bias reflects the actual loading conditions in the field.

Ephraim Suhir is on the faculty of the Portland State University, Portland, Oregon, Technical University, Vienna, Austria, and James Cook University, Queensland, Australia. He is also CEO of a Small Business Innovative Research (SBIR) ERS Co. in Los Altos, CA, USA, and is a "*Foreign Full Member"* (Academician) of the National Academy of Engineering, Ukraine. He is a "*Life Fellow"* of IEEE, the American Society of Mechanical Engineers (ASME), the Society of Optical Engineers (SPIE), and the International Microelectronics and Packaging Society (IMAPS); Ephraim is a Fellow of the American Physical Society (APS), the Institute of Physics (IoP), UK, and the Society of Plastics Engineers (SPE); and *Associate Fellow* of the American Institute of Aeronautics and Astronautics (AIAA). Ephraim has authored 450+ publications (patents, technical papers, book chapters, books), presented numerous keynote and invited talks worldwide, and received many professional awards, including 1996 Bell Laboratories Distinguished Member of Technical Staff (DMTS) Award (for developing effective methods for predicting the reliability of complex structures used in AT&T and Lucent Technologies products), and 2004 ASME Worcester Read Warner Medal (for outstanding contributions to the permanent literature of engineering and laying the foundation of a new discipline "Structural Analysis of Electronic Systems"). Ephraim is the third "Russian American," after S. Timoshenko and I. Sikorsky, who received this prestigious award. His most recent awards are 2019 IEEE Electronic Packaging Society (EPS) ***Field award*** for seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems and 2019 Int. Microelectronic Packaging Society's (IMAPS) ***Lifetime Achievement award*** for making exceptional, visible, and sustained impact on the microelectronics packaging industry and technology.