11. Fan-out Wafer/panel-level Packaging and Chiplet Design and Heterogeneous Integration Packaging

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Course Objective:
Fan-out wafer/panel-level packaging has been getting lots of tractions since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. These chips can be any kind of devices and do not have to be chiplets. On the other hand, for chiplets, they must use the heterogeneous integration to package them. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline:

1. Formation of FOWLP: (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First)
2. Fabrication of Redistribution Layers (RDLs): (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu Damascene + CMP, (c) Hybrid RDLs, and (d) Laser drill + LDI + PCB Cu-plating + Etching
3. Formation of FOPLP: (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First)
4. TSMC InFO: (a) InFO-PoP, and (b) InFO AiP Driven by 5G mm Wave
5. Samsung PLP: (a) PoP for Smart Watches and (b) SiP SbS for Smartphones
6. Warpages: (a) Warpage Types and (b) Allowable of Warpages
7. Reliability of FOWLP and FOPLP: (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations
8. Examples: (a) Chip-First Panel-Level Fan-Out Packaging of Mini-LED for RGB-Display, (b) Chip-Last Panel-Level Fan-Out Packaging of Application Processor Chipset, (c) 2.3D IC Integration with Chip-First Fan-Out RDL-Interposers, and (d) 2.3D IC
9. Chiplet Design and HI Packaging vs. System-on-Chip (SoC)
10. Advantages and Disadvantages of Chiplet Design and HI Packaging
11. Examples: (a) AMD Chiplet Design and HI Packaging (EPYZ and RYZEN), (b) Intel Chiplet Design and HI Packaging (FOVEROS, FOVEROS Direct, and Ponte Vecchio), (c) TSMC Chiplet Design and HI Packaging (SoIC + CoWoS and SoIC + InFO PoP)
12. Chiplets Lateral Interconnects (Bridges): (a) Intel's EMIB, (b) IBM's DBHi, (c) Applied Materials' Bridge Embedded in Fan-Out EMC, (d) SPIL's FO-EB, (e) TSMC's LSI, (f) ASE's sFOCoS, (g) IME's EFI, and (h) Amkor's S-Connect Fan-Out Interposer
13. Chiplet Design and HI Packaging on Organic Substrates: many examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h)

AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube

14. Assembly Technologies for Chiplet Design and HI Packaging: (a) SMT, (b) Solder Bumped Flip Chip, (c) CoW, (d) WoW, (e) TCB, and (f) Bumpless Cu-Cu Hybrid Bonding
15. Integration with Chip-Last Fan-Out RDL-Interposers
16. Chiplet Design and HI Packaging vs. System-on-Chip (SoC)
17. Advantages and Disadvantages of Chiplet Design and HI Packaging examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h) AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube
18. Chiplet Design and HI Packaging on Fan-Out RDL Substrate for High Performance Applications: many examples: (a) STATSChipPac's FOFC-eWLB, (b) ASE's FOCoS (Chip-First), (c) MediaTek's FO-RDLs, (d) TSMC's InFO_oS and InFO_MS, (e) Samsung's Si-Less RDL Interposer, (f) TSMC's RDL-Interposer, (g) ASE's FOCoS (Chip-Last), (h) Shinko's Organic RDL-Interposer, and (i) Unimicron's Hybrid Substrate

Who Should Attend:
If you (students, engineers, and managers) are involved with any aspect of the electronics, LED, MEMS, and optoelectronic industry, you should attend this course. It is equally suited for R&D professionals and scientists. Every attendee will receive more than 250 pages of handouts.

BIO: John H Lau has more than 40 years of R&D and manufacturing experience in semiconductor packaging and SMT assembly, John has published more than 500 peer-reviewed papers, 30 issued and pending US patents, and 21 textbooks on, e.g., Advanced MEMS Packaging (McGraw-Hill, 2010), Reliability of RoHS compliant 2D & 3D IC Interconnects (McGraw-Hill, 2011), Through-Silicon Via (TSV) for 3D Integration (McGraw-Hill, 2013), 3D IC Integration and Packaging (McGraw-Hill, 2016), Fan-Out Wafer-Level Packaging (Springer, 2018), Heterogeneous Integrations (Springer 2019). Assembly and Reliability of Lead-Free Solder Joints (Springer 2020), and Semiconductor Advanced Packaging (Springer, 2021). John is an elected IEEE Fellow, IMAPS Fellow, and ASME Fellow.