11. Chiplet, Heterogeneous Integration, and Co-Packaged Optics

Course Leader: John Lau – Unimicron

Course Description:

Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components with different sizes and functions, and from different fabless design houses and foundries into a system or subsystem on a common package substrate. Co-packaged optics (CPO) are heterogeneous integration of the optical engine which consists of photonic ICs (PIC) and the electrical engine (EE) which consists of the electronic ICs (EIC) as well as the switch ASIC (application specific IC). The advantages of CPO are: (a) to reduce the length of the electrical interface between the OE/EE (or PIC/EIC) and the ASIC, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging and CPO, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the introduction, recent advances, and trends in chiplet, HI, and CPO will be presented.

Course Outline:

1. System on Chip (SOC)
2. The Origin of Chiplets
3. Chiplet Design and HI Packaging (1. Partition, 2. Split)
4. Communication Between Chiplets (EMIB, UCIe, Bridge Embedded in Fan-Out EMC)
5. Chiplet Design and HI Packaging - Multiple System and HI
6. Potential R&D Topics in Chiplet Design and HI Packaging
7. Trends in Chiplet Design and HI Packaging
8. Silicon Photonic
9. Data Centers and Optical Transceivers
10. Optical Engine (OE) and Electrical Engine (EE)
11. OBO (on-board optics), NPO (near-board optics), and CPO (co-packaged optics)
12. 3D HI of PIC and EIC
13. 3D HI of ASIC Switch, PIC and EIC w/o Bridges
14. 3D HI of GPU, HBM, Switch, PIC, EIC (Driven by AI)
15. HI of ASIC Switch, PIC and EIC on Glass Substrate
16. Potential R&D Topics and Trends in Co-Packaged Optics

Who Should Attend:

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. Each attendee will receive more than 300 pages of lecture notes.

Bio: John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging has published more than 535 peer-reviewed papers (375 are the principal investigator), 50 issued and pending US patents (34 are the principal inventor), and 23 textbooks (all are the first author). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.