7. Flip Chip Technologies

Course Leader: Shengmin Wen – HaiSemi, Inc.

Course Description:
This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various types of wafer bumping technologies, substrate design and selection, underfill selection, Co-design and modeling, and reliability evaluation.

Course Outline:

1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Wafer Level Fan-Out; and Panel-Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend:
The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

Bio: Dr. Shengmin Wen has more than 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization and its consequence on packaging, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their project's success. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today's flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric

cracking, and electromigration.