The 2025 IEEE 75th Electronic Components and Technology Conference

CALL FOR PAPERS

May 27 – May 30, 2025 • Gaylord Texan Resort & Convention Center, Dallas, Texas, USA

INTRODUCTION

On behalf of the IEEE Electronic Components and ECTC Program Committee, it is my pleasure to invite you to submit an abstract for the anniversary 75th ECTC, to be held May 27–30, 2025, at the Gaylord Texan Resort and Convention Center in Dallas, Texas. This premier international conference, sponsored by the IEEE Electronics Packaging Society (EPS), covers a broad range of topics, including components, materials, assembly, reliability, modeling, interconnect design and technology, device and system packaging, heterogeneous integration, wafer level packaging, photonics and optoelectronics, IoT, 5G, quantum computing and systems, 2.5D and 3D integration technology, and other emerging technologies in electronics packaging.

The ECTC Program Committee consists of over 200 experts from diverse technical fields and is dedicated to creating an engaging technical program. The 74th ECTC was an outstanding success, setting new records with 704 abstract submissions, a record number of exhibitors, and 2,005 registered attendees from 26 countries. It featured 383 technical papers presented in 36 oral sessions and five interactive sessions, including a session dedicated to students. Additionally, nine special sessions covered a variety of advanced packaging topics, such as industry-government co-investments in North America, Asia, and Europe, advanced metrology, thermal management for AI/ML applications, RF packaging for communication and sensing, the Young Professional Network Panel, challenges of chiplets, workforce diversity, and a brand-new session on Emerging Start-Ups for Advanced Packaging. On Tuesday, the first full-day of the conference we held a Heterogeneous Integration Roadmap (HIR) workshop.

On Wednesday morning, Professor Keren Bergman delivered an excellent plenary talk on Petascale Photonic Chip Connectivity for Energy-Efficient AI Computing. The ECTC Exhibits showcased products and services from 128 companies, with invaluable support from our generous sponsors. The 75th ECTC will continue with the same tradition of being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling.

In 2025 we will celebrate the 75th anniversary of the ECTC. The 75th ECTC will include Special Sessions such as an HIR workshop and, concurrently, a diverse array of Professional Development Courses (PDCs) on the first day of the conference (Tuesday). Esteemed leaders in their respective fields will curate the Special Sessions, providing high-level introductions into the cutting-edge topics within electronics packaging. Renowned experts will conduct the PDCs, enabling participants to expand their technical expertise. During the following three days, six parallel technical sessions will offer the most recent research and advancements in electronics packaging R&D, along with special panel discussions that highlight industry trends and best practices. Complementing the technical program, the ECTC Exhibits will feature leading companies specializing in electronic components, materials, and packaging, showcasing their latest innovations. The anniversary 75th ECTC will continue with the same tradition of being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling.

On behalf of the ECTC Program Committee, I look forward to seeing you at the 75th anniversary of ECTC, during May 27–30, 2025, at the Gaylord Texan Resort and Convention Center in Dallas, Texas.

Przemyslaw Gromala, 75th ECTC Program Chair

MAJOR TOPICS

Highly rated abstracts are accepted for presentation at the ECTC conference. During abstract submission, authors are asked to choose the subcommittees whose topic areas best fit their abstracts. Please select two different program subcommittees in order of preference that should evaluate your submission for acceptance. Abstracts are rated according to the included original and previously unpublished, non-confidential, and non-commercial information on new developments, technology, and knowledge in the areas including, but not limited to, those given in the next ten paragraphs, one for each of ECTC's technical subcommittees.

Packaging Technologies: 2.XD/3D architectures/designs for energy efficient HPC, C2C links, structures, thermal solutions, and methods & processes; heterogeneous (chiplet) integration for 2.5D, 3D-IC for AI, neural nets, HBM, CPU, GPU, ASIC, and CPO; silicon, glass, diamond & organic interposer and advanced package technology; dual-Damascene Cu, Cu TSV, hybrid bonding, and backside power; embedded die, bridge, and passives; flexible, advanced substrates & modules; fan-out wafer and panel level packaging, advanced flip-chip, SiP, CSP, PoP; RF, wireless, MEMS, Sensors & IoT, automotive, wireless power and power electronics; SiC, GaN, PMIC, SPS; bio, medical, flexible, wearable & extreme environments packaging.

Applied Reliability: Reliability of 2D, 2.5D, Si bridge, 3D, chiplets, WLCSP, FOWLP, FOPLP & heterogeneous integration and co-packaged optics (CPO); interconnect reliability in micro-bump, micro-pillar, Cu-pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip & wire bonded packages, novel reliability test methods, life models, FA techniques & materials characterization, component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays and memory; reliability and test methods for thermal materials (TIM) and reliability related to liquid cooling and immersion cooling.

Assembly & Manufacturing Technology: Assembly and manufacturing challenges for new markets; die bonding methods and process challenges: D2D, D2W, W2W; wafer level process/materials technologies; die and package singulation manufacturing; new & next generation substrates; smart factory/manufacturing; assembly related test/yield hardware development/improvement; integrating advanced thermal solutions in manufacturing: design/performance, integrating solutions, thermal materials, low stress/high thermal; process advancements/yield enhancements; cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/compression/injection mold; heterogeneous integration and process: flip chip, chiplets, 3D stacking, bridge technology, large body, warpage management; shielding/protection technologies and manufacturing and market requirements.

Electrical Design & Analysis: 5G/6G, IoT, cloud computing, autonomous vehicles, AI/ML; antennas, sensors, power transfer, wired/wireless communications, RF to THz; multiphysics/multiscale modeling & characterization of interconnects, modules, components, and systems; chiplet, heterogeneous integration, chip-to-chip, die-to-die, SiP/MCM/system co-design (chip/package/board), UCIe, HBM/HPC; opto-electronic (OE) hybrid integration, analog packaging, power electronics modeling/characterization; high-speed/frequency (RF, mm-wave, THz) signal integrity, power integrity, and EMI/EMC.

Emerging Technologies: Packaging for quantum computing and other cryogenic applications; metrology for advanced packaging and emerging technologies; AI in electronics packaging and its applications; challenges in hardware security; AI electronics packaging and its applications; power electronics and energy storage; MEMS & NEMS; emerging, novel and unique flexible/stretchable/wearable hybrid electronics, medical devices and bioelectronics; additive, hybrid, nano, and smart manufacturing for electronics packaging; green and sustainable electronics, net zero strategy/technology; digital twins.

Interconnections: Interconnects for chiplets, heterogeneous integration, hybrid bonding, C2W, W2W, fan-out, panel-level, TSV, TGV; interconnects for 2.5D/3D, Si/glass/organic interposers, fine-pitch/multi-layer RDL, SiP, wafer-level system integration; interconnects for thermo-compression/laser assisted/transient liquid phase bonding, low temperature solder, flip-chip, micro-bump, Cu pillar, wirebond, Al ribbon bond; printable interconnects, flexible interconnect, quantum interconnects, optical interconnects, interconnects for SiC/GaN or WBG; interconnection materials, chemistries, metrology, characterization and reliability; conductive/non-conductive adhesives, ACF, underfill, molding compounds; chiplet interconnect design and validation, UCIe/BoW/etc. standards; thermal interface materials, thermal/mechanical/electrical tests and reliability.

Materials & Processing: Advanced materials and processes for hybrid bonding, fan-out, Si interposer, 2.5D/3D, chiplets, HI, TSV; advanced materials and processes for thermal and mechanical improvement for packaging; wafer & panel level packaging materials and process advancements; dielectrics and underfills, molding compounds, thermal interface materials; harsh environment resistant materials; temporary wafer bond/debond materials and processes, TCB and hybrid bonding, conductive adhesives; emerging electronic materials and processes; novel solder metallurgies; novel materials and processes for high density interconnect.

Photonics: Photonic components packaging for computing, communications, data processing, mobility, healthcare, green energy photonics, agriculture, horticulture, food, environmental, climate and atmosphere monitoring, space, automobile, underwater, industrial, defense, process integration, co-packaging (photonics, electronics, and laser integration), free space optics, microscopy and advanced spectroscopy, 3D printing of micro-optical components for packaging, assembly and manufacturing; packaging for the quantum photonics world; packaging of new photonics materials; optical characterization of packaging components; equipment and tools for photonics packaging; detachable fiber array unit; ultra-low power photonics and materials; heterogeneous materials; quantum dots; meta-surfaces and meta-materials.

Thermal/Mechanical Simulation & Characterization: Thermal/mechanical simulation and characterization at component, board, and system levels for all packaging technologies; reliability related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); material constitutive relations; chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; novel modeling techniques including multi-scale physics, co-design approaches; quantum computing; measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; application of artificial intelligence on modeling, characterization, and digital twins; credible simulations; CFD simulation.

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

Visit the ECTC website (www.ectc.net) for additional conference information.

Abstract and Manuscript Submission

As the Program Chair of the 75th ECTC, I extend a warm invitation for you to electronically submit your abstract at www.ectc.net, utilizing the "Author Info" tab. Your abstract should provide comprehensive details of your proposed technical paper, including findings and results, within a maximum limit of 700 words. Additionally, please include a concise paragraph, not exceeding 50 words, highlighting the novelty of your work. You also have the option to submit a supporting figure or table if desired. The deadline for abstract submission is October 7, 2024.

During the submission process, please ensure to provide the affiliation, contact telephone number, and e-mail address for all co-authors in the desired order. Additionally, include the mailing address of the contact author and specify the name of the presenting author. Please note that only co-authors are permitted to serve as presenters at ECTC. Submitted abstracts become the property of ECTC, and ECTC reserves the right to publish the abstracts accepted for the conference. ECTC also reserves the right to prohibit, limit, or decline any editing of submitted abstracts.

Prior to all submissions, please ensure that you have received the necessary clearance from management and co-authors, where applicable. By December 9, 2024, authors are notified of abstract acceptance along with instructions for manuscript preparation and paper presentation. Contact authors of accepted abstracts are kindly requested to confirm the acceptance, which signifies the commitment to submit the manuscript within the specified timeframe and present the paper in-person as an author on-site at the conference. The Program Committee may, at their discretion, consider submitted abstracts for inclusion in the Interactive Presentation sessions.

Upon acceptance of your abstract, please submit your manuscript (4-8 full pages) for review by February 21, 2025. **Manuscripts not submitted by this date may be removed and replaced in the final program at the discretion of the Program Committee.** To be included in the Conference Proceedings, your abstract must be accepted and your manuscript must fulfill all requirements, including timely response to reviewer requests following the manuscript submission deadline. Our Technical Committee members conduct a thorough review process to ensure content quality and scientific accuracy for all accepted manuscripts.

All abstracts and manuscripts must be original, previously unpublished, devoid of commercial content, and non-confidential. It is essential that your manuscript adheres to the specified ECTC format and upholds the principles of academic integrity by avoiding any instances of plagiarism and excessive redundancy (use of previously published work). All submitted manuscripts are checked for such plagiarism utilizing the IEEE CrossCheck service.

Similar to last year, first-time leading authors of successfully presented papers have the opportunity to participate in a special raffle prize drawing during the conference. Furthermore, following the conference, a collection of outstanding papers may be invited (with appropriate revisions) for peer-reviewed publication in special sections of the prestigious IEEE Transactions on Components, Packaging, and Manufacturing Technology.

If you have any questions, contact:
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Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose first author receives an ECTC personalized certificate and a check for $3,000.

Best Interactive Presentation Award: Each year the ECTC selects the best Interactive Presentation paper whose first author receives an ECTC personalized certificate and a check for $2,000.

Outstanding Paper Award: An outstanding conference paper is also selected for special recognition by the ECTC. The first author receives a personalized certificate and a check for $2,000.

Outstanding Interactive Presentation Award: An outstanding Interactive Presentation paper is also selected for special recognition by the ECTC. The first author receives a personalized certificate and a check for $1,500.

Intel Best Student Paper Awards: Intel Corporation is sponsoring awards for the best papers submitted and presented by a student at ECTC. The winning student will be presented with a certificate and a check for $2,500 (Best Student Paper) or $1,500 (Outstanding Student Paper).

Texas Instruments Outstanding Student Interactive Presentation Award: Texas Instruments is sponsoring an award for the best student Interactive Presentation at ECTC. The winning student will be presented with a certificate and a check for $1,000.

Sponsorship Opportunities to Enhance Your Presence at ECTC

ECTC offers many unique sponsorship opportunities that provide highly visible exposure for your company. Additional information is available at www.ectc.net under "Sponsors". Please contact:

Alan Huffman, ECTC Sponsorship Chair
Phone: +1-336-380-5124
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ECTC Exhibits

We invite you to be part of the ECTC Exhibits and showcase your products and services to engineers and managers from all areas of the microelectronics packaging industry. Over 2,000 attendees are expected for the 75th ECTC, representing companies from around the world.

Exhibit Dates: May 28–29, 2025

For more information, contact:
Sam Karikalan, ECTC Exhibits Chair
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The 2025 exhibit electronic application form link and exhibit information brochure will be posted online at www.ectc.net under the "Exhibits" section in August 2024. Prospective exhibitors should fill out an application via the form link to start the process of reserving an exhibit space for 2025. Please contact Sam Karikalan at samkarikalan@ieee.org for more information or with any questions.

Call for Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on topics described on the previous page. From the proposals received, up to 16 PDCs will be selected for offering at the 75th ECTC on Tuesday, May 27, 2025. Each selected course will be given a minimum honorarium of $1,500. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. Attendees of the PDCs will be offered Continuing Education Units (CEUs) or Professional Development Hours (PDHs). These CEUs and PDHs are recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives, Course Outline, Who Should Attend," 200-word proposals must be submitted via the ECTC website at www.ectc.net by October 7, 2025. Authors will be notified of course acceptance with instructions by December 9, 2025. If you have any questions, contact:

Kitty Pearsall, ECTC Professional Development Courses Chair
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IEEE EPS Society Travel Grant Program

IEEE EPS is pleased to continue the IEEE EPS Travel Grant Program for the 75th ECTC. The goals of this award are to foster maximum student participation in ECTC and to recognize students with superior ECTC papers. We encourage all student authors to apply for this prestigious grant that will allow you to participate fully in the premier conference for electronic packaging.

Description: Grants are available to apply towards actual travel expenses, including airfare, hotel, and meals. Grants will be awarded competitively, based on abstracts submitted by student authors. The student who is named as the primary author of each winning abstract will receive a travel grant.

Eligibility: The competition is open to all full-time graduate students enrolled at an accredited institution in a program of study within the scope of ECTC. The student must be listed as the primary author on the abstract. A maximum of two authors (one per paper) from any one institution will receive a travel grant.

Application Process: To apply, check the "IEEE EPS Society Travel Grant" box in the "Awards" section of the online abstract submission form. Pre-selected abstracts based on technical committee scores will be requested to submit an extended abstract.

Intel Student Paper Awards

Intel Corporation is sponsoring awards for the best paper and an outstanding paper submitted, first authored, and presented by a student at the ECTC. The winning student will be presented with a certificate and a check for $2,500 for Best Student Paper and $1,500 for Outstanding Student Paper.

Eligibility: To be considered for the award, the student must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author (contact author and first author) and present the paper at the upcoming conference. Finalists will be determined by a review of the completed manuscripts by the judging committee. Manuscripts will be reviewed for relevance to the competition topics, technical content, and originality.

The author of the best and the outstanding student paper will be notified after the conference and must submit an affidavit from the student's faculty advisor certifying that the student meets the eligibility requirements.

Application Process: To enter the Intel Student Paper Awards competition, please check the "Intel Best Student Paper Award" box in the "Awards" section of the online abstract submission form.

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