

SHERATON SAN DIEGO HOTEL & MARINA, SAN DIEGO, CALIFORNIA, USA • JUNE 1 - 4, 2021

Introduction



Conference (ECTC) Program Committee, it is my pleasure to invite you to submit an abstract for the 71st ECTC, to be held June 1 – 4, 2021, at The Sheraton San Diego Hotel and Marina, San Diego, California. This premier international conference, sponsored by the IEEE Electronics Packaging Society (EPS), covers a wide spectrum of electronic packaging technology topics, including components, materials, assembly, interconnect design, device and system packaging, heterogeneous integration, wafer level packaging, Si photonics and optoelectronics, LED, IoT, 5G and emerging Ditegration technology and reliability.

On behalf of the IEEE Electronic Components and Technology

technologies, 2.5D and 3D integration technology, and reliability.

The ECTC Program Committee, with more than 200 experts from broad-ranging technical areas, is committed to creating an engaging technical program for all. ECTC typically attracts more than 1,500 attendees from over 25 countries. Last year's 70th ECTC, originally scheduled to be held in-person in Lake Buena Vista, Florida, had to be converted to an online platform due to the pandemic. The virtual conference had over 7,500 attendees from more than 55 countries around the world with 346 video presentations featured in 45 technical sessions. Additionally, there were seven special sessions with 60 invited presentations. The 71st ECTC will continue with the same tradition of being the premium venue to showcase all the

Major Topics

Highly rated abstracts are accepted for presentation at the ECTC conference. It is important that authors identify the subcommittees whose topic areas best fit their abstracts. Abstracts should include original and previously unpublished, non-confidential, and non-commercial information on new developments, technology, and knowledge in the areas including, but not limited to, those given below for each technical subcommittee.

Applied Reliability: Reliability of 2D, 2.5D, Si bridge, 3D, WLCSP, FOWLP, FOPLP & heterogeneous integration; interconnect reliability in micro-pillar; Cu-pillar; TSV, RDL, stackeddie, hybrid-bond, flip chip & wire bonded packages; emerging product reliability including LED, memory, IoT and autonomous vehicles, medical/wearable electronics; novel reliability test methods, life models, FA techniques & materials characterization; component and board level reliability in computing, HPC, mobile, networking, automotive and harsh environments, AI, autonomous vehicles, and displays.

Assembly and Manufacturing Technology: Advances in fan out and panel level assembly; advances in 3D stacking – die and wafer bonding; challenges in heterogeneous process integration and manufacturing; advanced transfer and compression molding for double-side encapsulation; assembly and manufacturing advances in flexible and printed electronics; thermally enhanced packaging and assembly challenges; additive manufacturing for electronics packaging; advances in high power, high frequency 5G/RF packaging; chiplets – assembly challenges, materials and integration.

Emerging Technologies: Emerging, novel, and unique packaging and material technologies for: soft and intelligent packaging, flexible/stretchable hybrid electronics, implantable biosensors and bioelectronics, extreme harsh environment, green/bio-resorbable packaging, nanomanufacturing, paper sensors/electronics pop-up/origami, MEMS & NEMS, close-tomotor high-voltage power electronics, packaging for wide band gap devices, anti-tamper, cryptography, additive manufacturing, packaging for quantum computing and electro-optical integration, Al, ML and computer vision for packaging, point-of-care diagnostic packaging, packaging sensing and communication, and space hardened packaging technologies.

Interconnections: Interconnection technology and processing: Fan-out, panel-level, chiplets, SiP, flip-chip, 2.5D/3D, Si/glass/organic interposers, TSV, micro-bump, Cu pillar, wirebonds, high I/O thermo-compression/hybrid bonding, fine-pitch/multi-layer RDL, printable interconnects, flexible substrates; interconnect material, characterization and reliability: conductive/non-conductive adhesives, low temperature solder; under-fill, molding compounds, thermal interface materials, thermal/mechanical/electrical tests and reliability; interconnects design and technology for emerging applications: HPC, mobile, 5G, IoT, power and rugged electronics, medical and health, automotive, aerospace, flexible hybrid electronics, micro-LED display.

Materials & Processing: Wafer & panel level packaging materials; materials for harsh environments; packaging substrates; flexible, stretchable, & wearable electronics; wafer bond/ debond materials; TSV; emerging electronic materials & processes; novel solder metallurgies; dielectrics and underfills; molding compounds; thermal interface materials; advanced wirebonding, conductive adhesives. latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling.

The 71st ECTC program will include six parallel technical sessions in the mornings and afternoons over three days, along with other special topic panel discussions to present highlevel trends and best practices in the industry. Professional Development Courses (PDCs) will also be offered by world-class experts, enabling participants to broaden their technical knowledge base. The technical program and PDCs will be supplemented by Technology Corner Exhibits, which provide an opportunity for leading companies in the electronic components, materials, and packaging fields to exhibit their latest technologies and products. As the Program Chair of the 71st ECTC, I invite you to submit an abstract between 250 and 750 words that describes the scope, content, and key points of your proposed technical paper at www.ectc.net. The deadline for abstract and proposal submission is October 4, 2020. Manuscripts conforming to the ECTC format are due by February 19, 2021, for inclusion in the Conference Proceedings. All abstracts and manuscripts must be original, free of commercial content, and non-confidential. On behalf of the ECTC Program Committee, I look forward to seeing you at The Sheraton San Diego Hotel and Marina, San Diego California, USA at the 71st ECTC, June 1 – 4, 2021. At this time we plan to hold ECTC 2021 in person in San Diego; however, we are also developing plans for a successful hybrid or virtual conference if indicated by pandemic-related factors.

Ibrahim Guven 71st ECTC Program Chair

Packaging Technologies: Architectures, methods, and applications for 2.5 & 3D, TSV & interposer; advanced flip-chip, SiP, CSP, PoP, MEMS, sensors & IoT; automotive & power electronics; bio, medical, flexible & wearable packaging; embedded & advanced substrates; fanout, wafer & panel level processes; heterogeneous integration.

Photonics: Integrated photonic circuits, chips, wafer & panel level; lasers & LEDs; silicon & III-V photonics; optical sensors, interconnects, interposers, and quantum device packaging; photonics SiP; free-space optical communications, waveguide, backplane and circuit board technologies; automotive photonics, LiDAR, 3D sensing; optoelectronic fiber coupling assembly, materials and reliability; fiber optic transceivers.

RF, High-Speed Components & Systems: 5G, IoT, cloud computing, autonomous vehicles, Al/machine learning; antennas, sensors, power transfer, EM shielding, wired/ wireless communications, RF to THz; electrical and multi-physics modeling, simulation and characterization of interconnects, components, modules, and heterogeneous integration; signal/power integrity, chip/package/board co-design.

Thermal/Mechanical Simulation & Characterization: Component, board and system level modeling for microelectronics, 3D interconnects, 2.5D packaging, flexible substrates/systems, wafer-level package (WLP), ball grid array (BGA), fan-out packages, embedded packages with active and passive components, system-in-package (SiP), chiplet systems/packages, panel level packaging (PLP), power electronic modules, LED packaging, RF materials & RF/5G systems, and MEMS; reliability modeling related fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop test, material constitutive relations and characterization; chip-package interaction, wafer fabrication process related modeling novel modeling techniques including multi-scale physics, and co-design approaches, and wide range strain rate solutions; measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, probability, machine learning and digital twin; fab/thin wafer handling, wire bonding and assembly manufacture process.

Interactive Presentations: Highly encouraged at ECTC, presenter and attendee often communicate more efficiently here than in oral presentations. Abstracts can relate to any electronics packaging topic. Interactive presentation session papers are published and archived in equal merit with the other ECTC papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact: Ibrahim Guven, 71st ECTC Program Chair E-mail: iguven@vcu.edu

Abstracts must be received by October 4, 2020. All abstracts must be submitted electronically at www.ectc.net. You must include the affiliation, contact telephone number, and e-mail address for all authors, besides the mailing address for the presenting author:

Visit the ECTC website (www.ectc.net) for additional conference information.

Call for Professional Development Courses

See page two.

Abstract and Manuscript Submission

You are invited to submit an abstract between 250–750 words that describes the scope, content, and key points of your proposed paper via our website at www.ectc.net. Additional details on how to submit abstracts electronically can be found on the ECTC website under the "Author Info" tab. Submitted abstracts become the property of ECTC, and ECTC reserves the right to publish the abstracts accepted for the conference. ECTC also reserves the right to prohibit, limit, or reject any editing of submitted abstracts. Abstracts accepted for the conference may not be edited until manuscript submission. Abstracts must be received by October 4, 2020. Your submission must be cleared by management and co-authors as applicable and include the affiliation, contact telephone number, and e-mail address for all authors, besides the mailing address for the presenting author: Please select two different program subcommittees in order of preference that should evaluate your submission for acceptance. Authors will be notified of paper acceptance with instructions for publication by December 11, 2020. At the discretion of the Program Committee, submitted abstracts may be considered for Interactive Presentation sessions.

Manuscripts conforming to the ECTC format are due in final form for publication in the Conference Proceedings by February 19, 2021. **Manuscripts not submitted by this date may be removed and replaced in the final program at the discretion of the Program Committee.** The submitted content must be original, previously unpublished, non-confidential, and without commercial content. All submitted manuscripts are checked for plagiarism and excessive self-duplication of previously published work through the IEEE CrossCheck system. For additional information regarding abstract and paper submission, please contact:

> Ibrahim Guven, 71st ECTC Program Chair E-mail: iguven@vcu.edu

Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose author(s) receive an ECTC personalized wall plaque and share a check for \$2,500.

Best Interactive Presentation Award: Each year the ECTC selects the best Interactive Presentation paper whose author(s) receive an ECTC personalized wall plaque and share a check for \$1,500.

Outstanding Paper Award: An outstanding conference paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for \$1,000.

Outstanding Interactive Presentation Award: An outstanding Interactive Presentation paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for \$1,000.

Intel Best Student Paper Award: Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at ECTC. The winning student will be presented with a wall plaque and a check for \$2,500. See next column for details.

Texas Instruments Outstanding Student Interactive Presentation Award: Texas Instruments is sponsoring an award for the best student Interactive Presentation at ECTC. The winning student will be presented with a wall plaque and a check for \$1,000.

Technology Corner Exhibits

ECTC invites you to be part of the Technology Corner exhibit and showcase your products and services to engineers and managers from all areas of the microelectronics packaging industry. Over 1,500 attendees are expected for the 71st ECTC, representing companies from around the world.

Exhibit Dates: June 2 – 3, 2021 For more information contact: Alan Huffman, ECTC Exhibits Chair Phone: +1-919-248-9216

E-mail: alan.huffman@micross.com; ectc.exhibits@micross.com

The 2021 Exhibit Application form will be posted online at www.ectc.net under the "Exhibits" section in August 2020. Prospective exhibitors should fill out an application and return to the e-mail addresses above. ECTC exhibit booth allocation is first based on consecutive years of exhibit participation and/or Gold or Platinum Sponsorship. Please contact Alan Huffman at alan.huffman@micross.com for more information or with any questions.

Sponsorship Opportunities

to Enhance Your Presence at ECTC

ECTC also offers excellent opportunities for promotion and visibility through sponsorships at platinum, gold and silver levels as well as of badge lanyard, USB flash drive proceedings, media, refreshment breaks, program, and the student reception. Additional information is available at www.ectc.net under "Sponsors." Please contact:

Wolfgang Sauter, Sponsorship Chair Marvell Semiconductor Inc., USA Phone: +1-802-922-3083 E-mail: wsauter2@gmail.com

Call for Professional Development Courses

As a result of the 2020 ECTC going virtual, the Professional Development Courses were not presented this year. All 2020 PDC instructors have been invited to present their professional courses at the 2021 ECTC in San Diego, CA. As usual there will be 18, four-hour courses offered. All 2020 instructors are currently being contacted to ensure their participation at the 2021 ECTC. If for some reason we have an opening a notice will be sent out as soon as possible.

If you have any questions, contact: Kitty Pearsall 71st ECTC Professional Development Courses Chair Boss Precision, Inc. 1806 W. Howard Lane, Austin, TX 78728, USA Phone: +1-512-845-3287 E-mail: kittypearsall@gmail.com

IEEE EPS Society Travel Grant Program

IEEE EPS is pleased to continue the IEEE EPS Travel Grant Program for the 71st ECTC. The goals of this award are to foster maximum student participation in ECTC and to recognize students with superior ECTC papers.

Description: Grants are available to apply towards actual travel expenses, including airfare, hotel, and meals. Grants will be awarded competitively, based on abstracts submitted by student authors. The student who is named as the primary author of each winning abstract will receive a travel grant.

Eligibility: The competition is open to all full-time graduate students enrolled at an accredited institution in a program of study within the scope of ECTC. The student must be listed as the primary author on the abstract. A maximum of two authors (one per paper) from any one institution will receive a travel grant.

Application Process: To apply, check the "IEEE EPS Society Travel Grant" box in the "Awards" section of the online abstract submission form. Pre-selected abstracts based on technical committee scores will be requested to submit an extended abstract.

Intel Best Student Paper Award

Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at the ECTC. The winning student will be presented with a wall plaque and a check for \$2,500.

Eligibility: To be considered for the award, the student must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author and present the paper at the 71st ECTC. It is the convention at ECTC for the presenter to be listed as the first author. Finalists will be determined by review of the completed manuscripts by the judging committee. Manuscripts will be reviewed for relevance to the competition topics, technical content, and originality. The author of the best student paper will be notified after the conference and must submit an affidavit from the student's faculty advisor certifying that the student meets the eligibility requirements.

Application Process: To enter the Intel Best Student Paper Award competition, please check the "Intel Best Student Paper Award" box in the "Awards" section of the online abstract submission form.

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