Conference Programs & Exhibitor Listings

Welcome to the electronic packaging's premier conference!

ECTC 2013

The 63rd Electronic Components and Technology Conference

May 28-31, 2013

The Cosmopolitan of Las Vegas
Nevada, USA

Sponsored by:

Supported by:

For more information, visit: www.ectc.net

Welcome from the Mayor of Las Vegas

CAROLYN G. GOODMAN
MAYOR

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ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE

MAY 28 – 31, 2013

LAS VEGAS, NEVADA

Dear Friends,

As Mayor of the great City of Las Vegas, it is a pleasure to welcome you to the 2013 Electronic Components and Technology Conference at the Cosmopolitan.

Las Vegas continues to capture the world's imagination as a city where anything is possible. With world-class hotels, award-winning restaurants, luxurious spas, fantastic shopping, the finest golf courses, and spectacular entertainment, Las Vegas remains one of the most electrifying destinations in the world.

While visiting or relocating to our City, it is my hope that you will have a chance to explore Downtown Las Vegas, an area of our City that is undergoing a dramatic renaissance. It is evolving into a vibrant place for living, working, entertainment, and the arts. Downtown Las Vegas is comprised of an enticing mix that includes:

-The neon-drenched excitement of the Fremont Street Experience, visited by over 21 million people each year.

-Multi-million dollar casino and hotel renovations and expansions.

-Fremont East Entertainment District featuring trendy new gathering places for dining, dancing, cocktails and enjoyment.

-An emerging eclectic mix of live-in artists and galleries known as the 18b Arts District.

-Symphony Park, a phenomenal 61-acre planned development anchored by two key projects, the Cleveland Clinic Lou Ruvo Center for Brain Health, designed by renowned architect Frank Gehry, and The Smith Center for the Performing Arts, Las Vegas' first world-class performing arts facility.

-A collection of world-class museums including the Neon Museum Boneyard, which holds over 100 donated and rescued Las Vegas signs that date from the late 1930s through the early 90s; the Mob Museum, which provides a fascinating glimpse into our City's history; and the Discovery Children's Museum in Symphony Park, among others.

Please take this opportunity to enjoy all that our grand City has to offer. Again, best wishes for a joyful, productive, and memorable conference.

Sincerely,

Carolyn G. Goodman
Mayor, City of Las Vegas

WELCOME FROM ECTC GENERAL AND PROGRAM CHAIRS

On behalf of the Program Committee and Executive Committee, it is my pleasure to welcome you to the 63rd Electronic Components and Technology Conference (ECTC) at The Cosmopolitan of Las Vegas, Nevada, USA. This premier international conference is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

The ECTC Program Committee represents a wide range of disciplines and expertise from the electronics industry around the world. We have selected more than 300 high-quality papers to be presented at the conference in 36 oral sessions, four interactive presentation sessions, and one student posters session. The 36 oral sessions cover papers on 3D/TSV, embedded devices, LEDs, Co-Design, RF packaging, and electrical and mechanical modeling, in addition to topics such as advanced packaging technologies, all types and levels of interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, MEMS, and sensors. The program committee strives to address new trends as well as ongoing technological challenges. Four Interactive Presentation sessions feature technical presentations in a format that enhances and encourages interaction. One student poster session focuses on research conducted in academia presented by the emerging scientists. Authors from companies, research institutes, and universities from over 25 countries will present at the ECTC, making it a truly diverse and global conference.

In addition to the technical sessions, panel and special sessions focusing on crucial topics presented by industry experts enhance the technical program. In the special session titled "The Role of Wafer Foundries in Next Generation Packaging," held Tuesday, May 28, at 10 a.m., session chair Sam Karikalan will gather a panel of experts to present and discuss their proposed business models and strategies for embracing the next generation packaging needs of the industry. Key questions on cost, technology, assembly expertise and industry growth will be raised for the wafer foundries to address. Another special session will be held on Tuesday and will address "Modeling and Simulation Challenges in 3D Systems." This session co-chaired by Yong Liu and Dan Oh is made up of keynote speakers as well as highlighted 3D modeling papers and will be held at 2 p.m. The Panel Discussion on Tuesday evening at 7:30 p.m., chaired by Ricky Lee and Kouchi Zhang titled "LED for Solid-State Lighting – For a Brighter Future," will discuss emerging LED packaging technologies and market trends. The Plenary Session on Wednesday at 7:00 p.m., chaired by Lou Nicholls and titled "Packaging Challenges Across the Wireless Market Supply Chain," will unveil the latest challenges of this growing industry with speakers from across the supply chain. Thursday evening starts with the Gala Reception at 6:30 p.m. and is followed by the CPMT Seminar at 8:00 p.m., which is titled "Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications" and chaired by Kishio Yokouchi and Venky Sundaram.

The Professional Development Courses (PDCs), organized by the PDC Committee chaired by Kitty Pearsall, will be taught on Tuesday, May 28 (8:00 a.m.-5:30 p.m.). World-class experts in their fields offer 16 courses on different topics. Participants can catch up on new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the Technology Corner Exhibits where leading companies, primarily in the electronics components, materials, and packaging fields exhibit their latest technologies and products. The exhibitors invite you to their reception on Wednesday at 5:30 p.m. Along with our receptions and coffee breaks every day, luncheons are another great opportunity to network and discuss technical and business matters. It is my pleasure to announce that Dr. Chris Welty of IBM will be the invited keynote speaker at the ECTC Luncheon on Wednesday.

ECTC offers many opportunities. Whether you are a manager, engineer, executive or a student, I invite you to experience the exciting developments in electronic components and technology during the 2013 ECTC. I also would like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, instructors, session chairs, committee members, and arrangements, finance, publication, and publicity chairs, as well as all the volunteers for their support and hard work in making the 63rd ECTC a great success. I look forward to a great experience in exciting Las Vegas on May 28 - 31, 2013.

Wolfgang Sauter
General Chair
IBM Corporation

Beth Keser
Program Chair
Qualcomm Technologies, Inc.

WELCOME FROM ECTC SPONSORING ORGANIZATION

It's Vegas again!

According to the previous statistics, every time ECTC was held in Las Vegas, it was always a big crowd. I believe the same trend will continue in 2013. For people who survived from 2012 (if you know what I mean), you deserve a big treat and should enjoy yourself as much as possible in Vegas. Thanks to the effort of ECTC Executive Committee, this year we have the conference venue set up at the magnificent Cosmopolitan. Undoubtedly everybody will have a good time at this modern and well-equipped hotel.

In addition to the great venue, we also have a very strong technical program this year, in particular, on the 3D/TSV topics. I am very pleased to note that the ECTC Program Committee improved the Advance Program and compiled a table of "Session Summary by Interest Areas." This will be very helpful for the attendees to navigate themselves among interested topics and sessions. I would like to take this opportunity to thank the Program Committee members for their thoughtful planning and considerate arrangement.

As a common practice, there are a number of activities organized by CPMT within ECTC. In the evening of May 28, there will be a panel session on "LED for Solid-State Lighting." This panel will discuss emerging LED packaging technologies and global market trends. On May 30, CPMT will sponsor a plenary luncheon and several important awards will be presented during the luncheon. In the evening on the same day, a CPMT seminar will be held right after the Gala Reception. This seminar will focus on "Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications." On behalf of the IEEE CPMT Society, I would like to invite all of you to attend these special events.

See you all there!
Ricky Lee
President, IEEE CPMT Society

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
The hotel allows smoking on its premises in designated smoking areas; however, smoking is NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, or seminars as well. Thank you for your consideration and cooperation.

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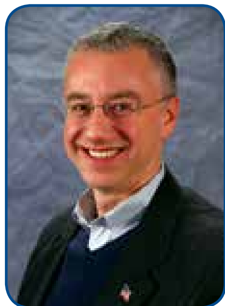

ECTC Luncheon Keynote Speaker

Wednesday, May 29, 2013 • 12:00PM
Chelsea 1 & 5

Engineering Challenges in Building Watson

Presenter: Dr. Chris Welty
Research Scientist at the
IBM T.J. Watson Research Center

Two years ago, the Watson Question Answering system received widespread attention and acclaim by winning a two-game tournament of Jeopardy!, the TV quiz show, against the best players in the game's history. While a significant advance in natural language processing, Watson was ultimately a system engineered by a talented team of researchers, and some of the challenges we faced and surmounted make good lessons for engineering in general.

Christoper A. Welty is a Research Scientist at IBM Thomas J. Watson Research Center in New York, and formerly a professor in the Computer Science Department of Vassar College and a distinguished lecturer of the Association for Computing Machinery. He is best known for his work on ontologies and in the Semantic Web.

Welty was one of the developers of Watson, the IBM computer that defeated the best players on the American game show Jeopardy!. He was one of the 12 original members of the Watson team and is identified as a member of its "Core Algorithms Team."

2013 iNEMI Roadmap - North American Workshop

Tuesday, May 28, 2013
1:00PM - 6:00PM
Condesa 6, 2nd Floor

Since 1994, iNEMI (the International Electronics Manufacturing Initiative) has been developing a biennial technology roadmap spanning a 10-year horizon. Since 2011 iNEMI has been holding roadmapping meetings at ECTC.

This year we will be holding an open meeting to prioritize the research needs identified in the 2013 Roadmap; the output will be the publication of the 2013 iNEMI Research Priorities.

Open to all conference attendees.

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located on the 4th floor in the Chelsea Commons Area.

Monday, May 27, 2013 – 3:00 p.m. - 5:00 p.m.

Tuesday, May 28, 2013 – 6:45 a.m. - 8:15 a.m.*
(AM PD Courses & Special Session Only)*

Tuesday, May 28, 2013 – 8:15 a.m. - 5:00 p.m.
(All conference attendees)

Wednesday, May 29, 2013 – 6:45 a.m. - 4:00 p.m.

Thursday, May 30, 2013 – 7:30 a.m. - 4:00 p.m.

Friday, May 31, 2013 – 7:30 a.m. - 12:00 p.m.

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time on Tuesday, May 28 as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees

Door Registration with Proceedings on USB drive

IEEE Member Full Registration	$725
IEEE Member Speaker / Session Chair	$625
IEEE Member One Day	$475
IEEE Member Speaker One Day	$350
Non-Member Full Registration	$870
Non-Member Speaker / Session Chair	$625
Non-Member One Day	$475
Non-Member Speaker One Day	$350
Exhibit Booth Attendant	$0
Student	$250
Student Speaker	$250
Exhibits Only	$20

Tuesday Professional Development Courses
IEEE Members and Non-Members

Tuesday AM or PM Course with luncheon	$475
Tuesday All-Day Courses with luncheon	$675
Tuesday Student All-Day Courses with luncheon	$125
Extra Luncheon Tickets for each day	$50
Extra Proceedings with registration	$100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

6:45 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Chelsea 2)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows XP and MS Office 2003.

7:00 a.m. Wednesday thru Friday
(Room Location: Chelsea 1)

Speaker Prep Room

Speakers should prepare and review their digital presentations as follows: 7:00 a.m. – 5:00 p.m., Tuesday – Friday (Room Location: Yaletown 3)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to any show or restaurant, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Message Center
Please use the hotel switchboard or the ECTC Registration Desk located on the 4th floor, Chelsea Commons, to leave and pickup messages. The hotel number is +1-877-551-7772.

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts, please contact Eric Perfecto at perfecto@us.ibm.com or +1-845-894-4400.

LUNCHEONS

Tuesday, May 28, 2013
Noon (Chelsea 2)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, May 29, 2013
Noon (Chelsea 1 & 5)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Chris Welty of IBM Corporation.

Thursday, May 30, 2013
Noon (Chelsea 1 & 5)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, May 31, 2013
Noon (Chelsea 1 & 5)
The ECTC Program Chair will sponsor a luncheon for conference attendees.

There will be a raffle for attendees.

SPECIAL SESSION, PANEL SESSION, PLENARY SESSION, CPMT SEMINAR AND MODELING SESSION

2013 SPECIAL SESSION

Tuesday, May 28, 2013
10:00 AM – Noon
Condesa 3, 2nd Floor

The Role of Wafer Foundries in Next Generation Packaging

Chair: Sam Karikalan, Broadcom Corporation

Speakers:
Jerry Tzou, TSMC
David McCann, GLOBALFOUNDRIES
Kurt Huang, UMC
Jon Casey, IBM Corporation
Herb Huang, SMIC

2013 ECTC PANEL SESSION

Tuesday, May 28, 2013
7:30 - 9:30 p.m.
Mont-Royal I & 2, 4th Floor

LED for Solid-State Lighting – For a Brighter Future

Chair: Ricky Lee, Hong Kong University of Science and Technology
Co-chair: Kouchi Zhang, TU Delft & Philips Lighting

Speakers:
Ling Wu, China Solid-State Lighting Alliance, China
Mark McClear, Cree Components, USA
Ron Bonne, Philips Lumileds, USA
Nils Erkamp, TNO, The Netherlands
Michael McLaughlin, Yole Development, USA

2013 ECTC PLENARY SESSION

Wednesday, May 29, 2013
7:00 - 9:00 p.m.
Mont-Royal I & 2, 4th Floor

Packaging Challenges Across the Wireless Market Supply Chain

Chair: Lou Nicholls, Amkor Technology

Speakers:
Timo Henttonen, Nokia
Steve Bezuk, Qualcomm Technologies, Inc.
Waite Warren, RFMD
Roger St. Amand, Amkor Technology
SoonJin Cho, SEMCO

2013 CPMT SEMINAR

Thursday, May 30, 2013
8:00 - 10:00 p.m.
Mont-Royal I & 2, 4th Floor

Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications

Chair: Kishio Yokouchi, Fujitsu Interconnect Technologies Ltd.
Co-chair: Venky Sundaram, Georgia Institute of Technology

Speakers:
Yuya Suzuki, Zeon Corporation
Yasuyuki Mizuno, Tsukuba Research Laboratory, Hitachi Chemical Co., Ltd.
Shin Teraki, NAMICS Corporation
Hirohisa Narahashi, The Research Institute for Bioscience Products & Fine Chemicals, Ajinomoto Co., Inc.

2013 ECTC MODELING SESSION

Tuesday, May 28, 2013 • 2:00 - 4:30 p.m.
Condesa 3, 2nd Floor

Modeling and Simulation Challenges in 3D Systems
Chair: Yong Liu, Fairchild Semiconductor
Co-Chair: Dan Oh, Altera

Keynote Speaker: Thermo-Mechanical Modeling of 3D Integration Technology: Impact of Actual Process Conditions and Non-ideal Material Properties on Modeling Results, Eric Beyne – IMEC

A Comparative Simulation Study of 3D/Through Silicon Stack Assembly Processes, Kamal Karimanal – Cielution LLC

Thermo-Mechanical Challenges for Processing and Packaging Stacked Ultrathin Wafers, Mario Gonzalez, Bart Vandevelde, Antonio La Manna, Bart Swinnen, and Eric Beyne – IMEC

Keynote Speaker: Cloud-Based Scalable Electromagnetic Solvers for 3D Package Modeling, Vikram Jandhyala – University of Washington, Nimbic

Signal and Power Integrity Analysis of a 256GB/s Double-Sided IC Package with a Memory Controller and 3D Stacked DRAM, Wendem Beyene, Hai Lan, Scott Best, David Secker, Don Mullen, Ming Li, and Tom Giovannini – Rambus Inc.

Optimization of 3D Stack for Electrical and Thermal Integrity, Rishik Bazaz, Jianyong Xie, and Madhavan Swaminathan – Georgia Institute of Technology

These sessions/seminars are open to all conference attendees.

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 28, 2013

Morning Courses 8:00 AM – 12:00 PM	Afternoon Courses 1:15 – 5:15 PM
Yaletown 4 **1."Lead Free Solder Joint Reliability Material Consideration"** Course Leader: NingCheng Lee – Indium Corporation	**Yaletown 4** **9."Packaging Failure Analysis – Failure Analysis and Analytical Tools"** Course Leaders: Rajen Dias and Deepak Goyal – Intel Corporation
Nolita 3 **2."Multi-Physics Modeling in IC Packaging and Microsystems"** Course Leader: Xuejun Fan – Lamar University	**Nolita 3** **10."Modeling and Simulation of Reliability in Electronic Packaging"** Course Leaders: Craig Hillman and Nathan Blattau – DfR Solutions
Nolita 2 **3."Thermal and Mechanical Simulation Techniques for 3D Stacking Yield and Reliability"** Course Leader: Kamal Karimanal - Cielution LLC	**Nolita 2** **11."TSV and Other Enabling Technologies for 3D IC Integration"** Course Leader: John Lau – Industrial Technology Research Institute
Nolita 1 **4."Wafer Level-Chip Scale Packaging (WL-CSP)"** Course Leader: Luu Nguyen – Texas Instruments, Inc.	**Nolita 1** **12."Chip Package Interaction with TSV Reliability for 40 nm and Below"** Course Leader: C. S. Premachandran – GLOBALFOUNDRIES
Mont-Royal 1 **5."Polymers and Nano-Composites for Electronic and Photonic Packaging"** Course Leaders: C.P. Wong – Georgia Tech; Daniel Lu – Henkel Corporation	**Mont-Royal 1** **13."Polymers in Electronic Packaging"** Course Leaders: Jeffrey Gotro – InnoCentrix, LLC
Mont-Royal 2 **6."Power Electronics Thermal Packaging and Reliability"** Course Leaders: Avram BarCohen and Patrick McCluskey – University of Maryland	**Mont-Royal 2** **14."Flip Chip Packaging"** Course Leader: Eric Perfecto – IBM Corporation
Chelsea 1 **7."Fundamental Concepts, Reliability and Mechanics in Electronic Packaging"** Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation	**Chelsea 1** **15."Design for Package Reliability"** Course Leaders: Darvin Edwards and Yaoyu Pang – Texas Instruments, Inc.
Chelsea 5 **8."High-Frequency Modeling and Optimization of Interconnections in Electronic Packaging"** Course Leaders: Ivan Ndip and Michael Toepper – Fraunhofer IZM	**Chelsea 5** **16."IC Package Design for Signal/Power Integrity and Electromagnetic Compatibility"** Course Leader: Sam Karikalan – Broadcom Corporation

REFRESHMENT BREAKS – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
MONT-ROYAL COMMONS & CHELSEA COMMONS

ECTC STUDENT RECEPTION
Tuesday, May 28, 2013
5:00 - 6:00 p.m.
Room: Chelsea 2
Host: Eric Perfecto – IBM Corporation

Students, have you ever wondered how the ECTC technical committees review and select papers? Or, just what subjects, content and paper organization make a standout ECTC paper? Then please come to the ECTC Student Reception. You'll have a chance to enjoy some good food and meet with representatives of each technical subcommittee. Don't miss this chance for an inside view of technical subcommittee operations. Sponsored by the IBM Corporation.

GENERAL CHAIR'S SPEAKERS RECEPTION
Tuesday, May 28, 2013
6:00 - 7:00 p.m.
Room: Blvd Pool North (Outside Pool Area, 4th floor, facing the Las Vegas Strip); Rain backup: Chelsea 2

Invited session chairs and speakers are requested to attend this reception.

TECHNOLOGY CORNER RECEPTION
Wednesday, May 29, 2013
5:30 - 6:30 p.m.
Room: Chelsea 3 & 4

All attendees and guests are invited to attend this exhibitor sponsored reception. Please use this time to mix and mingle with all exhibitors, learn about their products and services, and pick up a few giveaways.

63RD ECTC GALA RECEPTION
Thursday, May 30, 2013
6:30 p.m.
Room: Chelsea 1 & 5

All badged attendees and guests are invited to attend our Gala Reception. This is a great way to meet your conference colleagues, speakers, exhibitors, guests, and the ECTC Executive Committee.

CONTINUING EDUCATION UNITS

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 63rd ECTC.
CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the "IEEE CPMT Professional Development Certificate." Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Courses CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.

2012 ECTC PAPER AWARDS

Best of Conference Papers

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 62nd ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Poster Paper share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

(Session 28, paper 4)

Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up to 50,000G

Pradeep Lall, Kewal Patel, Ryan Lowe, Mark Strickland, Jim Blanche, Dave Geist, Randall Montgomery – Auburn University

Best Poster Paper

(Session 37, paper 17)

Void Formation during Reflow Soldering

Thomas D. Ewald – Robert Bosch GmbH, TU Dresden; Norbert Holle – Robert Bosch GmbH; Klaus-Jürgen Wolter – TU Dresden

Outstanding Papers

The winning authors for Conference Outstanding Session and Poster Papers receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

(Session 24, paper 6)

A 77 GHz SiGe Single-Chip Four-Channel Transceiver Module with Integrated Antennas in Embedded Wafer-Level BGA Package

M. Wojnowski, R. Lachner, J. Böck, G. Sommer, and K. Pressel – Infineon Technologies AG

Outstanding Poster Paper

(Session 37, paper 11)

3D Stacked Microfluidic Cooling for High Performance 3D ICs

Yue Zhang, Ashish Dembla, Yogendra Joshi, and Muhannad S. Bakir – Georgia Institute of Technology

Intel Best Student Paper

The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 62nd ECTC:

(Session 34, Paper 4)

Interlayer Dielectric Cracking in Back End of Line (BEOL) Stack

Sathyanarayanan Raghavan, Ilko Schmadlak and Suresh K. Sitaraman – Georgia Institute of Technology

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 28, 2013

8:00 a.m. – 6:00 p.m.
INEMI Meeting
Condesa 6, 2nd floor

8:00 a.m. – 5:00 p.m.
ITRS Assemblies & Packaging Technology Committee
Condesa 2, 2nd floor

5:00 p.m. – 7:00 p.m.
CPMT Region 8 Advisory Committee
Condesa 1, 2nd floor

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Yaletown 4, 4th floor

Wednesday, May 29, 2013

7:00 a.m. – 8:00 a.m.
CPMT Materials & Processes TC
Condesa 1, 2nd floor

7:00 a.m. – 8:00 a.m.
CPMT High-Density Substrates & Boards TC
Condesa 6, 2nd floor

4:30 p.m. – 5:30 p.m.
CPMT Technical Committee Chairs
Condesa 6, 2nd floor

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

6:30 p.m. – 7:30 p.m.
ECTC Interconnection Committee
Condesa 6, 2nd floor

Thursday, May 30, 2013

7:00 a.m. – 8:00 a.m.
CPMT Photonics TC
Bellavista Boardroom, 2nd floor

7:00 a.m. – 8:00 a.m.
CPMT RF & THz Technologies TC
Condesa 6, 2nd floor

7:00 a.m. – 8:00 a.m.
CPMT Thermal & Mechanical TC
Condesa 5, 2nd floor

5:30 p.m. – 6:30 p.m.
ECTC 2014 Program Committee Meeting
Nolita 1, 4th floor

8:00 p.m.
ECTC Governing/Executive Committee Reception
General Chair's Suite

Friday, May 31, 2013

7:00 a.m. – 8:00 a.m.
CPMT Nanotechnology TC
Condesa 1, 2nd floor

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Jardins Boardroom, 2nd floor

Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

Session 1: 3D Assembly and Reliability

Committee: Advanced Packaging

Mont-Royal 1

Session Co-Chairs:
John Knickerbocker – IBM Corporation
Sam Karikalan – Broadcom Corporation

1. ***8:00 a.m.* – *Reliability Studies on Micro-Bumps for 3D TSV Integration***
   Ho-Young Son, Sung-Kwon Noh, Hyun-Hee Jung, Woong-Sun Lee, Jae-Sung Oh, and Nam-Seog Kim – SK Hynix Inc.

2. ***8:25 a.m.* – *Reliability Evaluation of a CoWoS-Enabled 3D IC Package***
   Bahareh Banijamali, Suresh Ramalingam, and Liam Madden – Xilinx, Inc.; Chien-Chia Chiu, Cheng-Chieh Hsieh, Tsung-Shu Lin, Clark Hu, Shang-Yun Hou, Shin-Puu Jeng, and Doug C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

3. ***8:50 a.m.* – *TSV and Cu-Cu Direct Bond Wafer and Package-Level Reliability***
   K. Hummler, B. Sapp, and I. Ali – SEMATECH; J.R. Lloyd – SUNY, Albany; S. Kruger and S. Olson – SEMATECH; SUNY, Albany; S.B. Park, B. Murray, D. Jung, S. Cain, A. Park, and D. Ferrone – SUNY, Binghamton

4. ***10:00 a.m.* – *Generic Rules to Achieve Bump Electromigration Immortality for 3D IC Integration***
   Hsiao-Yun Chen, Da-Yuan Shih, Cheng-Chang Wei, Chih-Hang Tung, Yi-Li Hsiao, and Douglas Cheng-Hua Yu – Taiwan Semiconductor Manufacturing Company; Yu-Chun Liang and Chih Chen – National Chiao Tung University

5. ***10:25 a.m.* – *3D Integration Technologies Using Self-Assembly and Electrostatic Temporary Multichip Bonding***
   T. Fukushima, H. Hashiguchi, J. Bea, M. Murugesan, K.W. Lee, T. Tanaka, and M. Koyanagi – Tohoku University

6. ***10:50 a.m.* – *Electrical Investigation and Reliability of 3D Integration Platform Using Cu TSVs and Micro-Bumps with Cu/Sn-BCB Hybrid Bonding***
   Yao Jen Chang, C.H. Chiang, T.H. Yu, C.H. Fan, and K.N. Chen – National Chiao Tung University; C.T. Ko – National Chiao Tung University, Industrial Technology Research Institute (ITRI); Z.C. Hsiao, H.C. Fu, and W.C. Lo – Industrial Technology Research

7. ***11:15 a.m.* – *Assembly of 3D Chip Stack with 30um-Pitch Micro Interconnects Using Novel Arrayed-Particles Anisotropic Conductive Film***
   Y.W. Huang, Y.M. Lin, C.J. Zhan, S.T. Lu, S.Y. Huang, J.Y. Juang, C.W. Fan, S.C. Chung, J.S. Peng, S.M. Chen, Y.L. Lu, J.H. Lau, and P.C. Chang – Industrial Technology Research Institute (ITRI)

Session 2: 3D Materials and Processing

Committee: Materials & Processing

Mont-Royal 2

Session Co-Chairs:
Mikel Miller – Draper Laboratory
Bing Dang – IBM Corporation

1. ***8:00 a.m.* – *Development of 3D Through Silicon Stack (TSS) Assembly for Wide IO Memory to Logic Devices Integration***
   Dong Wook Kim, Ramachandran Vidhya, Brian Henderson, Urmi Ray, Sam Gu, Wei Zhao, Riko Radojcic, and Matt Nowak – Qualcomm Technologies, Inc.; Changmin Lee, Jongsik Paek, Kiwook Lee, and Ron Huemoeller – Amkor Technology, Inc.

2. ***8:25 a.m.* – *Investigation on the Properties and Processability of Polymeric Insulation Layers for Through Silicon Via***
   Songfang Zhao, Guoping Zhang, Chongnan Peng, and Rong Sun – Chinese Academy of Sciences; S.W. Ricky Lee – HKUST; Wenhui Zhu and Fangqi Lai – Kunshan Q Technology Ltd.

3. ***8:50 a.m.* – *Process Integration of 3D Si Interposer with Double-Sided Active Chip Attachments***
   P. J. Tzeng, J. Lau, C.J. Zhan, Y.C. Hsin, P.C. Chang, Y.H. Chang, J.C. Chen, S.C. Chen, C.Y. Wu, C.K. Lee, H.H. Chang, C.H. Chien, C.H. Lin, T.K. Ku, M.J. Kao – Industrial Technology Research Inst. (ITRI); M. Li, J. Cline, K. Saito, M. Ji – Rambus, Inc.

4. ***10:00 a.m.* – *Analyzing the Behavior and Shear Strength of Common Adhesives Used in Temporary Wafer Bonding***
   J.A. Sharpe, M.B. Jordan, S.L. Burkett, and M.E. Barkey – University of Alabama

5. ***10:25 a.m.* – *WSS and ZoneBOND Temporary Bonding Techniques Comparison for 80µm and 55µm Functional Interposer Creation***
   A. Jouve, K. Vial, E. Rolland, C. Laviron, M. Fournel, M. Pellat, P. Montmeat, N. Allouti, and R. Eleouet – CEA-LETI; P. Coudrain and C. Aumont – STMicroelectronics

6. ***10:50 a.m.* – *Low Cost, Room Temperature Debondable Spin-On Temporary Bonding Solution: A Key Enabler for 2.5D/3D IC Packaging***
   Ranjith S.E. John, Herman Meynen, Sheng Wang, Peng-Fei Fu, Craig Yeakle, Sang Wook W. Kim, and Lyndon J. Larson – Dow Corning Corporation; Scott Sullivan – Suss MicroTec

7. ***11:15 a.m.* – *Integration and Manufacturing Aspects of Moving from WaferBOND HT-10.10 to ZoneBOND Material in Temporary Wafer Bonding and Debonding for 3D Applications***
   Anne Jourdain, Alain Phommahaxay, Greet Verbinnen, Gayle Murdoch, Andy Miller, Kenneth Rebibis, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero, Jeremy Mc Cutcheon, Mark Privett, and Jason Neidrich – Brewer Science, Inc.

Session 3: Novel Interconnections

Committee: Interconnections

Nolita 1

Session Co-Chairs:
James E. Morris – Portland State University
Lei Shan – IBM Corporation

1. ***8:00 a.m.* – *Effects of Nanofiber Materials of Nanofiber Anisotropic Conductive Adhesives (Nanofiber ACAs) for Ultra-Fine Pitch Electronic Assemblies***
   Kyoung-Lim Suk and Kyung-Wook Paik – KAIST

2. ***8:25 a.m.* – *A Novel Non-TSV Approach to Enhancing the Bandwidth in 3-D Packages for Processor-Memory Modules***
   Dev Gupta – APSTL

3. ***8:50 a.m.* – *Three-Path Electroplated Copper Compliant Interconnects – Fabrication and Modeling Studies***
   Raphael Okereke and Suresh K. Sitaraman – Georgia Institute of Technology

4. ***10:00 a.m.* – *Ultra-Fine Trench Circuit on Polymer Film***
   Takaharu Hondo, Yosuke Nitta, Kei Nakamura, Hiroyuki Hirano, Masanobu Saruta, Toshiaki Inoue, and Osamu Nakao – Fujikura, Ltd.

5. ***10:25 a.m.* – *A Highly Integratable Millimeter-Wave Silicon Waveguide Array for Terabit Application***
   Qidong Wang, Daniel Guidotti, Jie Cui, Liqiang Cao, Tianchun Ye, and Lixi Wan – Chinese Academy of Sciences

6. ***10:50 a.m.* – *Aluminum to Aluminum Bonding at Room Temperature***
   F. Marion, B. Goubault de Brugière, A. Bedoin, M. Volpert, F. Berger, A. Gueugnot, R. Anciant, and H. Ribot – CEA-LETI

7. ***11:15 a.m.* – *Carbon Nanotube Array as High Impedance Interconnects for Sensing Device Integration***
   Dunlin Tan and Dominique Baillargeat – CINTRA; Chin Chong Yap and Beng Kang Tay – Nanyang Technological University; David Hee, Jong Jen Yu, Jean-Luc Reverchon, and Philippe Bois – Thales

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)

Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

Session 4: Reliability Test Methods	Session 5: New Directions in Packaging	Session 6: Optical Interconnects
Committee: Applied Reliability	**Committee:** Emerging Technologies	**Committee:** Optoelectronics
Nolita 2	**Nolita 3**	**Yaletown 4**
Session Co-Chairs: **John H. L. Pang – Nanyang Technological University** **Deepak Goyal – Intel Corporation**	**Session Co-Chairs:** **Vasudeva P. Atluri – Renavitas Technologies** **Joana Maria – IBM Corporation**	**Session Co-Chairs:** **Alex Rosiewicz – Gooch & Housego** **Ping Zhou – LDX Optronics, Inc.**
1. 8:00 a.m. – ***Define Electrical Packing Temperature Cycling Requirement with Field Measured User Behavior Data*** Min Pei, Ru Han, Daeil Kwon, Alan Lucero, Vasu Vasudevan, Robert Kwasnick, and Praveen S. Polasam – Intel Corporation	1. 8:00 a.m. – ***Large-Scale, Surface Tension Assisted Ball-in-Pit Self Population for Chip-to-Chip Passive Alignment*** Chaoqi Zhang – Georgia Institute of Technology; Hiren D. Thacker, Ivan Shubin, Ashok V. Krishnamoorthy, James G. Mitchell, and John E. Cunningham – Oracle Labs	1. 8:00 a.m. – ***Optical Backplane for Board-to-Board Interconnection Based on a Glass Panel Gradient-Index Multimode Waveguide Technology*** Lars Brusberg, Henning Schröder, and Julia Röder – Fraunhofer IZM; Richard Pitwon and Allen Miller – Xyratex Technology Ltd.; Simon Whalley – ILFA Feinstleitertechnik GmbH; Christian Herbst, Marcel Neitz, and Klaus-Dieter Lang – TU Berlin
2. 8:25 a.m. – ***Characterization of Aging Effects in Lead-Free Solder Joints using Nanoindentation*** Jeffrey C. Suhling, Mohammad Hasnine, Muhannad Mustafa, Barton C. Prorok, Michael J. Bozack, and Pradeep Lall – Auburn University	2. 8:25 a.m. – ***Through-Silicon-Via Process Control in Manufacturing for SiGe Power Amplifiers*** J.P. Gambino, T. Doan, J. Trapasso, C. Musante, D. Dang, and D. Vanslette – IBM Corporation; D. Grant, D. Marx, and R. Dudley – Tamar Technology	2. 8:25 a.m. – ***Single-Chip 4 TX + 4 RX Optical Module Based on Holey SiGe Transceiver IC*** Fuad E. Doany, Daniel M. Kuchta, Alexander V. Rylyakov, Christian W. Baks, Frank Libsch, and Clint L. Schow – IBM Corporation
3. 8:50 a.m. – ***Effects of Reliability Testing Methods on Microstructure and Strength at the Cu Wire-Al Pad Interface*** P. Su – Cisco Systems, Inc.; H. Seki, C. Ping, and S. Itoh – Sumitomo Bakelite; L. Huang, N. Liao, B. Liu, C. Chen, W. Tai, and A. Tseng – Advanced Semiconductor Engineering Group	3. 8:50 a.m. – ***High Frequency Scanning Acoustic Microscopy Applied to 3D Integrated Process: Void Detection in Through Silicon Vias*** A. Phommahaxay, H. Philipsen, Y. Civale, K. Vandermissen, S. Halder, G. Beyer, B. Swinnen, E. Beyne, and A. Miller – IMEC; I. De Wolf – IMEC, KU Leuven; P. Hoffrogge, S. Brand, and P. Czurratis – PVA TePla Analytical Systems GmbH	3. 8:50 a.m. – ***FPC-Based Compact 25-Gb/s Optical Transceiver Module for Optical Interconnect Utilizing Novel High-Speed FPC Connector*** Takatoshi Yagisawa, Takashi Shiraishi, Tadashi Ikeuchi, and Kazuhiro Tanaka – Fujitsu Laboratories Ltd.
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)		
4. 10:00 a.m. – ***Use of RF-Based Technique as a Metrology Tool for TSV Reliability Analysis*** Chukwudi Okoro, Pavel Kabos, Jan Obrzut, and Yaw S. Obeng – NIST; Klaus Hummler – SEMATECH	4. 10:00 a.m. – ***Self-Alignment Structures for Heterogeneous 3D Integration*** Hyung Suk Yang, Chaoqi Zhang, and Muhannad Bakir – Georgia Institute of Technology	4. 10:00 a.m. – ***Optical Packaging of Silicon Photonic Devices for External Connection of Parallel Optical Signals*** Yoichi Taira and Hidetoshi Numata – IBM Corporation
5. 10:25 a.m. – ***On the Use of High Precision Electrical Resistance Measurement for Analyzing the Damage Development During Accelerated Test of Pb-Free Solder Interconnects*** J. Zhang, S. van der Zwaag, and H.W. Zeijl – Delft University of Technology; G.Q. Zhang – Delft University of Technology, Philips Lighting	5. 10:25 a.m. – ***Optimization of Wire-Rod Electrostatic Fluid Accelerators*** Tsrong-Yi Wen, Tsan-Ting Shen, Hsiu-Che Wang, and Alexander Mamishev – University of Washington	5. 10:25 a.m. – ***Modeling, Design, and Fabrication of Ultra-High Bandwidth 3D Glass Photonics (3DGP) in Glass Interposers*** Bruce C. Chou, Vijay Sukumaran, Venky Sundaram, Gee-Kung Chang, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass Company; Jibin Sun – TE Connectivity
6. 10:50 a.m. – ***Unique Adhesion Testing and MSL Modeling*** Masazumi Amagai and Kentaro Takao – Texas Instruments	6. 10:50 a.m. – ***New Selective Wet Processing*** M. Balucani – Sapienza University of Rome, Rise Technology; D. Ciarniello – Rise Technology; P. Nenzi, R. Crescenzi, and K. Kholostov – Sapienza University of Rome; D. Bernardi – 2BG	6. 10:50 a.m. – ***Assembly Development of 1.3 Tb/s Full Duplex Optical Module*** Yehoshua Benjamin, Kobi Hasharoni, and Michael Mesh – Compass Electro Optical Systems
7. 11:15 a.m. – ***Acoustic Emission Detection of BGA Components in Spherical Bend*** W. Carter Ralph, Gregory L. Daspit, Andrew W. Cain, and Randall S. Jenkins – Southern Research Institute; Elizabeth F. Benedetto, Aileen M. Allen, and Keith Newman – Hewlett Packard	7. 11:15 a.m. – ***Microscrubbing: An Alternative Method for 3D Thermocompression Bonding CuCu Bumps and High Bump Density Devices with Low Force, Time, and Temperature*** Robert Daily, Wang Teng, Giovanni Capuz, and Andy Miller – IMEC	7. 11:15 a.m. – ***Low-Loss Design and Fabrication of Multimode Polymer Optical Waveguide Circuit with Crossings for High-Density Optical PCB*** Takaaki Ishigure, Keishiro Shitanda, and Takuya Kudo – Keio University; Shotaro Takayama, Tetsuya Mori, Kimio Moriya, and Koji Choki – Sumitomo Bakelite Co., Ltd.

Program Sessions: Wednesday, May 29, 1:30 p.m. - 5:10 p.m.

Session 7: Interposers

Committee: **Advanced Packaging**

Mont-Royal 1

Session Co-Chairs:
Subhash L. Shinde – Sandia National Laboratory
Peter Ramm – Fraunhofer EMFT

1. **1:30 p.m. – *Full Integration of a 3D Demonstrator with TSV First Interposer, Ultra Thin Die Stacking, and Wafer Level Packaging***
G. Parès, G. Simon – CEA-LETI; C. Karoui, A. Zaid, F. Dosseul, M. Feron – STMicroelectronics; A. Attard – BESI Austria; G. Klug – DISCO HiTec Europe; H. Luesebrink – PVA TePla AG; K. Martinschitz – EV Group; N. Launay – SPTS; S. Belhenini – LMR

2. **1:55 p.m. – *Fabrication and Testing of Thin Silicon Interposers with Multilevel Frontside and Backside Metallization and Cu-Filled TSVs***
D. Malta, M. Lueck, A. Huffman, C. Gregory, M. Butler, J. Lannon, and D.S. Temple – RTI International

3. **2:20 p.m. – *Interposer Technology for High Bandwidth Interconnect Applications***
Mikael Detalle, A. La Manna, J. De Vos, P. Nolmans, R. Daily, Y. Civale, G. Beyer, and E. Beyne – IMEC

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Chelsea 3 & 4)

4. **3:30 p.m. – *Package Demonstration of the Interposer with Integrated TSVs and Flexible Compliant Interconnects***
Ivan Shubin, Alex Chow, Hiren Thacker, Kannan Raj, Ashok Krishnamoorthy, James Mitchell, and John Cunningham – Oracle; Eugene Chow and Dirk DeBruyker – Palo Alto Research Center (PARC); Koji Fujimoto – Dai Nippon Printing Co., Ltd.

5. **3:55 p.m. – *Electrical and Morphological Characterization for High Integrated Silicon Interposer and Technology Transfer from 200mm to 300mm Wafer***
M. Sunohara, K. Miyairi, K. Mori, M. Higashi, and K. Murayama – Shinko Electric Industries Co., Ltd.; J. Charbonnier, M. Assous, J.P. Bally, T. Mourier, S. Minoret, D. Mercier, A. Toffoli, E. Martinez, H. Feldis, G. Simon, and F. Allain – CEA-LETI

6. **4:20 p.m. – *Demonstration of Low Cost, High Performance, and High Reliability of 2.5D Polycrystalline Silicon Interposer with Fine Pitch Through Vias, Redistribution Layers, and Cu Microbump Interconnections***
Venky Sundaram, Qiao Chen, Tao Wang, Hao Lu, Yuya Suzuki, Raj Pulugurtha, and Rao Tummala – Georgia Institute of Technology

7. **4:45 p.m. – *Development of Through Glass Via (TGV) Formation Technology Using Electrical Discharging for 2.5D/3D Integrated Packaging***
Shintaro Takahashi, Kohei Horiuchi, Kentaro Tatsukoshi, Motoshi Ono, and Nobuhiko Imajo – Asahi Glass Company, Ltd.; Tim Mobely – nMode Solutions, Inc.

Session 8: 3D Reliability and Packaging Challenges

Committee: **Applied Reliability**

Mont-Royal 2

Session Co-Chairs:
Toni Mattila – Aalto University
Jeffrey Suhling – Auburn University

1. **1:30 p.m. – *Thermomechanical and Electrochemical Reliability of Fine-Pitch Through-Package-Copper Vias (TPV) in Thin Glass Interposers and Packages***
Kaya Demir, Koushik Ramachandran, Qiao Chen, Vijay Sukumaran, Raghu Pucha, Venkatesh Sundaram, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass Co., Ltd.

2. **1:55 p.m. – *Impacts of Static and Dynamic Local Bending of Thinned Si Chip on MOSFET Performance in 3-D Stacked LSI***
H. Kino, J.C. Bea, M. Murugesan, K.W. Lee, T. Fukushima, M. Koyanagi, and T. Tanaka – Tohoku University

3. **2:20 p.m. – *Reliability Characterization of Chip-on-Wafer-on-Substrate (CoWoS) 3D IC Integration Technology***
Larry Lin, Tung-Chin Yeh, Jyun-Lin Wu, Gary Lu, Tsung-Fu Tsai, Larry Chen, and An-Tai Xu – Taiwan Semiconductor Manufacturing Company, Ltd.

4. **3:30 p.m. – *Accelerated Reliability Testing and Modeling of Cu-Plated Through Encapsulant Vias (TEVs) for 3D-Integration***
B. Wunderle, Jens Heilmann, and Sridhar Ganesh Kumar – TU Chemnitz; Ole Hoelck – TU Chemnitz, Fraunhofer IZM; Hans Walter, Olaf Wittler, Gunter Engelmann, and M. Jürgen Wolf – Fraunhofer IZM; Gottfried Beer and Klaus Pressel – Infineon Technologies AG

5. **3:55 p.m. – *Reliability Study for Large Silicon Interposers Report on Board***
C. Ferrandon, Y. Lamy, F. De Crecy, and G. Simon – CEA-LETI; S. Joblot, P. Coudrain, P. Bar, D. Yap, R. Coffy, and J.F. Carpentier – STMicroelectronics

6. **4:20 p.m. – *Fracture Mechanics Lifetime Modeling of Low Temperature Si Fusion Bonded Interfaces Used for 3D MEMS Device Integration***
Falk Naumann, Michael Bernasch, and Matthias Petzold – Fraunhofer IWM; Joerg Siegert and Sara Camiello – ams AG

7. **4:45 p.m. – *Extension of Micro-Raman Spectroscopy for Full-Component Stress Characterization of TSV Structures***
Qiu Zhao, J. Im, R. Huang, and P.S. Ho – University of Texas, Austin

Session 9: Advanced Flip Chip Technologies

Committee: **Interconnections**

Nolita 1

Session Co-Chairs:
Lou Nicholls – Amkor Technology, Inc.
William Chen – Advanced Semiconductor Engineering, Inc.

1. **1:30 p.m. – *Challenges of Chip-to-Package Interaction for 22nm Technology with Ultra Low k and Pb-Free Interconnects***
Chris Muzzy, Richard Bisson, John Cincotta, Danielle Degraw, Edward Engbrecht, Jason Gill, Naftali Lustig, Karen McLaughlin, Sylvain Ouimet, Joseph Ross, and David Turnbull – IBM Corporation

2. **1:55 p.m. – *Ultra-Thin and Ultra-High I/O Density Package-on-Package (3D Thin PoP) for High Bandwidth of Smart Systems***
Sung Jin Kim, Chinmay Honrao, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

3. **2:20 p.m. – *A PoP Structure to Support I/O over 1000***
Dyi-Chung Hu, Chun-Ting Lin, and Ying-Chih Chan – Unimicron Technology Corporation

4. **3:30 p.m. – *Investigation of Novel Solder Patterns for Power Delivery and Heat Removal Support***
Thomas Brunschwiler, Timo Tick, Gerd Schlottig, and Stefano Oggioni – IBM Corporation; Yassir Madhour – IBM Corporation, Swiss Institute of Technology

5. **3:55 p.m. – *Modified Thermosonic Flip-Chip Bonding Based on Electroplated Cu Microbumps and Concave Pads for High-Precision Low-Temperature Assembly Applications***
Thanh-Tung Bui, Motohiro Suzuki, Fumiki Kato, Naoya Watanabe, Shunsuke Nemoto, Katsuya Kikuchi, and Masahiro Aoyagi – National Institute of AIST

6. **4:20 p.m. – *10um Ag Flip-Chip by Solid-State Bonding at 250°C***
Wen P. Lin and Chin C. Lee – University of California, Irvine

7. **4:45 p.m. – *Transient Liquid Phase Sintered Attach for Power Electronics***
Hannes Greve and F. Patrick McCluskey – University of Maryland; Liang-Yu Chen – Ohio Aerospace Institute; Ian Fox – Aero Engine Controls

Program Sessions: Wednesday, May 29, 1:30 p.m. - 5:10 p.m.

Session 10: Advancements in Manufacturing Technology	Session 11: Biomedical Electronics	Session 12: High Brightness LEDs and Material
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committee:** **Optoelectronics**
Nolita 2	**Nolita 3**	**Yaletown 4**
Session Co-Chairs: **Shawn Shi – Medtronic Corporation** **Sharad Bhatt – Shanta Systems, Inc.**	**Session Co-Chairs:** **C. S. Premachandran – GLOBALFOUNDRIES** **Karlheinz Bock – Fraunhofer EMFT**	**Session Co-Chairs:** **Henning Schroeder – Fraunhofer IZM** **Stefan Weiss – Oclaro Switzerland GmbH**
1. ***1:30 p.m. – Strip Warpage Analysis of a Flip Chip Package Considering the Mold Compound Processing Parameters*** Eric Ouyang and MyoungSu Chae – STATS ChipPAC, Ltd.	1. ***1:30 p.m. – Smart Flexible Planar Electrodes for Electrochemotherapy and Biosensing*** Paolo Nenzi, Agnese Denzi, Konstantin Kholostov, Rocco Crescenzi, Francesca Apollonio, Micaela Liberti, Paolo Marracino, Ruggero Cadossi, and Marco Balucani – University of Rome; Alessia Ongaro – University of Ferrara	1. ***1:30 p.m. – Very High Power Density LED Modules on Aluminum Substrates with Embedded Water Cooling*** Marc Schneider, Benjamin Leyrer, Christian Herbold, and Stefan Maikowske – Karlsruhe Institute of Technology
2. ***1:55 p.m. – Thermoplastic Based System-in-Package for RFID Application*** Christine Kallmayer, Barbara Pahl, and Arian Grams – Fraunhofer IZM; Joao Marques and Klaus-Dieter Lang – TU Berlin; Thomas Suwald – NXP Semiconductors	2. ***1:55 p.m. – Flexible, Transparent Electronics for Biomedical Applications*** Michael Klopfer, G.P. Li, and Mark Bachman – University of California, Irvine; Chris Cordonier, Koutoku Inoue, and Hideo Honma – Kanto Gakuin University	2. ***1:55 p.m. – LED Matrix Light Source for Adaptive Driving Beam Applications*** Gordon Elger, Benno Spinger, Nico Bienen, and Nils Benter – Philips Technology GmbH
3. ***2:20 p.m. – 3D Printing of Structures with Embedded Circuit Boards Using Novel Holographic Optics*** Shuai Hou and John Tyrer – Loughborough University	3. ***2:20 p.m. – Epidermal Electronics for Seamless Monitoring of Biopotential Signals*** Mitul Dalal, Conor Rafferty, Yung-Yu Hsu, Henry Wei, Kevin Dowling, Briana Morey, Greg Levesque, Gil Huppert, Brian Elolampi, and Dan Davis – mc10, Inc.	3. ***2:20 p.m. – Substrate Reflectivity Study for High Brightness LED Package*** Chieh-Lung Lai, Song-Chun Wu, Jui-Feng Lai, and Hsien-Wen Chen – Siliconware Precision Industries Co., Ltd.
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Chelsea 3 & 4)		
4. ***3:30 p.m. – Low Temperature Fine Pitch Flex-on-Flex (FOF) Assembly Using Nanofiber Sn58Bi Solder Anisotropic Conductive Films (ACFs) and Ultrasonic Bonding Method*** Tae Wan Kim, Kyoung-Lim Suk, and Kyung-Wook Paik – KAIST	4. ***3:30 p.m. – Sensor Integrated Microfluidics for Compact Micro-Reactors*** Erik Jung, Martin Blechert, Victoria Schuldt, and Moritz Hubl – Fraunhofer IZM; Leopold Georg and Klaus-Dieter Lang – TU Berlin	4. ***3:30 p.m. – Evaluation of Directed Self-Assembly Process for LED Assembly on Flexible Substrates*** Anton Tkachenko, Robert F. Karlicek, Jr., and James J.Q. Lu – Rensselaer Polytechnic Institute
5. ***3:55 p.m. – Effective Voiding Control of QFN Via Solder Mask Patterning*** Derrick Herron, Yan Liu, and Ning-Cheng Lee – Indium Corporation	5. ***3:55 p.m. – 3-Axis MEMS Accelerometer-Based Implantable Heart Monitoring System with Novel Fixation Method*** Fjodors Tjulkins, Anh Tuan Thai Nguyen, Nils Hoivik, Knut E. Aasmundtveit, Erik Andreassen, Lars Hoff, and Kristin Imenes – Vestfold University College	5. ***3:55 p.m. – High Refractive Index and Transparency Nanocomposites as Encapsulant for High Brightness LED Packaging*** Yan Liu, Ziyin Lin, Xueying Zhao, and Kyoung-Sik Moon – Georgia Institute of Technology; Sehoon Yoo – Korea Institute of Industrial Technology; J. Choi – El Lighting Co.; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
6. ***4:20 p.m. – Warpage Analysis and Improvement for a Power Module*** Yong Liu, Yumin Liu, Zhongfa Yuan, Tyler Chen, Keunhyuk Lee, and Suresh Belani – Fairchild Semiconductor Corporation	6. ***4:20 p.m. – 3D IPAC – A New Passives and Actives Concept for Ultra-Miniaturized Electronic and Bioelectronic Functional Modules*** P. Markondeya Raj, Uei-Ming Jow, K.P. Murali, Himani Sharma, Dibyajat Mishra, Saumya Gandhi, Maysam Ghovanloo, and Rao Tummala – Georgia Institute of Technology; Jinxiang Dai and T. Danny Xiao – Inframat Corporation	6. ***4:20 p.m. – Realization of High-Quality Light Output Based on a Novel LED Packaging*** Shuiming Li, Fei Chen, Yi Sun, Bin Cao, and Sheng Liu – Huazhong University of Science & Technology; Kai Wang – Guangdong Real Faith Opto-Electronic Co., Ltd.
7. ***4:45 p.m. – Solder Joint Properties of Sn-Ag-Cu Solders on Environmental-Friendly Plasma Surface Finish*** Sang-Hyun Kwon, Kyoung-Ho Kim, Won-Il Seo, Chang-Woo Lee, and Sehoon Yoo – Korea Institute of Industrial Technology (KITECH); Nam-Sun Park – Jesagi Hankook Ltd.; Young-Bae Park – Andong National University	7. ***4:45 p.m. – Anti-Counterfeit, Miniaturized, and Advanced Electronic Substrates for Medical Device Applications*** Rabindra N. Das, Frank D. Egitto, and How Lin – Endicott Interconnect Technologies, Inc.	7. ***4:45 p.m. – Quasi-Conformal Phosphor Dispensing on LED for White Light Illumination*** S.W. Ricky Lee, Xungao Guo, Daoyuan Niu, and Jeffery C.C. Lo – Hong Kong University of Science & Technology

Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

Session 13: 3D Processing and Technology

Committee: Advanced Packaging

Mont-Royal 1

Session Co-Chairs:
Christopher Bower – Semprius, Inc.
Erik Jung – Fraunhofer IZM

1. *8:00 a.m.* – ***TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments***
D. Henry, A. Berthelot, R. Cuchet, and C. Chantre – CEA-LETI; J. Alozy and M. Campbell – CERN

2. *8:25 a.m.* – ***Dielectric Stack Engineering for Via-Reveal Passivation***
Kath Crook, Mark Carruthers, Daniel Archard, Steve Burgess, and Keith Buchanan – SPTS Technologies

3. *8:50 a.m.* – ***Low-Cost Micrometer-Scale Silicon Vias (SVs) Fabrication by Metal-Assisted Chemical Etching (MaCE) and Carbon Nanotubes (CNTs) Filling***
Liyi Li, Yagang Yao, Ziyin Lin, and Yan Liu – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)

4. *10:00 a.m.* – ***Impact of Post-Plating Anneal and Through-Silicon Via Dimensions on Cu Pumping***
Joke De Messemaeker, Olalla Varela Pedreira, Bart Vandevelde, Harold Philipsen, Ingrid De Wolf, Eric Beyne, and Kristof Croes – IMEC

5. *10:25 a.m.* – ***A Quick-Turn 3D Structured ASIC Platform for Cost-Sensitive Applications***
John Teifel, Richard S. Flores, Robert Jarecki, Todd Bauer, and Subhash L. Shinde – Sandia National Laboratories

6. *10:50 a.m.* – ***TSV-Based Quartz Crystal Resonator Using 3D Integration and Si Packaging Technologies***
Jian-Yu Shih, Cheng-Hao Chiang, Yu- Chen Hu, and Kuan-Neng Chen – National Chiao Tung University; Yen-Chi Chen, Chih-Hung Chiu, Chung-Lun Lo, and Chi-Chung Chang – TXC Corporation

7. *11:15 a.m.* – ***Total Cost Effective Scallop Free Si Etching for 2.5D & 3D TSV Fabrication Technologies in 300mm Wafer***
Yasuhiro Morikawa, Takahide Murayama, Yuu Nakamuta, Toshiyuki Sakuishi, Akiyoshi Suzuki, and Koukou Suu – ULVAC, Inc.

Session 14: 3D TSV Interconnects Reliability

Committees: Interconnections / Applied Reliability

Mont-Royal 2

Session Co-Chairs:
Akitsu Shigetou – National Institute for Materials Science
Scott Savage – Medtronic Microelectronics Center

1. *8:00 a.m.* – ***Model for Prediction of Package-on-Package Warpage and the Effect of Process and Material Parameters***
Pradeep Lall, Kewal Patel, and Vikalp Narayan – Auburn University

2. *8:25 a.m.* – ***Design for Reliability of Multi-Layer Thin Film Stretchable Interconnects***
Yung-Yu Hsu, Kylie Lucas, Dan Davis, Rooz Ghaffari, Brian Elolampi, Mitul Dalal, John Work, Stephen Lee, Conor Rafferty, and Kevin Dowling – mc10, Inc.

3. *8:50 a.m.* – ***A More Practical Method of Predicting Flip Chip Solder Bump Electromigration Reliability***
Shiguo (Richard) Rao – Vitesse Semiconductor Corporation

4. *10:00 a.m.* – ***Improvement of the Reliability of TSV Interconnections by Controlling the Crystallinity of Electroplated Copper Thin Films***
Ryosuke Furuya, Chuanhong Fan, Osamu Asai, Ken Suzuki, and Hideo Miura – Tohoku University

5. *10:25 a.m.* – ***Characterization of Plasticity and Stresses in TSV Structures in Stacked Dies using Synchrotron X-Ray Microdiffraction***
T. Jiang, C.L. Wu, J. Im, P.S. Ho, and R. Huang – University of Texas, Austin; P. Su, X. Liu, P. Chia, and L. Li – Cisco Systems, Inc.; H.Y Son, J.S Oh, K.Y. Byun, and N.S. Kim – SK Hynix Inc.

6. *10:50 a.m.* – ***X-Ray Micro-Beam Diffraction Determination of Full-Stress Tensors in Cu TSVs***
Chukwudi Okoro, Lyle E. Levine, Oleg Kirillov, and Yaw S. Obeng – NIST; Ruqing Xu, Jonathan Z. Tischler, and Wenjun Liu – Argonne National Laboratory; Klaus Hummler – SEMATECH

7. *11:15 a.m.* – ***Effect of Metal Finishing Fabricated by Electro and Electroless Plating Process on Reliability Performance of 30um-Pitch Solder Micro Bump Interconnection***
J.Y. Juang, S.Y. Huang, C.J. Zhan, Y.M. Lin, Y.W. Huang, C.W. Fan, S.C. Chung, S.M. Chen, J.S. Peng, Y.L. Lu, P.C. Chang, J.H. Lau, and M.L. Wu – Industrial Technology Research Institute (ITRI)

Session 15: Enabling Technologies for Flip Chip Assembly

Committee: Assembly & Manufacturing Technology

Nolita 1

Session Co-Chairs:
Valerie Oberson – IBM Corporation
Tom Poulin – Aerie Engineering

1. *8:00 a.m.* – ***Low-k ILD Reliability through Chip-Package Assembly: Engineering Appropriate Stress Tests and Process Certification Criteria***
Sudarshan Rangaraj, Jeffrey Hicks, Michael O'Day, Ankur Aggarwal, Terri Wilson, Ramanarayanan Panchapakesan, Rohit Grover, and Guotao Wang – Intel Corporation

2. *8:25 a.m.* – ***Flip Chip Assembly Method Employing Differential Heating/Cooling for Large Dies with Coreless Substrates***
Katsuyuki Sakuma, Edmund Blackshear, Krishna Tunga, Chenzhou Lian, Shidong Li, Marcus Interrante, Oswald Mantilla, and Jae-Woong Nah – IBM Corporation

3. *8:50 a.m.* – ***3D Integration of CMOS Image Sensor with Co-Processor Using TSV Last and Micro-Bumps Technologies***
P. Coudrain, N. Chevrier, A. Farcy, O. Le-Briz – STMicroelectronics; D. Henry, A. Berthelot, J. Charbonnier, S. Verrun, R. Franiatte, N. Bouzaida, G. Cibrario – CEA-LETI; F. Calmon, I. O'Connor – INL; T. Lacrevaz, B. Flechet, L. Fourneaud – Univ. de Savoie

4. *10:00 a.m.* – ***Methodology to Evaluate Pre-Applied Underfill Materials with Concurrent Flux Capability for Ultra-Fine Pitch Solder-Based Interconnects***
Sunoo Kim, Seth Kruger, Brian Sapp, and Sitaram Arkalgud – SEMATECH; Ho Hyung Lee and Seungbae Park – SUNY Binghamton

5. *10:25 a.m.* – ***No Clean Flux Technology for Large Die Flip Chip Packages***
Akihiro Horibe, Kang-Wook Lee, Keishi Okamoto, Hiroyuki Mori, and Yasumitsu Orii – IBM Corporation; Yuki Nishizako, Osamu Suzuki, and Yukio Shirai – NAMICS Corporation

6. *10:50 a.m.* – ***Ultra Large System-in-Package (SiP) Module and Novel Packaging Solution for Networking Applications***
Mudasir Ahmad, Mohan Nagar, and Weidong Xie – Cisco Systems, Inc.; Miguel Jimarez and ChangGyun Ryu – Amkor Technology, Inc.

7. *11:15 a.m.* – ***Low-Cost E-Band Flip-Chip Assembly and Materials***
Katarina Boustedt and Per Ligander – Ericsson AB

Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

Session 16: Interconnect Reliability

Committee: Applied Reliability

Nolita 2

Session Co-Chairs:
Vikas Gupta – Texas Instruments
Tz-Cheng Chiu – National Cheng Kung University

1. **8:00 a.m. – *Electromigration of Solder Balls for Wafer-Level Packaging with Different Under Bump Metallurgy and Redistribution Layer Thickness***
Christine Hau-Riege, Beth Keser, You-Wen Yau, and Steve Bezuk – Qualcomm Technologies, Inc.

2. **8:25 a.m. – *Electromigration Reliability and Current Carrying Capacity of Various WLCSP Interconnect Structures***
Ahmer Syed, Karthikeyan Dhandapani, Christopher Berry, Robert Moody, and Riki Whiting – Amkor Technology, Inc.

3. **8:50 a.m. – *Reliability Modeling and Testing of Advanced QFN Packages***
Li Li – Cisco Systems, Inc.

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)

4. **10:00 a.m. – *An Improved Model for Predicting Fatigue-Crack Propagation Behaviors in Multiple Solder Bumps on a BGA Package***
Takeshi Terasaki, Hisashi Tanie, Tetsuya Nakatsuka, Satoshi Kurauchi, Tadayuki Yamashita, and Yuichi Furusawa – Hitachi; Hironori Imai – SCSK Corporation

5. **10:25 a.m. – *Grain Structure Evolution and Its Impact on the Fatigue Reliability of Lead-Free Solder Joints in BGA Packaging Assembly***
Huili Xu and Choong-Un Kim – University of Texas, Arlington; Tae-Kyu Lee – Cisco Systems, Inc.

6. **10:50 a.m. – *Failure Analysis of Thermally and Mechanically Stressed Plastic Core Solder Balls***
M.M.V. Taklo, J. Seland Graff, and D. Nilsen Wright – SINTEF; H. Kristiansen – Conpart AS; L. Hoff – Vestfold University College; K. Waaler – WesternGeco AS

7. **11:15 a.m. – *An Eco-Friendly Cu-Zn Wetting Layer for Highly Reliable Solder Joints***
Young-Ho Kim, Sun-Chul Kim, and Young Min Kim – Hanyang University

Session 17: Adhesives and Underfill Materials

Committee: Materials & Processing

Nolita 3

Session Co-Chairs:
Stephanie Potisek – Dow Chemical
Dwayne Shirley – Qualcomm Technologies, Inc.

1. **8:00 a.m. – *Innovative Wafer-Level Encapsulation & Underfill Material for Silicon Interposer Application***
C. Ferrandon, A. Jouve, Y. Lamy, A. Schreiner, P. Montmeat, M. Pellat, M. Argoud, F. Fournel, G. Simon, and S. Cheramy – CEA-LETI; S. Joblot – STMicroelectronics

2. **8:25 a.m. – *Wafer Level Underfill Entrapment in Solder Joint During Thermocompression: Simulation and Experimental Validation***
A. Taluy – STMicroelectronics, University of Grenoble; A. Jouve, R. Franiatte, S. Chéramy, and N. Sillon – CEA-LETI; S. Joblot, J. Bertheau, A. Farcy, and P. Ancey – STMicroelectronics; A. Sylvestre – University of Grenoble

3. **8:50 a.m. – *Novel Surface Modification of Nanosilica for Low Stress Underfill***
Ziyin Lin, Yan Liu, and Kyoung-Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)

4. **10:00 a.m. – *The Optimization of the Composition of Non-Conductive Film and the Lamination to Wafer***
Satomi Kawamoto, Atsushi Saito, Yoshihide Fukuhara, Hiromi Sone, and Masaaki Hoshiyama – NAMICS Corporation

5. **10:25 a.m. – *Development of Highly Reliable Flip-Chip Bonding Technology Using Non-Conductive Adhesives (NCAs) for 20 µm Pitch Application***
Sun-Chul Kim, Myung-Hwan Hong, Ji-Hyun Lee, and Young-Ho Kim – Hanyang University

6. **10:50 a.m. – *High Thermal Conductive Adhesive Film for Cu and Al Plate Adhesion in Power Electronics Package***
Toshihisa Nonaka, Akira Shimada, Koichi Aoki, and Noburo Asahi – Toray Industries, Inc.

7. **11:15 a.m. – *The Effect of Coating Thickness on the Electrical Performance of Novel Isotropic Conductive Adhesives Prepared Using Metallised Polymer Micro-Spheres***
S. Jain, D.C. Whalley, M. Cottrill, and C. Liu – Loughborough University; T. Helland – MosaicSolutions AS; H. Kristiansen and K. Redford – Conpart AS

Session 18: Thermal and Mechanical Modeling & Simulation

Committee: Modeling & Simulation

Yaletown 4

Session Co-Chairs:
Erdogan Madenci – University of Arizona
Xuejun Fan – Lamar University

1. **8:00 a.m. – *Modeling and Experimental Study of Thin Bond Line Thermal Interface Material Failure***
Shidong Li, Tuhin Sinha, Taryn J. Davis, Kamal Sikka, and Paul Bodenweber – IBM Corporation

2. **8:25 a.m. – *3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages***
Siow Ling Ho – Institute of Microelectronics, A*STAR; Andrew A.O. Tay – National University of Singapore

3. **8:50 a.m. – *Effective Package-On-Package Warpage DOE Design with Analytical Method***
Shengmin Wen and Wei Lin – Amkor Technology

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)

4. **10:00 a.m. – *Damage Pre-Cursor Based Assessment of Impact of High Temperature Storage on Reliability of Leadfree Electronics***
Pradeep Lall, Kazi Mirza, Mahendra Harsha, and Jeff Suhling – Auburn University; Kai Goebel – NASA Ames Research Center

5. **10:25 a.m. – *A Preliminary Solder Joint Life Prediction Model by Experiment and Simulation for Translation of Use Condition to Temperature Cycling Test Condition***
Ru Han, Min Pei, Alan Lucero, Daeil Kwon, Yun Ge, Richard Harries, Pardeep Bhatti, and Tieyu Zheng – Intel Corporation

6. **10:50 a.m. – *Use of Compliant Interconnects for Drop Impact Isolation***
Wei Chen, Anirudh Bhat, and Suresh K. Sitaraman – Georgia Institute of Technology

7. **11:15 a.m. – *Prediction of Board-Level Performance of WLCSP***
Yumin Liu and Yong Liu – Fairchild Semiconductor Corporation

Program Sessions: Thursday, May 30, 1:30 p.m. - 5:10 p.m.

Session 19: Interposer Characterization	Session 20: Challenges in 3D Integration	Session 21: Advanced Substrate and Flip Chip Packaging
Committee: **Interconnections**	**Committee:** **Assembly & Manufacturing Technology**	**Committee:** **Advanced Packaging**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Matthew Yao – Rockwell Collins** **Katsuyuki Sakuma – IBM Corporation**	**Session Co-Chairs:** **Andy Tseng – Advanced Semiconductor Engineering, Inc.** **Wei Koh – Pacrim Technology**	**Session Co-Chairs:** **Young-Gon Kim – IDT** **Raj N. Master – Microsoft Corporation**
1. ***1:30 p.m. – High Speed Signaling Performance of Multilevel Wiring on Glass Substrates for 2.5D Integrated Circuit and Optoelectronic Integration*** Xiaoxiong Gu, Renato Rimolo-Donadio, Russell Budd, Christian Baks, Lavanya Turlapati, Christopher Jahnes, Daniel M. Kuchta, Clint L. Schow, and Frank Libsch – IBM Corporation	1. ***1:30 p.m. – Flux-Assisted Self-Assembly with Microbump Bonding for 3D Heterogeneous Integration*** Yuka Ito – Tohoku University, Sumitomo Bakelite Co., Ltd.; Takafumi Fukushima, Kang-Wook Lee, Tetsu Tanaka, and Mitsumasa Koyanagi – Tohoku University; Koji Choki – Sumitomo Bakelite Co., Ltd.	1. ***1:30 p.m. – Nano-Silica Composite Laminate*** Katsura Hayashi, Tadashi Nagasawa, Keisaku Matsumoto, and Shinya Kawai – Kyocera Corporation
2. ***1:55 p.m. – Unified Methodology for Heterogeneous Integration with CoWoS Technology*** Yi-Lin Chuang, Chung-Sheng Yuan, Ji-Jan Chen, Ching-Fang Chen, Ching-Shun Yang, Wei-Pin Changchien, Charles C.C. Liu, and Frank Lee – Taiwan Semiconductor Manufacturing Company	2. ***1:55 p.m. – Micro-Bump Bondability Design Rules for High Throughput 2.5D/3D ICs Assembly*** Chang-Lin Yeh, Yung-Yi Yeh, Jien-Cheng Chen, Jen-Chieh Kao, Chang-Chi Lee, and Ho-Ming Tong – Advanced Semiconductor Engineering, Inc.	2. ***1:55 p.m. – Copper-Filled Anodic Aluminum Oxide: A Potential Substrate Material for a High-Density Interconnection*** Michio Horiuchi, Yuuichi Matsuda, Yasue Tokutake, Ryo Fukasawa, and Tsuyoshi Kobayashi – Shinko Electric Industries
3. ***2:20 p.m. – Power Comparison of 2D, 3D, and 2.5D Interconnect Solutions and Power Optimization of Interposer Interconnects*** M. Ataul Karim and Paul D. Franzon – North Carolina State University; Anil Kumar – GLOBALFOUNDRIES	3. ***2:20 p.m. – Assembly Process Qualification and Reliability Evaluations for Heterogeneous 2.5D FPGA with HiCTE Ceramic*** Ganesh Hariharan, Raghunandan Chaware, Laurene Yip, Inderjit Singh, Kenny Ng, S.Y. Pai, Myongseob Kim, Henley Liu, and Suresh Ramalingam – Xilinx, Inc.	3. ***2:20 p.m. – Development of a Low CTE Chip Scale Package*** Tomoyuki Yamada, Masahiro Fukui, Kenji Terada, and Masaaki Harazono – Kyocera SLC Technologies Corporation; Charles Reynolds, Jean Audet, Sushumna Iruvanti, Hsichang Liu, Scott Moore, Yi Pan, and Hongqing Zhang – IBM Corporation
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Chelsea 3 & 4)		
4. ***3:30 p.m. – Large Silicon, Glass and Low CTE Organic Interposers to Printed Wiring Board SMT Interconnections Using Copper Microwire Arrays*** Xian Qin, Sebastian Gottschall, Nitesh Kumbhat, P. Markondeya Raj, Sungjin Kim, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology	4. ***3:30 p.m. – Thermally Enhanced Pre-Applied Underfills for 3D Integration*** Akihiro Horibe, Keishi Okamoto, Hiroyuki Mori, and Yasumitsu Orii – IBM Corporation; Kohichiro Kawate, Yorinobu Takamatsu, and Hiroko Akiyama – Sumitomo 3M, Ltd.	4. ***3:30 p.m. – Thermally Enhanced and Thin Profile Flip Chip Packages for Tablet Processor Applications*** Hamid Eslampour, Mukul Joshi, KyungOe Kim, Sun Wei, JaeHan Chung, TaeWoo Lee, HangChul Choi, and Roger Emigh – STATS ChipPAC, Ltd.
5. ***3:55 p.m. – Towards Alternative Technologies for Fine Pitch Interconnects*** J.P. Colonna, R. Segaud, F. Marion, M. Volpert, A. Garnier, L. Di Cioccio, F. De Crécy, C. Laviron, and S. Chéramy – CEA-LETI; Y. Beillard and S. Mermoz – CEA-LETI, STMicroelectronics	5. ***3:55 p.m. – Integration Challenges of TSV Backside Via Reveal Process*** Bo Kai Huang, Chien Ming Lin, Shin Jiang Huang, Ching Wen Chiang, Pin Cheng Huang, Guang Xin Chen, Chun Chieh Chao, and Chun Hung Lu – Siliconware Precision Industries Co., Ltd.	5. ***3:55 p.m. – Development of Chip-on-Chip with Face-to-Face Technology as a Low Cost Alternative for 3D Packaging*** J. Sutanto, D.H. Kang, S.Y. Ma, J.H. Yoon, K.S. Oh, M. Oh, K.R. Park, R. Lanzone, and R. Huemoeller – Amkor Technology, Inc.
6. ***4:20 p.m. – Warpage Control of Silicon Interposer for 2.5D Package Application*** K. Murayama, M. Aizawa, K. Hara, M. Sunohara, K. Miyairi, K. Mori, and M. Higashi – Shinko Electric Industries Co., Ltd.; J. Charbonnier, M. Assous, J.P. Bally, and G. Simon – CEA-LETI	6. ***4:20 p.m. – Yield and Reliability in 3D Interconnect and WLP - Ultra Thin Chip Stacking*** Helge Luesebrink – PVA TePla AG, BU Plasma Systems; Alastair Attard and Fabian Schnegg – Datacon Technology GmbH; Gabriel Pares – CEA-LETI	6. ***4:20 p.m. – Mechanical and Board Level Reliability Considerations of Lidless Flip Chip BGA Packaging*** Shin Low, Inderjit Singh, Ganesh Hariharan, Laurene Yip, and Nael Zohni – Xilinx, Inc.; Mulugeta Abtew, Gowri Shankar Solaiappan, Vineeth Vair, and Shane Lewis – Sanmina-SCI Corp.
7. ***4:45 p.m. – Development and Characterization of a Through-Multilayer TSV Integrated SRAM Module*** Yunhui Zhu, Xin Sun, Runiu Fang, Xiao Zhong, Yuan Bian, Meng Chen, Jing Chen, Wengao Lu, and Yufeng Jin – Peking Univ.; Shenglin Ma – Xiamen Univ., Peking Univ.; Min Miao – Peking Univ., Beijing Information Science and Technology Univ.	7. ***4:45 p.m. – Package-on-Package with Very Fine Pitch Interconnects for High Bandwidth*** Ilyas Mohammed, Reynaldo Co, and Rajesh Katkar – Invensas Corporation	7. ***4:45 p.m. – Mechanical Properties of Sn-Bi Bumps on Flexible Substrate*** Min-Su Kim – University of Science & Technology, Korea Institute of Industrial Technology (KITECH); Yong-Ho Ko – Korea Institute of Industrial Technology (KITECH), KAIST; Sehoon Yoo and Chang-Woo Lee – Korea Institute of Industrial Technology (KITECH)

Program Sessions: Thursday, May 30, 1:30 p.m. - 5:10 p.m.

Session 22: Solder and Material Characterization

Committee: Applied Reliability

Nolita 2

Session Co-Chairs:
Dongming He – Qualcomm Technologies, Inc.
Donna M. Noctor – Siemens Industry, Inc.

1. *1:30 p.m.* – ***Reliability and Failure Mechanism of Solder Joints in Thermal Cycling Tests***
Babak Arfaei – Universal Instruments Corporation, SUNY Binghamton; Sam Mahin-Shirazi, Shantanu Joshi, Peter Borgesen, and Eric Cotts – SUNY Binghamton; Martin Anselm – Universal Instruments Corporation; James Wilcox – IBM Corporation; Richard Coyle – Alcatel-Lucent

2. *1:55 p.m.* – ***Correlation of Reliability Models Including Aging Effects with Thermal Cycling Reliability Data***
Jeffrey C. Suhling, Mohammad Motalab, Muhannad Mustafa, Jiawei Zhang, John L. Evans, Michael J. Bozack, and Pradeep Lall – Auburn University

3. *2:20 p.m.* – ***Comparison of IMC Growth in Flip-Chip Assemblies with 100- and 200-µm-Pitch SAC305 Solder Joints***
Ye Tian – Huazhong University of Science and Technology, Georgia Institute of Technology; Xi Liu, Justin Chow, and Suresh K. Sitaraman – Georgia Institute of Technology; Yi Ping Wu – Huazhong University of Science and Technology

4. *3:30 p.m.* – ***Reliability and Shear Strength of 42Sn-57Bi-1Ag (Wt.%) Lead-Free Solder Joints after Thermal Aging and Salt Spray Testing***
M. Mostofizadeh, J. Pippola, and L. Frisk – Tampere University of Technology

5. *3:55 p.m.* – ***Plastic Deformation Effect on Sn Whisker Growth in Electroplated Sn and Sn-Ag Solders***
Sung K. Kang – IBM Corporation; Jaewon Chang and Hyuck-Mo Lee – KAIST; Jaeho Lee – Hongik University; Keun-Soo Kim – Hoseo University

6. *4:20 p.m.* – ***Effect of NCFs with Zn-Nanoparticles on the Interfacial Reactions of 40 um Pitch Cu Pillar/Sn-Ag Bump for TSV Interconnection***
Ji-Won Shin, Yong-Won Choi, Young Soon Kim, and Kyung-Wook Paik – KAIST; Un Byung Kang and Young Kun Jee – Samsung Electronics Company, Ltd.

7. *4:45 p.m.* – ***Advanced In Situ Characterization of TIM1 Reliability***
Peng Li, Yongmei Liu, Alfred La Mar, and Deepak Goyal – Intel Corporation

Session 23: Novel Technologies

Committee: Materials & Processing

Nolita 3

Session Co-Chairs:
Yoichi Taira – IBM Japan
Choong Kooi Chee – Intel Corporation

1. *1:30 p.m.* – ***Reduced Graphene Oxide Based Schottky Diode on Flex Substrate for Microwave Circuit Applications***
Amanpreet Kaur, Xianbo Yang, Kyoung Youl Park, and Premjeet Chahal – Michigan State University

2. *1:55 p.m.* – ***Ultra-Thin, Self-Healing Decoupling Capacitors on Thin Glass Interposers Using High Surface Area Electrodes***
Parthasarathi Chakraborti, Himani Sharma, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology

3. *2:20 p.m.* – ***Electrochemical Assembly of SAM on Copper for Epoxy/Copper Adhesion Improvement***
Stephen C.T. Kwok and Matthew M.F. Yuen – Hong Kong University of Science & Technology

4. *3:30 p.m.* – ***Chip-Side-Healing as a Basis for Robust Bare-Chip Assemblies***
Matthias Steiert and Jürgen Wilde – University of Freiburg

5. *3:55 p.m.* – ***Development of Biocompatible Coatings on Flexible Electronics***
Rabindra N. Das, Frank D. Egitto, and Mark Poliks – Endicott Interconnect Technologies, Inc.

6. *4:20 p.m.* – ***Development of Low Temperature Sintered Nano Silver Pastes Using MO Technology and Resin Reinforcing Technology***
Koji Sasaki and Noritsuka Mizumura – NAMICS Corporation

7. *4:45 p.m.* – ***Facile Synthesis of $BaTiO_3$ Nanorods and Their Shape Effects on the Dielectric Constants of Polymer Composites***
Pengli Zhu and Rong Sun – Chinese Academy of Science; C.P. Wong – Chinese University of Hong Kong

Session 24: Power and Signal Integrity

Committee: Modeling & Simulation

Yaletown 4

Session Co-Chairs:
Kemal Aygun – Intel Corporation
Daniel de Araujo – Nimbic, Inc.

1. *1:30 p.m.* – ***Simultaneous Switching Noise Model by Distributed Power Port and Ground Current Capture***
Seunghyun Hwang, Daehyun Chung, Venkat Satagopan, Sunil Sudhakaran, Daniel Lin, and Fathi Moghadam – NVIDIA Corporation

2. *1:55 p.m.* – ***System Level Signal and Power Integrity Analysis for 3200Mbps DDR4 Interface***
June Feng, Bipin Dhavale, Janani Chandrasekhar, Yuri Tretiakov, and Dan Oh – Altera Corporation

3. *2:20 p.m.* – ***Analysis of Power Integrity and Its Jitter Impact in a 4.3Gbps Low-Power Memory Interface***
Hai Lan, Xinhai Jiang, and Jihong Ren – Rambus, Inc.

4. *3:30 p.m.* – ***Unconditionally Stable Explicit Method for the Fast 3D Simulation of On-Chip Power Distribution Network***
Tadatoshi Sekine and Hideki Asai – Shizuoka University

5. *3:55 p.m.* – ***Power Delivery Network Analysis of 3D Double-Side Glass Interposers for High Bandwidth Applications***
Gokul Kumar, Srikrishna Sitaraman, Sung Jin Kim, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Jonghyun Cho and Joungho Kim – KAIST

6. *4:20 p.m.* – ***Fast Voltage Drop Modeling of Power Grid with Application to Silicon Interposer Analysis***
En-Xiao Liu and Er-Ping Li – Institute of High Performance Computing, A*STAR

7. *4:45 p.m.* – ***Power Delivery Modeling for 3D Systems with Non-Uniform TSV Distribution***
Huanyu He and Jian-Qiang Lu – Rensselaer Polytechnic Institute; Zheng Xu and Xiaoxiong Gu – IBM Corporation

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Chelsea 3 & 4)

Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

Session 25: 3D Microbump Structures and Silicon to Silicon Bonding	Session 26: High Speed Interconnects & Power Distribution in 3D Integration	Session 27: Wafer Level and Embedded Packaging
Committee: Interconnections	**Committee:** Electronic Components & RF	**Committee:** Advanced Packaging
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Tom Gregorich – Broadcom Corporation** **Li Li – Cisco Systems, Inc.**	**Session Co-Chairs:** **Rockwell Hsu – Tiva Systems Inc. at Cisco Systems, Inc.** **Amit P. Agrawal – Cisco Systems, Inc.**	**Session Co-Chairs:** **Luu T. Nguyen – Texas Instruments** **Altaf Hasan – Intel Corporation**
1. ***8:00 a.m. – Key Elements for Sub-50µm Pitch Micro Bump Processes*** J. De Vos, L. Bogaerts, T. Buisson, C. Gerets, G. Jamieson, K. Vandersmissen, A. La Manna, and E. Beyne – IMEC	1. ***8:00 a.m. – A DC-Blocking Dielectric Waveguide Via Design for High Speed Signaling at Millimeter Wave Frequencies*** Jose A. Hejase, Nanju Na, Nam Pham, and Lloyd Walls – IBM Corporation	1. ***8:00 a.m. – A Study of Wafer Level Package Board Level Reliability*** Steven Xu, Beth Keser, Christine Hau-Riege, Steve Bezuk, and You-Wen Yau – Qualcomm Technologies, Inc.
2. ***8:25 a.m. – Microstructural and Morphological Characterization of SnAgCu Micro-Bumps for Integration in 3D Interconnects*** J. Bertheau, R. Pantel, P. Coudrain, and N. Hotellier – STMicroelectronics; P. Bleuet and J. Charbonnier – CEA-LETI; F. Hodaj – SIMaP-UMR	2. ***8:25 a.m. – Characterization of Power Delivery Network by Using Optimized Power/Ground Port Termination Impedance*** Seungyong (Brian) Baek and Amit Agrawal – Cisco Systems, Inc.; Jiali Lai – University of California, Davis	2. ***8:25 a.m. – Optimization of Solder Height and Shape to Improve the Thermo-Mechanical Reliability of Wafer-Level Chip Scale Packages*** Su-Chun Yang, Chung-Jung Wu, Da-Yuan Shih, Chih-Hang Tung, Cheng-Chang Wei, Yi-Li Hsiao, Ying-Jui Huang, and Douglas Chen-Hua Yu – Taiwan Semiconductor Manufacturing Company
3. ***8:50 a.m. – Mechanism of Low Temperature Copper-to-Copper Direct Bonding for 3D TSV Package Interconnection*** J. Cho, S. Yu, M.P.C. Roma, S. Maganty, and S. Park – SUNY, Binghamton; E. Bersch, C. Kim, and B. Sapp – SEMATECH	3. ***8:50 a.m. – An Air-Dielectric Via Structure for 20Gbps+ Board Connectors*** Xin Wu and David Dunham – Molex, Inc.; Nanju Na and Jose A. Hejase – IBM Corporation	3. ***8:50 a.m. – Wafer Level Packaging for Ultra Thin (6 µm) High Brightness LEDs using Embedding Technology*** J. Kleff – TU Berlin; M. Töpper, L. Dietrich, and H. Oppermann – Fraunhofer IZM; S. Herrmann – OSRAM Opto Semiconductors GmbH
Refreshment Break: 9:15 a.m. - 10:00 a.m. (Mont-Royal Commons)		
4. ***10:00 a.m. – Room-Temperature High-Density Interconnection Using Ultrasonic Bonding of Cone Bump for Heterogeneous Integration*** Takanori Shuto, Keiichiro Iwanabe, Li Jing Qiu, and Tanemasa Asano – Kyushu University	4. ***10:00 a.m. – Multi-Layer Adaptive Power Management Architecture for TSV 3DIC Applications*** M.H. Chang and W. Hwang – National Chiao Tung Univ., ASE Group; W.C Hsieh, P.C. Wu, C.T. Chuang, and K.N. Chen – National Chiao Tung Univ.; C.C. Wang, C.Y. Ting, K.H. Chen, C.T. Chiu, and H.M. Tong – Advanced Semiconductor Engineering (ASE) Group	4. ***10:00 a.m. – Embedded Capacitors in the Next Generation Processor*** Yongki Min, Reynaldo Olmedo, Michael Hill, Kaladhar Radhakrishnan, Kemal Aygun, Mostafa Kabiri-Badr, Rahul Panat, Sriram Dattaguru, and Haluk Balkan – Intel Corporation
5. ***10:25 a.m. – Low Temperature (<180°C) Wafer-Level and Chip-Level In-to-Cu and Cu-to-Cu Bonding for 3D Integration*** Y.S. Chien, Y.P. Huang, R.N. Tzeng, C.T. Chuang, W. Hwang, J.C. Chiou, and K.N. Chen – National Chiao Tung University; M.S. Shy, T.H. Lin, K.H. Chen, C.T. Chiu, and H.M. Tong – Advanced Semiconductor Engineering (ASE) Group	5. ***10:25 a.m. – Wideband and Scalable Equivalent-Circuit Model for Differential Through Silicon Vias with Measurement Verification*** Kuan-Chung Lu and Tzyy-Sheng Horng – National Sun Yat-Sen University	5. ***10:25 a.m. – 3D Power Module with Embedded WLCSP*** Shichun Qu, Jihwan Kim, Glen Marcus, and Matt Ring – Fairchild Semiconductor
6. ***10:50 a.m. – Hybrid Au-Au Bonding Technology Using Planar Adhesive Structure for 3D Integration*** Masatsugu Nimura, Jun Mizuno, and Shuichi Shoji – Waseda University; Akitsu Shigetou – National Institute for Materials Science (NIMS); Katsuyuki Sakuma – IBM Corporation; Hiroshi Ogino and Tomoyuki Enomoto – Nissan Chemical Industries	6. ***10:50 a.m. – Wideband Ultralow Power Distribution Network Impedance Evaluation of Decoupling Capacitor Embedded Interposers for 3-D Integrated LSI System*** Katsuya Kikuchi and Masahiro Aoyagi – National Institute of AIST; Toshio Gomyo and Toshikazu Ookubo – Association of Super-Advanced Electronic Technologies (ASET); Toshio Sudo – Shibaura Institute of Technology; Kanji Otsuka – Meisei University	6. ***10:50 a.m. – From Wafer to Panel Level Mold Embedding*** T. Braun, K.F. Becker, J. Bauer, and R. Aschenbrenner – Fraunhofer IZM; S. Voges, T. Thomas, R. Kahle, and K.D. Lang – Technical University Berlin
7. ***11:15 a.m. – High Throughput Cu-Cu Bonding by Non-Thermocompression Method*** Chuan Seng Tan and Gang Yih Chong – Nanyang Technological University	7. ***11:15 a.m. – A New Approach to Power Integrity with Thinfilm Capacitors in 3D IPAC Functional Module*** Saumya Gandhi, P. Markondeya Raj, Venky Sundaram, Himani Sharma, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology	7. ***11:15 a.m. – Reliability of Embedding Concepts for Discrete Passive Components in Organic Circuit Boards*** R. Schwerz, B. Boehme, M. Roellig, and N. Meyendorf – Fraunhofer Institute for Non-Destructive Testing (IZFP-D); K.J. Wolter – TU Dresden

Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

Session 28: Drop and Dynamic Mechanical Reliability	Session 29: Substrates	Session 30: Electrical Modeling and Measurements
Committee: Applied Reliability	**Committee:** Materials & Processing	**Committee:** Modeling & Simulation
Nolita 2	**Nolita 3**	**Yaletown 4**
Session Co-Chairs: Darvin R. Edwards – Texas Instruments, Inc.; Lakshmi N. Ramanathan – Microsoft Corporation	**Session Co-Chairs:** Lejun Wang – Qualcomm Technologies, Inc.; Daniel D. Lu – Henkel Corporation	**Session Co-Chairs:** Wendem Beyene – Rambus Inc.; Jaemin Shin – Qualcomm Technologies, Inc.
1. ***8:00 a.m. – Effect of Strain Rate on Adhesion Strength of Anisotropic Conductive Films (ACF) Joints*** J. Meng, P. Stark, and A. Dasgupta – University of Maryland; M. Sillanpaa, Esa Hussa, Jukka P. Seppanen, Jouni A. Raunio, and Ilkka J. Saarinen – Nokia Corporation	1. ***8:00 a.m. – Site-Selective Fabrication of Patterned Transparent Copper Mesh on Flexible Substrates at Mild Temperature for Green, Low Cost Electronics*** Yunxia Jin, Dunying Deng, and Fei Xiao – Fudan University	1. ***8:00 a.m. – System-Level Clock Jitter Modeling for DDR Systems*** Yujeong Shim, Dan Oh, Chuan Thim Khor, Bipin Dhavale, Sunitha Chandra, Daniel Chow, Weichi Ding, Kundan Chand, Aman Aflaki, and Mayra Sarmiento – Altera Corporation
2. ***8:25 a.m. – An Approach to Board-Level Drop Reliability Evaluation with Improved Correlation with Use Conditions*** T.T. Mattila, L. Vajavaara, and J. Hokka – Aalto University; E. Hussa, M. Mäkelä, and V. Halkola – Nokia Corporation	2. ***8:25 a.m. – The New Primer with Copper Foil Corresponding to Semi-Additive Process for Package Substrates*** Hitoshi Onozeki, Tsubasa Inoue, Katsuji Yamagishi, Takahiro Tanabe, Takayuki Suzuki, Kenichi Ikeda, and Nobuyuki Ogawa – Hitachi Chemical Co., Ltd.	2. ***8:25 a.m. – Circuit/Channel Co-Design Methodology for Multimode Signaling*** Zhuo Yan and Paul D. Franzon – North Carolina State University; Kemal Aygün and Henning Braunisch – Intel Corporation
3. ***8:50 a.m. – A New and Effective Drop Test Evolution to Next-Gen Handheld Applications*** Dongji Xie, Min Woo, Zhongming Wu, and Tom McMullen – Nvidia Corporation; Ife Hsu and Ramgopal Uppalapati – Intel Corporation; Yingliang Zhou – Huawei; Andy Zhang – Texas Instruments, Inc.	3. ***8:50 a.m. – Dielectric Composite Material with Good Performance and Processability for Embedding of Active and Passive Components into PCBs*** Ryan Park, Jürgen Kress, and Norbert Galster – Atotech Germany GmbH; Seunghyun Cho – Dongyang Mirae University	3. ***8:50 a.m. – Characterization of a Low-Power, 6.4 Gbps DDR DIMM Memory Interface System*** R. Kollipara, S. Chang, C. Madden, H. Lan, L. Gopalakrishnan, S. Best, Y. Lu, S. Bangalore, G.E. Kumar, P.K. Venkatesan, K. Vyas, K. Kaviani, M. Bucher, L. Luo, and K. Prabhu – Rambus, Inc.
Refreshment Break: 9:15 a.m. - 10:00 a.m. (Mont-Royal Commons)		
4. ***10:00 a.m. – Effect of Aging on High-Strain Rate Mechanical Properties of SAC105 and SAC305 Lead-Free Alloys*** Pradeep Lall, Sandeep Shantaram, and Jeff Suhling – Auburn University; Dave Locker – US AMRDEC	4. ***10:00 a.m. – An Innovative Embedded Interposer Carrier for High Density Interconnection*** Yu-Hua Chen, Tzyy-Jang Tseng, and Dyi-Chung Hu – Unimicron Technology Corporation; Wei-Chung Lo – Industrial Technology Research Institute (ITRI)	4. ***10:00 a.m. – Characterization, Modeling, and Optimization of a 3D Embedded Trench Decoupling Capacitors in Si-RF Interposer*** Hélène Jacquinot – CEA-LETI; David Denis – IPDIA
5. ***10:25 a.m. – Brittle Fracture of Intermetallic Compounds in SAC Solder Joints under High Speed Ball Pull/Pin Pull and Charpy Impact Tests*** Chaoran Yang – Hong Kong Univ. of Science & Technology; Guangsui Xu – HKUST LED-FPD, South China Univ. of Technology; S.W. Ricky Lee – Hong Kong Univ. of Science & Technology, HKUST LED-FPD; Xinping Zhang – South China Univ. of Technology	5. ***10:25 a.m. – A Lead-Frame Pre-Mold Coreless Substrate Development*** Chang-Yi (Albert) Lan, C.S. Hsiao, Jensen Tsai, Eason Chen, and Otis Hong – Siliconware Precision Industries Co., Ltd.	5. ***10:25 a.m. – A Novel and Accurate Methodology for Design and Characterization of Wire-Bond Package Performance for 5-10GHz Applications*** Souvik Mukherjee and Django Trombley – Texas Instruments, Inc.
6. ***10:50 a.m. – Combined Vibration and Thermal Cycling Fatigue Analysis for SAC305 Lead Free Solder Assemblies*** J.H.L. Pang and F.L. Wong – Nanyang Technological University; K.T. Heng, Y.S. Chua, and C.E. Long – DSO National Laboratories	6. ***10:50 a.m. – DBC Substrate for Si- and SiC-Based Power Electronics Modules: Design, Fabrication and Failure Analysis*** Ling Xu, Yang Zhou, and Sheng Liu – Huazhong University of Science & Technology	6. ***10:50 a.m. – High Frequency Characterization and Analytical Modeling of Through Glass Via (TGV) for 3D Thin-Film Interposer and MEMS Packaging*** Cheolbok Kim and Yong-Kyu Yoon – University of Florida
7. ***11:15 a.m. – Effects of Varying Amplitudes on the Fatigue Life of Lead Free Solder Joints*** M. Obaidat, S. Hamasha, Y. Jaradat, A. Qasaimeh, and P. Borgesen – State University of New York, Binghamton; B. Arfaei and M. Anselm – Universal Instruments	7. ***11:15 a.m. – A Monolithic Aluminum Circuit Board Structure*** Shou-Jen Hsu and Chin C. Lee – University of California, Irvine	7. ***11:15 a.m. – PCB Pin-Field Considerations for 40 Gb/s SerDes Channels*** Michael J. Degerstrom, Devon J. Post, Barry K. Gilbert, and Erik S. Daniel – Mayo Clinic

Program Sessions: Friday, May 31, 1:30 p.m. - 5:10 p.m.

Session 31: TSV Innovation and Implementation	Session 32: Thermal and Mechanical Modeling: LED and 3D Structures	Session 33: MEMS and Sensor Packaging
Committee: Interconnections	**Committee:** Modeling & Simulation	**Committee:** Advanced Packaging
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: Gilles Poupon – CEA-LETI Wei-Chung Lo – ITRI	**Session Co-Chairs:** Suresh K. Sitaraman – Georgia Institute of Technology Sandeep Sane – Intel Corporation	**Session Co-Chairs:** S.W. Ricky Lee – Hong Kong Univ. of Science and Technology James Jian Zhang – Micron Technology, Inc.
1. 1:30 p.m. – ***Through Si Vias Using Liquid Metal Conductors for Reworkable 3D Electronics*** George A. Hernandez, Daniel Martinez, Charles Ellis, Michael Palmer, and Michael C. Hamilton – Auburn University	**1.** 1:30 p.m. – ***Drop Impact Simulation and Experimental Validation on High Power Light Emitting Diodes Modules*** Cao Li, Tao Peng, Xuefang Wang, Mingxiang Chen, and Sheng Liu – Huazhong University of Science & Technology	**1.** 1:30 p.m. – ***Hermetic Wafer Level Packaging of MEMS Components Using Through Silicon Via and Wafer to Wafer Bonding Technologies*** K. Zoschke, C.A. Manier, M. Wilke, N. Jürgensen, and H. Oppermann – Fraunhofer IZM; D. Ruffieux – CSEM; J. Dekker and H. Heikkinen – VTT Finland; S. Dalla Piazza – Micro Crystal AG; G. Allegato – STMicroelectronics; K.D. Lang – TU Berlin
2. 1:55 p.m. – ***Backside TSV Protrusions Induced by Thermal Shock and Thermal Cycling*** Dingyou Zhang and James Jian-Qiang Lu – Rensselaer Polytechnic Institute; Klaus Hummler and Larry Smith – SEMATECH	**2.** 1:55 p.m. – ***L70 Life Prediction for Solid State Lighting Using Kalman Filter and Extended Kalman Filter Based Models*** Pradeep Lall and Junchao Wei – Auburn University; Lynn Davis – RTI International	**2.** 1:55 p.m. – ***Size-Free MEMS-IC High-Efficient Integration by Using Carrier Wafer with Self-Assembled Monolayer (SAM) Fine Pattern*** Jian Lu, Hideki Takagi, and Ryutaro Maeda – National Institute of AIST; Yuta Nakano – National Institute of AIST, Tokyo University of Science
3. 2:20 p.m. – ***Microstructure Investigation of TSV Copper Film*** W.N. Putra – Institute of Microelectronics (A*STAR), Nanyang Technological University; H.Y. Li and A.D. Trigg – Institute of Microelectronics (A*STAR); C.L. Gan – Nanyang Technological University	**3.** 2:20 p.m. – ***Effect of Temperature Gradient on Moisture Diffusion in High Power Devices and the Applications in LED Packages*** Xuejun Fan – Lamar University, State Key Lab of Solid-State Lighting; Cadmus Yuan – State Key Lab of Solid-State Lighting, Chinese Academy of Sciences	**3.** 2:20 p.m. – ***Outgassing Characterization of MEMS Thin Film Packaging Materials*** B. Savornin, X. Baillin, D. Saint Patrice, P. Nicolas, P.L. Charvet, and J.L. Pornin – CEA-LETI; E. Blanquet and I. Nuta – SIMAP
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Mont-Royal Commons)		
4. 3:30 p.m. – ***Via-Middle Through-Silicon Via with Integrated Airgap to Zero TSV-Induced Stress Impact on Device Performance*** Yann Civale, Stefaan Van Huylenbroeck, Augusto Redolfi, Wei Guo, Khashayar Babaei, Patrick Jaenen, Antonio La Manna, Gerald Beyer, Bart Swinnen, and Eric Beyne – IMEC	**4.** 3:30 p.m. – ***Thermal and Mechanical Design and Analysis of 3D IC Interposer with Double-Side Active Chips*** Sheng-Tsai Wu, Heng-Chieh Chien, and John H. Lau – Industrial Technology Research Institute (ITRI); Ming Li, Julia Cline, and Mandy Ji – Rambus, Inc.	**4.** 3:30 p.m. – ***Surface Compliant Bonding Properties of Low-Temperature Wafer Bonding Using Sub-Micron Au Particles*** Hiroyuki Ishida and Takuya Yazaki – Suss MicroTec KK; Toshinori Ogashiwa, Yukio Kanehira, and Hiroshi Murai – Tanaka Kikinzoku Kogyo KK; Shin Ito and Jun Mizuno – Waseda University
5. 3:55 p.m. – ***Design and Fabrication of Ultra Low-Loss, High-Performance 3D Chip-Chip Air-Clad Interconnect Pathway*** Erdal Uzunlar, Rajarshi Saha, Vachan Kumar, Azad Naeemi, and Paul A. Kohl – Georgia Institute of Technology; Rohit Sharma – Indian Institute of Technology Ropar; Rizwan Bashirullah – University of Florida	**5.** 3:55 p.m. – ***Comparison of Thermal Performance between Glass and Silicon Interposers*** Sangbeom Cho, Yogendra Joshi, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass	**5.** 3:55 p.m. – ***Hermetic Wafer-Level Glass Sealing Enabling Reliable Low Cost Sensor Packaging*** Ulli Hansen and Simon Maus – MSG Lithoglas GmbH; Michael Töpper – Fraunhofer IZM
6. 4:20 p.m. – ***Development of Ultra-Low Capacitance Through-Silicon-Vias (TSVs) with Air-Gap Liner*** Qianwen Chen, Cui Huang, and Zheyao Wang – Tsinghua University	**6.** 4:20 p.m. – ***Simulation of Electromigration through Peridynamics*** Selda Oterkus, John Fox, and Erdogan Madenci – University of Arizona	**6.** 4:20 p.m. – ***Cu/Sn SLID Wafer-Level Bonding Optimization*** Thi-Thuy Luu, Ani Duan, Kaiying Wang, Knut Aasmundtveit, and Nils Hoivik – Vestfold University College
7. 4:45 p.m. – ***TSV Development, Characterization and Modeling for 2.5D Interposer Applications*** J.R. Tenailleau, F. Voiron, and C. Bunel – IPDIA; A. Brunet and S. Borel – CEA-LETI	**7.** 4:45 p.m. – ***The Effect of Corner Glue on BGA Package Temperature Cycling Performance: A Modeling Study*** Min Pei, Ru Han, Yun Ge, Sanjay Goyal, Venmathy Rajarathinam, and Muffadal Mukadam – Intel Corporation	**7.** 4:45 p.m. – ***Reliability of Flip-Chip Technologies for SiC-MEMS Operating at 500°C*** Roderich Zeiser, Lukas Lehmann, Volker Fiedler, and Jürgen Wilde – University of Freiburg

Program Sessions: Friday, May 31, 1:30 p.m. - 5:10 p.m.

Session 34: New Developments in Wirebond Technology	Session 35: Solder and Bonding	Session 36: System Components for RF and Millimeter Wave
Committees: Assembly & Manufacturing Technology / Interconnections	**Committee: Materials & Processing**	**Committee: Electronic Components & RF**
Nolita 2	**Nolita 3**	**Yaletown 4**
Session Co-Chairs: **Jie Xue – Cisco Systems, Inc.** **Changqing Liu – Loughborough University**	**Session Co-Chairs:** **Tieyu Zheng – Microsoft Corporation** **Myung Jin Yim – Broadcom Corporation**	**Session Co-Chairs:** **Lih-Tyng Hwang – National Sun Yat-Sen University** **P. Markondeya Raj – Georgia Institute of Technology**
1. 1:30 p.m. – *Investigation of Charge Induced Bond Pad Corrosion* Pei-Haw Tsao, Hung-Yu Chiu, H.C. Liao, K.C. Chen, M.C. Sung, Worth Chen, and Antai Xu – Taiwan Semiconductor Manufacturing Company, Ltd.	**1. 1:30 p.m. – *NiFe-Based Ball-Limiting-Metallurgy (BLM) for Microbumps at 50um Pitch in 3D Chip Stacks*** Bing Dang, Steven Wright, Joana Maria, Cornelia Tsang, Paul Andry, Lovell Wiggins, and John Knickerbocker – IBM Corporation	**1. 1:30 p.m. – *Low Cost BT Organic Material for Wireless 60 GHz Application*** Pouya Talebbeydokhti and Mohamed A. Megahed – Intel Corporation
2. 1:55 p.m. – *Effects of Bond Pad Probing for Cu Wire Bond Packages* John D. Beleran, Gaurav Mehta, Ninoy Milanes II, and Nathapong Suthiwongsunthorn – United Test and Assembly Center, Ltd. (UTAC); Eu Jin Lee – GLOBALFOUNDRIES	**2. 1:55 p.m. – *The Growth and Segregation of Intermetallic Compounds in the Bulk of Flip Chip Sn2.4Ag Solder Joint under Electrical Current Stressing*** Wei-Chieh Wang and Kwang-Lung Lin – National Cheng Kung University; Ying-Ta Chiu and Yi-Shao Lai – Advanced Semiconductor Engineering, Inc.	**2. 1:55 p.m. – *Novel Enhancement Techniques for Ultra-High-Performance Conformal Wireless Sensors and "Smart Skins" Utilizing Inkjet-Printed Graphene*** Taoran Le, Ziyin Lin, C.P. Wong, and M.M. Tentzeris – Georgia Institute of Technology
3. 2:20 p.m. – *A Study of Free Air Ball Formation in Palladium-Coated Copper and Bare Copper Bonding Wire* Noritoshi Araki, Ryo Oishi, and Takashi Yamada – Nippon Micrometal Corporation; Yasutomo Ichiyama – Nippon Steel Technoresearch Corporation	**3. 2:20 p.m. – *Voiding Mechanism and Control in BGA Joints with Mixed Solder Alloy System*** Yan Liu, Derrick Herron, Joanna Keck, and Ning-Cheng Lee – Indium Corporation	**3. 2:20 p.m. – *High Performance Plastic Molded QFN Package with Ribbon Bonding and a Defective PCB Ground*** Yi-Chieh Lin, Wen-Hsian Lee, Tzyy-Sheng Horng, and Lih-Tyng Hwang – National Sun Yat-Sen University
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Mont-Royal Commons)		
4. 3:30 p.m. – *Single Chip Plated Ni/Pd over ALCAP Bond Pads for Flip Chip Applications and Prototyping* Brian J. Lewis, Daniel F. Baldwin, Paul N. Houston, Fei Xie, and Le Hang La – Engent, Inc.	**4. 3:30 p.m. – *Low Temperature Camera Module Assembly Using Acrylic-Based Solder ACFs with Ultrasonic-Assisted Thermo-Compression Bonding Method*** Yoo-Sun Kim, Seung-Ho Kim, and Kyung-Wook Paik – KAIST	**4. 3:30 p.m. – *Enhanced Multilayer Organic Packages with Embedded Phased-Array Antennas for 60-GHz Wireless Communications*** Xiaoxiong Gu, Duixian Liu, Maxim Piz, Alberto Valdes-Garcia, Christian Baks, Bodhisatwa Sadhu, and Scott K. Reynolds – IBM Corporation; Dong Gun Kam – IBM Corporation, Ajou University; Arun Natarajan – IBM Corporation, Oregon State University
5. 3:55 p.m. – *Low Cost Silver Alloy Wire Bonding with Excellent Reliability Performance* C.H. Cheng, S.I. Chu, Y.Y. Shieh, C.Y. Sun, and C. Peng – Elite Semiconductor Memory Technology, Inc.; H.L. Hsiao – Tunghai University	**5. 3:55 p.m. – *High Temperature Ag-In Joints between Si Chips and Aluminum*** Yuan-Yun Wu and Chin C. Lee – University of California, Irvine	**5. 3:55 p.m. – *Ultra-Miniaturized and Surface-Mountable Glass-Based 3D IPAC Packages for RF Modules*** Y. Sato and M. Ono – Asahi Glass Company; S. Sitaraman, V. Sukumaran, B. Chou, J. Min, M. Swaminathan, V. Sundaram, and R. Tummala – Georgia Institute of Technology; C. Karoui, F. Dosseul, and C. Nopper – STMicroelectronics
6. 4:20 p.m. – *Corrosion of the Cu/Al Interface in Cu-Wire-Bonded Integrated Circuits* John Osenbach, B.Q. Wang, Sue Emerich, John DeLucca, and Dongmei Meng – LSI Corporation	**6. 4:20 p.m. – *Failure Mechanisms of Sintered Silver Interconnections for Power Electronic Applications*** Thomas Herboth, Michael Guenther, and Andreas Fix – Robert Bosch GmbH; Juergen Wilde – University of Freiburg	**6. 4:20 p.m. – *Integration of Piezoelectric Energy Harvesting and Antenna Elements on a Common Substrate*** Joshua C. Myers, B. Scott Strachan, Xianbo Yang, and Premjeet Chahal – Michigan State University
7. 4:45 p.m. – *Molded Reliability Study for Different Cu Wire Bonding Configurations* I. Qin, H. Xu, B. Milton, H. Clauberg, and B. Chylak – Kulicke and Soffa Industries, Inc.; H. Abe, D. Kang, Y. Endo, M. Osaka, and S Nakamura – Hitachi Chemical Company, Ltd.	**7. 4:45 p.m. – *Advanced Materials for Drop in Solution to Pb in High Temp Solders: The Next Generation of Zinc-Based Solder Alloy*** Jianxing Li and Brian Knight – Honeywell Electronic Materials; Bih Wen Fon and Shutesh Krishnan – On Semiconductor	**7. 4:45 p.m. – *Second-Harmonic Nonlinearities in RF Silicon Integrated Passive Devices*** Robert Frye – RF Design Consulting, LLC; Kai Liu – STATS ChipPAC, Inc.; Robert Melville – Emecon, LLC

Wednesday, May 29
Session 37: Interactive Presentations 1
9:00 a.m. - 11:00 a.m.
Committee: Interactive Presentations
Chelsea 3 & 4

Session Co-Chairs:
Mark Poliks – Endicott Interconnect Technologies, Inc.
Mark Eblen – Kyocera America, Inc.

1. ***Adaptable and Integrated Packaging Platform for MEMS-Based Combo Sensors Utilizing Innovative Wafer-Level Packaging Technologies***
Cheng-Hsiang Liu, Hong-Da Chang, Kuo-Hsiang Li, Chen-Han Lin, Chia-Jung Hsu, Tse-Yuan Lin, Hsin-Hung Chou, Hsiao-Chun Huang, and Hsin-Yi Liao – Siliconware Precision Industries Co., Ltd.
2. ***Electrochromic Properties of Tungsten Trioxide Nanostructures***
Yi-Hsuan Huang, Chung-Jung Hung, and Tseung-Yuen Tseng – National Chiao Tung University
3. ***Wettability of Sn-Bi and Sn-Ag-Cu Lead-Free Solder Pastes on Electroplated Co-P Films***
Donghua Yang, Nianduan Lu, and Liangliang Li – Tsinghua University
4. ***Enhanced Thermal Transport of Hexagonal Boron Nitride Filled Polymer Composite by Magnetic Field-Assisted Alignment***
Ziyin Lin, Yan Liu, and Kyoung-Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
5. ***Small Diameter Via Filling Electrodeposition by Periodical Reverse Current***
Taro Hayashi, Kazuo Kondo, Takeyasu Saito, Naoki Okamoto, and Masayuki Yokoi – Osaka Prefecture University; Minoru Takeuchi and Masaru Bunya – Nitto Boseki Co., Ltd.; Masao Marunaka and Takayuki Tsuchiya – ShinMaywa Industries, Ltd.
6. ***Moisture Induced Swelling in Epoxy Moulding Compounds***
H. Walter, O. Hölck, T. Braun, J. Bauer, and O. Wittler – Fraunhofer IZM; H. Dobrinski and J. Stuermann – Hella Fahrzeugkomponenten GmbH; K.D. Lang – Fraunhofer IZM, TU Berlin
7. ***Fine Pitch Flex-on-Flex (FOF) Assembly Using Nanofiber Solder Anisotropic Conductive Films (ACFs) and Ultrasonic Bonding Method***
Sang Hoon Lee, Kyung-Lim Suk, and Kyung-Wook Paik – KAIST
8. ***Flux Function Added Solder Anisotropic Conductive Films (ACFs) for High Power and Fine Pitch Assemblies***
Seung-Ho Kim, Yongwon Choi, Yoosun Kim, and Kyung-Wook Paik – KAIST
9. ***Microwave Induced Plasma Decapsulation of Stressed and Delaminated High Pin-Count Copper Wire Bonded IC Packages***
J. Tang, J.B.J. Schelen, and C.I.M. Beenakker – Delft University of Technology; C.H. Chen and S.K. Liang – Advanced Semiconductor Engineering, Inc.; E.G.J. Reinders and C.Th.A. Revenberg – MASER Engineering B.V.
10. ***Glass Carrier Wafers for the Silicon Thinning Process for Stack IC Applications***
Aric Shorey, Bor-Kai Wang, and Rachel Lu – Corning, Inc.
11. ***Versatile Z-Axis Interconnection-Based Coreless Technology Solutions for Next Generation Packaging***
R.N. Das, F.D. Egitto, J.M. Lauffer, E. Chenelly, and M.D. Poliks – Endicott Interconnect Technologies, Inc.
12. ***Oxidation Resistance and Joining Properties of Cr-Doped Zn Bonding for SiC Die-Attachment***
S.W. Park, T. Sugahara, S. Nagao, and K. Suganuma – Osaka University
13. ***Thermomechanical Reliability of Ag Flake Paste for Die-Attached Power Devices in Thermal Cycling***
Soichi Sakamoto, Shijo Nagao, and Katsuaki Suganuma – Osaka University
14. ***A Breakthrough in Power Electronics Reliability – New Die Attach and Wire Bonding Materials***
Thomas Krebs, Susanne Duch, Wolfgang Schmitt, Steffen Kötter, Peter Prenosil, and Sven Thomas – Heraeus Material Technologies GmbH & Co. KG
15. ***Bath Chemistry and Copper Overburden as Influencing Factors of the TSV Annealing***
P. Sättler and K.J. Wolter – TU Dresden; M. Böttcher and Catharina Rudolph – FhG ASSID
16. ***Nonlinear Viscoelastic Constitutive Model for Organic Laminate Substrate***
Tz-Cheng Chiu and Yao-Yu Chan – National Cheng Kung University; Yi-Shao Lai – Advanced Semiconductor Engineering, Inc.
17. ***Effect of Processing Factors on Dielectric Properties of $BaTiO_3$/Hyperbranched Polyester Core-Shell Nanoparticles***
Warda Benhadjala, Isabelle Bord-Majek, Laurent Béchou, and Yves Ousten – University of Bordeaux; Ephraim Suhir – University of California, Santa Cruz; Matthieu Buet, Fabien Rougé, and Vincent Gaud – Polyrise SAS
18. ***Strength of Solid-State Silver Bonding between Copper***
Yi-Ling Chen and Chin C. Lee – University of California, Irvine
19. ***Effect of Pad Design (SMD/NSMD), Via-in-Pad, and Reflow Profile Parameters on Voiding During the Lead-Free Solder Bumping Process***
Ganesh Pandiarajan, Ross Havens, and Krishnaswami Srihari – State University of New York, Binghamton; Satyanarayan Iyer and Gurudutt Chennagiri – SMART Modular Technologies, Inc.
20. ***Growth and Strength of the Solid Solution Phase (Ag) with Indium***
Yuan-Yun Wu and Chin C. Lee – University of California, Irvine
21. ***Assessment of Solder Pad Cratering Strength Using Cold Pin Pull Test Method with Pre-Fabricated Pin Arrays***
Qiming Zhang, Chaoran Yang, Mian Tao, and S.W. Ricky Lee – Hong Kong University of Science & Technology; Fubin Song – Celestica
22. ***Reliability of Isotropic Electrically Conductive Adhesives under Condensing Humidity Testing***
Laura Frisk, Sanna Lahokallio, Milad Mostofizadeh, Janne Kiilunen, and Kirsi Saarinen – Tampere University of Technology
23. ***Ethylene-Vinyl Acetate as a Low Cost Encapsulant for Hybrid Electronic and Fluidic Circuits***
Sarkis Babikian, Wesley A. Cox-Muranami, Edward Nelson, G.P. Li, and Mark Bachman – University of California, Irvine
24. ***Noise Coupling of Through-Via in Silicon and Glass Interposer***
Manho Lee, Jonghyun Cho, Joohee Kim, Jounghо Kim, and Jiseong Kim – KAIST

Wednesday, May 29
Session 38: Interactive Presentations 2
2:00 p.m. - 4:00 p.m.
Committee: Interactive Presentations
Chelsea 3 & 4

Session Co-Chairs:
Swapan Bhattacharya – Georgia Institute of Technology
Nam Pham – IBM Corporation

1. ***Fine-Pitch Backside Via-Last TSV Process with Optimization on Temporary Glue and Bonding Conditions***
E.H. Chen, T.C. Hsu, C.H. Lin, P.J. Tzeng, C.C. Wang, S.C Chen, J.C. Chen, C.C. Chen, Y.C. Hsin, P.C. Chang, Y.H. Chang, Y.M. Lin, S.C. Liao, and T.K. Ku, and S.C. Chen – Industrial Technology Research Institute (ITRI)
2. ***Investigation of Micromachined LTCC Functional Modules for High-Density 3D SIP Based on LTCC Packaging Platform***
M. Miao – Beijing Info. Sci. and Tech. University, Peking Univ.; Y. Jin, R. Fang, S. Guo, X. Zhang, and D. Hu – Peking Univ.; F. Mu and X. Xiang – 43rd Inst. of China Elec. Tech. Group Corp.; Y. Zhang and Z. Li – Beijing Info. Sci. and Tech. University
3. ***Advancements in Package-on-Package (PoP) Technology, Delivering Performance, Form Factor & Cost Benefits in Next Generation Smartphone Processors***
Hamid Eslampour, Mukul Joshi, SeongWon Park, HanGil Shin, and JaeHan Chung – STATS ChipPAC, Ltd.
4. ***Fabrication of 3D-IC Interposers***
John Keech, Satish Chaparala, Aric Shorey, Garrett Piech, and Scott Pollard – Corning, Inc.
5. ***Development of Double Sided with Double-Chip Stacking Structure Using Panel Level Embedded Wafer Level Packaging***
Yen-Fu Su and Kuo-Ning Chiang – National Tsing Hua University; Chun-Te Lin and Tzu-Ying Kuo – Industrial Technology Research Institute (ITRI)
6. ***Innovative Ultra Fine Line Ceramic Substrate for Semiconductor Package***
Nozomi Shimoishizaka, Takahiro Nakano, Mutsuo Tsuji, Eiji Yamaguchi, Hiroaki Fujimoto, and Hirata Katsunori – ConnectTec Japan Corporation
7. ***Development of Ultra-Thin Low Warpage Coreless Substrate***
Yu Sun, Xiaofeng He, Zhongyao Yu, and Lixi Wan – Institute of Microelectronics, Chinese Academy of Science
8. ***A Compact ROSA Module for Serial 40-Gb/s Optical Transceiver***
Sae-Kyoung Kang, Joon Ki Lee, Joon-Young Huh, Kwangjoon Kim, and Jonghyun Lee – Electronics and Telecommunications Research Institute
9. ***Fanout Flipchip eWLB (Embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions***
Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse – STATS ChipPAC
10. ***Novel Design and Reliability Assessment of a 3D DRAM Stacking Based on Cu-Sn Micro-Bump Bonding and TSV Interconnection Technology***
Cao Li, Xuefang Wang, Mingxiang Chen, Yaping Lv, and Sheng Liu – Huazhong University of Science & Technology, Wuhan National Lab for Optoelectronics; Shengjun Zhou – Wuhan National Lab for Optoelectronics, Shanghai Jiao Tong University
11. ***Assembly Tolerant Design of Multi-Cell Laser Power Converters for Wafer-Level Photonic Packaging***
S. Sohr, R. Rieske, K. Nieweglowski, and K.J. Wolter – TU Dresden
12. ***Reflection-Phase Variation of Cavity-Resonator-Integrated Guided-Mode-Resonance Reflector for Guided-Mode-Exciting Surface Laser Mirror***
Shogo Ura, Junichi Inoue, Tomonori Ogura, Kenzo Nishio, and Yasuhiro Awatsuji – Kyoto Institute of Technology; Kenji Kintaka – National Institute of AIST
13. ***Process Integration of Backside Illuminated Image Sensor with Thin Wafer Handling Technology***
H.H. Chang, C.H. Chien, H.C. Fu, W.L. Tsai, C.W. Chiang, C.T. Ko, Y.H. Chen, and W.C. Lo – Industrial Technology Research Institute (ITRI); K.C. Su and C.S. Li – Brewer Science
14. ***Impact of Wafer Thinning on High-k Metal Gate 20nm Devices***
A. Beece – Rensselaer Polytechnic Institute, GLOBALFOUNDRIES; R. Agarwal, J. Singh, S. Siddhartha, R. Alapati, and T. Alvanos – GLOBALFOUNDRIES; S. Chandrashekhar and B. Parameshwaran – Suss MicroTec; J. Dumas – Disco Hi-Tech America, Inc.
15. ***Design and Optimization of Planar Multimode Waveguides for High-Speed, Board-Level Optical Interconnects***
Krzysztof Nieweglowski, Ralf Rieske, Sebastian Sohr, and Klaus-Juergen Wolter – TU Dresden
16. ***Electronic-Microfluidic System for Sorting Particles and Whole Blood Using Gel Electrodes***
Jason Luo, Edward Nelson, G.P. Li, and Mark Bachman – University of California, Irvine
17. ***Wafer-Level Integration of Micro-Lens for THz Focal Plane Array Application***
Kyoung Youl Park, Nophadon Wiwatcharagoses, and Premjeet Chahal – Michigan State University
18. ***Advanced LED Package with Temperature Sensors and Microfluidic Cooling***
H. Ye – Delft Univ. of Technology, Organization for Applied Scientific Research (TNO); H. Van Zeijl, R. Sokolovskij, and G.Q. Zhang – Delft Univ. of Technology; A.W.J. Gielen – Netherlands Organization for Applied Scientific Research (TNO)
19. ***Micromachined Wearable/Foldable Super Wideband (SWA) Monopole Antenna Based on a Flexible Liquid Crystal Polymer (LCP) Substrate toward Imaging/Sensing/Health Monitoring Systems***
Cheolbok Kim, Kyoung Tae Kim, and Yong-Kyu Yoon – University of Florida; Jong Kyu Kim – Attached Institute of ETRI
20. ***Three Dimensional Interconnect Using Au and Pillar Bumps***
F.J. Wu, L.H. Ho, C.M. Kuo, C.J. Tu, C.T. Hsieh, C.H. Ni, S.C. Chang, C.Y. Wu, H.Y. Huang, K.A. Lin, and Y.M. Hsu – Chipbond Technology Corporation
21. ***Defect Analysis Using High Throughput Plasma FIB in Packaging Reliability Investigations***
F. Altmann, S. Klengel, J. Schischka, and M. Petzold – Fraunhofer IWM
22. ***High Frequency DC-DC Converter with Co-Packaged Planar Inductor and Power IC***
N. Wang, J. Barry, S. Kulkarni, F. Waldron, J. Rohan, J. O'Brien, A.M. Kelleher, S. Roy, C.Ó. Mathúna– Tyndall National Institute; J. Hannon, R. Foley, K. McCarthy- Univ. College Cork; M. Barry – Microelectronics Competence Centre Ireland
23. ***Kinetics Study of Intermetallic Growth and Its Reliability Implications in Pb-Free, Sn-Based Microbumps in 3D Integration***
Yiwei Wang, Jay Im, and Paul S. Ho – University of Texas, Austin; Seung-Hyun Chae – Texas Instruments, Inc.
24. ***Laminates for Miniaturized Integrated Bioelectronic Protein Analysis Systems***
Sara Saedinia, Kevin Limtao, G.P. Li, and Mark Bachman – University of California, Irvine; Kent Nastiuk and John Krolewski – University of Rochester Medical Center
25. ***A New 2.5D TSV Package Assembly Approach***
Y. Lu, W. Yin, B. Zhang, D. Yu, and D. Shangguan – National Center for Advanced Packaging, Chinese Academy of Sciences; L. Wan – Chinese Academy of Sciences; G. Xia and F. Qin – Beijing University of Technology; M. Ru and F. Xiao – Fudan University
26. ***Fabrication and Characterization of Novel Photodefined Polymer-Enhanced Through-Silicon Vias for Silicon Interposers***
Paragkumar A. Thadesar and Muhannad S. Bakir – Georgia Institute of Technology
27. ***Process Characteristics of a 2.5D Silicon Module Using Embedded Technology as a Feasible Solution for System Integration and Thinner Form-Factor***
Ren-Shin Cheng, Yin-Po Hung, Tzu-Ying Kuo, Yu-Min Lin, Fan-Jun Leu, and Tao-Chih Chang – Industrial Technology Research Institute (ITRI)

Thursday, May 30
Session 39: Interactive Presentations 3
9:00 a.m. - 11:00 a.m.
Committee: Interactive Presentations
Chelsea 3 & 4

Session Co-Chairs:
Ibrahim Guven – University of Arizona
Mark Poliks – Endicott Interconnect Technologies, Inc.

1. ***A Lumped/Discrete Port De-Embedding Method by Port Connection Error-Cancelling Network in Full-Wave Electromagnetic Modeling of 3D Integration and Packaging with Vertical Interconnects***
Zhaoqing Chen – IBM Corporation
2. ***Current Density Effects on the Electrical Reliability of Ultra Fine-Pitch Micro-Bump for TSV Integration***
Young-Bae Park, Seung-Hyun Kim, Jong-Jin Park, and June-Bum Kim – Andong National University; Ho-Young Son, Kwon-Whan Han, Jae-Sung Oh, and Nam-Seog Kim – SK Hynix Inc.; Sehoon Yoo – Korean Institute of Industrial Technology
3. ***Fixture-Free Measurement Technique for PDN Discrete Components***
Di Hu, Jaemin Shin, and Timothy Michalka – Qualcomm Technologies, Inc.
4. ***High-Performance RF Components Using Capacitively-Coupled Contacts over III-N Heterostructures***
F. Jahan, Y.H. Yang, and G. Simin – University of South Carolina; M. Gaevski, J. Deng, and R. Gaska – Sensor Electronic Technology, Inc.; M. Shur – Rensselaer Polytechnic Institute
5. ***High-Frequency (RF) Electrical Analysis of Through Silicon Via (TSV) for Different Designed TSV Patterns***
Hsin-Kai Huang, Chun-Hsun Lin, Chris Liu, Kwan-Chin Fan, and Hsin-Hung Lee – Siliconware Precision Industries Co., Ltd.
6. ***Fast Signal Integrity Methodology for PCB Pre-Layout Analysis and Layout Quality Check***
Jimmy Hsu, Thonas Su, Yuan-Liang Li, Edward Hsiung, Kai Xiao, Xiaoning Ye, and Kai-Bin Wu – Intel Corporation

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

7. ***3D Antenna for GHz Application and Vibration Energy Harvesting***
Konstantin Kholostov, Paolo Nenzi, Fabrizio Palma, and Marco Balucani – University of Rome
8. ***Electrical Performance Modeling of Unbalanced Comb Tree Networks on Advanced PCB Interconnects for High-Rate Clock Signal Distribution***
Thomas Eudes and Blaise Ravelo – ESIGELEC; Thierry Lacrevaz and Bernard Fléchet – Université de Savoie
9. ***Far-End Crosstalk Cancellation Using Via Stub for DDR4 Memory Channel***
Chien-Ming Nieh – University of Florida; Jongbae Park – Intel Corporation
10. ***Practical Investigations of Fiber Weave Effects on High-Speed Interfaces***
Gerardo Romo-Luevano, Jaemin Shin, and Timothy Michalka – Qualcomm Technologies, Inc.
11. ***High-Speed Packages with Imperfect Power and Ground Planes***
Kai Liu, Ma Phoo Pwint Hlaing, Yong Taek Lee, Hyun Tai Kim, Gwang Kim, Susan Park, and Billy Ahn – STATS ChipPAC, Ltd.; Robert Frye – RF Design Consulting, LLC
12. ***A Miniaturized Module for Bluetooth/GPS by Embedding Capacitors in Printed-Circuit-Board and Using Interposer***
Jong-In Ryu, Se-Hoon Park, Dongsu Kim, Jun-Chul Kim, and Jong-Chul Park – Korea Electronics Technology Institute
13. ***Optimal Common-Mode Choke Selection for the High Definition Video Interface for the Mobile Application***
Junwoo Lee, Youchul Jeong, and Baegin Sung – Silicon Image, Inc.
14. ***Pre-Emphasis Parameter Optimization for High Speed Channels Using De-Convolution Approach***
Jifeng Mao and Umesh Chandra – Dell Force10
15. ***Graphene Heat Spreader for Thermal Management of Hot Spots***
Zhaoli Gao – Chalmers University of Technology, Hong Kong University of Science and Technology; Yong Zhang and Johan Liu – Chalmers University of Technology, Shanghai University; Yifeng Fu – SHT Smart High Tech AB; Matthew Yuen – Hong Kong University
16. ***Modeling and Simulation of Low Duty Ratio Buck Synchronous Converter under Large Load Current Switching***
Jai P. Agrawal – Purdue University
17. ***Compact TSV-Based Wideband Bandpass Filters on 3-D IC***
Ying-Cheng Tseng and Tzong-Lin Wu – National Taiwan University; Peng-Shu Chen, Wei-Chung Lo, and Shih-Hsien Wu – Industrial Technology Research Institute (ITRI)
18. ***Implementation of a MIMO Antenna Design for USB Dongle Applications***
Yu-Kai Tseng, Yi-Chieh Lin, and Lih-Tyng Hwang – National Sun Yat-Sen University
19. ***Efficient Complex Broadside Coupled Trace Modeling and Estimation of Crosstalk Impact Using Statistical BER Analysis for High Volume, High Performance Printed Circuit Board Designs***
Arun Reddy Chada, Songping Wu, Jun Fan, and James L. Drewniak – Missouri S&T EMC Laboratory; Bhyrav Mutnury – Dell, Inc.; Daniel N. de Araujo – Nimbic
20. ***Terahertz Micropolarizers Using Carbon Microfibers***
Amanpreet Kaur, Kyoung Youl Park, Xianbo Yang, Nophadon Wiwatcharagoses, and Premjeet Chahal – Michigan State University
21. ***Layout Parameter Optimization Based Power and Signal Integrity Performance Improvement of High-Speed Interfaces of Wirebond Packages***
Om P. Mandhana and Jin Zhao – Intel Corporation
22. ***3D IC-Package-Board Co-Analysis Using 3D EM Simulation for Mobile Applications***
Darryl Kostka – CST of America; Taigon Song and Sung Kyu Lim – Georgia Institute of Technology
23. ***3D eWLB – Horizontal and Vertical Interconnects for Integration of Passive Components***
M. Wojnowski, G. Sommer, K. Pressel, and G. Beer – Infineon Technologies AG
24. ***mmW Characterization of Wafer Level Passivation for 3D Silicon Interposer***
Y. Lamy, O. El Bouayadi, C. Ferrandon, A. Schreiner, A. Jouve, and L. Dussopt – CEA-LETI; T. Lacrevaz, C. Bermond, and B. Fléchet – IMEP-LAHC; S. Joblot – STMicroelectronics

Thursday, May 30
Session 40: Interactive Presentations 4
2:00 p.m. - 4:00 p.m.
Committee: Interactive Presentations
Chelsea 3 & 4

Session Co-Chairs:
Patrick Thompson – Texas Instruments, Inc.
Rao Bonda – Amkor Technology

1. ***Piezoresistive Stress Sensor for Inline Monitoring During Assembly and Packaging of QFN***
Thomas Schreier-Alt and Frank Ansorge – Fraunhofer IZM; Gerhard Chmiel – Elmos Semiconductor AG; Klaus-Dieter Lang – TU Berlin
2. ***Thermo-Mechanical Reliability of Copper-Filled and Polymer-Filled Through Silicon Vias in 3D Interconnects***
Xiang Gao, Run Chen, Xuefang Wang, and Sheng Liu – Huazhong University of Science & Technology, Wuhan National Lab for Optoelectronics; Xiaobing Luo – Huazhong University of Science & Technology, Wuhan National Lab for Optoelectronics
3. ***Electrochemical Reactions in Solder Mask of Flip Chip-Plastic Ball Grid Array Package***
Kang-Wook Lee, Stephane Barbeau, Francois Racicot, Douglas Powell, Charles Arvin, Thomas Wassick, and Joseph Ross – IBM Corporation
4. ***Design and Assembly Process Simulation for an Automotive Power Module***
Yong Liu, Qiuxiao Qian, Byoungok Lee, Taekkeun Lee, Joonseo Son, and Oseob Jeon – Fairchild Semiconductor Corporation
5. ***Investigation of Copper-Tin Transient Liquid Phase Bonding Reliability for 3D Integration***
A. Garnier, C. Grémion, R. Franiatte, D. Bouchu, R. Anciant, and S. Chéramy – CEA-LETI
6. ***Development of PCB Design Guide and PCB Deformation Simulation Tool for Slim PCB Quality and Reliability***
Soonwan Chung, Gyun Heo, Jae Kwak, Seunghee Oh, Yongwon Lee, Changsun Kang, and Tackmo Lee – Samsung Electronics Company, Ltd.
7. ***Thermal Cycling Effect on Intermetallic Formation with Various Surface Finish of Micro Bump Interconnect for 3D Package***
Mu-Hsuan Chan, Yi-Chian Liao, Chun-Tang Lin, Kuan-Weir Chuang, Huei-Nuan Huang, Chi-Tung Yeh, Wen-Tsung Tseng, and Jeng-Yuan Lai – Siliconware Precision Industries Co., Ltd.
8. ***Development of 300 mm TSV Interposer with Redistribution Layers on Both Sides Using MEMS Processes***
S. Yoshimi, K. Fujimoto, and M. Akazawa – Dai Nippon Printing Co., Ltd., NMEMS Tech. Research Org.; H. Matsumoto, H. Mawatari, and K. Suzuki – Dai Nippon Printing Co., Ltd.; T. Itoh and R. Maeda – NMEMS Tech. Research Org.
9. ***Optical Transceiver Sub-System Package Based on SiOB with 8×14Gbps Two-Way Bandwidth***
Fengman Liu, Binbin Yang, Baoxia Li, Haidong Wang, and Lixi Wan – Institute of Microelectronics, Chinese Academy of Sciences
10. ***Understanding Loss Mechanisms of Passive Interconnects with Innovative/Cost Effective Structure Implementations for Supporting 28Gbps and Beyond Transmission***
Namhoon Kim, Joong-Ho Kim, Ray Anderson, Paul Wu, and Suresh Ramalingam – Xilinx, Inc.
11. ***Numerical Comparison of the Thermal Performance of 3D Stacking and Si Interposer Based Packaging Concepts***
H. Oprins, B. Vandevelde, M. Badaroglu, M. Gonzalez, G. Van der Plas, and E. Beyne – IMEC
12. ***Investigation of Modern Electrically Conductive Adhesives for Die-Attachment in Power Electronics Applications***
Johanna Ocklenburg and Jürgen Wilde – University of Freiburg; Eugen Rastjagaev – Infineon Technologies Austria AG
13. ***Shape Engineering of the Fillers in Stretchable, Electrically Conductive Adhesives: Its Effect on Percolation and Conductivity Change During Stretching***
Zhuo Li, Kristen Hansen, and Kyoung-Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
14. ***Electrochemically Etched TSV for Porous Silicon Interposer Technologies***
Paolo Nenzi, Konstantin Kholostov, Rocco Crescenzi, and Marco Balucani – University of Rome; Hanna Bondarenka and Vitaly Bondarenko – BSUIR
15. ***Role of FBEOL Al Pads and Hard Dielectric for Improved Mechanical Performance in Lead-Free C4 Products***
E. Misra, T. Daubenspeck, T. Wassick, K. Tunga, D. Questad, G. Osborne, T.M. Shaw, and K. McLaughlin – IBM Corporation
16. ***Modeling and Simulation of the Comb Structure in the Presence of Imperfections***
Zhang Luo, Sheng Liu, Gang Cao, and Xiaojie Chen – Huazhong University of Science & Technology, Wuhan National Laboratory for Optoelectronics
17. ***Realization of Ultra-Low Power I/O***
L. Shan, T. Dickson, Y. Kwark, C. Baks, D. Becker, R. Krabbenhoft, and T. Chainer – IBM Corporation; S. Mueller – TU Hamburg; M. Hoshino, J. Kodemura, and M. Hashimoto – Zeon Corporation; T. Jimbo and C. Blatt – Zeon Chemicals
18. ***Assembly Level Digital Image Correlation under Reflow and Thermal Cycling Conditions***
W.C. Ralph – Southern Research Institute; G.F. Raiser – Medtronic, Inc.
19. ***Thermo-Mechanical Simulations of a Copper to Copper Direct Bonded 3D TSV Chip-Package Interaction Test Vehicle***
Ah-Young Park, Daniel Ferrone, Stephen Cain, Dae Young Jung, Bruce T. Murray, and Seungbae Park – SUNY Binghamton; Klaus Hummler – SEMATECH
20. ***Characterization and Modeling of Copper TSVs for Silicon Interposers***
D. Malta, C. Gregory, M. Lueck, J. Lannon, J. Lewis, and D. Temple – RTI International; P. DiFonzo – U.S. Department of Defense; F. Naumann and M. Petzold – Fraunhofer IWM
21. ***Design, Fabrication and Assembly of a Novel Electrical and Microfluidic I/Os for 3D Chip Stack and Silicon Interposer***
Li Zheng, Yue Zhang, and Muhannad S. Bakir – Georgia Institute of Technology
22. ***Homogenization of TSV Interposer and Quick Assessment of Its Thermomechanical Influence on 3D Packages***
Cheng-Fu Chen – University of Alaska, Fairbanks
23. ***Post Assembly Warpage Prediction Using Refined Zigzag Element***
Bahattin Kilic – Intel Corporation; Atila Barut and Erdogan Madenci – University of Arizona
24. ***Atomistic Study of Welding of Carbon Nanotubes onto Metallic Substrates***
Xiaohui Song – Wuhan National Lab for Optoelectronics, Henan Academy of Sciences; Mingxiang Chen and Zhinyin Gan – Wuhan National Lab for Optoelectronics

Friday, May 31
Session 41: Student Interactive Presentations 1
8:30 a.m. - 10:30 a.m.
Committee: Interactive Presentations
Chelsea 3

Session Co-Chairs:
Mark Poliks – Endicott Interconnect Technologies, Inc.
Mark Eblen – Kyocera America, Inc.

1. ***Analyses of Propagation Behavior of Crack at Interface between Die-Attach and Cu Base and Cracks' Effects on Reliability of High Brightness Light-Emitting Diode (LED)***
Xiang Gao and Sheng Liu – Huazhong University of Science & Technology, Wuhan National Laboratory for Optoelectronics; Xin Wu and Yong Xu – Wayne State University
2. ***Packaging and Sensing Platform using Opto-Electronic Zinc Oxide Nano-Heterostructure Integration***
Anurag Gupta, Mitchell Spryn, Bruce Kim, and Susan Burkett – University of Alabama; Eugene Edwards, Christina Brantley, and Paul Ruffin – U.S. Army AMRDEC
3. ***Fluxless Tin Bonding of Silicon Chips to Iron***
Shou-Jen Hsu and Chin C. Lee – University of California, Irvine
4. ***A Small Flat-Plate Vapor Chamber Fabricated by Copper Powder Sintering and Diffusion Bonding for Cooling Electronic Packages***
Run Hu, Tinghui Guo, Xiaolei Zhu, Sheng Liu, and Xiaobing Luo – Huazhong University of Science & Technology
5. ***Buffered Distributed Spray MOCVD Reactor for LED Production***
Shaolin Hu and Zhiyin Gan – Huazhong University of Science & Technology, Guangdong RealFaith Semiconductor Equipment Co., Ltd.; Sheng Liu – Huazhong University of Science & Technology
6. ***Injection Molding of a WDM System for POF Communication***
S. Höll, M. Haupt, and U.H.P. Fischer – Harz University of Applied Studies and Research
7. ***TSV Electrical and Mechanical Modeling for Thermo-Mechanical Delamination***
Kaushal Kannan, Sukeshwar Kannan, Bruce Kim, and Susan Burkett – University of Alabama; Suresh Sitaraman – Georgia Institute of Technology
8. ***D-Band Characterization of Co-Planar Wave Guide and Microstrip Transmission Lines on Liquid Crystal Polymer***
Wasif T. Khan, A. Cagri Ulusoy, and John Papapolymerou – Georgia Institute of Technology
9. ***Optimization of Underfill Material for Better Reliability and Thermal Behavior of 3D Packages with TSVs***
Yeonsung Kim and S.B. Park – SUNY, Binghamton
10. ***3D Modeling of High Count Fine Pitch Flip Chip Assemblies***
W. Kpobie – Ecole Nationale d'Ingénieurs de Metz (ENIM), CEA-LETI; N. Bonfoh, C. Dreistadt, and P. Lipinski – Ecole Nationale d'Ingénieurs de Metz (ENIM); M. Fendler – CEA-LETI
11. ***High Aspect Ratio Sub-100 nm Silicon Vias (SVs) by Metal-Assisted Chemical Etching (MaCE) and Copper Filling***
Liyi Li – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
12. ***Stretchable/Printed RF Devices Via High-Throughput, High-Definability, Soft-Lithography Fabrication***
Zhuo Li, Liyi Li, Kyoung-Sik Moon, Fan Cai, and John Papapolymerou – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
13. ***Stress Analysis in 3D IC Having Thermal Through Silicon Vias (TTSV)***
Shabaz Basheer Patel, Tamal Ghosh, Asudeb Dutta, and Shivgovind Singh – Indian Institute of Technology Hyderabad
14. ***Electronic Packages for High Pressure Applications: A Dome-Shaped Cavity Design***
Eric Jian Rong Phua – Institute of Microelectronics; Riko I Made, Ahmed Sharif, Chee Cheong Wong, Zhong Chen, Daniel Rhee Min Woo, and Chee Lip Gan – Nanyang Technological University
15. ***3D Chips Can Be Cool: Thermal Study of VeSFET-Based ICs***
Xiang Qiu and Malgorzata Marek-Sadowska – University of California, Santa Barbara; Wojciech Maly – Carnegie Mellon University
16. ***Power Dissipation Analysis for Different Configurations of TSVs at High (GHz) Frequencies***
Aditya Vikram Singh, Divanshu Chaturvedi, Shiv Govind Singh, and Mohammed Zafar Ali Khan – Indian Institute of Technology Hyderabad
17. ***Fabrication of Deep Vias/Grooves as Interconnection Path by Wet Etching for Wafer Level Packaging of GaAs Based Image Sensor***
Shuangfu Wang, Jiaotuo Ye, and Le Luo – Chinese Academy of Sciences
18. ***An Experimental Verified Model for Cu Electrodeposition Simulation for the Filling of High Aspect Ratio Through Silicon Vias***
H. Wu and Z.A. Tang – Dalian University of Technology; Z. Wang, C. Song, D. Yu, and L. Wan – Chinese Academy of Sciences; W. Cheng – Jiangsu R&D Center for Internet of Things
19. ***Fabrication of Gel Glass Containing High Rendering Phosphor Mixture Via Sol-Gel Process for LED Packaging***
Liang Yang, Zhicheng Lv, Mingxiang Chen, and Sheng Liu – Huazhong University of Science & Technology
20. ***Implementation of Semiconducting Nanowires for the Design of THz Detectors***
Xianbo Yang, Amanpreet Kaur, and Premjeet Chahal – Michigan State University
21. ***Study of Low Load and Temperature, High Heat-Resistant Solid-Phase Sn-Ag Bonding with Formation of Ag_3Sn Intermetallic Compound Via Nanoscale Thin Film Control for Wafer-Level 3D-Stacking for 3D LSI***
Kiyoto Yoneta, Ryohei Sato, Yoshiharu Iwata, Koichiro Atsumi, Kazuya Okamoto, and Yukihiro Sato – Osaka University
22. ***A Compact Inductively Coupled Connector for Mobile Devices***
Wenxu Zhao, Peter Gadfort, Evan Erickson, and Paul D. Franzon – North Carolina State University

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Technology Corner Exhibits

Wednesday, May 29, 2013 • 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.
Thursday, May 30, 2013 • 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.

Interactive Presentation Sessions

Wednesday, May 29, 2013 morning Interactive Presentations • 9:00 a.m. - 11:00 a.m.
Wednesday, May 29, 2013 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.
Thursday, May 30, 2013 morning Interactive Presentations • 9:00 a.m. - 11:00 a.m.
Thursday, May 30, 2013 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.
Friday, May 31, 2013 Student Interactive Presentations • 8:30 a.m. - 10:30 a.m.

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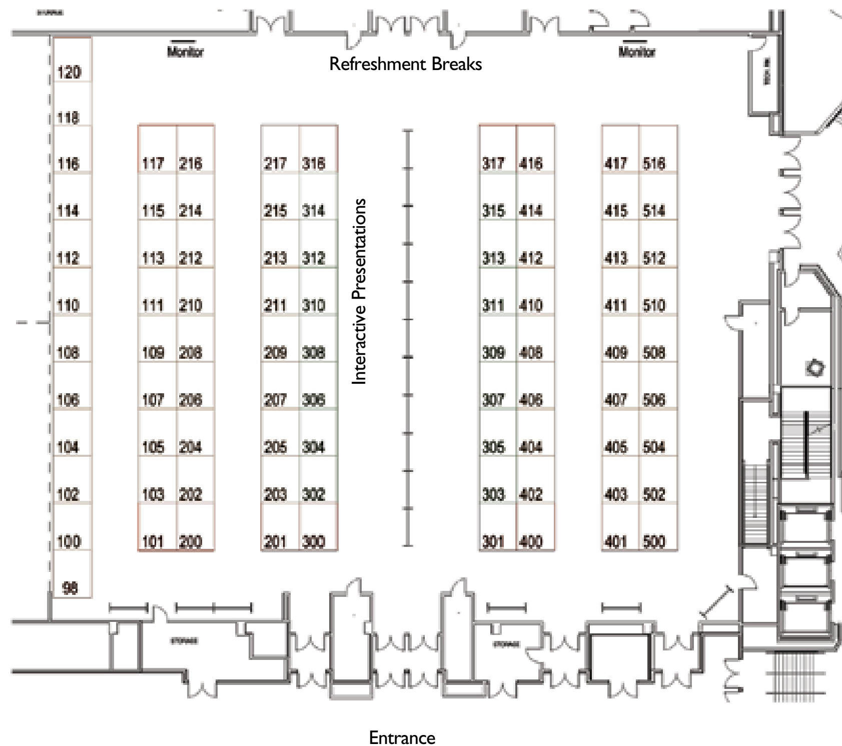

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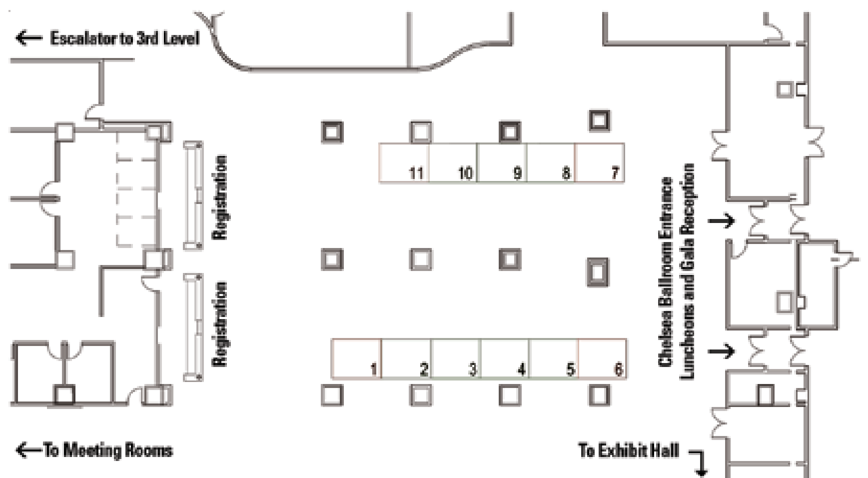

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Fujitsu Interconnect Technologies Limited (FICT), a wholly owned company of Fujitsu Limited of Japan, provides innovative design and manufacturing solutions for package substrates and printed circuit boards (PCBs) to meet the needs of its global customer base. FICT's solutions enable its customers to migrate to newer, complex designs, while reducing manufacturing time and total cost. Multilayer PCB - Advanced technology high-end printed circuit boards (PCBs) design and manufacturing for network systems and high-end servers. FCBGA - Ultra-Thin & High-density wiring structure, applying core layer free, full build-up, and full stacked-via technology.

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HD Microsystems is a joint venture company of Hitachi Chemical and DuPont Electronics specializing in spin-applied polyimide (PI) and polybenzoxazole (PBO) wafer dielectric coatings.HDM will highlight new polymeric materials as well as innovative process technologies for WLP and 3D/TSV applications, including stress buffer materials (SB), redistribution dielectric layers (RDL), wafer bonding adhesives (temporary and permanent) and interlayer dielectrics (ILD).

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Henkel offers a complete range of semiconductor packaging materials designed to meet the requirements of today's challenging devices. Our superior technology known through the leading brands of Ablestik™, Hysol®, and Multicore® includes die attach pastes, dicing die attach films for stacked package applications, Wafer Backside Coating™ die attach solders, liquid encapsulants, package-level underfills, mold compounds, tacky fluxes and solder spheres.

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Worldwide Suppliers of Materials for the Electronics and Semiconductor Market – Heraeus supplies solder paste, sinter paste, fluxes, soft solder wire, solder spheres, solder powders, thermally and electrically conductive adhesives and variety of other adhesives to the package and component assembly markets. Moreover, the Business Unit Bonding Wires provides bonding wires made of gold, aluminum, aluminum alloys and copper, as well as precious and non-precious metal ribbons. The Contact Materials Division of Heraeus offers a wide range of innovative products to address your contact material requirements.

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Hesse Mechatronics, a worldwide company based in Paderborn, Germany, designs and manufactures high speed fine pitch wedge bonders for production of RF, microwave, optoelectronic, military and consumer electronics devices and heavy wire bonders for production of power electronics and automotive devices. The company's fully automatic wedge bonders handle light and heavy wire applications with aluminum and gold round wire from 12.5 micron (.0005) to 500 microns (.020) in diameter, in addition to ribbon wire from 6 x 35 microns up to .3 x 2 mm, including HCR™ (High Current Ribbon). The company's heavy wire bonders also handle copper wire and ribbon. The NEW Bondjet BJ931 High Speed Fully Automatic Dual-Head Wedge Bonder meets the latest technology and flexibility demands for automotive and power electronics applications.

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High Connection Density, Inc. (HCD) is a premier supplier of board-to-board, flex-to-board, and package-to-board solderless connectors for BGA, LGA and socket applications. HCD's SuperButton® and SuperSpring® technology-based products are the perfect solution for projects requiring high frequency, high current and low resistance. Designed for manufacturability, HCD offers its innovative proprietary technology at competitive prices.

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Huntsman Advanced Materials is a leading global supplier of synthetic and formulated polymer systems for customers requiring high performance materials which outperform the properties, functionality and durability of traditional materials. In the electronics market, we provide advanced organic protective solutions to build, structure and assemble printed circuit boards and to encapsulate, insulate and bond electrical and electronic components. Our brands, such as Araldite® adhesive and laminating systems, Probimer® solder masks and Euremelt® hot melt adhesives, are pioneers in the industry, serving customers for more than 50 years. Our customers benefit from sound technical expertise and products that are tailor-made to meet their requirements.

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As the world leader in nanomechanical metrology, Hysitron® is dedicated to the development of next-generation testing solutions for microelectronics characterization. Hysitron provides innovative solutions to industry's most challenging material integration problems with our comprehensive nanomechanical testing suite of techniques and modular metrology platforms that keep you at the forefront of materials reliability. Stop by our booth to learn about our exciting new developments in microelectronics characterization and for in-depth discussions with our applications specialists about our latest testing solutions. Hysitron is continuously redefining what is possible for materials R&D, failure analysis, and process control.

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IBM Microelectronics - a world leader in semiconductor and packaging technology has formed a Packaging Joint Development Ecosystem with leading assembly, materials, and equipment providers. This ecosystem leverages IBM's research and development resources with synergistic skills from partner companies to solve shared challenges and drive industry leadership in semiconductor flip chip packaging. IBM's packaging technologies raise the bar on product performance, power efficiency, integration and reliability. Advances in semiconductor device performance and the transition to environmentally friendly interconnects drive complexity in the design and implementation of appropriate packaging solutions. Increased use of multi-core processors that drive larger die size, greater I/O counts and enhanced cooling requirements have made the co-development of silicon and packaging solutions essential to the successful implementation of both. It's time to differentiate your semiconductor packaging technology….Smarter technology for a Smarter Planet.

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IMAT is a global source for wafers of all sizes with thermal oxide, various metal thin films, patterned photoresist and dry films, plated copper, and other processes. Established in 1995, our staff has met the needs of a wide range of IC manufacturers, equipment vendors, and research facilities. Metal films include Ta, Cu, Ti, Al, W, Pt, Ru, Pd, Au, Ag, Co, Ni and Cr, silicides, and alloys are also available. Photolithography services include mask design and layout for your custom applications or you may select from our library of existing masks. We have established some processes for 450mm substrate sizes such as metal evaporation, anneal, and resist coat. We will be incorporating more capabilities in the near future. Ask us about your requirements.

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Industrial Technology Research Institute (ITRI) celebrates 40 year anniversary in 2013,, is a non-profit organization conducting in applied research and technological services. Electronics and Optoelectronics Research Laboratories (EOL) is one of the core labs , devoting to advanced researches in semiconductor technologies and optoelectronics developments.

EOL has played a key role in Taiwan's prominent electronic and optoelectronic industries by staying tuned with global trends of technology. EOL has successfully empowered Taiwan and Worldwide partners/industries in further enhancing their competitiveness in manufacturing technologies and product developments.

The core competences of EOL are briefly introduced below:
• NVM Technology; • Roll-to-Roll flexible technology & OLED lighting; • Bio-photonic system and 3D Imaging Technology; • LED Optoelectronic Semiconductor Technology; • 3D IC/3D Integration & SiP Packaging Technology on Si/Glass/AlN;
• Power packing and Intelligent power Module.

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TDM (Topography and Deformation Measurement) is a patented INSIDIX technology that helps the development engineer increase the reliability of his products, from simple components to highly complex packaging, and allows the failure analysis engineer to understand more accurately the root causes of failures observed in operations. The TDM operating system combines a powerful, internally developed heating/cooling sequence with a sophisticated optical set-up for 3D topography analysis/warpage measurement under thermal stress of all kinds of materials, components and sub-systems. TDM can impose the same thermal profiles and cycles on the devices that they will actually experience during the production process and during normal use. Throughout the thermal cycle, TDM measures the 3D deformation and warpage related to the imposed thermal stress, thus revealing faults that would likely occur during normal production and use.

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Interconnect Systems, Inc. (ISI) is a leading provider of advanced packaging and interconnect solutions for top-tier OEMs in a wide range of industries including military/aerospace, computing/telecom, medical, industrial, and automotive. ISI pioneered the concept of Next Level Integration, an alternative design path that integrates at the module level rather than the silicon level, resulting in lower production costs and faster time-to-market. ISI's breadth of products includes miniaturized FPGA systems, high density modules, 3D and advanced packaging, IC obsolescence adapters, and standard/custom interconnect solutions.

The company's in-depth design and process development knowledge and extensive manufacturing capabilities allow it to quickly execute on Next Level Integration projects and thus provide a comprehensive turnkey solution for its customers.

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A global leader in semiconductor interconnect solutions, Invensas invents, productizes and acquires novel technology to provide broader and more complete solutions for its customers. The company uses interconnectology to extend its design capabilities from chip-level to board module and system-level, innovating in areas such as mobile computing and communications, memory and data storage, and 3D-IC technologies

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J-DEVICES Corporation is a leading OSAT (Outsourced Semiconductor Assembly and Test) company, providing turnkey semiconductor backend services and expanding service capability with an extremely high growth rate. We are continuously developing the best assembly and testing technology to continue achieving globally competitive cost and contribute to our customers' success. Besides various types of general packaging such as SOP, QFN, QFP, BGA, FBGA, FCBGA, SiP, PoP, MEMS and CIS packages with best-in-class quality, WFOP (Wafer level Fan Out Package) is one of our innovative milestones aligning to the migration of 3D packaging in the future. We provide 2D/2.5D/3D packaging solutions of outstanding performance with competitive cost. Let your imagination run with what and how WFOP will carry into your products.

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JSR's unique THB series of negative tone resists address the needs of metal plating and bumping processes. Excellent plating tolerance and ease of stripping allow for fast processing with excellent exposure throughput and superior process margins. THB cross-links on exposure and is developable in standard TMAH yielding high aspect ratio profiles for film thicknesses from 5 to 100um. JSR's WPR is a thick photosensitive dielectric that is ideal for redistribution layers, stress buffer layers and passivation. Available in positive and negative tone, WPR is patternable and aqueous developable and provides for low residual stress and low cure temperature.

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KYOCERA SLC Technologies (KST) merges cutting-edge design with a wide range of semiconductor packaging technologies to provide advanced routing technology with thin multilayer structure. We offer superior substrates for IC packages and high density circuit boards for high performance, high reliability and good cost performance.

KST created SHDBU substrates for high-speed applications with high I/O count flip chip BGA. SHDBU substrates have high density build-up and CPCORE as a core material CPCORE has features of both multilayer ceramic technology and multilayer organic technology and is flexible in routing design for enhanced electrical performance.

KYOCERA SLC Technologies also provides FC-WSPs in response to the demand for thin and small substrates for markets such as digital handset equipment.

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Metryx manufactures innovative mass metrology equipment for use in semiconductor manufacturing. All microelectronic devices are manufactured through a sequence of steps, adding or removing materials. Patented technology from Metryx enables any mass change in these ultra-thin steps to be determined with unprecedented atomic layer accuracy.

The mass response is used to characterize materials and processes, or is implemented in statistical process control (SPC) of the complete manufacturing sequence. Mass metrology provides a rapid inline measurement on product wafers enabling an increase in test coverage with high throughput. Mass as an SPC response has been adopted by 200mm and 300mm Volume Manufacturers for advanced technology nodes.

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Moldex3D has been providing the professional CAE analysis solution for the plastic injection molding industry since 1995. Moldex3D IC Packaging provides a complete series of molding solutions that help engineers to simulate the complex chip encapsulation process, validate mold design, and optimize process conditions. It helps designers to fully analyze the chip encapsulation process from filling, curing, cooling, to advanced manufacturing demands, such as underfill encapsulation, post-molding annealing, stress distribution, or structural evaluation. Significant molding problems can be predicted and solved upfront, which helps engineers enhance chip quality and prevent potential defects more efficiently. Moldex3D is committed to provide the advanced technologies and solutions for industrial demands, and Moldex3D has extended its worldwide sales and service network to provide local, immediate and professional service.

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For more than 30 years Multitest has been a partner to the international semiconductor industry providing leading solutions for standard IC and sensor test. Multitest offers a comprehensive portfolio of test equipment and accessories that is unique in the industry: gravity, pick & place and strip handlers for standard IC and sensor test, a broad range of Kelvin, RF and fine pitch contactors based on Cantilever and vertical probe technology and finally load boards. Multitest "Plug &Yield™" stands for fully integrated and ideally harmonized set-ups that combine and leverage the strengths of each component. Multitest's products have been awarded with several industry prices. The latest award was for the in-process test solution for 3D packages.

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Nagase ChemteX is a leading company for semiconductor encapsulant of epoxy resin. Our line-up products and applications are as follow, Non-Conductive Paste(NCP) for Fine pitch FC-PKG, Underfill for Pb-free, Liquid Molding Compound(LMC) for FO-PKG like e-WLB and Wafer Process Encapsulated Film(WPEF) for 3D PKG. We can developing for the package of Ultra Low K, Cu Post and 3D(CoW, TSV and TMV).

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NAMICS CORPORATION is a leading source for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components, and solar cells. NAMICS subsidiary, DIEMAT, Inc. located in Byfield, MA, specializes in the development of innovative thermally conductive adhesives and sealing glasses. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Korea, Singapore, and China, NAMICS serves its worldwide customers with enabling products for leading edge applications.

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NANIUM is a world-class provider of semiconductor assembly, packaging and test engineering and manufacturing services, and a leader in 300mm wafer-level packaging (WLP). The company offers in-house capabilities for the entire development chain, from design to multiple packaging technologies, and the flexibility to tailor solutions that respond to the most specific and demanding customer requirements. Since production start in 2010, more than a quarter billion eWLB components have been shipped. NANIUM is continuously developing new solutions, like System-in-Package (SiP) at the wafer level, to stay at the leading edge of this technology. Since end of 2012, WLCSP based on fan-in technologies is complementing the existing fan-out WLP offer, which targets high pin count and high performance products, SiPs and 3D integration.

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Newport is a leading supplier of high precision dispense and assembly equipment for the semiconductor and microelectronics industry offering systems for the manufacture of Microwave, Optical, MCM's and MEM's devices. With over two decades of advanced packaging application experience, Newport products support multiple interconnect technologies, including epoxy die bonding, eutectic attach and flip chip. The ultra-precision Newport MRSI-M3 with 3 micron accuracy, MRSI-M5 with 5 micron accuracy and MRSI-605 Assembly Work Cells specialize in thin die handling and 3D packaging and the Newport MRSI-175Ag Epoxy Dispenser is the leader for high precision conductive epoxy dispensing including 125 micron dots

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Nordson DAGE is the market leading provider of award winning test and inspection systems for mechanical testing of electronic components and is recognized as the industry standard. The 4000PLUS platform compliments the 4000 series test systems, for advanced bondtesting such as wire, lead and ribbon pull, BGA sphere and package fatigue, PCB 3 point bend testing, hot bump pull for PCB pad cratering testing in accordance with IPC9708, and shear testing. The 4000HS high speed bondtester, capable of testing solder bumps in high speed shear and high speed cold bump pull modes, is becoming a viable alternative to board level drop testing. The 4000HS, in addition to total and fractional values , provides bond energy results, proving invaluable for failure mode analysis the detection of lead-free brittle fractures.

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Ormet Circuits, Incorporated (Ormet) is a privately held company, engaged in the design, manufacture, and sale of conductive pastes for use in the manufacture of advanced electronic devices. Ormet pastes are lead-free, highly electrically and thermally conductive and provide good intermetallic joints at relatively low temperatures.

Nippon Steel & Sumikin Chemical Co., Ltd., as a core member of the Nippon Steel & Sumitomo Metal Corp. Group, is the key industry of chemical products fields, which are the products of coal tar chemicals, petroleum chemistry, gasses, synthetic resins and electronics materials. We have developed a high degree of expertise in the application of these products to respond a huge variety of needs in the industrial society.

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Packaging Technologies GmbH (PAC TECH), a group member of NAGASE & CO., Ltd., is comprised of two unique business units:

Advanced Packaging Equipment Manufacturing: Automatic wet chemical lines for high volume electroless NiAu & NiPdAu bumping (PacLine 300 A50), laser solder jetting equipment (SB2-Jet), wafer-level solder ball transfer systems (Ultra-SB2), and laser-assisted flip-chip bonders (Laplace).

Wafer Level Packaging & Bumping Services: Subcontract wafer bumping with electroless Ni/Au or Ni/Pd under-bump-metallization (UBM) for FC or WLCSP solder bumping, as well as NiPdAu for wire bonding. PAC TECH also offers AOI, X-Ray, RDL, Thinning, Backmetal, Laser Marking, Dicing and Tape & Reel.

Headquartered in Nauen, Germany, PAC TECH has 100% subsidiaries: PAC TECH USA - Packaging Technologies Inc. (Silicon Valley, USA) & PAC TECH ASIA Sdn. Bhd. (Penang, Malaysia).

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Palomar Technologies, a former subsidiary of Hughes Aircraft, is the global leader of automated high-accuracy, large work area die attach and wire bond equipment and precision contract assembly services. Customers utilize the products, services and solutions from Palomar Technologies to meet their needs for optoelectronic packaging, complex hybrid assembly and micron-level component attachment.

Palomar Technologies Assembly ServicesTM ("Assembly Services"), located in Carlsbad, CA, is the contract assembly, process development, test and prototyping division of Palomar Technologies. Assembly Services provides process expertise with high-precision die attach, wire bond and component placement services, offering its customers an alternative route to meet complex packaging needs for without investing in capital equipment.

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Pure Technologies manufactures low (0.02, 0.01 cph/cm2), ultra-low (0.005, 0.002 cph/2) and super ultra-low (<0.001 cph/cm2) alpha emitting Tin (Sn), Lead-Free (including all SAC) alloys, Pb and Pb/Sn alloys. These ALPHALO® products are available in various shapes and sizes – ingots, anodes, slugs, pellets, foil, rods, bricks, PbO and SnO powder, etc. for wafer-level packaging, interconnects, and sphere and powder/paste manufacturing. ALPHA-LO® reduces or eliminates soft errors from alpha particle emissions from solders, enhances performance reliability and reduces corporate liability. All materials are guaranteed and certified to be at secular equilibrium and are tested and retested over time before shipping to insure that the alpha emission rate is stable and will not increase over time.

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QualiTau offers a variety of reliability and parametric test equipment for the characterization and development of new materials used in the manufacture of Integrated Circuits. The DSPT 9012 (Desktop Semiconductor Parametric Tester) is a PC Controlled SMU test instrument built specifically for semiconductor device characterization and testing. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection, Dielectric Breakdown, Solder Bump at up to 8 Amps, and Electromigration at test temperatures up to 450C.

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Quik-Pak, a division of Delphon, provides IC packaging and assembly services. The company's newest offering is its OmPP package. These pre-molded QFN packages are cost-effective, come in a variety of sizes and are ideal for prototype or production volume applications. Quik-Pak also specializes in a variety of services that together provide a full turn-key packaging and assembly solution including wafer preparation, die/wire bonding, remolding and marking/branding. Custom assembly services are also offered for Flip Chip, Ceramic Packages, Chip-on-Board, Stacked Die, MEMS, etc

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64th ECTC Call for Papers

First Call For Papers

64th Electronic Components and Technology Conference

www.ectc.net

To be held May 27 - May 30, 2014

at the Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:

3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, electronic (digital, analog, & RF),and optoelectronic & photovoltaic device packaging.

Applied Reliability:

3D package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:

Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:

Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:

Emerging packaging concepts and technologies, emerging 3D packaging concepts, novel approaches to packaging, organic IC & TFT, microfluidics and MEMs, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:

First- and second-level interconnections: designs, structures, processes, performance, reliability, test including TSV, Si interposer, and interconnections for 3D integration, flip chip, solder bumping and Cu-pillar, wafer-level packaging, advanced wirebonds, non-traditional interconnections (e.g. ECA, CNT, graphene, optical, etc), electromigration for 2.5D and 3D, substrates and PCB solutions for the next generation systems, system packaging and heterogeneous integration.

Materials & Processing:

Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 3D.

Modeling & Simulation:

Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, signal and power integrity, fracture and warpage in packages, material and fabrication modeling, first-level and second-level interconnects, high-speed interconnects.

Optoelectronics:

Fiber optical interconnects, active optical cables, parallel optical transceivers, silicon and III-V photonics devices, optical chip-scale and heterogeneous integration, micro-optical system integration and photonic system-in-package, optoelectronic assembly and reliability, materials and manufacturing technology, high-efficiency LEDs and high power lasers, and integrated optical sensors.

Interactive Presentations:

Papers may be submitted on any of the listed major topics; presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentations allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting the theme of an oral session or submitted specifically for interactive presentation, and abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

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Abstracts must be received by October 14, 2013. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/ Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 14, 2013. If you have any questions, contact:

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64th Electronic Components & Technology Conference

Walt Disney World Swan & Dolphin
Lake Buena Vista, Florida, USA • May 27 - 30, 2014

The fun and splendor of Walt Disney World and the greater Orlando area awaits you in 2014. In the heart of the Walt Disney World® Resort, the award-winning Walt Disney World Swan and Dolphin Resort is your gateway to Central Florida's greatest theme parks and attractions. The resort is located in between Epcot® and Disney's Hollywood Studios™, and nearby Disney's Animal Kingdom® Theme Park and Magic Kingdom® Park. Come discover our 17 world-class restaurants and lounges, sophisticated guest rooms with Westin Heavenly Beds® and the luxurious Mandara Spa. Enjoy five pools, two health clubs, tennis, nearby golf, and many special Disney benefits, including complimentary transportation to Walt Disney World Theme Parks and Attractions, and the Extra Magic Hours benefit.

Just minutes from the Walt Disney World Swan and Dolphin Resort is Downtown Disney's West Side and Marketplace. Downtown Disney's West Side showcases top-notch restaurants, a 24-screen AMC Pleasure Island movie theater, and other uncommon shops. Here you'll also find the exquisite Cirque du Soleil La Nouba live entertainment show and the DisneyQuest Indoor Interactive theme park.

Downtown Disney Marketplace provides an appealing place to take a break from Disney Theme Parks and Water Parks. Check out the largest Disney character store in the world. Or, for more of a respite, relax and dine at a lakeside restaurant.

Should you decide to explore outside the Greater Lake Buena Vista area, Orlando boasts other parks and recreation areas tailor made for whatever your pleasure. Favorites include Universal Orlando, SeaWorld, Gatorland, and Winter Park.

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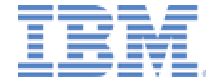

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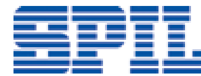

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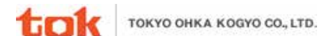

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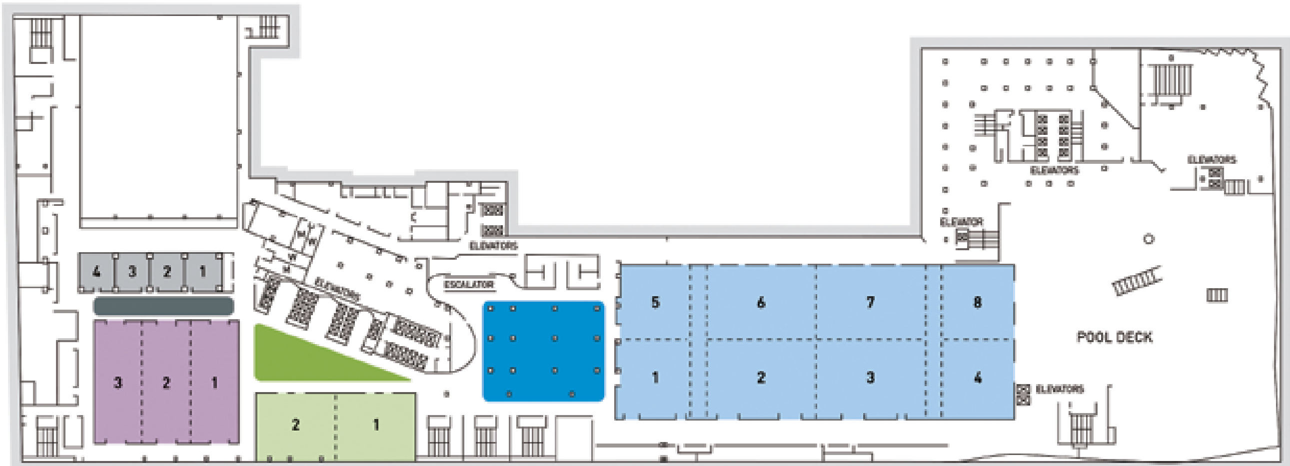


HARMON AVENUE

YALETOWN
YALETOWN COMMONS
NOLITA
MONT-ROYAL
MONT-ROYAL COMMONS
CHELSEA
CHELSEA COMMONS

Conference At A Glance

Monday, May 27, 2013

3:00 p.m. – 5:00 p.m.
Registration – Chelsea Commons, 4th Floor

Tuesday, May 28, 2013

6:45 a.m. – 8:15 a.m.
AM PD Courses Registration Only
Registration – Chelsea Commons, 4th Floor

7:00 a.m. – 7:45 a.m.
PD Courses Instructor and Proctors Briefing & Breakfast
Chelsea 2

7:00 a.m. – 5:00 p.m.
Speakers Prep
Yaletown 3

8:00 a.m. – Noon
AM PD Courses
See page 8 for locations

9:00 a.m. – 5:00 p.m.
iNEMI Roadmap Meeting
Condesa 6, 2nd floor

10:00 a.m. – Noon
Special Session
Condesa 3, 2nd floor

10:00 a.m. – 10:20 a.m.
AM PD Course Break
Mont-Royal Commons & Chelsea Commons

11:00 a.m. – 1:15 p.m.
Conference Registration
PM PD Courses Registration – Chelsea Commons, 4th Floor

Noon
PD Courses Luncheon
Chelsea 2

1:00 p.m. – 5:00 p.m.
Technology Corner Set-up
Chelsea 3 & 4

1:15 p.m. – 5:00 p.m.
Conference Registration
Chelsea Commons, 4th Floor

1:15 p.m. – 5:15 p.m.
PD PM Courses
See page 8 for locations

2:00 p.m. – 4:30 p.m.
Special Modeling Session
Condesa 3, 2nd floor

3:00 p.m. – 3:20 p.m.
PM PD Course Break
Mont-Royal Commons & Chelsea Commons

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Chelsea 2

6:00 p.m. – 7:00 p.m.
General Chair's Speakers Reception (by Invitation)
Outside Pool Area, 4th floor, facing the Las Vegas Strip
(Rain backup: Chelsea 2)

7:30 p.m. – 9:00 p.m.
Panel Session
Mont-Royal 1 & 2, 4th floor

Wednesday, May 29, 2013

6:45 a.m. – 4:00 p.m.
Conference Registration
Chelsea Commons, 4th Floor

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Chelsea 1

7:00 a.m. – 5:00 p.m.
Speakers Prep
Yaletown 3

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4 , 5, 6
See pages 10 thru 11 for Locations

9:00 a.m. – 11:00 a.m.
Session 37: Interactive Presentations 1
Chelsea 3 & 4

9:00 a.m. – Noon
Technology Corner Exhibits
Chelsea 3 & 4

9:15 a.m. – 10:00 a.m.
Refreshment Break
Chelsea 3 & 4

Noon
ECTC Luncheon
Chelsea 1 & 5

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Chelsea 3 & 4

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12 See pages 12 thru 13 for Locations

2:00 p.m. – 4:00 p.m.
Session 38: Interactive Presentations 2
Chelsea 3 & 4

2:45 p.m. – 3:30 p.m.
Refreshment Break
Chelsea 3 & 4

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Chelsea 3 & 4

7:00 p.m. – 9:00 p.m.
Plenary Session
Mont-Royal 1 & 2, 4th floor

Thursday, May 30, 2013

7:00 a.m. – 5:00 p.m.
Speakers Prep
Yaletown 3

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Chelsea 1

7:30 a.m. – 4:00 p.m.
Conference Registration
Chelsea Commons, 4th Floor

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14 thru 15 for Locations

9:00 a.m. – 11:00 a.m.
Session 39: Interactive Presentations 3
Chelsea 3 & 4

9:00 a.m. – Noon
Technology Corner Exhibits
Chelsea 3 & 4

9:15 a.m. – 10:00 a.m.
Refreshment Break
Chelsea 3 & 4

Noon
CPMT Luncheon
Chelsea 1 & 5

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Chelsea 3 & 4

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16 thru 17 for Locations

2:00 p.m. – 4:00 p.m.
Session 40: Interactive Presentations 4
Chelsea 3 & 4

2:45 p.m. – 3:30 p.m.
Refreshment Break
Chelsea 3 & 4

6:30 p.m. – 7:30 p.m.
Gala Reception
Chelsea 1 & 5

8:00 p.m. – 10:00 p.m.
CPMT Seminar
Mont-Royal 1 & 2, 4th floor

Friday, May 31, 2013

7:00 a.m. – 5:00 p.m.
Speakers Prep
Yaletown 3

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Chelsea 1

7:30 a.m. – Noon
Conference Registration
Chelsea Commons, 4th Floor

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18 thru 19 for Locations

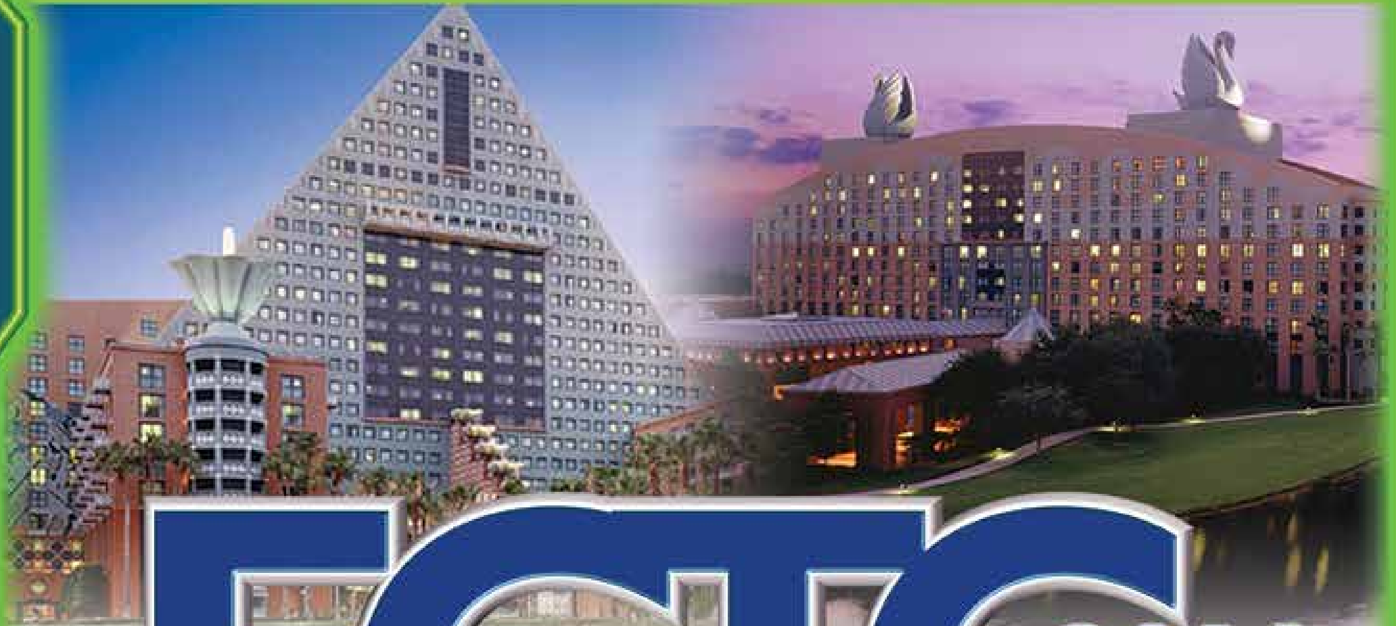
8:30 a.m. – 10:30 a.m.
Student Interactive Presentations
Chelsea 3

9:15 a.m. – 10:00 a.m.
Refreshment Break
Mont-Royal Commons

Noon
Program Chair Luncheon
Chelsea 1 & 5

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20 thru 21 for Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Mont-Royal Commons



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