Conference Program and Exhibitor Listings

Welcome to the electronic packaging's premier conference!

ECTC 2012

The 62nd Electronic Components and Technology Conference

May 29 - June 1, 2012

Sheraton San Diego Hotel & Marina
San Diego, California, USA

Sponsored by:

CPMT — IEEE

Supported by:

ecia — EIA

For more information, visit: www.ectc.net

Welcome from the Mayor of San Diego

JERRY SANDERS
MAYOR

April 4, 2012

Greetings,

Thank you for choosing San Diego for the 62nd Electronic Components and Technology Conference. San Diegans are tremendously proud of their city, a city known worldwide for its warm hospitality and sunny disposition. I'm certain, you, too, will be impressed with all San Diego has to offer.

Best known for its near-perfect climate, natural beauty and fun-filled outdoor recreational activities, San Diego is consistently rated among the nation's top convention destinations and is a perfect match for the 62nd Electronic Components and Technology Conference.

San Diego is characterized by a relaxed and friendly spirit that represents the best of the Southern California lifestyle. The pulse of the city is creative, entrepreneurial and energetic.

Once you've experienced what millions of visitors love about our community, you are destined to fall in love with San Diego. With miles of breathtaking sandy beaches, beautiful parks, renowned family attractions, sophisticated and eclectic dining, rich arts and culture and a dynamic nightlife, San Diego's many charms are impossible to resist.

On behalf of the City of San Diego, I welcome you to America's Finest City!

Sincerely,

JERRY SANDERS
Mayor

CITY ADMINISTRATION BUILDING, 202 C STREET, SAN DIEGO, CALIFORNIA 92101 (619) 236-6330

WELCOME FROM ECTC GENERAL AND PROGRAM CHAIRS

The Executive and Program Committees of the Electronic Components and Technology Conference (ECTC) welcome you to our 62nd conference at the San Diego Sheraton Marina and Resort, San Diego, Calif. This premier international conference is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

The ECTC Program Committee represents a wide range of disciplines and expertise from the electronics industry around the world. We have selected more than 300 high-quality papers to be presented at the conference in 36 oral sessions, four interactive presentation session and one student posters session. The 36 sessions run through the daytime and cover peer-reviewed papers on 3D/TSV, sensors and MEMS, embedded devices, LEDs, co-design, RF packaging, microfluidics, and inkjet, in addition to conventional packaging topics such as advanced packaging technologies, all types and levels of interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, electronic components and simulation. The program committee strives to address new trends as well as ongoing technological issues. Four Interactive Presentation sessions feature technical peer-reviewed presentations presented in a format that enhances and encourages interaction. One student poster session focuses on research conducted in the academia presented by the budding scientists. Authors from companies, research institutes, and universities in nearly 20 countries will present at the ECTC, making it a truly diverse and global conference.

In addition to the technical sessions that are held during the day, four panel sessions focusing on crucial topics presented by industry experts enhance the technical program. In the special session titled "Next Generation Packaging and Integration: The Transformed Role of the Packaging Foundry," session chair Raj Pendse will gather a panel of experts to present and discuss the increased level of integration in the changing landscape and what subcontracted assembly companies are doing to address customer demand. This panel is intended to serve as an excellent roadmap review for the industry where significant portion relies on subcontracted assembly.

The Panel Discussion on Tuesday evening at 7:30 pm, chaired by Rolf Aschenbrenner and Ricky Lee and titled "Power Electronics: A Booming Market," will focus on power electronics from a packaging perspective. The Plenary Session on Wednesday 7:00 pm, chaired by Christopher Bower and titled "Photonics: Expanding Markets and Emerging Technologies," will unveil the less-known world of photonics research and discuss how it can help improve the semiconductor revenues. Thursday evening starts with the Gala Reception at 6:30 pm and is followed by the CPMT Seminar at 8:00 pm, which is titled "Advanced Coreless Package Substrate and Material Technologies" and chaired by Kishio Yokouchi and Venky Sundaram.

The Professional Development Courses (PDC), organized by the PDC Committee chaired by Kitty Pearsall, will be taught on Tuesday (8:00 am-5:30 pm). World-class experts in their fields offer 16 courses on different topics. Participants can catch up on new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the Technology Corner Exhibits where leading companies primarily in the electronics components, materials, and packaging fields exhibit their latest technologies and products. The exhibitors invite you to their reception on Wednesday at 5:30 pm. Along with our receptions and coffee breaks every day, luncheons are another great opportunity to network and discuss technical and business matters. It is our pleasure to announce that Greg Bartlett, the CTO of GLOBALFOUNDRIES will be the invited keynote speaker at the ECTC Luncheon on Wednesday.

The International Electronics Manufacturing Initiative (iNEMI) will host the North American Workshop to solicit input for the 2013 iNEMI roadmap on Tuesday (8:00 am- 6:00 pm).

There is always more than we can explain at the ECTC. Whether you are a manager, engineer, executive or a student, we invite you to experience the exiting developments in electronic components and technology. We would like to take this opportunity to thank our sponsors, exhibitors, authors and speakers, instructors, session chairs, committee members; and arrangement, finance, publication, and publicity chairs, as well as all the volunteers for their support and hard work. We also thank all conference attendees in advance for making the 62nd ECTC a great success. We hope you will like the program and enjoy the conference, and appreciate your feedback.

David McCann
General Chair
GLOBALFOUNDRIES

Senol Pekin
Program Chair
Intel Corporation

WELCOME FROM ECTC SPONSORING ORGANIZATION

This is 2012! There have been many predictions about 2012, including the most devastating one. No matter which version of predictions you believe in, there is one thing for sure: the 62nd Electronic Components and Technology Conference in San Diego will continue the glory from the previous series of ECTC conferences and achieve a big success!

The core of ECTC is its technical program, which typically consists of 36 oral sessions in three full days. Together with two half-day interactive sessions and one student posters session, the whole technical program accommodates approximately 350 papers from authors/presenters all over the world in academia and industry. These papers were selected from a pool of more than 700 abstract submissions, which were reviewed by technical sub-committees that consist of about 150 dedicated experts worldwide in electronic packaging and manufacturing. Such a rigorous procedure ensures the outstanding quality of ECTC technical proceedings. The other three pillars of ECTC are professional development courses, panels, and industrial exhibition. Every year these events attract big crowds for participation. With the conference location in southern California, the 62nd ECTC will undoubtedly maintain its momentum in these three areas.

Starting in 2011, the IEEE Components, Packaging & Manufacturing Technology (CPMT) Society has become the sole sponsor to ECTC. This enables an effective and consistent operation of the conference. Being the president of the sponsoring organization, I would like to extend the warm welcome from IEEE CPMT to all attendees of the 62nd ECTC. I also would like to take this opportunity to thank numerous volunteers who contributed to the success of the 62nd ECTC. There will be a luncheon hosted by IEEE CPMT on Thursday, May 31. Please join us as we extend our hospitality and appreciation.

See you then!
Ricky Lee
President, IEEE CPMT Society

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner Exhibits and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables, particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
The hotel does not allow smoking on it premise. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, or seminars as well. Thank you for your consideration and cooperation.

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote Speaker

Wednesday, May 30, 2012 • Noon
Grande Ballroom

Bridging the Gap between the Silicon and Packaging Worlds

Presenter: Gregg Bartlett
Chief Technology Officer at GLOBALFOUNDRIES

Gregg Bartlett is Chief Technology Officer at GLOBALFOUNDRIES, where he is responsible for the company's technology strategy, advanced node development, technology partnerships, and alliances. Gregg joined GLOBALFOUNDRIES in 2009 after a 25-year career in technical and management positions at Freescale Semiconductor and its predecessor, Motorola's Semiconductor Products Sector.

Immediately prior to joining GLOBALFOUNDRIES, Gregg served as Vice President of Design Technology at Freescale, where he was responsible for design methodology and the creation of design IP and collateral for advanced solutions across high-performance networking, automotive, wireless and analog product markets.

He is a member of the board of directors of the Semiconductor Research Corporation, as well as various consortium governance committees. Gregg received his bachelor's degree in chemical engineering from Kansas State University.

2012 iNEMI Roadmap - North American Workshop

Tuesday, May 29, 2012

Since 1994, iNEMI (the International Electronics Manufacturing Initiative) has been developing a biennial technology roadmap spanning a 10-year horizon. In 2004, iNEMI expanded the initiative to proactively include global input. This year ECTC is hosting one of the several regional meetings intended to solicit input for the 2013 iNEMI Roadmap. Open to all conference attendees.

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk in the Bayview Foyer, Marina Tower of the Sheraton San Diego Hotel & Marina.

Monday, May 28, 2012 – 3:00 p.m. - 5:00 p.m.
(PD Courses & Conference)

Tuesday, May 29, 2012 – 6:45 a.m. - 8:15 a.m.
(AM PD Courses & Special Session Only)

Tuesday, May 29, 2012 – 11:00 a.m. - 1:15 p.m.
(PM PD Courses Only)

Tuesday, May 29, 2012 – 1:15 p.m. - 5:00 p.m.
(Conference)

Wednesday, May 30, 2012 – 6:45 a.m. - 4:00 p.m.

Thursday, May 31, 2012 – 7:30 a.m. - 4:00 p.m.

Friday, June 1, 2012 – 7:30 a.m. - 12:00 p.m.

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses.

Door Registration Fees

Door Registration with Proceedings on USB drive

Joint ITHERM & ECTC	$1,000
IEEE Member Full Registration	$725
IEEE Member Speaker / Session Chair	$625
IEEE Member One Day	$475
IEEE Member Speaker One Day	$350
Non-Member Full Registration	$870
Non-Member Speaker / Session Chair	$625
Non-Member One Day	$475
Non-Member Speaker One Day	$350
Student	$250
Student Speaker	$250
Exhibits Only	$20

Tuesday Professional Development Courses
IEEE Members and Non-Members

Tuesday AM or PM Course with luncheon	$475
Tuesday All-Day Courses with luncheon	$675
Tuesday Student All-Day Courses with luncheon	$125
Extra Luncheon Tickets for each day	$50
Extra Proceedings with Registration	$100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Executive Center 4)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows XP and MS Office 2003.

7:00 a.m. Wednesday thru Friday
(Room Location: Grande Ballroom B)

Speaker Prep Room

Speakers should prepare and review their digital presentations as follows: 7:00 a.m. – 5:00 p.m., Tuesday – Friday (Room Location: Marina 3)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

Companion Hospitality Room

8:00 a.m. - 4:00 p.m.	Wednesday - Thursday (Room Location: 411 & 415 / 4th floor)
8:00 a.m. - Noon	Friday (Room Location: 411 & 415 /4th floor)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to any show or restaurant, or give suggestions for that special night out. The Concierge can help to make your visit to San Diego a memorable one!

Message Center
Please use the hotel switchboard or the ECTC Registration Desk located at the Bayview Foyer to leave and pickup messages. The hotel number is +1-619-291-2900.

Press Room
Press interviews will be scheduled on an as-requested basis. Check at the ECTC Registration Desk (Bayview Foyer) to schedule an interview while onsite. You may also coordinate an interview with conference leadership or presenting technical experts by contacting Eric Perfecto at perfecto@us.ibm.com or +1-845-894-4400.

LUNCHEONS

Tuesday, May 29, 2012 Noon (Grande Ballroom A)

The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, instructors, proctors and PDC committee members.

Wednesday, May 30, 2012 Noon (Grande Ballroom A - C)

The Electronic Components and Technology Conference and the Lucheon Sponsor ASE will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Gregg Bartlett of GLOBALFOUNDRIES.

Thursday, May 31, 2012 Noon (Grande Ballroom A - C)

The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, June 1, 2012 Noon (Grande Ballroom B - C)

The ECTC Program Chair will sponsor a luncheon for conference attendees.

There will be a raffle for attendees.

SPECIAL SESSION, PLENARY SESSION, PANEL SESSION AND CPMT SESSION

SPECIAL SESSION

Tuesday, May 29, 2012 • 10:00 AM – Noon
Nautilus I

Next Generation Packaging and Integration - the Transformed Role of the Packaging Foundry

Chair: Raj Pendse, STATS ChipPAC, Inc.

Speakers:
Robert Darveaux, Amkor Technology
Bill Chen, Advanced Semiconductor Engineering (ASE)
Mike Ma, Siliconware Precision Industries (SPIL)
Steve Anderson, STATS ChipPAC, Inc.
Dan Tracy, SEMI

ECTC PLENARY SESSION

Wednesday, May 30, 2012 • 7:00 - 9:00 p.m.
Harbor Island I & II

Photonics: Expanding Markets & Emerging Technologies

Chair: Christopher Bower, Semprius Inc.

Speakers:
Ashok Krishnamoorthy, Oracle
Jeff Perkins, Yole Development
Sheng Liu, Huazhong University of Science and Technology
Alexander Fang, Aurrion
Timo Aalto, VTT Technical Research Centre of Finland
Frank Libsch, IBM Corporation

ECTC PANEL SESSION

Tuesday, May 29, 2012 • 7:30 - 9:30 p.m.
Harbor Island I & II

Power Electronics - A Booming Market

Co-chair: Rolf Aschenbrenner, Fraunhofer IZM
Co-chair: Ricky Lee, Hong Kong University of Science and Technology

Speakers:
Dan Kinzer, Fairchild Semiconductor Corp.
Klaus-Dieter Lang, Fraunhofer IZM
Lionel Cadix, Yole Development
Ljubisa Stevanovic, GE Global Research
Bernd Roemer, Infineon Technologies AG

CPMT SEMINAR

Thursday, May 31, 2012 • 8:00 PM - 10:00 PM
Harbor Island I & II

Advanced Coreless Package Substrate & Material Technologies

Co-chair: Kishio Yokouchi, Fujitsu Interconnect Technologies Ltd.
Co-chair: Venky Sundaram, Georgia Institute of Technology

Speakers:
Yuji Nishitani, Sony Corp.
Tanaka Kuniyuki, Shinko Electric Industries Co., Ltd.
Takeshi Eriguchi, Asahi Glass Co., Ltd.
Masateru Koide, Fujitsu Advanced Technologies Ltd.

These sessions/seminars are open to all conference attendees.

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 29, 2012

Morning Courses 8:00 a.m. – Noon	Afternoon Courses 1:15 – 5:15 p.m.
Seabreeze **1. Lead-Free Solder Joint Reliability – Material Consideration** Course Leader: Ning-Cheng Lee – Indium Corporation	**Seabreeze** **9. Package Failure Analysis – Failure Analysis and Analytical Tools** Course Leaders: Rajen Dias and Deepak Goyal – Intel Corporation
Harbor Island I **2. Multi-Physics Modeling in IC Packaging and Microsystems** Course Leader: Xuejun Fan – Lamar University	**Harbor Island I** **10. Near Junction Remediation of On-Chip Hot Spots** Course Leaders: Avram Bar-Cohen – University of Maryland; Karl J. L. Geisler – General Dynamics Advanced Information Systems
Marina 2 **3. Wafer Level Chip Scale Packaging (WL-CSP)** Course Leader: Luu Nguyen –Texas Instruments, Inc.	**Marina 2** **11. Technology Advances in 3D-TSV Integration and Packaging of Micro-Nano-Systems** Course Leader: James J.Q. Lu – Rensselaer Polytechnic Institute
Marina 4 **4. 3D Integration: Alternative to Continued Scaling** Course Leader: Philip Garrou – Microelectronic Consultants of NC	**Marina 4** **12. 3D IC Packaging & Integration, and 3D Si Integration** Course Leader: John Lau – Industrial Technology Research Institute
Harbor Island II **5. Polymers/Nano-Composites-Electronic & Photonic Packaging: Recent Advances** Course Leaders: C.P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation	**Harbor Island II** **13. Polymers in Electronic Packaging** Course Leader: Jeffrey Gotro – InnoCentrix, LLC
Harbor Island III **6. Analog and Power Electronics Packaging** Course Leader: Yong Liu – Fairchild Semiconductor Corporation	**Harbor Island III** **14. Flip Chip Technology** Course Leader: Eric Perfecto – IBM Corporation
Marina 6 **7. Fundamental Concepts of Reliability & Mechanics in Electronic Packaging** Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation	**Marina 6** **15. Design for Package Reliability** Course Leaders: Darvin Edwards and Yaoyu Pang – Texas Instruments, Inc.
Spinnaker **8. Methods for Efficient High-Frequency Modeling and Optimization of Interconnections in Electronic Packaging** Course Leaders: Ivan Ndip and Michael Toepper – Fraunhofer IZM	**Spinnaker** **16. IC Package Design Signal & Power Integrity & EMC** Course Leader: Sam Karikalan – Broadcom Corporation

REFRESHMENT BREAKS – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
HARBOR ISLAND FOYER

ECTC STUDENT RECEPTION
Tuesday, May 29, 2012
5:00 - 6:00 p.m.
Executive Center Break Area
Host: Eric Perfecto – IBM Corporation

Students, have you ever wondered how the ECTC technical committees review and select papers? Or just what subjects, content and paper organization make a standout ECTC paper? Then please come to the ECTC Student Reception. You'll have a chance to enjoy some good food and meet with representatives of each technical subcommittee. Don't miss this chance for an inside view of technical subcommittee operations. Sponsored by the IBM Corporation.

GENERAL CHAIR'S SPEAKERS RECEPTION
Tuesday, May 29, 2012
6:00 - 7:00 p.m.
Grande Ballroom A

Invited session chairs and speakers are requested to attend a reception in Grande Ballroom A.

TECHNOLOGY CORNER RECEPTION
Wednesday, May 30, 2012
5:30 - 6:30 p.m.

An Exhibitor Sponsored Reception will be held in the Pavilion, located in the white tented area just outside the Bayview Foyer. All attendees and guests are invited.

62ND ECTC GALA RECEPTION
Thursday, May 31, 2012
6:30 p.m.

All badged attendees and guests are invited to attend a reception outside on the Bayview Lawn area. The rain backup will be Grande Ballroom B - C.

CONTINUING EDUCATION UNITS

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 62nd ECTC.
CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the "IEEE CPMT Professional Development Certificate." Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Courses CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.

2011 ECTC PAPER AWARDS

Best of Conference Papers – 2011

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 61st ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Poster Paper share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

(Session 32, paper 4)

Characterization and Failure Analysis of TSV Interconnects: From Non-Destructive Defect Localization to Material Analysis with Nanometer Resolution

Michael Krause, Frank Altmann, Christian Schmidt, and Matthias Petzold – Fraunhofer IWM; D. Malta and D. Temple – RTI International

Best Poster Paper

(Session 39, paper 9)

Conformal Atomic Layer Deposition (ALD) of Alumina on High Surface-Area Porous Copper Electrodes to Achieve Ultra-High Capacitance Density on Silicon Interposers

Hongtao Kanika Sethi, Himani Sharma, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

Outstanding Papers – 2011

The winning authors for Conference Outstanding Session and Poster Papers receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

(Session 7, paper 4)

Advanced Reliability Study of TSV Interposers and Interconnects for the 28nm Technology FPGA

Bahareh Banijamali, Suresh Ramalingam, Kumar Nagarajan, and Raghu Chaware – Xilinx, Inc.

Outstanding Poster Paper

(Session 38, paper 14)

Maximum Channel Density in Multimode Optical Waveguides for Parallel Interconnections

Takaaki Ishigure, Ryota Ishiguro, Hisashi Uno, and Hsiang-Han Hsu – Keio University

Intel Best Student Paper – 2011

The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 61st ECTC:

(Session 16, Paper 3)

Aging Aware Constitutive Models for SnAgCu Solder Alloys

S. Chavali, Y. Singh, P. Kumar, G. Subbarayan, I. Dutta and D. R. Edwards – Purdue University

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 29, 2012

9:00 a.m. – 5:00 p.m.
iNEMI Meeting
Nautilus 3

9:00 a.m. – 5:30 p.m.
ITRS Assemblies & Packaging Technology Committee
Executive Center 1

5:00 p.m. – 7:00 p.m.
CPMT Region 8 Advisory Committee
Meeting Room 514, 5th floor

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Marina 6

Wednesday, May 30, 2012

7:00 a.m. – 8:00 a.m.
CPMT Materials TC
Meeting Room 514, 5th floor

7:00 a.m. – 8:00 a.m.
CPMT High-Density Board Packaging TC
Meeting Room 511, 5th floor

4:30 p.m. – 5:30 p.m.
CPMT Technical Committee Chairs
Meeting Room 518, 5th floor

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, May 31, 2012

6:45 a.m. – 7:45 a.m.
CPMT Transactions Editors / AEs
Marina 2

7:00 a.m. – 8:00 a. m.
CPMT Education TC
Meeting Room 514, 5th floor

5:30 p.m. – 6:30 p.m.
ECTC 2013 Program Committee Meeting
Harbor Island III

8:00 p.m.
62nd ECTC Governing/Executive Committee Reception
General Chair's Suite
(by invitation only)

Friday, June 1, 2012

7:00 a.m. – 8:00 a.m.
CPMT RF & Wireless TC
Marina 2

7:00 a.m. – 8:00 a.m.
CPMT Nano Packaging TC
Meeting Room 514, 5th floor

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Executive Center 3B

Program Sessions: Wednesday, May 30, 8:00 a.m. - 11:40 a.m.

Session 1: 3D Interconnect: Bonding and Assembly	Session 2: Next Generation Packaging Reliability	Session 3: MEMS Integration and Processing
Committee: Interconnections	**Committee: Applied Reliability**	**Committees: Emerging Technologies / Electronic Components & RF**
Harbor Island II	**Harbor Island I**	**Harbor Island III**
Session Co-Chairs: **Changqing Liu – Loughborough University** **James Lu – Rensselaer Polytechnic Institute**	**Session Co-Chairs:** **Sridhar Canumalla – Microsoft Corporation** **Jeffrey Suhling – Auburn University**	**Session Co-Chairs:** **John Cunningham – Oracle** **P. Markondeya Raj – Georgia Institute of Technology**
1. ***8:00 a.m. – Structural Design, Process, and Reliability of a Wafer-Level 3D Integration Scheme with Cu TSVs based on Micro-Bump/ Adhesive Hybrid Wafer Bonding*** C.T. Ko, Z.C. Hsiao, P.S. Chen, J.H. Huang, H.C. Fu, Y.J. Huang, C.W. Chiang, C.K. Lee, H.H. Chang, W.L. Tsai, and Y.H. Chen – ITRI; Y.J. Chang – National Chiao Tung University	1. ***8:00 a.m. – Board Level Solder Joint Assembly and Reliability for Ultra Thin BGA Packages*** Mohammad M. Hossain, Srinivasa R. Aravamudhan, Marilyn Nowakowski, Xiaoqing Ma, Satyajit S. Walwadkar, Vijay Kulkarni, and Sriram Muthukumar – Intel Corporation	1. ***8:00 a.m. – Electronic Packaging of Sensors for Lower Limb Prosthetics*** J. Kelly Lee and Nancy Stoffel – College of Nanoscale Science and Engineering; Kevin Fite – Clarkson University
2. ***8:25 a.m. – Evaluation of 3D Interconnect Routing and Stacking Strategy to Optimize High Speed Signal Transmission for Memory on Logic*** J. Roullard, S. Capraro, T. Lacrevaz, C. Bermond, G. Houzet, and B. Flechet – Université de Savoie; A. Farcy – STMicroelectronics; J. Charbonnier, C. Fuchs, C. Ferrandon, and P. Leduc – CEA-LETI	2. ***8:25 a.m. – Safe Working Process Strain Limits for Large Area Array Packages: Observations from Spherical Bend Testing*** John McMahon, Brian Gray, and Brian P. Standing – Celestica	2. ***8:25 a.m. – Cost Effective Thin Film Packaging for Wide Area MEMS*** J.L. Pornin, D. Saint-Patrice, C. Gillot, E. Lagoutte, M. Pellat, and S. Fanget – CEA-LETI
3. ***8:50 a.m. – Study of Low Temperature and High Heat-Resistant Fluxless Bonding via Nanoscale Thin Film Control toward Wafer-Level Multiple Chip Stacking for 3D LSI*** Eiji Morinaga, Yuichi Oka, Hiroaki Nishimori, Haruhiko Miyagawa, Ryohei Satoh, Yoshiharu Iwata, and Ryota Kanezaki – Osaka University	3. ***8:50 a.m. – Board Level Drop Test Modeling*** Masazumi Amagai and Jang Seungmin – Texas Instruments, Inc.	3. ***8:50 a.m. – Low Temperature Sealing Process for Vacuum MEMS Encapsulation*** D. Saint-Patrice, J.L. Pornin, B. Savornin, G. Rodriguez, S. Danthon, and S. Fanget – CEA-LETI
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Pavilion)		
4. ***10:00 a.m. – High Density Metal-Metal Interconnect Bonding with Pre-Applied Fluxing Underfill*** Christopher Gregory, Matthew Lueck, Alan Huffman, John M. Lannon, Jr., and Dorota S. Temple – RTI International	4. ***10:00 a.m. – Methods for Reliability Assessment of MEMS Devices – Case Studies of a MEMS Microphone and a 3-Axis MEMS Gyroscope*** J. Hokka, J. Raami, H. Hyvönen, M. Broas, J. Makkonen, J. Li, T. Mattila, and M. Paulasto-Kröckel – Aalto University	4. ***10:00 a.m. – On-Chip THz 3D Antennas*** Paolo Nenzi, Francesco Tripaldi, Volha Varlamava, Fabrizio Palma, and Marco Balucani – University of Rome
5. ***10:25 a.m. – Characterization of a Novel Fluxless Surface Preparation Process for Die Interconnect Bonding*** Eric F. Schulte, Keith A. Cooper, and Matthew Phillips – SET North America; Subhash L. Shinde – Sandia National Laboratory	5. ***10:25 a.m. – Stress Evolution in an Encapsulated MEMS Package Due to Viscoelasticity of Packaging Materials*** Seungbae Park, Dapeng Liu, Yeonsung Kim, and Hohyung Lee – SUNY Binghamton; Sam Zhang – Analog Devices, Inc.	5. ***10:25 a.m. – A CMOS Embedded RF-MEMS Tunable Capacitor for Multi-Band/Multi-Mode Smartphones*** Y. Kurui, H. Yamazaki, Y. Shimooka, T. Saito, E. Ogawa, T. Ogawa, T. Ikehashi, Y. Sugizaki, and H. Shibata – Toshiba Corporation
6. ***10:50 a.m. – Development of Anhydride-Based NCFs for Cu/Sn-Ag Eutectic Bonding and Process Optimization for Fine Pitch TSV Chip Stacking*** Ji-Won Shin, Yong-Won Choi, Young Soon Kim, and Kyung-Wook Paik – KAIST; Un Byung Kang, Young Kun Jee, and Ji Hwan Hwang – Samsung Electronics Company, Ltd.	6. ***10:50 a.m. – Reliability Analyses on a TSV Structure for CMOS Image Sensor*** Ben-Je Lwo and Chung-Yen Ni – National Defense University	6. ***10:50 a.m. – High Power Laminate MEMS RF Switch*** Sung Jun Kim, Yang Zhang, Minfeng Wang, Mark Bachman, and G.P. Li – University of California, Irvine
7. ***11:15 a.m. – "Dual-Purpose" Remateable Conductive Ball-in-Pit Interconnects for Chip Powering and Passive Alignment in Proximity Communication Enabled Multi-Chip Packages*** Hiren D. Thacker, Ivan Shubin, Ying Luo, Kannan Raj, James G. Mitchell, Ashok V. Krishnamoorthy, and John E. Cunningham – Oracle	7. ***11:15 a.m. – Dynamic Bending Test Analysis of Inkjet-Printed Conductors on Flexible Substrates*** Eerik Halonen, Aki Halme, Tapio Karinsalo, Pekka Iso-Ketola, Matti Mäntysalo, and Riku Mäkinen – Tampere University of Technology	7. ***11:15 a.m. – A Novel Electrostatic Radio Frequency Micro Electromechanical Systems (RF MEMS) with Prognostics Function*** Yunhan Huang, Michael Osterman, and Michael Pecht – University of Maryland

Program Sessions: Wednesday, May 30, 8:00 a.m. - 11:40 a.m.

Session 4: Signal and Power Analysis

Committee:
Modeling & Simulation

Nautilus 1

Session Co-Chairs:
Henning Braunisch – Intel Corporation
Michael Lamson – Consultant

1. ***8:00 a.m. – The Design of Higher-Order Reference Voltage Generation Circuits for Single-Ended Memory Interfaces***
   Wendem T. Beyene – Rambus, Inc.

2. ***8:25 a.m. – Efficient and Accurate Modeling of Effective Medium for Interconnects in Lossy Shielded Layered Medium using Fast Convergent Series***
   Sidharath Jain and Jiming Song – Iowa State University; Telesphor Kamgaing and Yidnekachew Mekonnen – Intel Corporation

3. ***8:50 a.m. – System-Level SoC Near-Field (NF) Emissions: Simulation to Measurement Correlation***
   Rajen Murugan, Souvik Mukherjee, Minhong Mi, Lionel Pauc, and Claudio Girardi – Texas Instruments, Inc.; Dipanjan Gope, Daniel de Araujo, Swagato Chakraborty, and Vikram Jandhyala – Nimbic Inc.

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Pavilion)

4. ***10:00 a.m. – Statistical Analysis of Inter-Symbol-Interference and Crosstalk for Coding Buses***
   Yu Chang, Dan Oh, and Ralf Schmitt – Rambus, Inc.

5. ***10:25 a.m. – Simulation Challenges in Designing High Speed Serial Links***
   Arun Reddy Chada – Missouri University of Science and Technology; Bhyrav Mutnury, Douglas Wallace, Douglas Winterberg, and Minchuan Wang – Dell Inc.; Antonio Ciccomancini Scogna – CST of America, Inc.

6. ***10:50 a.m. – A New Approach to Deriving Packaging System Statistical Eye Diagram Based on Parallel Non-Linear Transient Simulations using Multiple Short Signal Bit Patterns***
   Zhaoqing Chen, Wiren Dale Becker, and George Katopis – IBM Corporation

7. ***11:15 a.m. – Optimizing the Timing Center for High-Speed Parallel Buses***
   Dan Oh, Arun Vaidyanath, Chris Madden, and Yohan Frans – Rambus, Inc.; Woopoung Kim – Qualcomm, Inc.

Session 5: LEDs and Emerging Optoelectronics Integration

Committee:
Optoelectronics

Nautilus 3

Session Co-Chairs:
Alex Rosiewicz – EM4
Hiren Thacker – Oracle Labs, Oracle

1. ***8:00 a.m. – High Power LED Subassemblies for Automotive Front Light Application***
   G. Elger, B. Spinger, R. Peters, N. Benter, H. Willwohl, S. Honma, U. Bohnenkamp, A. Stolarski, M. Sikkens, A. Emmerich, and H. Gijsbers – Philips Technology GmbH; N. Lesch – Philips Lumileds

2. ***8:25 a.m. – Application Specific LED Packaging for Automotive Forward-Lighting Application and Design of Whole Lamp Module***
   Fei Chen, Zhangming Mao, Xing Fu, Cao Li, Mengxiong Zhao, and Sheng Liu – Huazhong University of Science and Technology; Kai Wang – Guangdong Real Faith Optoelectronics, Inc.

3. ***8:50 a.m. – Index Matched Fluidic Packaging of High Power UV LED Clusters on Aluminum Substrates for Improved Optical Output Power***
   Marc Schneider, Benjamin Leyrer, Christian Herbold, Stefan Maikowske, and Jürgen Brandner – Karlsruhe Institute of Technology

4. ***10:00 a.m. – Advanced Thin Glass Based Photonic PCB Integration***
   Henning Schröder and Lars Brusberg – Fraunhofer IZM; Norbert Arndt-Staufenbiel and Klaus-Dieter Lang – TU Berlin; Karim Richlowski and Christian Ranzinger – Contag GmbH

5. ***10:25 a.m. – A Laminate Cantilever Waveguide Optical Switch***
   Jonas Tsai, Arthur Yang Zhang, G.P. Li, and Mark Bachman – University of California, Irvine

6. ***10:50 a.m. – Pick and Align–High Precision Active Alignment of Optical Components***
   Michael Leers, Matthias Winzen, Erik Liermann, Heinrich Faidel, Thomas Westphalen, Joern Miesner, Joerg Luttmann, and Dieter Hoffmann – Fraunhofer Institute for Laser Technology ILT

7. ***11:15 a.m. – Fabrication of Low Cost Wafer-Level Micro-Lens Arrays with Spacers using Glass Molds by Combining a Chemical Foaming Process (CFP) and a Hot Forming Process (HFP)***
   Shunjin Qin, Jintang Shang, Tingting Wang, Wenlin Kuai, and Wenlong Wei – Southeast University; Li Zhang and Chiming Lai – Jiangyin Changdian Advanced Packaging Co. Ltd.; Siyuan Lv – Nanjing Foreign Language School

Session 6: Novel Interconnections

Committee:
Interconnections

Nautilus 5

Session Co-Chairs:
James E. Morris – Portland State University
Tom Gregorich – MediaTek

1. ***8:00 a.m. – Metal-Coated Mono-Sized Polymer Core Particles for Fine Pitch Flip-Chip Interconnects***
   Mark W. Sugden, Changqing Liu, David Hutt, and David Whalley – Loughborough University; Helge Kristiansen – Conpart A.S.

2. ***8:25 a.m. – THz Ribbon Waveguides using Polymer-Ceramic Nanocomposites***
   Xianbo Yang and Premjeet Chahal – Michigan State University

3. ***8:50 a.m. – Thermocompression Bonding of Ag-MWCNTs Nanocomposite Films as an Alternative Die-Attach Solution for High-Temperature Packaging of SiC Devices***
   Vanessa Smet, Mamun Jamal, Alan Mathewson, and Kafil M. Razeeb – Tyndall National Institute

4. ***10:00 a.m. – Novel Interconnect Methodologies for Ultra-Thin Chips on Foils***
   A. Sridhar, H. Fledderus, R.H.L. Kusters, and J. van den Brand – TNO/Holst Centre; M. Cauwe – IMEC

5. ***10:25 a.m. – Gold Passivated Mechanically Flexible Interconnects (MFIs) with High Elastic Deformation***
   Chaoqi Zhang, Hyung Suk Yang, and Muhannad S. Bakir – Georgia Institute of Technology

6. ***10:50 a.m. – Microsolder/Adhesive Hybrid Joints for High-Density, High-Power, High-Reliability, and Reworkable Module Interconnection in Mobile Phones***
   Kiwon Lee and Kyung-Wook Paik – KAIST; Ilkka J. Saarinen and Lasse Pykari – Nokia Corporation

7. ***11:15 a.m. – Hybrid Au-Underfill Resin Bonding with Lock-and-Key Structure***
   Masatsugu Nimura, Jun Mizuno, and Shuichi Shoji – Waseda University; Akitsu Shigetou – National Institute for Materials Science; Katsuyuki Sakuma – IBM Corporation; Hiroshi Ogino and Tomoyuki Enomoto – Nissan Chemical Industries

Program Sessions: Wednesday, May 30, 1:30 p.m. - 5:10 p.m.

Session 7: Interposer Technology

Committee:
Advanced Packaging

Harbor Island II

Session Co-Chairs:
Christopher Bower – Semprius, Inc.
John Knickerbocker – IBM Corporation

1. ***1:30 p.m. – Integrating Through-Silicon Vias with Solder Free, Compliant Interconnects for Novel, Large Area Interposers***
   Ivan Shubin, Alex Chow, Hiren D. Thacker, Kannan Raj, Ashok V. Krishnamoorthy, James G. Mitchell, and John E. Cunningham – Oracle; Eugene M. Chow and Dirk DeBruyker – Palo Alto Research Center (PARC); Koji Fujimoto – DNP America, LLC

2. ***1:55 p.m. – Process Integration and Testing of TSV Si Interposers for 3D Integration Applications***
   J. Lannon Jr., A. Hilton, A. Huffman, M. Lueck, E. Vick, S. Goodwin, G. Cunningham, D. Malta, C. Gregory, and D. Temple – RTI International

3. ***2:20 p.m. – High Density and Low-Cost Silicon Interposer using Thin-film and Organic Lamination Processes***
   Jong-Min Yook, Jun Chul Kim, Se-Hoon Park, Jong-In Ryu, and Jong Chul Park – Korea Electronics Technology Institute

4. ***3:30 p.m. – Assembly and Reliability Challenges in 3D Integration of 28nm FPGA Die on a Large High Density 65nm Passive Interposer***
   Raghunandan Chaware, Kumar Nagarajan, and Suresh Ramalingam – Xilinx, Inc.

5. ***3:55 p.m. – TSV Technology for 2.5D IC Solution***
   Meng-Jen Wang, Chang-Ying Hung, Chin-Li Kao, Pao-Nan Lee, Chi-Han Chen, Chih-Pin Hung, and Ho-Ming Tong – Advanced Semiconductor Engineering, Inc.

6. ***4:20 p.m. – Development of Substrates for Through Glass Vias (TGV) For 3DS-IC Integration***
   Aric Shorey, Scott Pollard, Alex Streltsov, Garrett Piech, and Robert Wagner – Corning, Inc.

7. ***4:45 p.m. – Low-Cost and Low-Loss 3D Silicon Interposer for High Bandwidth Logic-to-Memory Interconnections without TSV in the Logic IC***
   Venky Sundaram, Qiao Chen, Gokul Kumar, Fuhan Liu, and Rao Tummala – Georgia Institute of Technology; Yuya Suzuki – Zeon Corporation

Session 8: 3D Reliability

Committees: Applied Reliability / Interconnections

Harbor Island I

Session Co-Chairs:
Vikas Gupta – Texas Instruments, Inc.
Wei-Chung Lo – ITRI

1. ***1:30 p.m. – High-Frequency Measurements of TSV Failures***
   Joohee Kim, Daniel Jung, Jonghyun Cho, Jun So Pak, and Joungho Kim – KAIST; Jong Min Yook and Jun Chul Kim – Korea Electronics Technology Institute

2. ***1:55 p.m. – Electrical Characterization Method to Study Barrier Integrity in 3D Through-Silicon Vias***
   Y.L. Li, D. Velenis, T. Kauerauf, M. Stucchi, Y. Civale, A. Redolfi, and K. Croes – IMEC

3. ***2:20 p.m. – Outstanding and Innovative Reliability Study of 3D TSV Interposer and Fine Pitch Solder Micro-Bumps***
   Bahareh Banijamali, Suresh Ramalingam, Henley Liu, and Myongseob Kim – Xilinx, Inc.

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Pavilion)

4. ***3:30 p.m. – Chip Package Interaction in Micro Bump and TSV Structure***
   Ha-Young You, Yuchul Hwang, Jun-Woo Pyun, Young-Gyun Ryu, and Hyoung-Sub Kim – Samsung Electronics Co., Ltd.

5. ***3:55 p.m. – Effect of Intermetallic Formation on Electromigration Reliability of TSV-Microbump Joints in 3D Interconnect***
   Yiwei Wang, Tengfei Jiang, Jay Im, and Paul S. Ho – University of Texas, Austin; Seung-Hyun Chae, Rajiv Dunne, Yoshimi Takahashi, Kazuaki Mawatari, Philipp Steinmann, and Tom Bonifield – Texas Instruments, Inc.

6. ***4:20 p.m. – Electromigration Behavior of 3D-IC TSV Interconnects***
   Thomas Frank and Lorena Anghel – STMicroelectronics; Stephane Moreau, Lucile Arnaud, Patrick Leduc, and Aurelie Thuaire – CEA-LETI; Cedrick Chappaz – STMicroelectronics

7. ***4:45 p.m. – In-Depth Raman Spectroscopy Analysis of Various Parameters Affecting the Mechanical Stress near the Surface and Bulk of Cu-TSVs***
   Ingrid De Wolf, Veerle Simons, Vladimir Cherman, Riet Labie, Bart Vandevelde, and Eric Beyne – IMEC

Session 9: Sensors and MEMS

Committee:
Advanced Packaging

Harbor Island III

Session Co-Chairs:
Ricky Lee – Hong Kong Univ. of Science & Technology
James Zhang – Micron Technology, Inc.

1. ***1:30 p.m. – Assembly and Packaging Technologies for High Temperature SiC-Sensors***
   Roderich Zeiser, Phillipp Wagner, and Jürgen Wilde – University of Freiburg

2. ***1:55 p.m. – Drop Impact Reliability of MEMS Inertial Sensors with Membrane Suspensions for Mobile Phones***
   Jong Woon Kim, Heung Woo Park, Min Kyu Choi, Won Kyu Jeung, and Jung Won Lee – Samsung Electro-Mechanics Company, Limited

3. ***2:20 p.m. – Chip on Board Development for a Novel MEMS Accelerometer for Seismic Imaging***
   Zhuqing Zhang, Jennifer Wu, Sheldon Bernard, and Robert G. Walmsley – Hewlett Packard Company

4. ***3:30 p.m. – Failsafe Wafer-Level Packaging of a Piezoelectric MEMS Actuator***
   M.A. Matin, K. Ozaki, D. Akai, K. Sawada, and M. Ishida – Toyohashi University of Technology

5. ***3:55 p.m. – Hermetic Wafer-Level Packaging for RF MEMs: Effects on Resonator Performance***
   M. David Henry, K. Douglas Greth, Janet Nguyen, Christopher D. Nordquist, Randy Shul, Mike Wiwi, Thomas A. Plut, and Roy H. Olsson III – Sandia National Laboratories

6. ***4:20 p.m. – 3D MEMS High Vacuum Wafer Level Packaging***
   S. Nicolas, S. Caplet, F. Greco, M. Audoin, X. Baillin, and S. Fanget – CEA-LETI

7. ***4:45 p.m. – Investigation of a Unified LTCC-Based Micromachining and Packaging Platform for High Density/Multifunctional Microsystem Integration***
   Min Miao, Yufeng Jin, Hua Gan, Jing Zhang, Yunsong Qiu, Yang Zhang, Yangfei Zhang, Rui Cao, Zhensong Li, and Chengchen Gao – Peking University; Zhengyi Wang and Fangqing Mu – 43rd Institute of China Electronics Technology Group Corporation

Program Sessions: Wednesday, May 30, 1:30 p.m. - 5:10 p.m.

Session 10: Conductive and Non-Conductive Adhesives

Committee:
Materials & Processing

Nautilus 1

Session Co-Chairs:
Stephanie Potisek – Dow Chemical
Lejun Wang – Medtronic, Inc.

1. ***1:30 p.m. – NCF for Pre-Applied Process in Higher Density Electronic Package Including 3D-Package***
   Kazutaka Honda, Akira Nagai, Makoto Satou, Shinsuke Hagiwara, Satoru Tuchida, and Hidenori Abe – Hitachi Chemical Co., Ltd.

2. ***1:55 p.m. – Non-Conductive Film and Compression Molding Technology for Self-Assembly-Based 3D Integration***
   T. Fukushima, Y. Ohara, J. Bea, M. Murugesan, K.W. Lee, T. Tanaka, and M. Koyanagi – Tohoku University

3. ***2:20 p.m. – Effect of NCF Design for the Assembly of Flip Chip and Reliability***
   Satomi Kawamoto, Masaki Yoshida, Shin Teraki, and Hidenori Iida – NAMICS Corporation

4. ***3:30 p.m. – Highly Conductive, Flexible, Bio-Compatible Poly-Urethane based Isotropic Conductive Adhesives for Flexible Electronics***
   Zhuo Li, Rongwei Zhang, Yan Liu, and Taoran Le – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong

5. ***3:55 p.m. – Low Temperature Curable Anisotropic Conductive Films (ACFs) with Photo-Active Curing Agent (PA-ACFs)***
   Il Kim and Kyung-Wook Paik – KAIST

6. ***4:20 p.m. – Novel Interconnect Materials for High Reliability Power Converters with Operation Temperatures above 150°C***
   Susanne Duch, Thomas Krebs, Yvonne Loewer, Wolfgang Schmitt, and Muriel Thomas – Heraeus Materials Technology GmbH & Co.

7. ***4:45 p.m. – Usability of ECA Materials in High Temperature Sensor Applications***
   Sanna Lahokallio and Laura Frisk – Tampere University of Technology

Session 11: Advanced Flip Chip and Underfill Assembly

Committee:
Assembly & Manufacturing Technology

Nautilus 3

Session Co-Chairs:
Wei Koh – Powertech Technology, Inc.
Tom Poulin – Aerie Engineering

1. ***1:30 p.m. – Differential Heating/Cooling Chip Joining Method to Prevent Chip Package Interaction Issue in Large Die with Ultra Low-k Technology***
   Katsuyuki Sakuma, Kurt Smith, Krishna Tunga, Eric Perfecto, Thomas Wassick, Frank Pompeo, and Jae-Woong Nah – IBM Corporation

2. ***1:55 p.m. – Advanced Flip-Chip Package Solution for 28nm Si Node and Beyond***
   C.S. Liu, C.S. Chen, C.H. Lee, H.Y. Tsai, H.P. Pu, M.D. Cheng, T.H. Kuo, H.W. Chen, C.Y. Wu, M.J. Lii, and Doug C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

3. ***2:20 p.m. – Development of Large Die Fine Pitch Flip Chip BGA using TCNCP Technology***
   Yanggyoo Jung, Minjae Lee, Sunwoo Park, Dongsu Ryu, Youshin Jung, Chanha Hwang, Choonheung Lee, Sungsoon Park, and Miguel Jimarez – Amkor Technology; Myung-June Lee – Altera Corporation

4. ***3:30 p.m. – Low Temperature Touch Down and Suppressing Filler Trapping Bonding Process with Wafer Level Pre-Applied Underfilling Film Adhesive***
   Toshihisa Nonaka, Shoichi Niizeki, Noboru Asahi, and Koichi Fujimaru – Toray Industries, Inc.

5. ***3:55 p.m. – Mixed Pitch BGA (mpBGA) Packaging Development for High Bandwidth-High Speed Networking Devices***
   John Savic, Mohan Nagar, Weidong Xie, Mudasir Ahmad, David Senk, and Anurag Bansal – Cisco Systems, Inc.; Nokibul Islam, Gun Oh Park, Raj Pendse, HangChul Choi, and SangHo Lee – STATS ChipPAC, Ltd.

6. ***4:20 p.m. – Copper Pillar Bumped Sapphire Flip Chip on Leadframe Package Development***
   John Yang – Peregrine Semiconductor

7. ***4:45 p.m. – Ultrasonic-Assisted Thermo-Compression Bonding Method for High-Performance Solder Anisotropic Conductive Film (ACF) Joints***
   Yoo-Sun Kim, Kiwon Lee, and Kyung-Wook Paik – KAIST

Session 12: Solder and Material Characterization

Committee:
Applied Reliability

Nautilus 5

Session Co-Chairs:
Lakshmi N. Ramanathan – Microsoft Corporation
Dongming He – Qualcomm, Inc.

1. ***1:30 p.m. – Investigation of Phosphorous Impact on Lead-Free BGA Solder Joint and Failure Mechanism***
   Ming Sun, Muh-Ren Lin, Tim Chaudhry, and Robert Lutze – Broadcom Corporation

2. ***1:55 p.m. – Aging Impact on the Accelerated Thermal Cycling Performance of Lead-Free BGA Solder Joints in Various Stress Conditions***
   Tae-Kyu Lee and Hongtao Ma – Cisco Systems, Inc.

3. ***2:20 p.m. – High Strain Rate Behaviour of Lead-Free Solders Depending on Alloy Composition and Thermal Aging***
   K. Meier and K.J. Wolter – TU Dresden; F. Kraemer – Saarland University

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Pavilion)

4. ***3:30 p.m. – Effect of Microstructure Evolution on Pb-Free Solder Joint Reliability in Thermomechanical Fatigue***
   Liang Yin and Michael Meilunas – Universal Instruments Corporation; Babak Arfaei, Luke Wentlent, and Peter Borgesen – SUNY, Binghamton

5. ***3:55 p.m. – Sensitivity of Grain Structure and Fatigue Reliability of Pb-Free Solder Joint on the Position in PBGA Packaging Assembly***
   Huili Xu, Woong Ho Bang, and Choong-Un Kim – University of Texas, Arlington; Tae-Kyu Lee – Cisco Systems, Inc.

6. ***4:20 p.m. – Creep Behavior of Joint-Scale Sn1.0Ag0.5Cu Solder Shear Samples***
   Cillian Burke, Jeff Punch, and Maurice Collins – University of Limerick

7. ***4:45 p.m. – Improved Predictions of Lead Free Solder Joint Reliability that Include Aging Effects***
   Mohammad Motalab, Zijie Cai, Jeffrey C. Suhling, Jiawei Zhang, John L. Evans, Michael J. Bozack, and Pradeep Lall – Auburn University

Program Sessions: Thursday, May 31, 8:00 a.m. - 11:40 a.m.

Session 13: 3D TSV Manufacturing	Session 14: Flip Chip Interconnect and Electromigration	Session 15: Innovative Processes and Techniques
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Harbor Island II	**Harbor Island I**	**Harbor Island III**
Session Co-Chairs: **Andy Tseng – Advanced Semiconductor Engineering, Inc.** **Hirofumi Nakajima – Renesas Electronics Co.**	**Session Co-Chairs:** **Lou Nicholls – Amkor Technology, Inc.** **Bernd Ebersberger – Intel Mobile Communications**	**Session Co-Chairs:** **Bing Dang – IBM Corporation** **Hongtao Ma – Bridgelux, Inc.**
1. ***8:00 a.m. – Challenges and Improvements for 3D-IC Integration using Ultra Thin (25µm) Devices*** A. La Manna, T. Buisson, M. Detalle, K.J. Rebibis, D. Velenis, W. Zhang, and E. Beyne – IMEC	1. ***8:00 a.m. – Novel Design and Integration Enhancements in the Final Polymeric Passivation for Improved Mechanical Performance and C4 Electromigration in Pb-Free C4 Products*** E. Misra, T. Daubenspeck, T. Wassick, K. Tunga, G. Lafontant, D. Questad, G. Osborne, and T. Sullivan – IBM Corporation; G.J. Scott – Amkor Technology	1. ***8:00 a.m. – Metrology and Inspection Requirements for 3D Stacking of IC's*** Sandip Halder, Andy Miller, Mireille Maenhoudt, Gerald Beyer, Bart Swinnen, and Eric Beyne – IMEC; David Grant, David Marx, Russ Dudley, and Maurice Ford – Tamar Technology
2. ***8:25 a.m. – Development of Cost-Effective Wafer Level Process for 3D-Integration with Bumpless TSV Interconnects*** K. Fujimoto, N. Maeda, H. Kitada, Y.S. Kim, S. Kodama, and T. Ohba – University of Tokyo; T. Nakamura – Fujitsu Laboratories Ltd.; K. Suzuki – Dai Nippon Printing Co., Ltd.	2. ***8:25 a.m. – High Current-Carrying and Highly-Reliable 30µm Diameter Cu-Cu Area-Array Interconnections without Solder*** Sadia A. Khan, Nitesh Kumbhat, Pulugurtha Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Abhishek Goyal – Indian Institute of Technology Roorkee; Kodai Okoshi – Namics Corporation; Georg Meyer-Berg – Infineon Technologies AG	2. ***8:25 a.m. – Characterization of the Annealing Behavior for Copper-Filled TSVs*** P. Saettler and K.J. Wolter – TU Dresden; M. Boettcher – FhG ASSID
3. ***8:50 a.m. – High Aspect Ratio TSVs Fabricated by Magnetic Self-Assembly of Gold-Coated Nickel Wires*** A.C. Fischer, S.J. Bleiker, N. Somjit, N. Roxhed, T. Haraldsson, G. Stemme, and F. Niklaus – KTH Royal Institute of Technology	3. ***8:50 a.m. – Reliability Study of Lead-Free Flip-Chips with Solder Bumps Down to 30 µm Diameter*** Stefan Härter, Andreas Reinhardt, and Jörg Franke – University of Erlangen-Nuremberg; Rainer Dohle and Jörg Goßler – Micro Systems Engineering GmbH	3. ***8:50 a.m. – Locally Induced Stress in Stacked Ultrathin Si Wafers: XPS and Micro-Raman Study*** M. Murugesan, T. Fukushima, and M. Koyanagi – NICHe; H. Nohira – Tokyo City University; H. Kobayashi – ASET; T. Tanaka – Tohoku University
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Pavilion)		
4. ***10:00 a.m. – Assembly Process and Reliability Assessment of TSV/RDL/IPD Interposer with Multi-Chip-Stacking for 3D IC Integration SiP*** C.J. Zhan, P.J. Tzeng, J.H. Lau, M.J. Dai, H.C. Chien, C.K. Lee, S.T. Wu, K.S. Kao, S.Y. Huang, C.W. Fan, S.C. Chung, and Y.W. Huang – ITRI	4. ***10:00 a.m. – Effect of Joule Heating on Electromigration Reliability of Pb-Free Interconnect*** Minhua Lu, Steven L. Wright, Gerard McVicker, and Sri M. Sri-Jayantha – IBM Corporation	4. ***10:00 a.m. – Process Development for High-Current Electrochemical Deposition of Copper Pillar Bumps*** Wei Koh – Pacrim Technology; Barry Lin – Powetech Technology Inc.
5. ***10:25 a.m. – A CMOS Compatible Chip-to-Chip 3D Integration Platform*** Yuksel Temiz, Michael Zervas, Carlotta Guiducci, and Yusuf Leblebici – École Polytechnique Fédérale de Lausanne	5. ***10:25 a.m. – Mechanically Compliant Lead-Free Solder Metallurgy: The Key Element in Enabling Extreme Low-K Large-Die Flip Chip Devices*** Mengzhi Pang, Matt Kaufmann, Henry Sze, Reza Sharifi, Keith Tan, Chong Wei Neo, Ram Ramakrishna, Sam Karikalan, and Reza Khan – Broadcom Corporation	5. ***10:25 a.m. – Wafer Bumping, Assembly, and Reliability Assessment of µbumps with 5µm Pads on 10µm Pitch for 3D IC Integration*** C.K. Lee, C.J. Zhan, J.H. Lau, Y.J. Huang, H.C. Fu, J.H. Huang, Z.C. Hsiao, S.W. Chen, S.Y. Huang, C.W. Fan, Y.M. Lin, and K.S. Kao – ITRI
6. ***10:50 a.m. – A New Carrier Structure for TSV Thin Wafer Handling*** Ming-Chih Chen, Frank Hsieh, and Dyi-Chung Hu – Unimicron Technology, Inc.	6. ***10:50 a.m. – 40µm Ag-AgIn Flip-Chip Interconnect Process at 180°C*** Wen P. Lin, Chu-Hsuan Sha, and Chin C. Lee – University of California, Irvine	6. ***10:50 a.m. – In-Situ Strain Measurement with Metallic Thin Film Sensors*** Christine Taylor and Suresh K. Sitaraman – Georgia Institute of Technology
7. ***11:15 a.m. – Electrical Testing of Blind Through-Silicon Via (TSV) for 3D IC Integration*** Jui-Feng Hung, John H. Lau, Peng-Shu Chen, Shih-Hsien Wu, Shinn-Juh Lai, Ming-Lin Li, Shyh-Shyuan Sheu, Pei-Jer Tzeng, Zhe-Hui Lin, Tzu-Kun Ku, Wei-Chung Lo, and Ming-Jer Kao – ITRI	7. ***11:15 a.m. – Electromigration Behavior in Low Temperature Flip Chip Bonding*** Kei Murayama and Mitsutoshi Higashi – Shinko Electric Industries Co., Ltd.; Taiji Sakai and Nobuaki Imaizumi – Fujitsu Laboratories Ltd.	7. ***11:15 a.m. – Environmentally Friendly Dry De-Smear of Fine-Via by Ultra High Density Nonequilibrium Atmospheric Pressure Plasma*** Yoshiyuki Iwata and Hajime Sakamoto – Ibiden Co., Ltd.; Keigo Takeda and Masaru Hori – Nagoya University

Program Sessions: Thursday, May 31, 8:00 a.m. - 11:40 a.m.

Session 16: 3D Electrical Analysis	Session 17: Lead Free Solders	Session 18: Innovative Test Methods
Committee: **Modeling & Simulation**	**Committee:** **Materials & Processing**	**Committee:** **Applied Reliability**
Nautilus 1	**Nautilus 3**	**Nautilus 5**
Session Co-Chairs: **Wendem Beyene – Rambus** **Daniel de Araujo – Nimbic, Inc.**	**Session Co-Chairs:** **Mikel Miller – Draper Laboratory** **Dong Wook Kim – Qualcomm, Inc.**	**Session Co-Chairs:** **Darvin R. Edwards – Texas Instruments, Inc.** **Tim Chaudhry – Broadcom Corporation**
1. ***8:00 a.m. – Fast Electrical-Thermal Co-Simulation using Multigrid Method for 3D Integration*** Jianyong Xie and Madhavan Swaminathan – Georgia Institute of Technology	1. ***8:00 a.m. – Electromigration Performance of Printed Sn0.7Cu Bumps with Immersion Tin Surface Finishing for Flip Chip Applications*** Kuei Hsiao Kuo, Jason Lee, Stan Chen, F.L. Chien, Rick Lee, and John Lau – Siliconware Precision Industries Co., Ltd.	1. ***8:00 a.m. – A New Physical Model for Life-Time Prediction of Pb-Free Solder Joints in Electromigration Tests*** Tian Tian, Jung-Kyu Han, Daechul Choi, and King-Ning Tu – University of California, Los Angeles; A.M. Gusak and O.Yu Liashenko – Cherkasy National University
2. ***8:25 a.m. – Accurate Electrical Simulation and Design Optimization for Silicon Interposer Considering the MOS Effect and Eddy Currents in the Silicon Substrate*** Jing Zhou, Lixi Wan, Fengwei Dai, Huijuan Wang, Chongshen Song, Tianmin Du, Yanbiao Chu, Maoyun Pan, Daniel Guidotti, Liqiang Cao, and Daquan Yu – Chinese Academy of Sciences	2. ***8:25 a.m. – The Dependence of the Sn Grain Structure of Pb-Free Solder Joints on Composition and Geometry*** Gregory Parks, Babak Arfaei, Michael Benedict, and Eric Cotts – Binghamton University; Minhua Lu and Eric Perfecto – IBM Corporation	2. ***8:25 a.m. – Generalized Method for Characterizing Mechanical Loads in Mobile Devices*** Ari Lumbantobing and Sanjay Tiku – Microsoft Corporation
3. ***8:50 a.m. – Characterization and Modeling of Si-Substrate Noise Induced by RF Signal Propagating in TSV of 3D-IC Stack*** M. Brocard, P. Le Maître, P. Bar, A. Farcy, P. Coudrain, and N. Hotellier – STMicroelectronics; C. Bermond and T. Lacrevaz – Université de Savoie; R. Anciant, P. Leduc, H. Ben Jamaa, and S. Chéramy – CEA-LETI	3. ***8:50 a.m. – Influence of IMCs Volume Ratio in Microscale Solder Joints on their Mechanical Integrity*** Zhiwen Chen, Bing An and Yiping Wu – Huazhong University of Science & Technology; Changqing Liu and Rob Parkin – Loughborough University	3. ***8:50 a.m. – Interfacial Fracture Properties of Cu-EMC Interfaces at Pressure Cooker Test Conditions*** M. Sadeghinia, K.M.B Jansen, and L.J. Ernst – Delft University of Technology; H. Pape – Infineon Technologies AG
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Pavilion)		
4. ***10:00 a.m. – PDN Impedance and Noise Simulation of 3D SiP with a Widebus Structure*** Hiroki Takatani, Yosuke Tanaka, Yoshiaki Oizono, Yoshitaka Nabeshima, Takafumi Okumura, and Toshio Sudo – Shibaura Institute of Technology; Atsushi Sakai, Shiro Uchiyama, and Hiroaki Ikeda – Association of Super-Advanced Electronics Technologies	4. ***10:00 a.m. – Chemical Reactions of Silver and Indium at 180°C Annealing*** Yuan-Yun Wu, Wen P. Lin, and Chin C. Lee – University of California, Irvine	4. ***10:00 a.m. – Measurement of Die Stresses in Microprocessor Packaging Due to Thermal and Power Cycling*** Jordan Roberts, Mohammad Motalab, Safina Hussain, Jeffrey C. Suhling, Richard C. Jaeger, and Pradeep Lall – Auburn University
5. ***10:25 a.m. – Development of an Optimized Power Delivery System for 3D IC Integration with TSV Silicon Interposer*** Zhe Li, Hong Shi, John Xie, and Arif Rahman – Altera Corporation	5. ***10:25 a.m. – Soldering Reactions under Space Confinement for 3D IC Applications*** C.R. Kao, H.Y. Chuang, W.M. Chen, T.L. Yang, M.S. Kuo, Y.J. Chen, J.J. Yu, and C.C. Li – National Taiwan University	5. ***10:25 a.m. – Flip Chip Power Cycling System Development and Lead Free Bump Power Cycling Reliability*** M.K.C. Wu, H.Y. Pan, L. Lin, C. Chiu, T. Chou, G. Lu, P. Liu, G. Wu, H.P. Pu, H.Y. Tsai, K. Wu and B. Kiang – Taiwan Semiconductor Manufacturing Company, Ltd.
6. ***10:50 a.m. – Modeling of Power Delivery into 3D Chips on Silicon Interposer*** Zheng Xu, Xiaoxiong Gu, Michael Scheuermann, Buckwell C. Webb, and John U. Knickerbocker – IBM Corporation; Kenneth Rose and Jian-Qiang Lu – Rensselaer Polytechnic Institute	6. ***10:50 a.m. – Systematic Investigation of Sn-Ag and Sn-Cu Modified by Minor Alloying Element of Titanium*** W.M. Chen and C.R. Kao – National Taiwan University; S.K. Kang – IBM Corporation	6. ***10:50 a.m. – Development of Early Process Control Indicators for Reliability Drop Test Performance of eWLB Products*** Alexandre Azevedo, André Cardoso, Jorge Teixeira, Oriza Tavares, and Rui Marques – Nanium SA
7. ***11:15 a.m. – Effects of On-Chip Decoupling Capacitors and Silicon Substrate on Power Distribution Networks in TSV-Based 3D-ICs*** Kiyeong Kim, Jun So Pak, and Joungho Kim – KAIST; Hyungdong Lee – Hynix Semiconductor, Inc.	7. ***11:15 a.m. – Synthesis and Characterization of Nanoscaled Solder Material*** Andrej Novikov and Mathias Nowottnick – University of Rostock	7. ***11:15 a.m. – Microstructure and Stress Characterization around TSV using In-Situ PIT-in-SEM*** Gyujei Lee – Hynix Semiconductor, Inc.; Seoul National University; Min-Jae Choi, Suk-Woo Jeon, and Kwang-Yoo Byun – Hynix Semiconductor, Inc.; Dongil Kwon – Seoul National University

Program Sessions: Thursday, May 31, 1:30 p.m. - 5:10 p.m.

Session 19: Thru Via Technologies	Session 20: Co-Design for the 3D Ecosystem	Session 21: Flip Chip Technologies
Committee: Advanced Packaging	**Committee:** Interconnections	**Committee:** Advanced Packaging
Harbor Island II	**Harbor Island I**	**Harbor Island III**
Session Co-Chairs: Rozalia Beica – Lam Research AG; Sam Karikalan – Broadcom Corporation	**Session Co-Chairs:** Gilles Poupon – CEA-LETI-MINATEC; Voya Markovich – Endicott Interconnect Technologies, Inc.	**Session Co-Chairs:** Raj N. Master – Microsoft Corporation; Daniel Baldwin – Engent, Inc.
1. 1:30 p.m. – ***Robust TSV Via-Middle and Via-Reveal Process Integration Accomplished through Characterization and Management of Sources of Variation*** N. Kumar, S. Ramaswami, J. Dukovic, J. Tseng, R. Ding, N. Rajagopalan, B. Eaton, R. Mishra, R. Yalamanchili, Z. Wang, S. Xia, and K. Sapre – Applied Materials, Inc.	1. 1:30 p.m. – ***Effects of Silicon Substrate Coupling Phenomena on Signal Integrity for RF or High Speed Communications in 3D-IC*** E. Eid, T. Lacrevaz, G. Houzet, C. Bermond, and B. Fléchet – Université de Savoie; A. Farcy – STMicroelectronics; F. Calmon – Institute des Nanotechnologies de Lyon; P. Leduc – CEA-LETI	1. 1:30 p.m. – ***Low Cost Cu Column fcPoP Technology*** Hamid Eslampour, YoungChul Kim, SeongWon Park, and TaeWoo Lee – STATS ChipPAC, Inc.
2. 1:55 p.m. – ***A Novel Scallop Free TSV Etching Method in Magnetic Neutral Loop Discharge Plasma*** Yasuhiro Morikawa, Takahide Murayama, Toshiyuki Sakuishi, Manabu Yoshii, and Koukou Suu – Ulvac, Inc.	2. 1:55 p.m. – ***Nonlinear Effects of TSV and Harmonic Generation*** Jonghyun Cho, Joohee Kim, Jun So Pak, and Joungho Kim – KAIST; Junho Lee, Hyngdong Lee, and Kunwoo Park – Hynix Semiconductor, Inc.	2. 1:55 p.m. – ***Reliability of Large Die Ultra Low-k Lead-Free Flip Chip Packages*** Laurene Yip – Xilinx, Inc.
3. 2:20 p.m. – ***Electrical and Morphological Assessment of Via Middle and Backside Process Technology for 3D Integration*** Jean-Philippe Colonna, Gennie Garnier, Pascal Chausse, Roselyne Segaud, Amandine Jouve, Catherine Brunet-Manquat, Severine Cheramy, and Nicolas Sillon – CEA-LETI; Perceval Coudrain, Christophe Aumont, Nicolas Hotellier, and Thomas Frank – STMicroelectronics	3. 2:20 p.m. – ***The Size Dependency of Full IMC Solder Joint for 3D Interconnection*** Liping Mo, Fengshun Wu and Weisheng Xia – Huazhong University of Science & Technology; Changqing Liu – Loughborough University	3. 2:20 p.m. – ***Preferred Orientation of 30um Fine Pitch Sn2.5Ag Micro-Bumps Studied by Synchrotron Polychromatic X-Ray Laue Microdiffraction*** Tian Tian and King-Ning Tu – University of California, Los Angeles; Kai Chen, Martin Kunz, and Nobumichi Tamura – Lawrence Berkeley National Laboratory; Chau-Jie Zhan and Tao-Chih Chang – ITRI
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Pavilion)		
4. 3:30 p.m. – ***Process Modeling of Dry Etching for the 3D-Integration with Tapered TSVs*** Martin Wilke, Michael Töpper, Hue Quoc Huynh, and Klaus Dieter Lang – Fraunhofer IZM	4. 3:30 p.m. – ***GTL High Speed I/O in 3D ICs for TSV and Interconnect Signal Integrity Characterization*** Hyunho Baek and William R. Eisenstadt – University of Florida; Shadi Harb – Intel Corporation	4. 3:30 p.m. – ***Cu Pillar Exposed-Die Molded FCCSP for Mobile Devices*** Albert Chang-Yi Lan, C.S. Hsiao, John Lau, Erik So, and B.H. Ma – Siliconware Precision Industries Co., Ltd.
5. 3:55 p.m. – ***All-Wet Cu-Filled TSV Process using Electroless Co-Alloy Barrier and Cu Seed*** Fumihiro Inoue, Tomohiro Shimizu, Hiroshi Miyake, Ryohei Arima, and Shoso Shingubara – Kansai University	5. 3:55 p.m. – ***Electrical Characterization of Through Silicon Vias (TSVs) with an On Chip Bus Driver for 3D IC Integration*** S.S. Sheu and S.H. Wu – National Central University; Z.H. Lin, C.S. Lin, J.H. Lau, S.H. Lee, K.L. Su, T.K. Ku, J.F. Hung, P.S. Chen, S.J. Lai, and W.C. Lo – ITRI	5. 3:55 p.m. – ***Coreless Substrate Technology Investigation for Ultra-Thin CPU BGA Packaging*** Mathew Manusharow, Sriram Muthukumar, Emily Zheng, Asim Sadiq, and Cliff Lee – Intel Corporation
6. 4:20 p.m. – ***Thermal effects on Through-Silicon Via (TSV) Signal Integrity*** Manho Lee, Jonghyun Cho, Joohee Kim, Jun So Pak, and Joungho Kim – KAIST; Hyungdong Lee, Junho Lee, and Kunwoo Park – Hynix Semiconductor, Inc.	6. 4:20 p.m. – ***Co-Design and Optimization of a 256-GB/s 3D IC Package with a Controller and Stacked DRAM*** David Secker, Mandy Ji, John Wilson, Scott Best, Ming Li, and Julia Cline – Rambus Inc.	6. 4:20 p.m. – ***Evaluation and Verification of Enhanced Electrical Performance of Advanced Coreless Flip-Chip BGA Package with Warpage Measurement Data*** GaWon Kim, JiHeon Yu, ChulWoo Park, SeoungJoon Hong, JinYoung Kim, Glenn Rinne, and ChoonHeung Lee – Amkor Technology Korea, Inc.
7. 4:45 p.m. – ***Enhanced Barrier Seed Metallization for Integration of High-Density High Aspect-Ratio Copper-Filled 3D Through-Silicon Via Interconnects*** Yann Civale, Silvia Armini, Harold Philipsen, Augusto Redolfi, Dimitrios Velenis, Kristof Croes, Nancy Heylen, Zaid El-Mekki, Kevin Vandersmissen, Gerald Beyer, Bart Swinnen, and Eric Beyne – IMEC	7. 4:45 p.m. – ***Electrical Analyses of TSV-RDL-Bump of Interposers for High-Speed 3D IC Integration*** Tseshih Sung, Kevin Chiang, Daniel Lee, and Mike Ma – Siliconware Precision Industries Co., Ltd.	7. 4:45 p.m. – ***fcCuBE Technology: A Pathway to Advanced Si-Node and Fine Pitch Flip Chip*** Hamid Eslampour, Mukul Joshi, KeonTaek Kang, HyunII Bae, and YoungChul Kim – STATS ChipPAC, Inc.

Program Sessions: Thursday, May 31, 1:30 p.m. - 5:10 p.m.

Session 22: Precision Components, Sensors and RF Packaging

Committee:
Electronic Components & RF

Nautilus 1

Session Co-Chairs:
Amit P. Agrawal – Cisco Systems, Inc.
Lih-Tyng Hwang – National Sun Yat-Sen University

1. *1:30 p.m.* – ***Integration of Precision Resistors and Capacitors with Near-Zero Temperature Coefficients in Silicon and Organic Packages***
   P. Markondeya Raj, K.P. Murali, Saumya Gandhi, and Rao Tummala – Georgia Institute of Technology; Kirk Slenes and Nathan Berg – TPL Inc.

2. *1:55 p.m.* – ***Low Cost QFN Package Design for Millimeter-Wave Applications***
   Yi-Chieh Lin, Yu-Chih Lin, Tzyy-Sheng Horng, and Lih-Tyng Hwang – National Sun Yat-Sen University; Chi-Tsung Chiu and Chih-Pin Hung – Advanced Semiconductor Engineering

3. *2:20 p.m.* – ***A Novel U-Shaped Magnetic Shield for Perpendicular MRAM***
   Takahito Watanabe and Shintaro Yamamichi – Renesas Electronics Corporation

Session 23: Assembly Challenges of Area Array Packages

Committee:
Assembly & Manufacturing Technology

Nautilus 3

Session Co-Chairs:
Paul Houston – Engent
Sylvain Ouimet – IBM Corporation

1. *1:30 p.m.* – ***Assembly Yield Improvement of an Asymmetric Surface Mountable Transformer***
   Lejun Wang, Chunho Kim, Scott Sleeper, Gavin Hall, Julie Dobbins, and Molly McGuire – Medtronic

2. *1:55 p.m.* – ***Low-Cost and Fine-Pitch Micro-Ball Mounting Technology for WLCSP***
   Y.H. Lin, Frank Kuo, Y.F Chen, C.S. Ho, J.Y. Lai, Stan Chen, F.L. Chien, Rick Lee, and John Lau – Siliconware Precision Industries Co., Ltd.

3. *2:20 p.m.* – ***Investigation of the Assembly Reflow Process and PCB Design on the Reliability of WLCSP***
   Yong Liu, Qiuxiao Qian, Shichun Qu, Stephen Martin, and Oseob Jeon – Fairchild Semiconductor Corporation

Session 24: Inkjet Technology and Embedded Devices

Committees: Electronic Components & RF / Emerging Technologies

Nautilus 5

Session Co-Chairs:
Rockwell Hsu – Cisco Systems, Inc.
Karlheinz Bock – Fraunhofer EMFT

1. *1:30 p.m.* – ***System Integration of Smart Packages using Printed Electronics***
   Matti Mäntysalo – Tampere University of Technology; Li Xie, Fredrik Jonsson, Yi Feng, Ana López Cabezas, and Li-Rong Zheng – KTH Royal Institute of Technology

2. *1:55 p.m.* – ***Inkjet-Printed Graphene-Based Wireless Gas Sensor Modules***
   Taoran Le, Vasileios Lakafosis, Ziyin Lin, C.P. Wong, and M.M. Tentzeris – Georgia Institute of Technology

3. *2:20 p.m.* – ***Inkjet Printed Flexible User Interface Module***
   Santtu Koskinen and Matti Mäntysalo – Tampere University of Technology; Lasse Pykäri – Nokia

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Pavilion)

4. *3:30 p.m.* – ***Behavior Model of Switching DC-DC Converter for Improving Power Delivery Network Design***
   Seungyong Baek, Philip Pun, and Amit Agrawal – Cisco Systems, Inc.

5. *3:55 p.m.* – ***Planar Surface Plasmonic Structures for Terahertz Circuits and Sensors***
   Premjeet Chahal, Joshua Myers, Kyoung Youl Park, Collin Meierbachtol, and Naveen Nair – Michigan State University

6. *4:20 p.m.* – ***Optimized SAW Chemical Sensor with Microfluidic Packaging***
   Robert W. Brocato, Terisse A. Brocato, Joel R. Wendt, Carlos A. Sanchez, and Larry G. Stotts – Sandia National Laboratories

7. *4:45 p.m.* – ***A Surface Micromachined High Directivity GPS Patch Antenna with a Four-Leaf Clover Shape Metamaterial Slab***
   Cheolbok Kim, Kyoung Tae Kim, and Yong-Kyu Yoon – University of Florida; Kyung-Hoon Lee – ETRI; Sangrok Lee – ShinHeung College

4. *3:30 p.m.* – ***Systematic Studies of Second Level Interconnection Reliability of Edge and Corner Bonded Lead-Free Array-Based Packages under Mechanical and Thermal Loading***
   Hongbin Shi and Toshitsugu Ueda – Waseda University; Daquan Yu – Chinese Academy of Sciences

5. *3:55 p.m.* – ***Assessment of Non-Uniform Temperature Effect on BGA De-Component Process***
   Kun Tang, Fubin Song, S.W. Ricky Lee, and Jeffery, C.C. Lo – Hong Kong University of Science & Technology

6. *4:20 p.m.* – ***Voltage In-Situ Electrical Metrology for Test-to-Failure BGA Component Shock Margin Assessment***
   Ramgopal Uppalapati, Sanjay Goyal, Mike Williams, and Satish Parupalli – Intel Corporation

7. *4:45 p.m.* – ***Validated Methodology for Short-Design-Cycle Chip, Package and System Interaction***
   Mudasir Ahmad, Qiang Wang, and Weidong Xie – Cisco Systems, Inc.

4. *3:30 p.m.* – ***Modeling and Design of an Ultra-Miniaturized WLAN Sub-System with Chip-Last Embedded PA and Digital Dies***
   Gokul Kumar, Srikrishna Sitaraman, Vivek Sridharan, Nithya Sankaran, Fuhan Liu, Nitesh Kumbhat, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Vijay Nair and Telesphor Kamgaing – Intel Corporation; Frank Juskey – TriQuint Corporation

5. *3:55 p.m.* – ***Scalable Modeling and Wideband Measurement Techniques for a Signal TSV Surrounded by Multiple Ground TSVs for RF/High-Speed Applications***
   Kuan-Chung Lu and Tzyy-Sheng Horng – National Sun Yat-Sen University; Hsin-Hung Lee, Kung-Chin Fan, Tzu-Yuan Huang, and Chun-Hsun Lin – Siliconware Precision Industries Co., Ltd.

6. *4:20 p.m.* – ***A 77 GHz SiGe Single-Chip Four-Channel Transceiver Module with Integrated Antennas in Embedded Wafer- Level BGA Package***
   M. Wojnowski, R. Lachner, J. Böck, G. Sommer, and K. Pressel – Infineon Technologies AG; C. Wagner – DICE GmbH & Co. KG

7. *4:45 p.m.* – ***Ultralow Impedance Analysis and Evaluation of Power Distribution Network for Decoupling Capacitor Embedded Interposers of 3-D Integrated LSI System***
   Katsuya Kikuchi and Masahiro Aoyagi – National Institute of Advanced Industrial Science and Technology (AIST); Chihiro Ueda and Kanji Otsuka – Meisei University; Toshio Gomyo and Toshikazu Ookubo – Association of Super-Advanced Electronic Technologies

Program Sessions: Friday, June 1, 8:00 a.m. - 11:40 a.m.

Session 25: 3D Integration

Committee:
Advanced Packaging

Harbor Island II

Session Co-Chairs:
Subhash L. Shinde – Sandia National Laboratory
Luu T. Nguyen – Texas Instruments

1. ***8:00 a.m. – Addressing Bandwidth Challenges in Next Generation High Performance Network Systems with 3D IC Integration***
Li Li, Peng Su, Jie Xue, and Mark Brillhart – Cisco Systems, Inc.; John Lau, P.J. Tzeng, C.K. Lee, C.J. Zhan, M.J. Dai, H.C. Chien, and S.T. Wu – ITRI

2. ***8:25 a.m. – 3D Multi-Stacking of Thin Dies based on TSV and Micro-Inserts Interconnections***
J. Souriau and L. Castagné – CEA-LETI; J. Liotard – STMicroelectronics; K. Inal, J. Mazuir, and F. Le Texier – ENSM.SE/CMP-GC; G. Fresquet – Fogale; M. Varvara and N. Launay – SPTS Technologie sas.; B. Dubois and T. Malia – Gemalto

3. ***8:50 a.m. – Polyimide Based Temporary Wafer Bonding Technology for High Temperature Compliant TSV Backside Processing and Thin Device Handling***
K. Zoschke, T. Fischer, M. Toepper, T. Fritzsch, and H. Oppermann – Fraunhofer IZM; O. Ehrmann and K.D. Lang – TU Berlin; T. Itabashi – Hitachi Chemical DuPont MicroSystems Ltd.; M. Zussman – HD MicroSystems; M. Souter – Tamarack Scientific

4. ***10:00 a.m. – Development of a Stacked WCSP Package Platform using TSV (Through Silicon Via) Technology***
Rajiv Dunne, Yoshimi Takahashi, Kazuaki Mawatari, Masamitsu Matsuura, Tom Bonifield, Philipp Steinmann, and David Stepniak – Texas Instruments, Inc.

5. ***10:25 a.m. – 2.5D and 3D Technology Challenges and Test Vehicle Demonstrations***
J.U. Knickerbocker, P.S. Andry, E. Colgan, B. Dang, T. Dickson, X. Gu, C. Haymes, C. Jahnes, Y. Liu, J. Maria, R.J. Polastre, and C.K. Tsang – IBM Corporation

6. ***10:50 a.m. – 3D-TSV Vertical Interconnection Method using Cu/SnAg Double Bumps and B-Stage Non-Conductive Adhesives (NCAs)***
Yongwon Choi, Jiwon Shin, and Kyung-Wook Paik – KAIST

7. ***11:15 a.m. – Numerical and Experimental Characterization of the Thermal Behavior of a Packaged DRAM-on-Logic Stack***
H. Oprins, V.O. Cherman, B. Vandevelde, G. Van der Plas, P. Marchal, and E. Beyne – IMEC

Session 26: Advanced Wirebonding

Committee:
Interconnections

Harbor Island I

Session Co-Chairs:
Flynn Carson – STATS ChipPAC, Inc.
William Chen – Advanced Semiconductor Engineering, Inc.

1. ***8:00 a.m. – Pd-Coated Cu Wire Bonding Technology: Chip Design, Process Optimization, Production Qualification and Reliability Test for High Reliability Semiconductor Devices***
Inderjit Singh and Shin Low – Xilinx, Inc.; Ivy Qin, Cuong Huynh, Horst Clauberg, and Bob Chylak – Kulicke and Soffa Industries, Inc.; Hui Xu and Viola L. Acoff – University of Alabama

2. ***8:25 a.m. – Evaluation of Back End of Line Structures Underneath Wirebond Pads in Ultra Low-k Device***
Toyohiro Aoki, Takashi Hisada, Keishi Okamoto, John C. Malinowski, Keith F. Beckham, and Shinichi Harada – IBM Corporation; Yong-Seok Yang and Joon-Su Kim – Amkor Technology, Korea

3. ***8:50 a.m. – Low Cost Pd Coated Ag Bonding Wire for High Quality Fab in Air***
Suresh Tanna, Jairus L. Pisigan, and John Persic – Microbonds, Inc.; W.H. Song, Christopher Halmo, and Michael Mayer – University of Waterloo

4. ***10:00 a.m. – An Evaluation of Effects of Molding Compound and Substrate Material Properties on Reliability of Cu Wire BGA Components***
Peng Su – Cisco Systems, Inc.; Hidetoshi Seki, Yoshinori Nishitani, Chen Ping, Shin-ichi Zenbutsu, and Shingo Itoh – Sumitomo Bakelite Co. Ltd.; Louie Huang, Nicholas Liao, Bill Liu, Curtis Chen, Winnie Tai, and Andy Tseng – ASE

5. ***10:25 a.m. – Cu Wire and Pd-Cu Wire Package Reliability and Molding Compounds***
Hidenori Abe – Hitachi Chemical Company, Ltd.; Dong Chul Kang, Takashi Yamamoto, Takashi Yagihashi, Yoshinori Endo, Hiroyuki Saito, Takahiro Horie, Hironori Tamate, Yoshinori Ejiri, and Naoki Watanabe – Hitachi Chemical Company., Ltd.

6. ***10:50 a.m. – Copper Wire Bond Analysis: Pad Design Effects and Process Considerations***
John D. Beleran, Yong Bo Yang, Hyman G. Robles, and Antonino Milanes – United Test And Assembly Center, Ltd. (UTAC); Alfred Yeo and Chan Kai Chong – Global Foundries, Ltd.

7. ***11:15 a.m. – Effect of EFO Settings on Microstructure and Hardness in the FAB of Copper Bonding Wire***
Dong Liu, Haibin Chen, and Jingshen Wu – Hong Kong University of Science & Technology; Fei Wong, Kan Lee, and Ivan Shiu – NXP Semiconductors Hong Kong, Ltd.

Session 27: Bonding Materials and Processes

Committee:
Materials & Processing

Harbor Island III

Session Co-Chairs:
Kwang-Lung Lin – National Cheng Kung University
C Robert Kao – National Taiwan University

1. ***8:00 a.m. – Fluxless Tin Bonding of Silicon Chips to Aluminum Substrates***
Shou-Jen Hsu, Chu-Hsuan Sha, and Chin C. Lee – University of California, Irvine

2. ***8:25 a.m. – Low-Temperature, Surface-Compliant Wafer Bonding using Sub-Micron Gold Particles for Wafer-Level MEMS Packaging***
Hiroyuki Ishida and Takuya Yazaki – Suss MicroTec; Toshinori Ogashiwa and Yukio Kanehira – Tanaka Kikinzoku Kogyo; Shin Ito and Jun Mizuno – Waseda University

3. ***8:50 a.m. – Electron Microscopy Study on Intermetallic Compound Formation in Cu-Al Bond Interface***
In-Tae Bae and Dae Young Jung – SUNY Binghamton; Yong Du – Advanced Semiconductor Engineering

Refreshment Break: 9:15 a.m. - 10:00 a.m. (Harbor Island Foyer)

4. ***10:00 a.m. – Evaluation of the Crystallinity of Grain Boundaries of Electronic Copper Thin Films for Highly Reliable Interconnections***
Naoki Saito, Naoakazu Murata, Kinji Tamakawa, Ken Suzuki, and Hideo Miura – Tohoku University

5. ***10:25 a.m. – Evaluation of Self-Assembled Monolayer Treatment for Wire Bonding with ENEPIG Surface Finish***
Jeremy Palmer, Dahwey Chu, and Lu Fang – Sandia National Laboratories

6. ***10:50 a.m. – Silver Alloy Wire Ball Bonding***
Liao Jun Kai, Liang Yi Hung, Li Wei Wu, Men Yeh Chiang, Don Son Jiang, C.M. Huang, and Yu Po Wang – Siliconware Precision Industries Co., Ltd.

7. ***11:15 a.m. – Low Cost Palladium Coating Process and Its Effect on Free-Air-Ball Softness and Second Bond Strength of Cu Bonding Wires***
John Persic, Jairus L. Pisigan, Suresh Tanna, and Yong Guo – Microbonds, Inc.; W.H. Song and Michael Mayer – University of Waterloo

Program Sessions: Friday, June 1, 8:00 a.m. - 11:40 a.m.

Session 28: New Trends in Mechanical Modeling and Characterization

Committee:
Modeling & Simulation

Marina 6

Session Co-Chairs:
L. J. Ernst – Delft University of Technology
Bruce Kim – The University of Alabama

1. *8:00 a.m.* – ***Modeling for Critical Design and Performance of Wafer Level Chip Scale Package***
   Yong Liu, Qiuxiao Qian, Matt Ring, Jihwan Kim, and Dan Kinzer – Fairchild Semiconductor Corporation

2. *8:25 a.m.* – ***Prediction of Tin-Whiskers Generation during Thermal Cycle Test using Stress and Mass-Diffusion Analysis***
   Takeshi Terasaki, Takahiko Kato, Tomio Iwasaki, Yasutaka Ookura, and Masato Nakamura – Hitachi, Ltd.; Hideki Ishii and Kenji Yamamoto – Renesas Electronics Corp.

3. *8:50 a.m.* – ***Finite Element Modeling of Anomalous Moisture Diffusion with Dual Stage Model***
   Xuejun Fan and Vishal Nigaraj – Lamar University

4. *10:00 a.m.* – ***Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up to 50,000G***
   Pradeep Lall, Kewal Patel, and Ryan Lowe – Auburn University; Mark Strickland, Jim Blanche, Dave Geist, and Randall Montgomery – NASA Marshall Space Flight Center

5. *10:25 a.m.* – ***Design and Assembly of a Double-Sided 3D Package with a Controller and a DRAM Stack***
   Xi Liu and Suresh K. Sitaraman – Georgia Institute of Technology; Ming Li, Don Mullen, and Julia Cline – Rambus, Inc.

6. *10:50 a.m.* – ***Establishing Mode Mix Dependency of Fracture Toughness in Microelectronic Components with Reduced Experimental Effort***
   H. Pape, I. Maus, and H.S. Nabi – Infineon Technologies; L.J. Ernst – Delft University of Technology; B. Wunderle – TU Chemnitz

7. *11:15 a.m.* – ***Failure Prediction in Fully Coupled Thermal and Deformational Fields with Peridynamics***
   Abigail Agwai – Intel Corporation; Ibrahim Guven and Erdogan Madenci – University of Arizona

Session 29: Novel Approaches in Wafer Level Manufacturing

Committee:
Assembly & Manufacturing Technology

Seabreeze

Session Co-Chairs:
Shichun Qu – Fairchild Semiconductor
Jie Xue – Cisco Systems, Inc.

1. *8:00 a.m.* – ***Wafer Level Underfill for Area Array Cu Pillar Flip Chip Packaging of Ultra Low-k Chips on Organic Substrates***
   Jae-Woong Nah, Michael Gaynes, Eric Perfecto, and Claudius Feger – IBM Corporation

2. *8:25 a.m.* – ***Metrology for Characterization of Wafer Thickness Uniformity during 3DS-IC Processing***
   Tom Dunn, Chris Lee, Mark Tronolone, and Aric Shorey – Corning, Inc.

3. *8:50 a.m.* – ***Novel Sidewall Interconnection using Perpendicular Circuit Die with Non-Solder Bumps for 3D Chip Stack***
   Sun-Rak Kim, Il Kim, and Seung S. Lee – KAIST; Jae Hak Lee – KIMM

4. *10:00 a.m.* – ***Advanced Low Profile PoP Solution with Embedded Wafer Level PoP (eWLB-PoP) Technology***
   Seung Wook Yoon, Jose Alvin Caparas, Yaojian Lin, and Pandi C. Marimuthu – STATS ChipPAC, Ltd.

5. *10:25 a.m.* – ***Temporary Wafer Bonding Defect Impact Assessment on Substrate Thinning: Process Enhancement through Systematic Defect Track Down***
   A. Phommahaxay, G. Verbinnen, S. Suhard, P. Bex, J. Pancken, M. Lismont, A. Van den Eede, A. Jourdain, and B. Swinnen – IMEC; T. Woitke, P. Bisson, and W. Spiess – Suss MicroTec

6. *10:50 a.m.* – ***Novel Approaches of Wafer Level Packaging for MEMS Devices***
   Cheng-Hsiang Liu, Hong-Da Chang, Hsin-Yi Liao, Kuo-Hsiang Li, Chen-Han Lin, Wei-Yu Chen, and Tse-Yuan Lin – Siliconware Precision Industries Co., Ltd.

7. *11:15 a.m.* – ***Silicon-Based System in Packaging for Light Emitting Diodes***
   Bin Cao, Shan Yu, Huai Zheng, and Sheng Liu – Huazhong University of Science & Technology

Session 30: Interconnect Reliability

Committee:
Applied Reliability

Spinnaker

Session Co-Chairs:
S.B. Park – Binghamton University
Scott Savage – Medtronic Microelectronics Center

1. *8:00 a.m.* – ***Effects of Surface Finish Conditions on Interfacial Reaction Characteristics and Mechanical Reliability of Novel Sn-1.2Ag-0.7Cu-0.4In Solder Bump***
   Jae-Myeong Kim, Byung-Hyun Kwak, and Young-Bae Park – Andong National University; Myeong-Hyeok Jeong and Sehoon Yoo – Korea Institute of Industrial Technology

2. *8:25 a.m.* – ***Micro-Interconnection Reliability: Thermal, Electrical and Mechanical Stress***
   S.L. Wright, C.K. Tsang, J. Maria, B. Dang, R. Polastre, P. Andry, and J. Knickerbocker – IBM Corporation

3. *8:50 a.m.* – ***Effects of UBM Structure/Material on the Reliability Performance of 3D Chip Stacking with 30um-Pitch Solder Micro Bump Interconnections***
   Shin-Yi Huang, Chau-Jie Zhan, Yu-Wei Huang, Yu-Min Lin, Chia-Wen Fan, Su-Ching Chung, Kuo-Shu Kao, Jing-Yao Chang, Mei-Lun Wu, John H. Lau, and Tai-Hung Chen – ITRI; Tsung-Fu Yang – Topco Scientific Co., Ltd.

4. *10:00 a.m.* – ***Electromigration of SnAg Bump with Ni UBM on Various Substrate Pad Finishes with SnCu Presolder***
   Tung-Chin Yeh, Tsung-Fu Tsai, Larry Lin, Roger Hsieh, and Kenneth Wu – Taiwan Semiconductor Manufacturing Company, Ltd.

5. *10:25 a.m.* – ***Isothermal Shear Fatigue Mechanism of Lead Free Solder Joints***
   Huili Xu, Woong Ho Bang, and Choong-Un Kim – University of Texas, Arlington; Hong-Tao Ma, Tae-Kyu Lee, and Kuo-Chuan Liu – Cisco Systems, Inc.

6. *10:50 a.m.* – ***Electromigration Measurements in Thin-Film IPD and eWLB Interconnections***
   Robert Frye – RF Design Consulting, LLC; Kai Liu, KyawOo Aung, and M. Pandi Chelvam – STATS ChipPAC, Ltd.

7. *11:15 a.m.* – ***Effect of High Strain-Rate on Mechanical Properties of SAC105 and SAC305 Lead-Free Alloys***
   Pradeep Lall, Sandeep Shantaram, and Jeff Suhling – Auburn University; Dave Locker – US AMRDEC

Refreshment Break: 9:15 a.m. - 10:00 a.m. (Harbor Island Foyer)

Program Sessions: Friday, June 1, 1:30 p.m. - 5:10 p.m.

Session 31: Applications with 3D Technologies	Session 32: Advanced Substrate and Wafer Level Packaging	Session 33: Substrates and Thermal Interface Materials
Committees: Interconnections / Emerging Technologies	**Committee: Advanced Packaging**	**Committee: Materials & Processing**
Harbor Island II	**Harbor Island I**	**Harbor Island III**
Session Co-Chairs: **Akitsu Shigetou – National Institute for Materials Science** **Nancy Stoffel – GE Global Research**	**Session Co-Chairs:** **Young-Gon Kim – IDT** **Altaf Hasan – Intel Corporation**	**Session Co-Chairs:** **Don Frye – Polyera Corp.** **Tieyu Zheng – Intel Corporation**
1. *1:30 p.m. – Via Last Technology for Direct Stacking of Processor and Flash* R. Puschmann, M. Boettcher, I. Bartusseck, F. Windrich, C. Fiedler, P. John, C. Manier, K. Zoschke, J. Grafe, H. Oppermann, and M.J. Wolf – Fraunhofer IZM; M. Ziesmann – NXP Semiconductors	1. *1:30 p.m. – Application of Coreless Substrate to Package on Package Architectures* Robert Nickerson, Reynaldo Olmedo, Russell Mortensen, Choong Kooi Chee, Sanjay Goyal, Ai Ling Low, and Charles Gealer – Intel Corporation	1. *1:30 p.m. – Evaluation of Raw Substrate Variation from Different Suppliers and Processes, and their Impact on Package Warpage* Wei Lin, Shengmin Wen, Akito Yoshida, and JeongMin Shin – Amkor Technology
2. *1:55 p.m. – 3D-Interconnect Approach for High End Electronics* Rabindra N. Das, Frank D. Egitto, John Lauffer, Barry Bonitz, Bill Wilson, Francesco Marconi, Mark D. Poliks, and Voya R. Markovich – Endicott Interconnect Technologies, Inc.	2. *1:55 p.m. – Chip-Last Fan-Out Package with Embedded Power ICs in Ultra-Thin Laminates* Nitesh Kumbhat, Koushik Ramachandran, Fuhan Liu, Brent Wagner, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology	2. *1:55 p.m. – Low Cost System-in-Package Module using Next Generation Low Loss Organic Material* Yuya Suzuki, Srikrishna Sitaraman, Abhilash Goyal, Fuhan Liu, Nitesh Kumbhat, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Masakazu Hashimoto, Toshihiko Jimbo, and Ryota Mori – Zeon
3. *2:20 p.m. – TSV-Based Decoupling Capacitor Schemes in 3D-IC* Eunseok Song, Jun So Pak, and Joungho Kim – KAIST	3. *2:20 p.m. – Low Warpage Coreless Substrate for Large-Size LSI Packages* Mamoru Kurashina, Daisuke Mizutani, Masateru Koide, Manabu Watanabe, Kenji Fukuzono, and Hitoshi Suzuki – Fujitsu	3. *2:20 p.m. – Enhancement of Barrier Properties of Encapsulants for Harsh Environment Applications* T. Braun, J. Bauer, K.F. Becker, M. Koch, and R. Aschenbrenner – Fraunhofer IZM; L. Georgi and K.D. Lang – TU Berlin
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Harbor Island Foyer)		
4. *3:30 p.m. – Enabling Technologies for Advanced Wafer Level Camera Integration* C. Bouvier, S. Bolis, D. Saint-Patrice, A. Pouydebasque, F. Jacquet, C. Bridoux, S. Moreau, G. Simon, and N. Sillon – CEA-LETI; E. Vigier-Blanc – STMicroelectronics SAS	4. *3:30 p.m. – Innovative Fan-Out Wafer Level Package using Lamination Process and Adhered Si Wafer on the Backside* H.S. Hsu, David Chang, Kenny Liu, Nicholas Kao, Mark Liao, and Steve Chiu – Siliconware Precision Industries Co., Ltd.	4. *3:30 p.m. – Thermal Performance Characterization of Nano Thermal Interface Materials after Power Cycling* Shuangxi Sun – Shanghai University; Luo Xin and Johan Liu – Shanghai University, Chalmers University of Technology; Carl Zandén and Björn Carlberg – Chalmers University of Technology; Lilei Ye – SHT Smart High-Tech AB
5. *3:55 p.m. – Low Cost 3D Multilevel Interconnect Integration for RF and Microwave Applications* Ayad Ghannam and David Bourrier – LAAS-CNRS; Lamine Ourak, Christophe Viallon, and Thierry Parra – LAAS-CNR, University of Toulouse	5. *3:55 p.m. – Development and Characterization of Next Generation eWLB (Embedded Wafer Level BGA) Packaging* Yonggang Jin, Jerome Teysseyre, and Xavier Baraton – STMicroelectronics; S.W. Yoon, Yaojian Lin, and Pandi C. Marimuthu – STATS ChipPAC, Ltd.	5. *3:55 p.m. – Structural Functionality Analysis of Nanostructured Thermal Interface Materials* Xiangdong Xue, Chris Bailey, Hua Lu, and Ohidul Alam – University of Greenwich
6. *4:20 p.m. – A Low-Cost Approach to High-k Thin Film Decoupling Capacitors on Silicon and Glass Interposers* Saumya Gandhi, Shu Xiang, P. Markondeya Raj, Venky Sundaram, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology	6. *4:20 p.m. – Optical Characteristics and Reliability Evaluation of Wafer Level White LED Package* Akiya Kimura, Susumu Obata, Toshiya Nakayama, Ryuichi Togawa, Takayoshi Fujii, Hiroshi Koizumi, Kazuhito Higuchi, Yosuke Akimoto, Miyuki Shimojuku, and Akihiro Kojima – Toshiba Corporation	6. *4:20 p.m. – Single/Few-Layer Boron Nitride-Based Nanocomposites for High Thermal Conductivity Underfills* Ziyin Lin, Yagang Yao, Andrew Mcnamara, and Kyoung-Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
7. *4:45 p.m. – Fine Pitch Copper PoP for Mobile Applications* Philip Damberg, Ilyas Mohammed, and Reynaldo Co – Invensas, Inc.	7. *4:45 p.m. – Wafer Level Compression Molding Compounds* Taku Hasegawa, Hidenori Abe, and Takatoshi Ikeuchi – Hitachi Chemical Co., Ltd.	7. *4:45 p.m. – Nano-Micro Particle Filled Thermal Interface Materials: Towards Materials Development, Characterization, Assembly, and Performance Evaluation* Rabindra N. Das, Evan Chenelly, Erich Kopp, Dave Alcoe, Mark D. Poliks, and Voya R. Markovich – Endicott Interconnect Technologies, Inc.

Program Sessions: Friday, June 1, 1:30 p.m. - 5:10 p.m.

Session 34: 3D Systems and Emerging Packages-Thermal and Thermo-Mechanical Studies	Session 35: Optical Interconnects	Session 36: Integrated Microfluidics
Committee: Modeling & Simulation	**Committee: Optoelectronics**	**Committee: Emerging Technologies**
Marina 6	**Seabreeze**	**Spinnaker**
Session Co-Chairs: **Yong Liu – Fairchild Semiconductor Corporation** **Xuejun Fan – Lamar University**	**Session Co-Chairs:** **Andrew Shapiro – JPL** **Kannan Raj – Sun Labs, Oracle**	**Session Co-Chairs:** **Mark Bachman – University of California, Irvine** **Joana Maria – IBM Corporation**
1. ***1:30 p.m. – A Finite Element Analysis of Board Level Temperature Cycling Reliability of Embedded Wafer Level BGA (eWLB) Package*** Seng Guan Chow, Yaojian Lin, Eric Ouyang, and Billy Ahn – STATS ChipPAC, Inc.	1. ***1:30 p.m. – Terabit/Sec 48-Channel Fiber-Coupled Optical Module based on Holey CMOS Transceiver IC*** Fuad E. Doany, Benjamin G. Lee, Alexander V. Rylyakov, Daniel M. Kuchta, Christopher Jahnes, Christian Baks, Frank Libsch, and Clint L. Schow – IBM Corporation	1. ***1:30 p.m. – Characteristics of Blood Flow in Microchannels and Relevant Impact on Modelling Blood Behaviour in Biochip Separators*** Xiangdong Xue – University of Greenwich; Xueyong Wei – University of Cambridge
2. ***1:55 p.m. – Hybrid Thermal Solution for 3D-ICs: Using Thermal TSVs with Placement Algorithm for Stress Relieving Structures*** Jui-Hung Chien, Yung-Fa Chou, and Ding-Ming Kwai – ITRI; Hao Yu, Nien-Yu Tsai, and Shih-Chieh Chang – National Tsing Hua University; Chiao-Ling Lung – ITRI, National Tsing Hua University; Chin-Chi Hsu and Ping-Hei Chen – National Taiwan University	2. ***1:55 p.m. – Cost-Effective Low-Loss Flexible Optical Engine with Microlens-Imprinted Film for High-Speed On-Board Optical Interconnection*** Takashi Shiraishi, Takatoshi Yagisawa, Tadashi Ikeuchi, Satoshi Ide, and Kazuhiro Tanaka – Fujitsu Laboratories, Ltd.	2. ***1:55 p.m. – Integration of On-Chip Glass Microfluidic System by a Chemical Foaming Process (CFP)*** Jintang Shang, Xinhu Luo, Shunjin Qin, Yu Zou, Xiao Xie, and Junwen Liu – Southeast University; Wei Lin and C.P. Wong – Georgia Institute of Technology
3. ***2:20 p.m. – Development of Through Silicon Via (TSV) Interposer for Memory Module Flip Chip Package*** Nicholas Kao, Eason Chen, Daniel Lee, and Mike Ma – Siliconware Precision Industries Co., Ltd.	3. ***2:20 p.m. – Small-Aperture Guided-Mode-Resonance Filter with Cavity Resonators*** Shogo Ura, Tatsuya Majima, Koji Hatanaka, Junichi Inoue, Kenzo Nishio, and Yasuhiro Awatsuji – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology	3. ***2:20 p.m. – Plastic Injection Micromolding of THz Circuits and Microfluidic Sensors*** Kyoung Youl Park, Nophadon Wiwatcharagoses, Cecilia Acosta Silveira, and Premjeet Chahal – Michigan State University
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Harbor Island Foyer)		
4. ***3:30 p.m. – Interlayer Dielectric Cracking in Back End of Line (BEOL) Stack*** Sathyanarayanan Raghavan and Suresh K. Sitaraman – Georgia Institute of Technology; Ilko Schmadlak – Freescale Semiconductor	4. ***3:30 p.m. – Scaling Hybrid-Integration of Silicon Photonics in Freescale 130nm to TSMC 40nm-CMOS VLSI Drivers for Low Power Communications*** J.E. Cunningham, I. Shubin, H.D. Thacker, J.H. Lee, G.L. Li, X. Zheng, J. Lexau, R. Ho, J.G. Mitchell, Y. Luo, J. Yao, and K. Raj – Oracle	4. ***3:30 p.m. – Combination of Channel- and Droplet-Based Microfluidics for Complex PoC-Devices*** Erik Jung, Jörg Bauer, Tanja Braun, and Victoria Schuldt – Fraunhofer IZM; Leopold Georgi – TU Berlin; Khaled Metwally, Laurent Robert, and Chantal Khan-Malek – CNRS FEMTO Innovation
5. ***3:55 p.m. – Prognostication of Accrued Damage in Board Assemblies under Thermal and Mechanical Stresses*** Pradeep Lall and Ryan Lowe – Auburn University; Kai Goebel – NASA Ames Research Center	5. ***3:55 p.m. – Demonstration of High-Bandwidth Data Transmission above 240 Gbps for Optoelectronic Module with Low-Loss and Low-Crosstalk Polynorbornene Waveguides*** Yuka Ito, Shinsuke Terada, Mayank Kumar Singh, Shinya Arai, and Koji Choki – Sumitomo Bakelite Co., Ltd.	5. ***3:55 p.m. – Silicon Integrated Micro Batteries based on Deep Reactive Ion Etching and Through Silicon Via Technologies*** R. Hahn, K. Markquardt, M. Thunmann, M. Töpper, M. Wilke, M. Ferch, Q.H. Huynh, and K.D. Lang – Fraunhofer IZM
6. ***4:20 p.m. – Generic Thermal Analysis for Phone and Tablet Systems*** Siva P. Gurrum, Darvin R. Edwards, Thomas Marchand-Golder, Jotaro Akiyama, Satoshi Yokoya, Jean-Francois Drouard, and Franck Dahan – Texas Instruments, Inc.	6. ***4:20 p.m. – Single-Mode Glass Waveguide Platform for DWDM Chip-to-Chip Interconnects*** Lars Brusberg and Henning Schröder – Fraunhofer IZM; Marco Queisser and Klaus-Dieter Lang – TU Berlin	6. ***4:20 p.m. – Using Polymer and Ionic Liquid as Liquid Droplet Study in Single-Plate Electrowetting System*** Edward K.L. Chan and Matthew M.F. Yuen – Hong Kong University of Science & Technology
7. ***4:45 p.m. – Cohesive Zone Modeling of 3D Delamination in Encapsulated Silicon Devices*** Siow Ling Ho, Shailendra P. Joshi, and Andrew A.O. Tay – National University of Singapore	7. ***4:45 p.m. – Ultralow EMI Interconnection Module for Mobile Devices using 3D-Flexible Hybrid Multi-Fin Optoelectronic FPC*** Hiroshi Uemura, Kentaro Kobayashi, Kohei Hiyama, Hideto Furuyama, Yoshiaki Sugizaki, and Hideki Shibata – Toshiba Corporation	7. ***4:45 p.m. – Microfluidic Thermal Component for Integrated Microfluidic Systems*** Sarkis Babikian, Liang Wu, G.P. Li, and Mark Bachman – University of California, Irvine

Interactive Presentations: Wednesday, May 30 and Thursday, May 31, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, May 30
Session 37: Interactive Presentations 1
9:00 a.m. - 11:00 a.m.
Committee: Interactive Presentations
Pavilion

Session Co-Chairs:
Mark Poliks – Endicott Interconnect Technologies, Inc.
Ibrahim Guven – University of Arizona

1. ***Newly Developed Ultra Low CTE Materials for Thin Core PKG***
   Masato Miyatake, Hikari Murai, Shin Takanezawa, Shinji Tsuchikawa, Masaaki Takekoshi, Tomohiko Kotake, and Masahisa Ose – Hitachi Chemical Co., Ltd.
2. ***Fabrication and Electrical Characterization of Embedded Actives and Passives for System Level Analysis: Towards Size, Weight and Power (SWaP) Reduction***
   Rabindra N. Das, Steven G. Rosser, Robert Welte, John M. Lauffer, Richard Kelly, Mark D. Poliks, and Voya R. Markovich – Endicott Interconnect Technologies, Inc.
3. ***Polyhedral Oligomeric Silsesquioxanes (POSS)-Filled Underfill with Excellent High Temperature Performance***
   Ziyin Lin and Kyoung-sik Moon – Georgia Institute of Technology; Shunyi Lau – Chinese University of Hong Kong; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
4. ***Package-on-Package for Chip Cooling with Embedded Fluidics***
   Tiffany Chua, Sarkis Babikian, Liang Wu, G.P. Li, and Mark Bachman – University of California, Irvine
5. ***A Study on the Chip-Package-Interaction for Advanced Devices with Ultra Low-k Dielectric***
   Seok Won Lee, Byoung Wook Jang, Jong Kook Kim, Yoon Ha Jung, Young Bae Kim, Ho Geon Song, Sa Yoon Kang, Young Min Kang, San Man Lee, Ki Chul Park, Chi Sun Ju, and Gun Rae Kim – Samsung Electronics Company, Ltd.
6. ***Ultra Low-Cost Through-Silicon Holes (TSHs) Interposers for 3D IC Integration SiPs***
   Sheng-Tsai Wu, John H. Lau, Heng-Chieh Chien, Jui-Feng Hung, Ming-Ji Dai, Yu-Lin Chao, Ra-Min Tain, Wei-Chung Lo, and Ming-Jer Kao – ITRI
7. ***Fabrication and Characterization of Wafer-Level Deep TSV Arrays***
   Michael Zervas, Yuksel Temiz, and Yusuf Leblebici – École Polytechnique Fédérale de Lausanne
8. ***Impact of the Winding Area of Enameled Wire on Packaging Performance of a Closed Loop Hall Effect Current Sensor***
   Fu'an Li, Xiaobing Luo, Xingguo Cheng, and Sheng Liu – Huazhong University of Science and Technology
9. ***MEMS Gyroscope Yield Simulation Based on Monte Carlo Method***
   Zhang Luo and Sheng Liu – Huazhong University of Science & Technology; Xiaoping Wang – FineMEMS Inc.; Min Jin – Hunan University
10. ***High-Density Capacitors with Conformal High-K Dielectrics on Etched-Metal Foils***
    Parthasarathi Chakraborti, Himani Sharma, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology
11. ***3D Stacked Microfluidic Cooling for High Performance 3D Ics***
    Yue Zhang, Ashish Dembla, Yogendra Joshi, and Muhannad S. Bakir – Georgia Institute of Technology
12. ***Copper Conductive Adhesives for Printed Circuit Interconnects***
    Siyuan Qi, Robert Litchfield, David A. Hutt, Bala Vaidhyanathan, and Changqing Liu – Loughborough University; Patrick Webb – Manufacturing Technology Centre; Stephen Ebbens – University of Sheffield
13. ***Low Temperature Bonding using Non-Conductive Adhesive for 3D Chip Stacking with 30mm-Pitch Micro Solder Bump Interconnections***
    Yu-Min Lin, Chau-Jie Zhan, Kuo-Shu Kao, Chia-Wen Fan, Su-Ching Chung, Yu-Wei Huang, Shin-Yi Huang, Jing-Yao Chang, John H. Lau, and Tai-Hung Chen – ITRI; Tsung-Fu Yang – Topco Scientific Company, Ltd.
14. ***Plasma Etch and Low Temperature PECVD Processes for Via Reveal Applications***
    Dave Thomas, Keith Buchanan, Hefin Griffiths, Kath Crook, Mark Carruthers, Oliver Ansell, and Dan Archard – SPTS Technologies
15. ***A Mobile TV/GPS Module by Embedding a GPS IC in Printed-Circuit-Board***
    Jong-In Ryu, Se-Hoon Park, Dongsu Kim, Jun-Chul Kim, and Jong-Chul Park – Korea Electronics Technology Institute
16. ***Coating Techniques for 3D-Packaging Applications***
    M. Töpper, M. Wilke, J. Röder, T. Fischer, and Ch. Lopper – Fraunhofer IZM
17. ***Void Formation during Reflow Soldering***
    Thomas D. Ewald – Robert Bosch GmbH, TU Dresden; Norbert Holle – Robert Bosch GmbH; Klaus-Jürgen Wolter – TU Dresden

Wednesday, May 30
Session 38: Interactive Presentations 2
2:00 p.m. - 4:00 p.m.
Committee: Interactive Presentations
Pavilion

Session Co-Chairs:
Swapan Bhattacharya – Georgia Institute of Technology
Rao Bonda – Amkor Technology

1. ***The Study of Silicon Passivation Polymer Adhesion to Epoxy Mold Compound Through Button Shear Strength***
   Shin Low and Inderjit Singh – Xilinx, Inc.; Takeshi Mori – Sumitomo Bakelite Co. Ltd.; Hironari Mori – Sumitomo Plastics America, Inc.
2. ***A General Co-Design Approach to Multi-Level Package Modeling based on Individual Single-Level Package Full-Wave S-Parameter Modeling Including Signal and Power/Ground Ports***
   Zhaoqing Chen – IBM Corporation
3. ***Sustained Damage and Remaining Useful Life Assessment in Lead-Free Electronics Subjected to Sequential Multiple Thermal Environments***
   Pradeep Lall, Mahendra Harsha, and Jeff Suhling – Auburn University; Kai Goebel – NASA Ames Research Center
4. ***Development of Micro-Alloying Method for Cu Pillar Solder Bump by Solid Liquid Interaction***
   Wen Yin, Fengwei Dai, Chongshen Song, Zhang Bo, and Lixi Wan – Chinese Academy of Sciences; Daquan Yu – Chinese Academy of Sciences, Jiangsu R&D Center for Internet of Things; Han Yu and Jiangyan Sun – Shanghai Sinyang Semiconductor Materials Co., Ltd.
5. ***Factors Affecting Pb-Free Flip Chip Bump Reliability Modeling for Life Prediction***
   Ahmer Syed, Gil Sharon, and Robert Darveaux – Amkor Technology
6. ***Optimized Reliability Test Design to Reduce Uncertainties in Reliability Assessment***
   Daeil Kwon and Alan E. Lucero – Intel Corporation
7. ***Design, Fabrication, and Calibration of Stress Sensors Embedded in a TSV Interposer in a 300mm Wafer***
   P.J. Tzeng, J.H. Lau, M.J. Dai, S.T. Wu, H.C. Chien, Y.L. Chao, C.C. Chen, S.C. Chen, C.Y. Wu, C.K. Lee, C.J. Zhan, and J.C. Chen – ITRI
8. ***Highly-Reliable Silicon and Glass Interposers-to-Printed Wiring Board SMT Interconnections: Modeling, Design, Fabrication and Reliability***
   Xian Qin, Nitesh Kumbhat, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology
9. ***Development of Damage-Less Wet-Chemical Silicon-Wafer Thinning Process for Three-Dimensional Integration***
   Naoya Watanabe and Masahiro Aoyagi – AIST; Takumi Miyazaki and Kazuhiro Yoshikawa – PRE-TECH AT Co., Ltd.
10. ***Nano Filler Dispersion in Polymer Composites for Electronic Packaging***
    Zhuo Li, Yi Gao, Kyoung-Sik Moon, and Allen Tannenbaum – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
11. ***Topology Bandpass Filter with Spiral Capacitors***
    Young K. Song, Chu Hsuan Sha, and Chin C. Lee – University of California, Irvine
12. ***Flexible System for Real-Time Plasma Decapsulation of Copper Wire Bonded IC Packages***
    J. Tang, J.B.J. Schelen, and C.I.M. Beenakker – Delft University of Technology
13. ***High Productivity and Damage-Free Ultrasonic Anisotropic Conductive Film (ACF) Bonding for Touch Screen Panel (TSP) Assemblies***
    Seung-Ho Kim and Kyung-Wook Paik – KAIST; Young-Jae Kim and Ho Joon Park – Samsung Electro-Mechanics Company, Limited

Thursday, May 31
Session 39: Interactive Presentations 3
9:00 a.m. - 11:00 a.m.
Committee: Interactive Presentations
Pavilion

Session Co-Chairs:
Ibrahim Guven – University of Arizona
Nam Pham – IBM Corporation

1. ***Aspects of Scaling to Mesoscale Models Derived from the Molecular Scale for Understanding Epoxy Interfaces***
   Nancy Iwamoto – Honeywell Performance Materials and Technologies
2. ***A Compact Thermal Model to Predict the Junction Temperature of High Power Light Emitting Diode Package***
   Run Hu, Zhangming Mao, Huai Zheng, Quan Chen, Sheng Liu, and Xiaobing Luo – Huazhong University of Science & Technology
3. ***Channel Design Methodology for 28Gbps SerDes FPGA Applications with Stacked Silicon Interconnect Technology***
   Namhoon Kim, Daniel Wu, Jack Carrel, Joong-Ho Kim, and Paul Wu – Xilinx, Inc.
4. ***Design, Modeling, and Fabrication of mm^3 Three-Dimensional Integrated Antennas***
   Peter Gadfort and Paul D. Franzon – North Carolina State University
5. ***Decoupling Optimization for IC-Package and PCB Systems Considering High Performance Microprocessor Core and Signal Interface Interactions***
   Om P. Mandhana – Sigrity, Inc.
6. ***Extraction of Electrical Properties of Nanomagnetic Materials through Meander-Shaped Inductor and Inverted-F Antenna Structures***
   Kyu Han, Madhavan Swaminathan, P. Markondeya Raj, Himani Sharma, K.P. Murali, and Rao Tummala – Georgia Institute of Technology; Vijay Nair – Intel Corporation
7. ***Reverse Wire Bonding and Phosphor Printing for LED Wafer Level Packaging***
   Jeffery C.C. Lo, S.W. Ricky Lee, Rong Zhang, and Mei Li – Hong Kong University of Science & Technology
8. ***Multiple Voltage-Supplies in TSV-Based Three-Dimensional (3D) Power Distribution Networks***
   Zheng Xu, Xiaoxiong Gu, Michael Scheuermann, Buckwell C. Webb, and John U. Knickerbocker – IBM Corporation; Kenneth Rose and Jiang Qiang Lu – Rensselaer Polytechnic Institute
9. ***Comprehensive, Scalable Design Guidance for Serpentine Time Delay Variation in Digital System***
   Jaemin Shin and Timothy Michalka – Qualcomm, Inc.
10. ***Investigation of Integrated Passive Device with Through-Silicon Via***
    Kai Liu, MaPhooPwint Hlaing, YongTaek Lee, HyunTai Kim, Gwang Kim, and Billy Ahn – STATS ChipPAC, Inc.; Robert Frye – RF Design Consulting
11. ***A New Methodology for Board-Level Harmonic Analysis of Multi-Level Packages***
    Cheng-fu Chen – University of Alaska, Fairbanks
12. ***Surface Plasmon-Assisted Terahertz Imaging Array***
    Kyoung Youl Park, Collin S. Meierbachtol, Nophadon Wiwatcharagoses, and Premjeet Chahal – Michigan State University
13. ***Modular Assembly of Diode Lasers in a Compact and Reliable Setup for a Wide Range of Applications***
    A. Sahm, C. Fiebig, S. Spießberger, E. Luvsandamdin, K. Paschke, G. Erbert, and G. Tränkle – Ferdinand Braun Institute; M. Schiemangk – Humboldt-Universität zu Berlin
14. ***Refined but Handy Electrical Models of TSV Useable from Low to High Density and for RF or Fast Digital Signals in 3D-IC***
    L. Fourneaud, T. Lacrevaz, C. Bermond, Y. Gaeremynck, and B. Flechet – Université de Savoie; J. Charbonnier and C.. Fuchs – CEA-LETI; A. Farcy – STMicroelectronics
15. ***Thermal Evaluation and Analyses of 3D IC Integration SiP with TSVs for Network System Applications***
    Heng-Chieh Chien, John H. Lau, Yu-Lin Chao, Ming-Ji Dai, and Ra-Min Tain – ITRI; L. Li, P. Su, J. Xue, and M. Brillhart – Cisco Systems, Inc.
16. ***The Effect of Sintering Profile and Printed Layer Variations with Inkjet-Printed, Large-Area Applications***
    Vesa Pynttäri, Eerik Halonen, Matti Mäntysalo, and Riku Mäkinen – Tampere University of Technology

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

17. ***Efficient Parametric Modeling and Analysis for Backplane Channel Characterization***
Xiaoxiong Gu, Michael Cracraft, Renato Rimolo Donadio, and Young Kwark – IBM Corporation; Ki Jin Han – IBM Corporation, Ulsan National Institute of Science and Technology
18. ***Non-Causal Behavior: The Cause for Concern***
Wesley Martin, Jerry Bartley, Matt Doyle, Richard Ericson, and George Zettles – IBM Corporation
19. ***Characterization of Al Wire Wedge Bonding in Power Electronics Package***
Yumin Liu, Yong Liu, Daren Keller, Suresh Belani, and Michael Dube – Fairchild Semiconductor Corporation

Thursday, May 31
Session 40: Interactive Presentations 4
2:00 p.m. - 4:00 p.m.
Committee: Interactive Presentations Pavilion

Session Co-Chairs:
Rao Bonda – Amkor Technology
Patrick Thompson – Texas Instruments, Inc.

1. ***Remedies to Control Electromigration: Effects of CNT Doped Sn-Ag-Cu Interconnects***
Sha Xu and Y.C. Chan – City University of Hong Kong; Xiaoxin Zhu, Hua Lu, and Chris Bailey – University of Greenwich; Hiren Kotadia and Samjid H. Mannan – King's College London
2. ***Cu and Al-Cu Composite-Material Interconnects for Power Devices***
Jamin Ling, Tao Xu, Raymond Chen, Orlando Valentin, and Christoph Luechinger – Kulicke and Soffa Industries, Inc.
3. ***Compliant Interconnects for Reduced Cost of a Ceramic Ball Grid Array Carrier***
Maaike M.V. Taklo, Andreas Larsson, and Astrid-Sofie Vardøy – SINTEF ICT; Helge Kristiansen – Conpart AS; Lars Hoff – Vestfold University College; Knut Waaler – WesternGeco AS
4. ***Novel Low-Volume Solder-on-Pad (SoP) Material and Process for Flip Chip Bonding using Au Stud Bumps***
Kwang-Seong Choi, Ho-Eun Bae, Su-Jeong Jeon, Hyun-Cheol Bae, and Yong-Sung Eom – ETRI
5. ***Design and Process Development of a Stacked SRAM Memory Chip Module with TSV Interconnection***
Shenglin Ma, Xin Sun, Yunhui Zhu, Zhiyuan Zhu, Qinghu Cui, Meng Chen, Yongqiang Xiao, Jing Chen, Wengao Lu, and Yufeng Jin – Peking University; Min Miao – Peking University, Beijing Information Science & Technology University
6. ***Bio-Inspired Surface Treatment on Touch Screen Panels (TSPs) for Adhesion Enhancement***
Il Kim, Seung-Ho Kim, Inseong You, Haeshin Lee, and Kyung-Wook Paik – KAIST
7. ***Low Slow-Wave Effect and Crosstalk for Low-Cost ABF-Coated TSVs in 3D IC Interposer***
Yu-Jen Chang, Tai-Yu Zheng, Hao-Hsiang Chuang, Chuen-De Wang, Yi-Chang Lu, Yih-Peng Chiou, and Tzong-Lin Wu – National Taiwan University; Peng-Shu Chen, Tzu-Ying Kuo, Chau-Jie Zhan, Shih-Hsien Wu, and Wei-Chung Lo – ITRI
8. ***Study of Pd Mixing during Pd-Cu Wire Ball Formation and Impact on Wire Bond Quality***
Flynn Carson, Jae Hak Yee, Soo San Park, and Edward Fontanilla – STATS ChipPAC
9. ***Vertical Tree 3-Dimensional TSV Clock Distribution Network in 3D IC***
Dayoung Kim, Joohee Kim, Junso Pak, and Joungho Kim – KAIST; Hyungdong Lee, Junho Lee, and Kunwoo Park – Hynix Semiconductor Inc.
10. ***Design of a Liquid Bridge Heat Switch System based on the Liquid Bridge Control for the Electronics Cooling***
Su-Heon Jeong, Sung-Ki Nam, and Sun-Kyu Lee – Gwang-ju Institute of Science and Technology; Wataru Nakayama – Thermtech International
11. ***Broad-Side Crosstalk Mitigation in Dual-Stripline Design***
Jimmy Hsu and Kai Xiao – Intel Corporation
12. ***Chip to Wafer Direct Bonding Technologies for High Density 3D Integration***
L. Sanchez, L. Bally, B. Montmayeul, F. Fournel, J. Dafonseca, E. Augendre, L. Di Cioccio, V. Carron, and T. Signamarcheix – CEA-LETI; R. Taibi and S. Mermoz – STMicroelectronics; G. Lecarpentier – SET
13. ***Microfluidic Chips Fabrication from UV Curable Adhesives for Heterogeneous Integration***
V.R.S.S. Mokkapati – National University of Singapore; Ole Bethge – Technical University of Vienna; Rainer Hainberger and Hubert Brueckl – Austrian Institute of Technology
14. ***Cost Trade-Off Analysis of PoP versus 3D TSV***
Chet A. Palesko and Alan C. Palesko – SavanSys Solutions, LLC; E. Jan Vardaman – TechSearch International, Inc.
15. ***High Density Compliant Contacting Technology for Integrated High Power Modules in Automotive Applications***
Paolo Nenzi, Rocco Crescenzi, Nicola Pio Belfiore, and Marco Balucani – University of Rome; Alexander Dolgyi, Alexy Klyshko, and Vitaly Bondarenko – Belarussian State University of Informatics and Radioelectronics
16. ***Development of Ultra Dense Edge Interconnects for Die to Die Connections based on Immersion Solder Bridging***
Dahwey Chu and Lauren E.S. Rohwer – Sandia National Laboratories
17. ***A Cost-Effective and Compact 28-Gb/s ROSA Module using a Novel TO-CAN Package***
Sae-Kyoung Kang, Joon Ki Lee, Joon-Young Huh, Jyung Chan Lee, and Kwangjoon Kim – Electronics and Telecommunications Research Institute
18. ***A New Approach towards an Optimum Design and Manufacture of Microfluidic Devices based on Ex Situ Fabricated Hydrogel based Thin Films' Integration***
Weiwei Zhao and Changqing Liu – Loughborough University; Tommaso Santaniello – Loughborough University, University of Milan; Patrick Webb – Manufacturing Technology Centre; Cristina Lenardi – University of Milan, Fondazione Filarete
19. ***Design and Fabrication of Low-Loss, Horizontal and Vertical Interconnect Links using Air-Clad Transmission Lines and Through Silicon Vias***
Rohit Sharma, Erdal Uzunlar, Vachan Kumar, Rajarshi Saha, Xinyi Yeow, Azad Naeemi, and Paul Kohl – Georgia Institute of Technology; Rizwan Bashirullah – University of Florida

Friday, June 1
Session 41: Student Posters
8:30 a.m. - 10:30 a.m.
Committee: Interactive Presentations Grande Ballroom A

Session Co-Chairs:
Mark Eblen – Kyocera
Patrick Thompson – Texas Instruments, Inc.

1. ***High-Efficient Optics for Different LED Packaging Types in Forward-Lighting Application***
Fei Chen and Sheng Liu – Huazhong University of Science and Technology; Kai Wang – Guangdong Real Faith Optoelectronics Inc.
2. ***Metamaterial Transmission Line Based Reconfigurable X-Band Phase Shifter Design***
Nophadon Wiwatcharagoses, Kyoung Youl Park, and Premjeet Chahal – Michigan State University
3. ***Phosphor Size Dependence of Lumen Efficiency and Spatial CCT Uniformity for Typical White LED Emitters***
Yun Shuai, Nguyen T. Tran, Jiun Pyng You, and Frank G. Shi – University of California, Irvine
4. ***Assembly and Alignment of Proximity Communication Enabled Multi-Chip Packages using Elastomeric Bump Interposers***
Hyung Suk Yang – Georgia Institute of Technology; Hiren D. Thacker, Ivan Shubin, John E. Cunningham, and James G. Mitchell – Oracle
5. ***The Process and Reliability Tests of Glass-to-Glass Laser Bonding for Top-Emission OLED Device***
Yuneng Lai, Zunmiao Chen, Yuanhao Huang, and Jianhua Zhang – Shanghai University
6. ***60 GHz Tapered-Helix Antenna for WPAN Applications***
Paolo Nenzi, Francesco Tripaldi, Frank Silvio Marzano, Fabrizio Palma, and Marco Balucani – University of Rome
7. ***Resonance-Based Addressing in Laminate MEMS Devices***
Minfeng Wang, Yang Zhang, G.P. Li, and Mark Bachman – University of California, Irvine
8. ***A Study on the Intermetallic Growth of Fine-Pitch Cu Pillar/SnAg Solder Bump for 3D-TSV Interconnection***
Yong-Sung Park, Ji-Won Shin, Yong-Won Choi, and Kyung-Wook Paik – KAIST
9. ***Double Stub Matching in Multilayered Printed Circuit Board using Vias***
Andreas Hardock, Renato Rimolo-Donadio, Heinz-Dietrich Brüns, and Christian Schuster – TU Hamburg-Harburg
10. ***Highly Compact Surface Micromachined Metamaterial Circuits using Multilayers of Low-Loss Benzocyclobutene for Microwave and Millimeter Wave Applications***
David E. Senior – University of Florida, Universidad Tecnológica de Bolívar; Xiaoyu Cheng and Yong-Kyu Yoon – University of Florida
11. ***40μm Ag/Au Composite Flip-Chip Interconnect using Solid State Atomic Bonding at 200°C***
Wen P. Lin, Chu-Hsuan Sha, and Chin C. Lee – University of California, Irvine
12. ***Nanomanufacturing of Large Area Carbon Nanofibers using Tube Nozzle Electrospinning (TNE), Lithography and Carbonization Processes***
Pit Fee Jao, Sheng-Po Fang, David E. Senior, Kyong Tae Kim, and Yong-Kyu Yoon – University of Florida
13. ***Embedded Actives for Terahertz Circuit Applications: Imaging Array***
Xianbo Yang and Premjeet Chahal – Michigan State University
14. ***Vertically Aligned Nickel Nanowire/Epoxy Composite for Electrical and Thermal Conducting Material***
Hyeong-Gi Lee and Kyung-Wook Paik – KAIST
15. ***A Compact 100 MHz to 7 GHz Frequency Equalizer based on Distributed Passive Circuits***
Xiaoyu Cheng, David E. Senior, and Yong-Kyu Yoon – University of Florida
16. ***Low Latency High Throughput Memory-Processor Interface***
Qidong Wang, Daniel Guidotti, Jie Cui, Liqiang Cao, Tianchun Ye, and Lixi Wan – Chinese Academy of Sciences; Fujiang Lin and Guang Zhu – University of Science and Technology of China; Qian Wang – Tsinghua University
17. ***Metamaterial-Inspired Miniaturized Microwave Sensing Probes***
Nophadon Wiwatcharagoses, Kyoung Youl Park, and Premjeet Chahal – Michigan State University
18. ***Active Cooling Analysis of the Micro Pump used in IGBT Power Module***
Ling Xu, Yang Zhou, Yang Zhang, Bulong Wu, Mingxiang Chen, Xiaobing Luo, and Sheng Liu – Huazhong University of Science & Technology
19. ***Liquid Encapsulation for Monochromatic LED Emitter Packages: Enhancement of Thermal-Optical Performance and Reliability***
Jiun Pyng You, Yu-Chou Shih, Yeong-Her Lin, Bohan Yan, and Frank G. Shi – University of California, Irvine
20. ***A Novel Wafer-Level Metal/BCB Interconnection between Both Sides of Wafer using TSV and Its Microwave Performance***
Jiajie Tang, Xiao Chen, Gaowei Xu, and Le Luo – Chinese Academy of Sciences
21. ***An Investigation on Structure and Materials of Laminated Organic Solar Cell Packaging***
Xing Chen, Simin Wang, Zhang Luo, Shengzhi Zhang, Zhicheng Lv, Hao Jiang, and Sheng Liu – Huazhong University of Science & Technology
22. ***Robust, Novel, and Low Cost Superhydrophobic Nanocomposites Coating for Reliability Improvement of Microelectronics***
Yan Liu, Ziyin Lin, and Kyoung-sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
23. ***ZnO Quantum Dots-Filled Encapsulant for LED Packaging***
Yan Liu, Ziyin Lin, Xueying Zhao, and Kyoung-sik Moon – Georgia Institute of Technology; Sehoon Yoo – Korea Institute of Industrial Technology (KITECH); C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
24. ***Combination of Translucent Eu:YAG Glass Ceramic with LED Chip***
Liang Yang, Zhicheng Lv, Mingxiang Chen, and Sheng Liu – Huazhong University of Science & Technology
25. ***The Role of Friction Coefficient on the Stitch Bondability in Pd Coated Cu and Bare Cu Wire Bonding***
A. Rezvani, C. Nan, and M. Mayer – University of Waterloo; I. Qin – Kulicke and Soffa, Inc.
26. ***Novel Core-Shell Nanocomposites for RF Embedded Capacitors: Processing and Characterization***
Warda Benhadjala, Isabelle Bord, Laurent Béchou, and Yves Ousten – Université de Bordeaux; Ephraim Suhir – University of California, Santa Cruz; Matthieu Buet and Fabien Rougé – Polyrise SAS
27. ***Reliability and Microstructural Studies of Sn-Ag-Cu Lead-Free Solder Joints in Pulse-Heated Reflow Soldering***
M. Mostofizadeh, K. Kokko, and L. Frisk – Tampere University of Technology

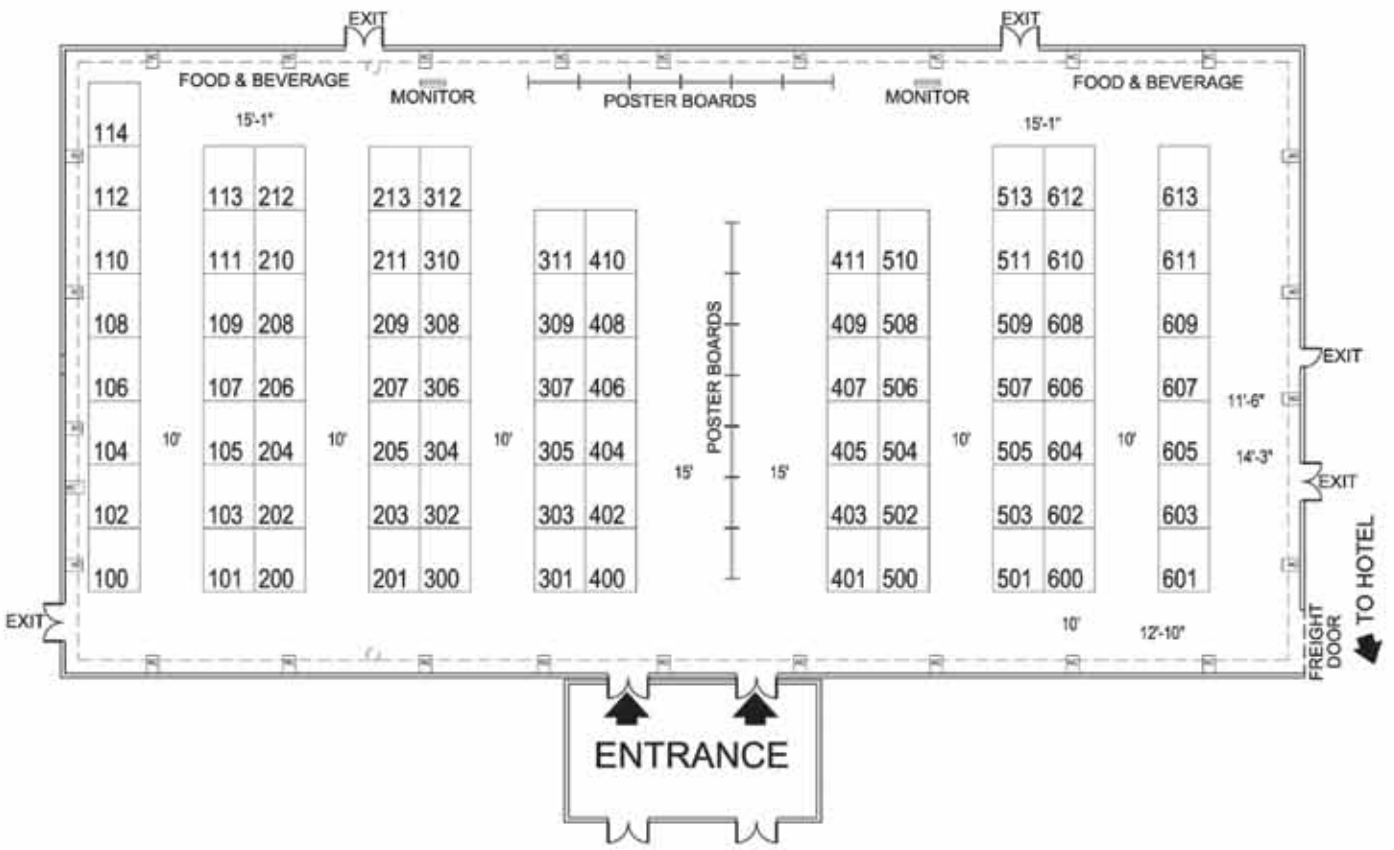
TECHNOLOGY CORNER BOOTH AND POSTER LAYOUT

Technology Corner Exhibits

Wednesday, May 30, 2012 • 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.
Thursday, May 31, 2012 • 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.

Interactive Presentation Sessions

Wednesday, May 30, 2012 morning Interactive Presentations • 9:00 a.m. - 11:00 a.m.
Wednesday, May 30, 2012 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.
Thursday, May 31, 2012 morning Interactive Presentations • 9:00 a.m. - 11:00 a.m.
Thursday, May 31, 2012 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.



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Nikon Metrology offers the most complete metrology product portfolio, including X-ray and Computed Tomography inspection systems and state-of-the-art vision measuring instruments featuring optical and mechanical 3D metrology solutions. These innovative metrology solutions respond to the advanced inspection requirements of manufacturers active in aerospace, electronics, automotive, medical, consumer and other industries.

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Nordson DAGE is the market leading provider of award winning test and inspection systems for destructive and non-destructive mechanical testing of electronic components and is recognized as the industry standard. Nordson DAGE continues to invest significantly in research and development to remain at the cutting edge of bond testing technology. The 4000PLUS platform compliments the range of test systems for both traditional and the more specialist applications such as ribbon pull, BGA sphere and package fatigue, PCB 3 point bend testing, and hot bump pull for PCB pad cratering testing in accordance with IPC9708.The 4000HS high speed bondtester, capable of testing solder bumps in high speed shear and high speed cold bump pull modes, is becoming a viable alternative to board level drop testing. In addition to highly accurate force measurements, the 4000HS provides bond energy results, including total and fractional values. Bond energy values are proving invaluable for failure mode analysis, particularly in the detection of lead-free brittle fractures. Furthermore, they can be used to evaluate various materials (alloys, UBM, finish, substrate) and to monitor bumping production processes. The tool has applications in development, failure analysis, QA and production. Nordson DAGE also provides 2D and CT X-ray inspection systems, including the flagship, award-winning XD7600NT Diamond FP, which have been specifically and ergonomically designed for the printed circuit board (PCB) and semiconductor industries. These X-ray inspection systems provide high resolution nano-focus analysis not only within failure analysis laboratories but also within the production environment. The unique Nordson DAGE NT sealed-transmissive type of X-ray tube is at the heart of the Nordson DAGE NT X-ray inspection systems. It supersedes and out-performs the closed and open tube types that are available in earlier systems. The sealed-transmissive tube is the only way to genuinely improve X-ray image resolution whilst still providing true high power and all without compromising the resolution and magnification. The new X-Plane™ Analysis system option allows X-ray inspection in any plane without cutting the board.

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Pac Tech is one of the leading subcontractor houses for wafer bumping. The emphasis is concentrated on a low cost electroless bumping process on wafer level, based on Ni/Au as an Under Bump Metallization (UBM) and solder application (eutectic PbSn or lead-free) by stencil printing. This process is suitable for 4, 5, 6, 8 and 12 inch wafers with Al- or Cu-metallization. Pac Tech offers also manual and fully automatic equipment for electroless Ni/Au bumping on Al and Cu metallization, as well as completes turnkey solutions which include the transfer of the technology and delivery of chemicals. Furthermore, Pac Tech builds laser based bumping (SB2) and Flip-Chip assembly (Laplace) equipment. The SB2 equipment is suitable for fluxless solder jetting on R&D for CSP, BGA, Flip Chip, HDD and MEMS as well as for automated production environments. The Laplace (Laser Placer) FlipChip bonder offers low stress assembly solutions for flex and rigid substrates, like LCD drivers, RFID labels, MEMS and optical devices, SIP applications.

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Palomar Technologies, a former subsidiary of Hughes Aircraft, is the global leader of automated high-accuracy, large work area die attach and wire bond equipment and precision contract assembly services. Customers utilize the products, services and solutions from Palomar Technologies to meet their needs for optoelectronic packaging, complex hybrid assembly and micron-level component attachment.

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Pure Technologies manufactures low (0.02, 0.01 cph/cm^2), ultra-low (0.005, 0.002 cph/^{2}) and super ultra-low (<0.001 cph/cm^2) alpha emitting Tin (Sn), Lead-Free (including all SAC) alloys, Pb and Pb/Sn alloys. These *ALPHALO*® products are available in various shapes and sizes – ingots, anodes, slugs, pellets, foil, rods, bricks, PbO and SnO powder, etc. for wafer-level packaging, interconnects, and sphere and powder/paste manufacturing. *ALPHA-LO*® reduces or eliminates soft errors from alpha particle emissions from solders, enhances performance reliability and reduces corporate liability. All materials are guaranteed and certified to be at secular equilibrium and are tested and retested over time before shipping to insure that the alpha emission rate is stable and will not increase over time.

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QualiTau offers a variety of reliability and parametric test equipment for the characterization and development of new materials used in the manufacture of Integrated Circuits. The DSPT 9012 (Desktop Semiconductor Parametric Tester) is a PC Controlled SMU test instrument built specifically for semiconductor device characterization and testing. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection, Dielectric Breakdown, Solder Bump at up to 8 Amps, and Electromigration at test temperatures up to 450°C.

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Quik-Pak, a division of Delphon Industries, provides IC packaging and assembly services. The company's newest offering is its OmPP package. These pre-molded QFN packages are cost-effective, come in a variety of sizes and are ideal for prototype or production volume applications. Quik-Pak also specializes in a variety of services that together provide a full turn-key solution including wafer preparation, die/wire bonding, remolding and marking/branding. Custom assembly services are also offered for Flip Chip, Ceramic Packages, Chip-on-Board, Stacked Die, MEMS, etc

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RTI International's Center for Materials and Electronic Technologies is a world leader in advanced interconnect and packaging technologies. RTI provides access to state of the art wafer bumping and WLP technologies, supporting small and mid-volume customers as well as developmental applications. As a recognized leader in 3D integration, RTI has developed a comprehensive platform of technologies and works with commercial, government, and academic clients from around the world to develop and implement solutions. In addition to its focus on advanced interconnect technologies, RTI also conducts research and development in sensors and actuators, electronic material characterization, and novel device microfabrication. The Center is staffed with full time engineers and researchers developing new technologies and solutions in conjunction with our clients. Fully integrated fabrication and analytical facilities allow RTI to support a diverse project base, from process development, proof of concept and prototyping, to small-scale production.

RTI International is a non-profit research institute offering innovative research, technical expertise, and fabrication capabilities to governments and businesses worldwide.

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SET, Smart Equipment Technology (Former Suss MicroTec Device Bonder Division) is a world leading supplier of High Accuracy Assembly and Nano Imprint Lithography Solutions. As a supplier of semiconductor equipment dedicated to high-end applications for over 30 years and with more than 300 Device Bonders installed worldwide, SET is globally renowned for the unsurpassed bonding accuracy (± 0.5 µm) and the high flexibility of its die and flip-chip bonders. SET's product portfolio ranges from manual loading versions to fully automated operation. The SET systems cover a wide range of bonding applications and offer the unique ability to handle both fragile and small components onto substrates up to 300mm.

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Shin-Etsu Microsi, Inc. is a wholly owned subsidiary of Shin-Etsu Chemical Ltd. Shin-Etsu MicroSi is a world class supplier of packaging materials for the semiconductor industry. With a global support network, which includes Sales Engineers, R&D, Manufacturing, Quality Assurance, and Logistics, we are able to quickly develop and provide new technologies to benefit our customers. This allows our clients to meet their ever changing technical, commercial and environmental needs by implementing Shin-Etsu MicroSi's technology. Shin-Etsu MicroSi is known for supplying high performance Thermal Interface Materials, Underfills, Molding Compounds, High Purity Silicone Encapsulants, and Die Attach Materials.

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Shinko Electric Industries Co., LTD. is a leading manufacturer of a wide variety of materials used in the packaging of integrated circuits such as: Organic Substrates, Leadframes, TO-Headers and Heatspreaders. With headquarters located in Nagano, Japan and offices worldwide, Shinko strives to provide the ultimate in service and solutions for our customers. For more about Shinko please visit our website at www.shinko.com.

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SIGRITY provides software tools and technical services for power, ground and signal integrity analysis of high performance IC packages and printed circuit boards. SIGRITY analysis tools utilize a fast electromagnetic field solver that takes into account coupling between vias, reflection from edges, resonance, power and ground voltage fluctuations, and electromagnetic radiation. SIGRITY's package physical design products provide eDriven capability and facilitate design reuse. Worldwide leading companies as well as high-tech start-ups have successfully adopted SIGRITY's software tools for applications in various pre- and post-layout power and signal integrity analyses.

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Founded in 1973 and headquartered in Chicago, IL, Sonoscan®, Inc. is a worldwide leader and innovator in Acoustic Micro Imaging (AMI) technology. Sonoscan manufactures and markets acoustic microscope instruments and accessories to nondestructively inspect and analyze products. Our C-SAM® scanning acoustic microscope provides unmatched accuracy and robustness setting the standard in AMI for the inspection of products for hidden internal defects such as poor bonding, delaminations between layers, cracks and voids. In addition, Sonoscan offers analytical services through regional testing laboratories in Asia, Europe and the U.S. and educational workshops for beginners to advanced on AMI technology.

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SPTS Technologies designs, manufactures, sells, and supports etch, PVD, CVD and thermal capital equipment and process technologies for the global semiconductor and micro-device industries, providing advanced wafer processing solutions to MEMS, advanced packaging, LED, high speed RF device, and power management markets.

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STATS ChipPAC is a leading service provider of semiconductor packaging design, bump, probe, assembly, test and distribution solutions. A trusted partner to leading semiconductor companies worldwide, STATS ChipPAC provides fully integrated, multi-site, end-to-end packaging and testing solutions that bring products to market faster. With advanced process technology and a global manufacturing presence spanning Singapore, South Korea, China, Malaysia and Thailand, STATS ChipPAC offers a full range of backend turnkey services for a wide variety of electronics applications. STATS ChipPAC has a leadership position in advanced package technology such as fan-in and fan-out wafer level packaging, flip chip interconnect, Through Silicon Via, 2.5D and 3D integration to meet the increasing market demand for next generation devices with higher levels of performance, increased functionality and compact sizes.

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SUSS MicroTec - Shaping the Future
With over 60 years of engineering experience and thousands of active systems installed worldwide, SUSS MicroTec is amongst the leading suppliers of process equipment for semiconductors and related markets. The solution portfolio covers all performance steps for photomask and wafer processing ranging from cleaning, coating, baking, developing, aligning, to wafer bonding and is complemented by micro-optical components.

From Advanced Packaging to 3D Integration
SUSS MicroTec has been at the forefront of companies supporting the advanced packaging industry with dedicated lithography solutions. With the trend leading towards 3D architectures for IC integration and packaging, we support 3D Packaging and 3D Interconnect processes with precision equipment for thick resist and high topography applications, Through-Silicon-Via (TSV) manufacturing, bonding and de-bonding solutions, stacking technologies as well as products for the production of CMOS image sensors.

MEMS and Compound Semiconductor Manufacturing
With a full range of wafer-processing equipment and extensive experience in warped wafer handling solutions, SUSS MicroTec has positioned itself as the leader in high-volume Micro-Electro-Mechanical-Systems (MEMS) manufacturing. Our equipment is specifically designed to handle non-standard substrates like fragile compound semiconductors and incorporates specialized hardware such as coaters, aligners and bonders optimized for LED manufacturing.

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Tamar Technology develops and manufactures high-speed non-contact metrology solutions for 3DIC advanced packaging and related processes for MEMS, CMOS image sensors, compound semiconductors, LED, and other market areas.

Tamar's proprietary sensor technology offers maximum flexibility and includes their Optical Stylus Probe (OSP), Wafer Thickness Sensor (WTS), and Visible Thickness Sensor (VTS) to support a variety of applications.

The measurement capability provided by these sensors include through silicon via (TSV) depth with unlimited aspect ratio, wafer thickness and total thickness variation (TTV) for single and multi-layer wafers, remaining silicon thickness (RST), wafer shape, thin Si thickness, thick films and polymer thickness, and other critical measurement requirements.

Tamar's WaferScan system is modular in design so the user can configure it with one or more sensors to maximize the measurement flexibility and value. The system can be configured for semi or fully automated operation and the high speed data rates allow the user the flexibility to integrate the measurement technology in-line to monitor production real-time depending on process requirements.

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Manufacturer of LASER SYSTEMS, UV STEPPERS, UV SCANNERS and MASK ALIGNERS. Tamarack supplies photolithography and laser micromachining systems. We specialize in applications including: LASER DEBONDING 3D TSV; WLFO & WLCSP; Solar Cells, Organic Electronics, MEMS, Medical Devices and HDI. Our Excimer and Solid State ablation systems are ideal for direct pattern etching thin metals from wafers to seed layer removal or other electronic circuits. In addition, laser drill RDL Vias and Trenches for WLCSP with selective material removal, down to 1um. Systems designed for 300mm, Roll-to-Roll, Reel-to-Reel and Sheet handling. Resolution capabilities to 1um. Machines designed for 24/7 production environments.

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TechSearch International, Inc. was founded in 1987 as a market research and consulting company specializing in emerging semiconductor packaging trends. Multi- and single-client services encompass market research, technology trends, strategic planning, and technology licensing. Research topics include wafer level packaging, flip chip interconnect, CSPs, BGAs, 3D integration with TSVs, manufacturing in China and India, multichip packages (MCPs) such as stacked die CSPs and System-in-Package (SiP), embedded components, microvia substrates, LED assembly, and Pb-free manufacturing. Market forecasts and trends in advanced semiconductor packages and materials are available. In conjunction with SavanSys Solutions, wire bond, flip chip and WLP trade-off cost models are offered. TechSearch International professionals have an extensive network of more than 15,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

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For over 50 years TOK has been supplying superior quality chemicals and equipment to the microelectronics and semiconductor manufacturers of the world. TOK is now offering materials and equipment to enable fabrication of 3DIC with TSVs. These products include photoresists for plating (Au, Ni, Cu, Pb/Sn, SN/Ag), photo definable insulators, and the "Zero Newton" system, an innovative turn-key solution for temporary wafer handling that can be tailored to meet the demanding needs of companies on the forefront of 3DIC packing technology. Please visit our booth to learn more about TOK's products and how TOK can help you solve your most challenging advanced packaging requirements.

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Toray Engineering Co., Ltd provides Flip Chip Bonding Equipment for Semiconductor Packaging (FC 2000), Optoelectronics (OF2000) and LCD devices (CL2000FW, OS2000). Also, Vacuum Encapsulation Equipment (VE500) and various Flexible substrates (TCP,interposer) manufacturing equipment such as resist coater, proximity exposer, etching, developing line are available.

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Torrey Hills Technologies, LLC is a leader in developing and delivering quality yet affordable component parts and production equipment for multiple industries. Its wide range of products include tungsten-copper, molybdenum-copper, Cu/Mo/Cu, Cu/Mo70Cu/Cu heat sinks, and fast fire and infrared belt furnaces that can work in a variety of atmospheres serving both electronics and solar cell industries. Headquartered in San Diego, CA, its mission is to help customers achieve higher profitability by the provision of innovative products and services.

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Ushio America, a leading global supplier of semiconductor fabrication equipment, subsystems and components, has engaged in development, manufacturing and sales in a wide range of product fields. As a world premier photolithography light source provider, the Ushio Group leverages the industry's most advanced development capabilities to meet the increasingly sophisticated and divergent product requirements of the global semiconductor industry.

Ushio offers wide range lithography systems, including the full-field projection exposure equipment, UX4-3Di FFPL300, WLP stepper UX7-3Di STEP300 and stepper for organic substrate, UX5-3Di STEP500. Subsystems and components solutions for Nano Imprints Lithography templates cleaning subsystems, mask cleaning subsystems, UV LED components, EUV Lithography Source subsystems as well as the industry-benchmarked superior UV lamps are also available.

Ushio provides manufacturing solutions for a wide range of semiconductor process applications including 2.5D and 3D packaging, EUV lithography, NGL, LEDs and compound semiconductors.

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XYZTEC, a leading global supplier of bond test equipment, offers the most flexible bond testing platform on the market today! The Condor series features a single platform with multiple test capabilities allowing end-users the added flexibility of performing many types of tests all on one system. In addition to standard bond testing applications such as wire pull, ball shear, die shear, the Condor series has the capability to perform peel testing, push testing, high impact testing, fatigue testing, and creep testing.

XYZTEC is the only bond test supplier that offers a Revolving Measurement Unit, featuring four different measurement sensors to address 80% of your test requirements. The joysticks are ergonomically friendly, easily move the XY stage to the desired position, and feature 12 logically arranged buttons for increased operator efficiency. The Condor EZ software features onboard graphics and intelligent wizards, providing intuitive operator control as well as sophisticated SPC software thus ensuring complete documentation of the test protocol. Check out our new web site at www.xyztec.com.

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Yield Engineering Systems (YES) provides a wide variety of processing equipment including high reliability polymer processing tools for WLP type processes and plasma systems for underfill treatment.

YES manufactures quality equipment for the Semiconductor, Photovoltaic, FPD, MEMS, Medical, Nanotech Industries and more.

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Beginning in 1998 with Yole Développement, we have grown to become a group of companies providing market research, technology analysis, strategy consulting, media in addition to finance services. With a solid focus on emerging applications using silicon and/or micro manufacturing Yole Développement group has expanded to include more than 40 associates worldwide covering MEMS, MedTech, Advanced Packaging, Compound Semiconductors, Power Electronics, LED, and Photovoltaics. The group supports companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

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Zeon Corporation, a leading Japanese technology polymer company, and subsidiary Zeon Chemicals L.P., USA have developed two innovative state-of-the-art packaging materials: 1) "Ultra-Low Loss Build-Up Film" used for Build-Up substrate for IC packages, GPU, WLP, Si Interposer and any application requiring superior electrical properties, and 2) "Ultra-Low Loss PCB Materials" low-loss laminate for both high k and low k applications such as milli-wave radars, high-speed servers and circuits, and RF/mobile applications for technology leading devices. "Ultra-Low Loss Build-Up Film" provides high density, high speed, and reliable IC or GPU packages with properties such as low CTE, 4/4um L/S, low dielectric constant, low loss tangent, and low moisture absorption. In addition to those properties, it allows forming very fine copper lines on high smooth surfaces, with its Ra around 70nm while maintaining superior peel strength performance. Ultra-Low Loss PCB Materials: Both prepreg and copper-clad laminate are available to form multilayer printed-circuit board with the strength of extremely low loss tangent, high modulus, 20/20um or even less L/S with ultra-smooth surface, and either high or low dielectric constant depending on the desired application. The low k variety is ideal for high-performance servers, as well as milli-wave applications where conventional products fall short either in signal integrity or challenges in high cost processing. The high k version is an ideal replacement for LTCC where high performance and miniaturization are roadmap items.

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Booth 410

Adhesives and encapsulants for electronics and optoelectronics assembly. Products include electrically conductive and thermally conductive adhesives, ultra-low stress adhesives, ACPs and NCPs, UV curable glob top encapsulants, and underfill and reworkable underfill encapsulants for flip chips, WLPs, CSPs, BGAs, and POPs.

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First Call For Papers

63rd Electronic Components and Technology Conference

www.ectc.net

To be held May 28 - May 31, 2013

Cosmopolitan of Las Vegas, Las Vegas, Nevada, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:

3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, optoelectronic & photovoltaic device packaging.

Applied Reliability:

3D package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:

Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:

Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:

Emerging packaging concepts and technologies, emerging 3D packaging concepts, novel approaches to packaging, organic IC & TFT, microfluidics and MEMs, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:

Design, structure, processes, performance, reliability (including electromigration), and test of first- and second-level interconnections. Interconnections for 3D integration including TSV and silicon interposers; interconnections in substrates, PCBs and systems. Solder bumping and Cu-pillar for flip chip packaging, wafer-level packaging, advanced wirebond interconnections, non-solder interconnections and connectors.

Materials & Processing:

Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 3D.

Modeling & Simulation:

Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, fracture and warpage in packages, and high-speed interconnects.

Optoelectronics:

Optical system integration and photonic system-in-package, power efficient optical subsystems, fiber optical interconnects, optical-PCB, active optical cables, optical transceivers, optoelectronic assembly and reliability, high-efficiency LEDs and high power lasers, integrated optical sensors, silicon photonics, polymer and thin glass based waveguide technology.

Interactive Presentations (formerly Posters):

Papers may be submitted on any of the listed major topics and presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentation papers allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting into topic of an oral session, highly rated abstracts that are submitted specifically for interactive presentation, or abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

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Abstracts must be received by October 8, 2012. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 8, 2012. If you have any questions, contact:

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The Cosmopolitan of Las Vegas
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The spectacular city of Las Vegas awaits you in 2013. As the entertainment capital of the world, there are over 100 spectacular live shows and entertainment venues to see daily. Las Vegas also touts world-class cuisine with an array of restaurants by world famous chefs.

One of the newest attractions to Las Vegas is The Cosmopolitan hotel itself. Located directly adjacent to the world-renown Bellagio and its famed fountain show, the Cosmopolitan is of the newest hotels in Vegas. The hotel itself is a $4 billion stunning architectural statement with a chandelier bar that spans two stories. It also has some of the country's top chefs, three distinctive pools, and 44,000 square feet of salon, spa, and fitness areas.

Should you want to put aside Vegas' bright lights and casinos, visit many of the natural wonders that surround this city. Over five major parks and wonders are in close proximity. From Red Rock Canyon to Death Valley or Hoover Dam to Grand Canyon National Park, there is so much to do and see.

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Conference At A Glance

Monday, May 28, 2012

3:00 p.m. – 5:00 p.m.
Registration – Bayview Foyer
Marina Tower

Tuesday, May 29, 2012

6:45 a.m. – 8:15 a.m.
AM PD Courses
Registration Only
Registration – Bayview Foyer,
Marina Tower

7:00 a.m. – 7:45 a.m.
PD Courses Instructor and
Proctors Briefing & Breakfast
Executive Center 4

7:00 a.m. – 5:00 p.m.
Speakers Prep – Marina 3

8:00 a.m. – Noon
AM PD Courses
See page 8 for locations

9:00 a.m. – 5:00 p.m.
iNEMI Roadmap Meeting
Nautilus 3

10:00 a.m. – Noon
Special Session
Nautilus I

10:00 a.m. – 10:20 a.m.
AM PD Course Break
Harbor Island Foyer

11:00 a.m. – 1:15 p.m.
Conference Registration
PM PD Courses Registration Only
Bayview Foyer, Marina Tower

Noon
PD Courses Luncheon
Grande Ballroom A

1:00 p.m. – 5:00 p.m.
Technology Corner Set-up
Pavilion

1:15 p.m. – 5:00 p.m.
Conference Registration
Bayview Foyer, Marina Tower

1:15 p.m. – 5:15 p.m.
PD PM Courses
See page 8 for locations

3:00 p.m. – 3:20 p.m.
PM PD Course Break
Harbor Island Foyer

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Executive Center Break Area

6:00 p.m. – 7:00 p.m.
General Chair's Speakers
Reception (by Invitation)
Grande Ballroom A

7:30 p.m. – 9:00 p.m.
Panel Session
Harbor Island I & II

Wednesday, May 30, 2012

6:45 a.m. – 4:00 p.m.
Conference Registration
Bayview Foyer, Marina Tower

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Grande Ballroom B

7:00 a.m. – 5:00 p.m.
Speakers Prep – Marina 3

8:00 a.m. – 4:00 p.m.
Companion Hospitality Room
Rooms 411 and 415 (5th Floor)

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4 , 5, 6
See pages 10 thru 11 for
Locations

9:00 a.m. – 11:00 a.m.
Session 37: Interactive
Presentations I
Pavilion

9:00 a.m. – Noon
Technology Corner Exhibits
Pavilion

9:15 a.m. – 10:00 a.m.
Refreshment Break
Pavilion

Noon
ECTC Luncheon
Grande Ballroom A - C

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Pavilion

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12
See pages 12 thru 13 for
Locations

2:00 p.m. – 4:00 p.m.
Session 38: Interactive
Presentations 2
Pavilion

2:45 p.m. – 3:30 p.m.
Refreshment Break
Pavilion

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Pavilion

7:00 p.m. – 9:00 p.m.
Plenary Session
Harbor Island I & II

Thursday, May 31, 2012

7:00 a.m. – 5:00 p.m.
Speakers Prep
Marina 3

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Grande Ballroom B

7:30 a.m. – 4:00 p.m.
Conference Registration
Bayview Foyer, Marina Tower

8:00 a.m. – 4:00 p.m.
Companion Hospitality Room
Rooms 411 and 415 (5th Floor)

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14 thru 15 for
Locations

9:00 a.m. – 11:00 a.m.
Session 39: Interactive
Presentations 3
Pavilion

9:00 a.m. – Noon
Technology Corner Exhibits
Pavilion

9:15 a.m. – 10:00 a.m.
Refreshment Break
Pavilion

Noon
CPMT Luncheon
Grande Ballroom A - C

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Pavilion

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16 thru 17 for
Locations

2:00 p.m. – 4:00 p.m.
Session 40: Interactive
Presentations 4
Pavilion

2:45 p.m. – 3:30 p.m.
Refreshment Break
Pavilion

6:30 p.m. – 7:30 p.m.
Gala Reception
Bayview Lawn Area
Rain Backup:
Grande Ballroom B - C

8:00 p.m. – 10:00 p.m.
CPMT Seminar
Harbor Island I & II

Friday, June 1, 2012

7:00 a.m. – 5:00 p.m.
Speakers Prep
Marina 3

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Grande Ballroom B

7:30 a.m. – Noon
Conference Registration
Bayview Foyer
Marina Tower

8:00 a.m. – Noon
Companion Hospitality Room
Rooms 411 and 415 (5th Floor)

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18 thru 19 for
Locations

8:30 a.m. – 10:30 a.m.
Student Poster Session
Grande Ballroom A

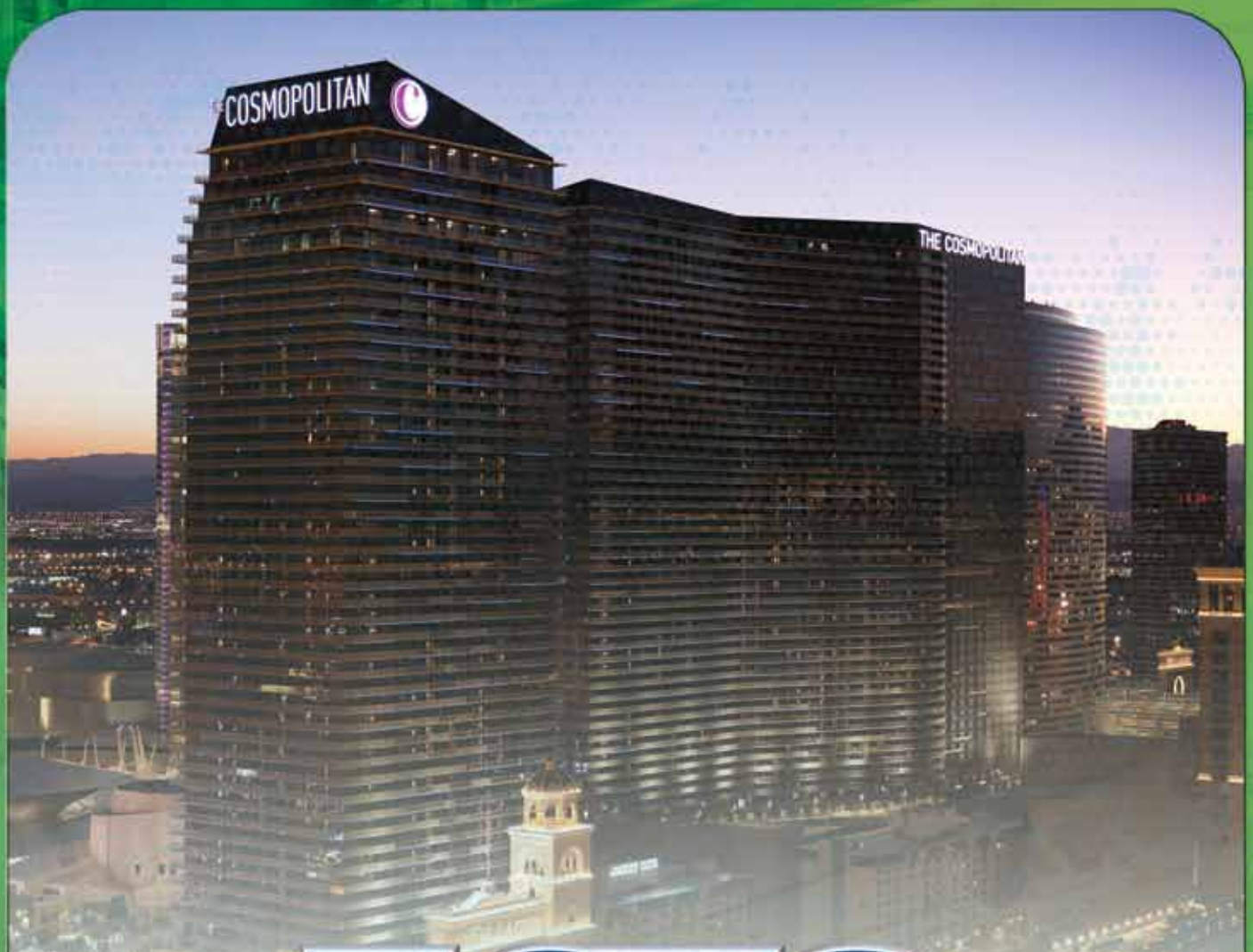
9:15 a.m. – 10:00 a.m.
Refreshment Break
Southern Hemisphere Ballroom
Harbor Island Foyer

Noon
Program Chair Luncheon
Grande Ballroom B - C

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20 thru 21 for
Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Harbor Island Foyer

***All ECTC events will be taking place in the Sheraton San Diego Hotel & Marina ***



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