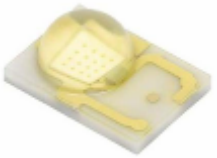
# LED Manufacturing:

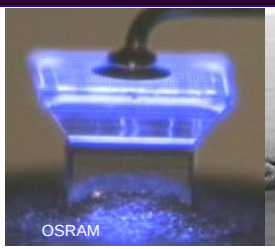
## Could Silicon Displace Sapphire?

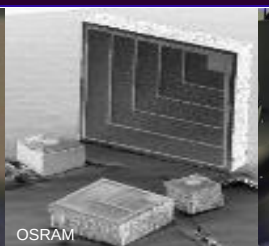

Verticle Inc


Lumileds


Aixtron


CREE


OSRAM


OSRAM


Cascade Microtec

YOLE DÉVELOPPEMENT

**75 cours Emile Zola, F-69100 Lyon-Villeurbanne, France**
**Tel: +33 472 83 01 80 – Fax: +33 472 83 01 83**
**Web: http://www.yole.fr**

# LED Prices: where do we stand?

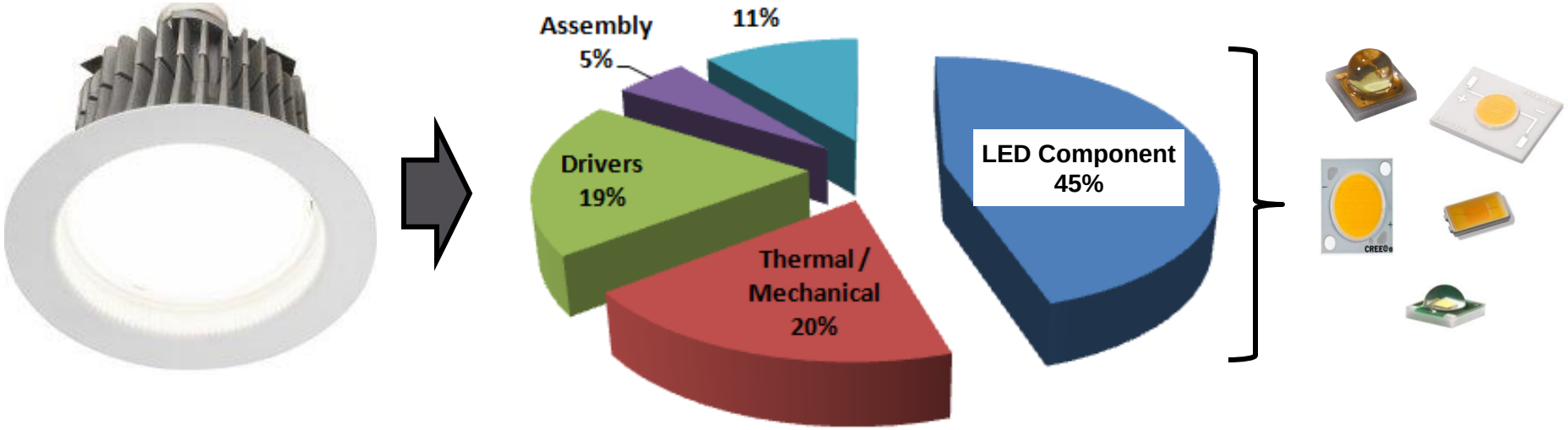
## LED price already “right” for some applications but need further improvements for others.




*All sources: 60 W equivalent ~ 800 lumens, warm White, tier 1 brand only, typical price in the US

# Luminaire Cost Structure

## The packaged LED is only one contributor but represents the single largest BOM opportunity:




*Downlight picture: CREE LR6, Cost breakdown from DOE SSL roundtable 2011, Packaged LED pictures: Cree, Everlight, Osram, Philips Lumileds.*

# The Path to Cost Reduction

$$\text{Cost} = \frac{\$\$}{\text{Lumen}}$$

**Manufacturing Cost**

- *Higher equipment throughput*
- *Higher yields*
- *Economy of scale*
- *Materials*

**>2-4x ?**

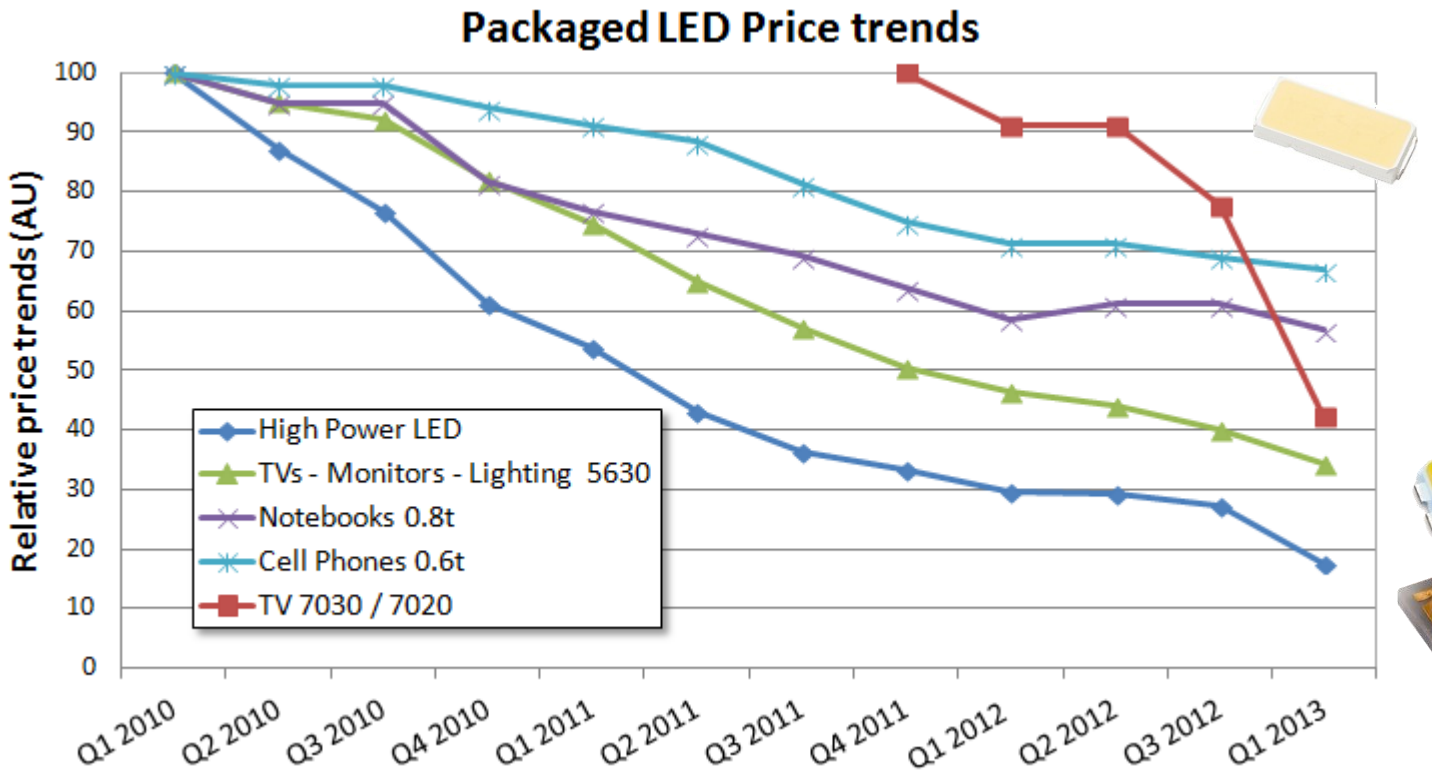
**LED performance**

- Higher Efficiency (lumen/W)
- More light / chip (driving current)

**2-3x ?**

# 2010-2013 Trends

## Significant ASP drop with performance improvements…






Mid-High power
"7030 / 7020"

Low power
Side view, 0.4 to 0.8t

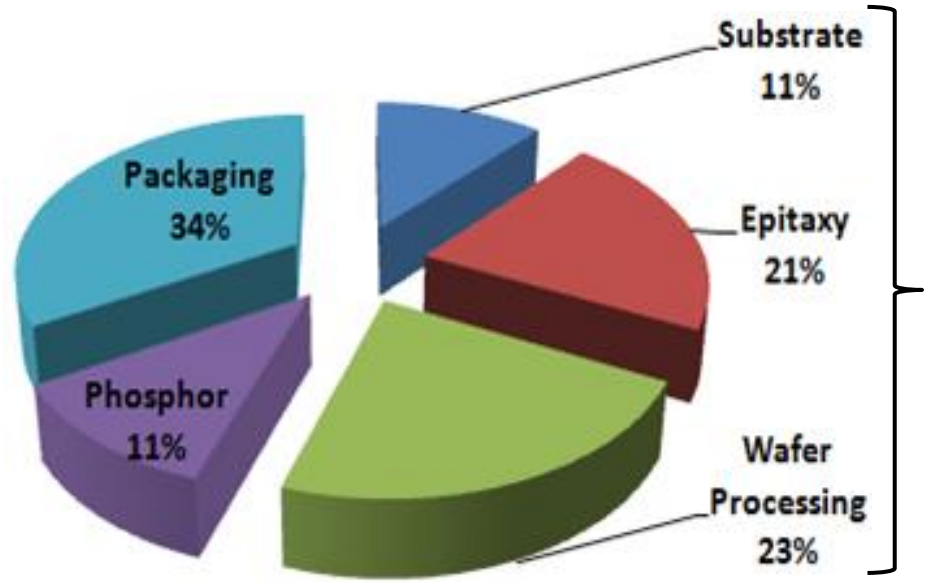
Mid power
"5630 / "6030

High power "1W – single chip"

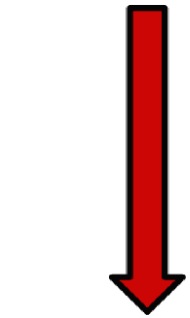
## …but more is needed for massive adoption in some applications

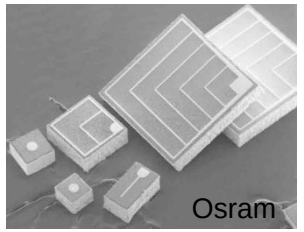
# Packaged LED Cost Structure

## Si wafers are less expensive than sapphire




Front End

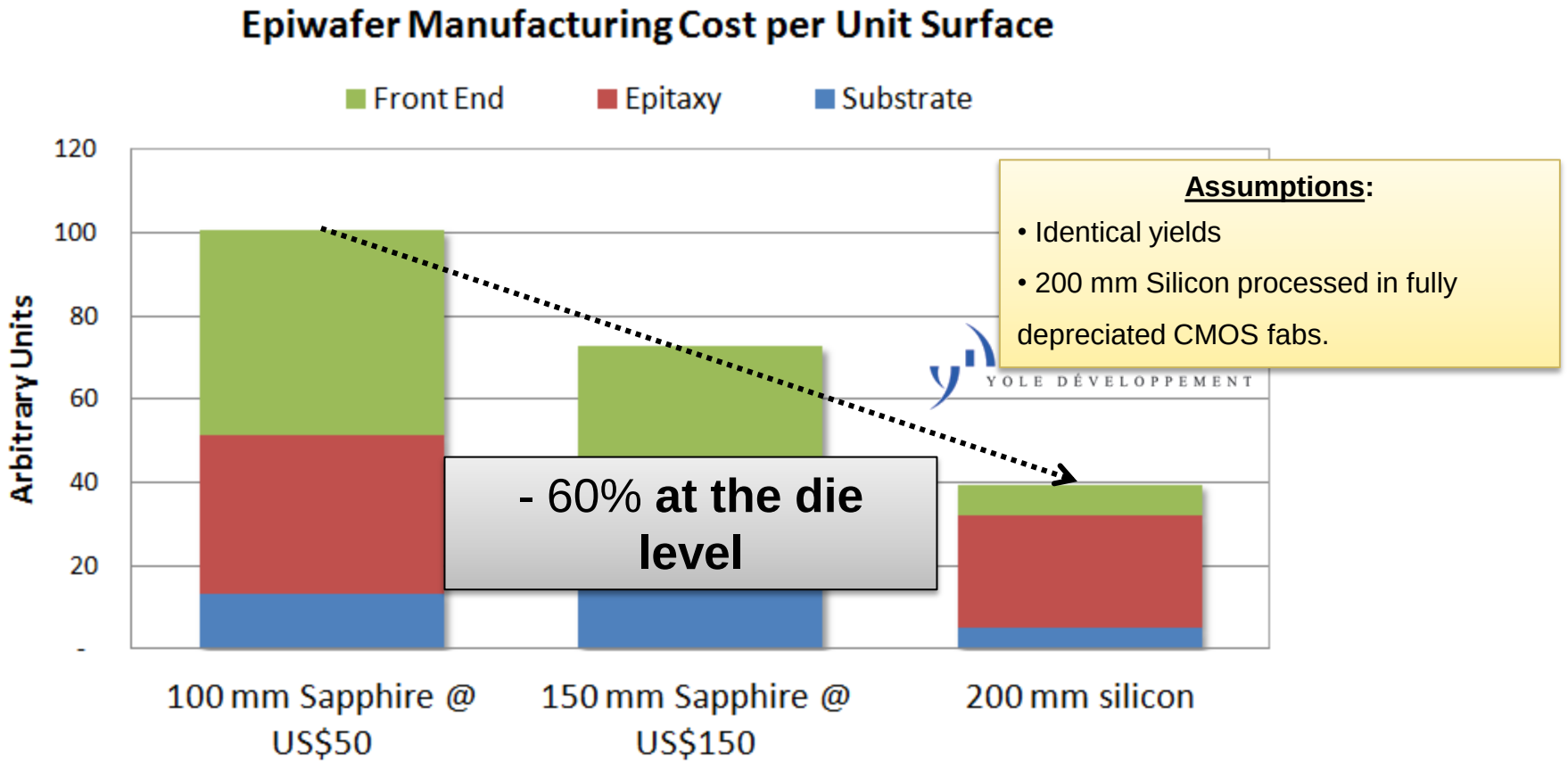





Example of a high power 1W HB-LED cost structure
(Source: Yole, System plus consulting)

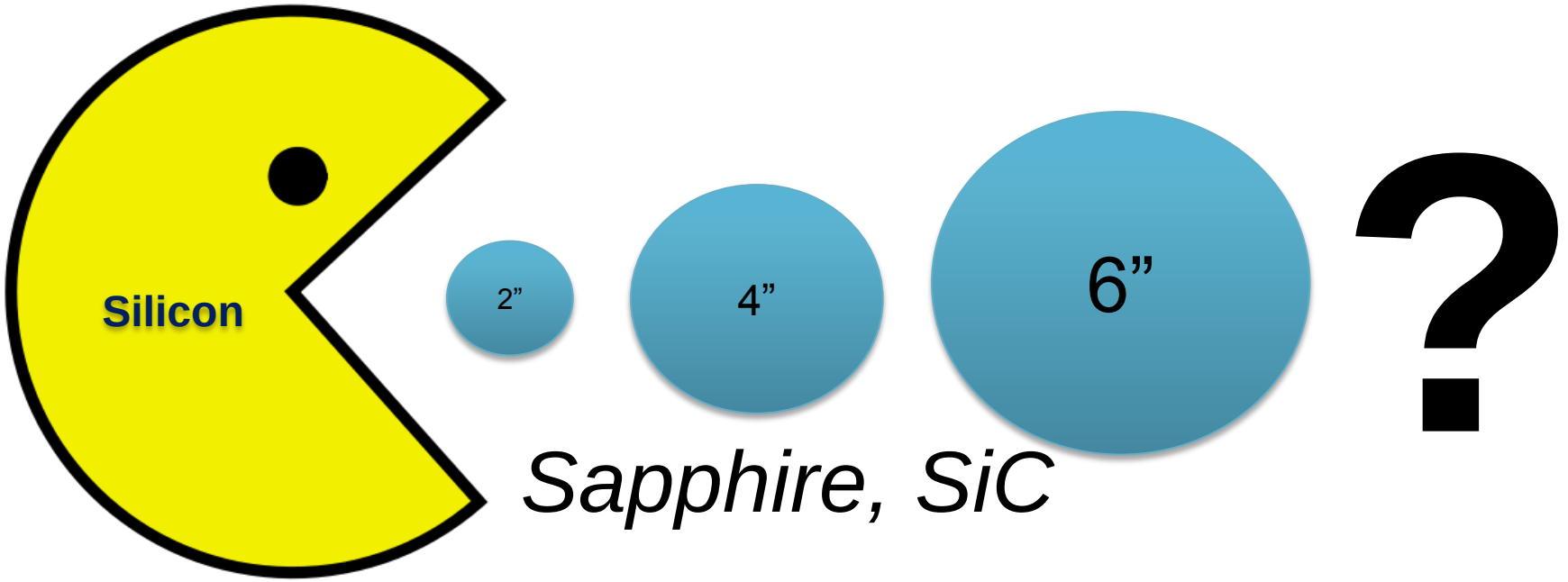
## Is this really the incentive?

# LED-on-Silicon: Potential Cost Benefits




**Benefit of Si would stem from switching to 8” and using fully depreciated & highly automated CMOS fabs.**

# Is Silicon Taking Over (yet)?

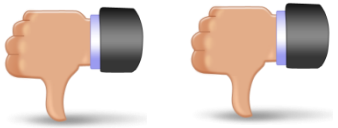


# Potential Benefits:

| CMOS processing | Wafer Price | Higher Thermal Conductivity | Non Transparent Material |
|---|---|---|---|
| • Mature, efficient (automated) & high yield<br>• Large process toolbox | Silicon is cheaper than sapphire and will likely remain so. | Better Temperature Homogeneity | More accurate Surface Temperature Measurement |
| **• Low cost: up to 10x improvement vs. 2” sapphire (!?)**<br>**• New LED structures ?** | **• Low wafer price**<br>**• 200 mm available**<br>**• But not semi standard (yet?)** | **Improved Binning Yield ?** | **Improved Run/Run repeatability ?** |

**Direct manufacturing cost** **Potential yield benefits**

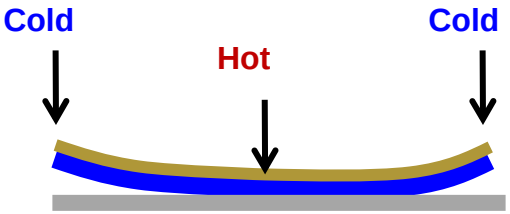
# Main Challenges:

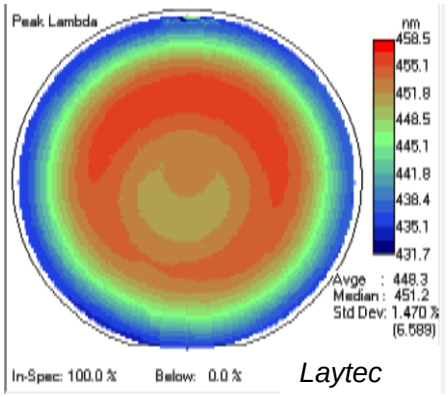
| | Lattice Mismatch | Thermal Expansion Coefficient Mismatch | Melt Back | Blue Light Absorption by Wafer |
|---|---|---|---|---|
| **Impact** | **Epitaxial Defect** | • **Wafer Bow →**<br>• **In-homogeneity**<br>• **Layer Cracking** | **Poor epitaxy** | **Poor light output** |
| **Sapphire** | Bad  | Bad  | No | No |
| **Silicon** | Worse  **Buffer layers** | Much worse  **Strain Engineering** | Yes | Yes |

# Main Challenge: TEC Mismatch

## Before Epitaxy:

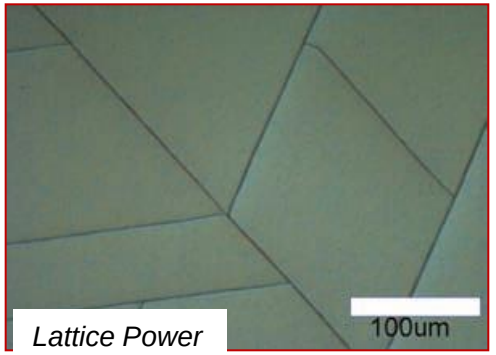

## During Epitaxy:




**Inhomogeneity → low binning yields**

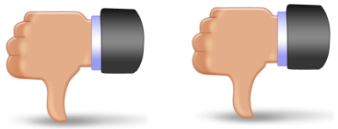
## After epitaxy:


**GaN layer Cracking**

## Solutions: Strain management layers, patterned substrates, nanostructures…

# Main Challenges:

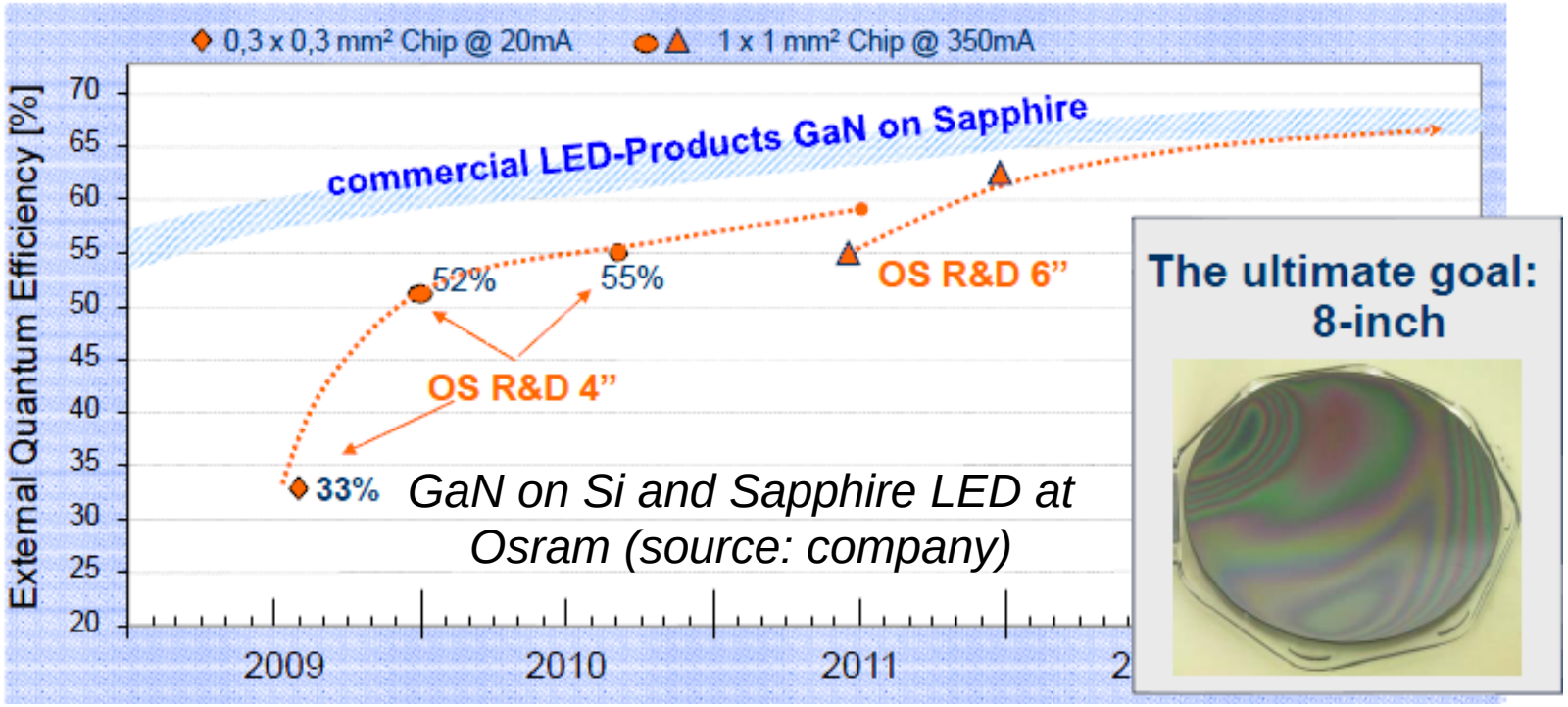
| | Lattice Mismatch | Thermal Expansion Coefficient Mismatch | Melt Back | Blue Light Absorption by Wafer |
|---|---|---|---|---|
| **Impact** | **Epitaxial Defect** | **• Wafer Bow →**<br>**• Inhomogeneity**<br>**• Layer Cracking** | **Poor epitaxy** | **Poor light output** |
| **Sapphire** | Bad  | Bad  | No  | No  |
| **Silicon** | Worse  **Buffer layers** | Much worse  **Strain Engineering** | Yes  **AlN Buffer** | Yes  **Substrate Lift Off** |

# Conditions for Success

## #1: Must equal LED on Sapphire performance.

# Performance Status: Example

## Absolute LED on Si performance still behind sapphire state of the art but catching up (Bridgelux, Lattice Power, Osram…)



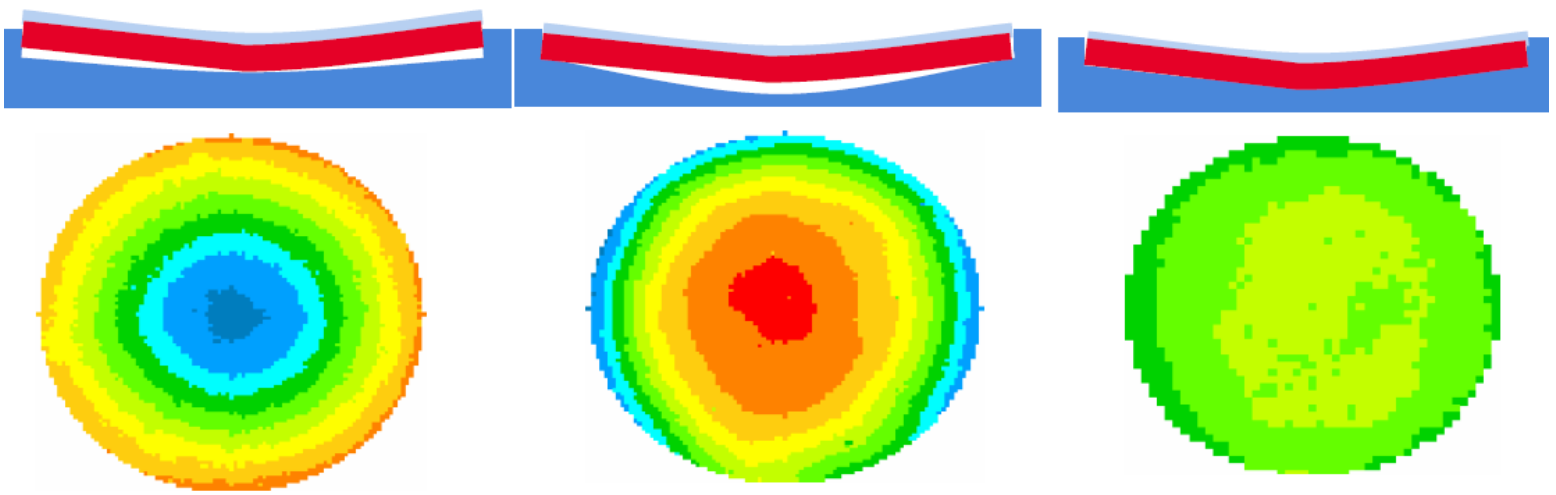

Performance: 634 mW @ 3.15 V, 350 mA, 1 mm2 chip → chip operated at 35 A/cm$^2$, standard package

# Conditions for Success

## #2: Must reach manufacturing yields similar to sapphire/SiC.

# Manufacturing & Binning Yields

## Main Issue:
## Wafer bow during epitaxy.
## Getting worse with larger diameter!

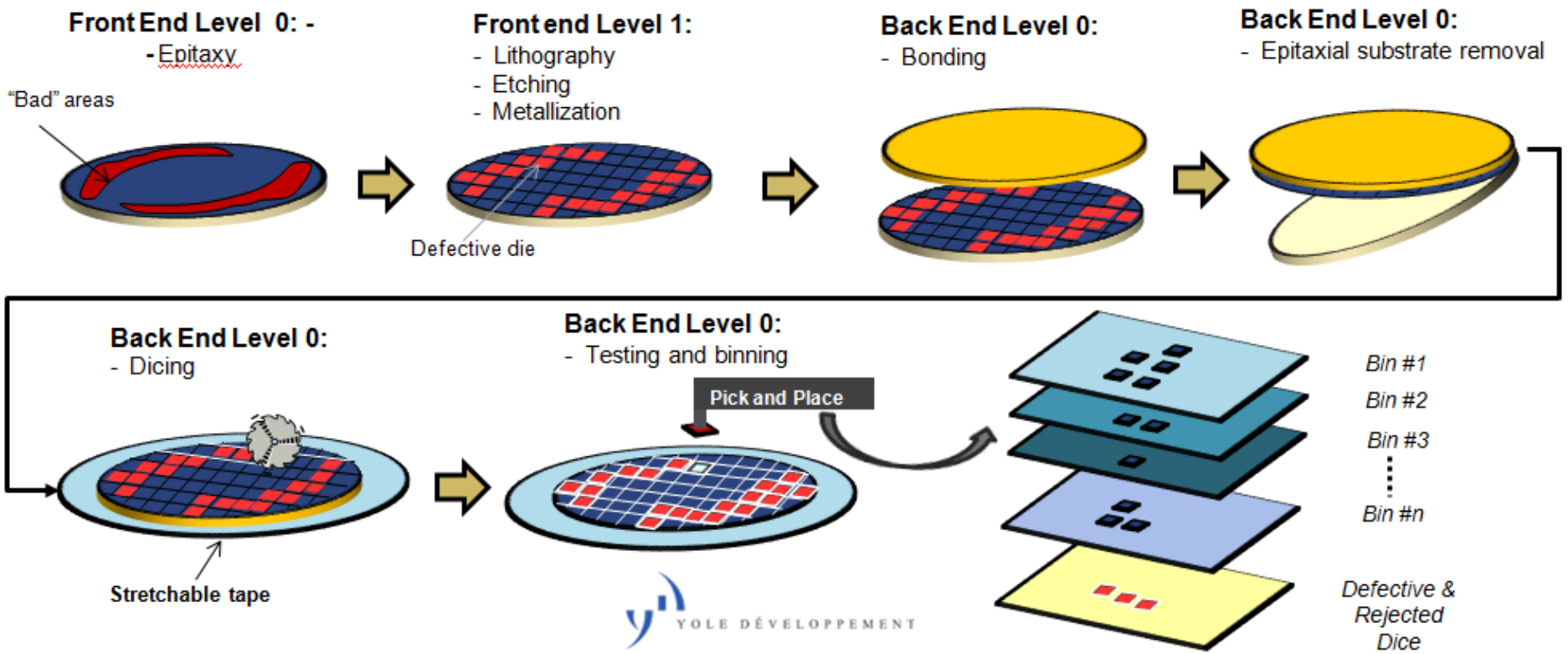


*Wafer mapping of the Photoluminescence of Multi Quantum Wells with wafers seating in pockets with different shapes. Source: Aixtron*

## Solutions include thicker wafers, curved pockets: requires extremely stable and reproducible process

# Are Yields Still important if Processing Since CMOS Processing is Cheaper?

## Yes: bad die carry the same cost as good ones!




## Yields currently still lower than on 4” or 6” sapphire

# Conditions for Success

## #3: Must be compatible with CMOS, ideally on 200 mm wafers (China: 150 mm fabs also available)

# Compatibility with CMOS Fabs

| | Diameter | Epiwafer Bow | Wafer Thickness | Contamination | Wafer Reflectivity |
|---|---|---|---|---|---|
| | 6” mininum<br>≥8” better | < 50 – 60 um | 725 um<br>(200 mm wafers) | No gold | Reflective surface |
| **LED on $Al_2O_3$** | Available but (still) expensive  | Can be managed but need very thicker wafers  | 6”: 1 to 1.3 mm<br>Not compatible!  | Used for bonding and other layers  | Incompatible with equipment sensors and automations  |
| **LED on Si** | Available and cheap.<br>150, 200, 300 mm  | OK with strain management layers.  | > 725 um: can be thinned down  | Used for bonding and other layers  | OK  |

# Conditions for Success: Summary

- **Performance Must equal LED on Sapphire.**
  - Coming close.

?

- **Must reach yields similar to Sapphire/SiC**
  - Still far away and needing significant improvement

?

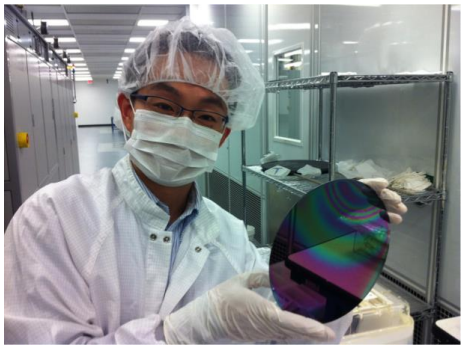
- **Must be CMOS compatible, 200 mm preferable**
  - Still some efforts needed

**Incentive for LED-On-Si is COST not performance!**

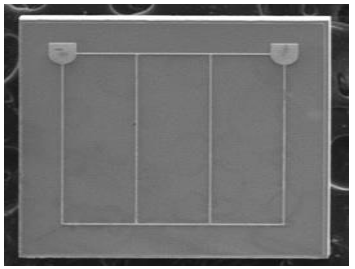
# Players and Recent News

- **Most LED makers have LED on Si research programs:**
  - OSRAM
  - Philips Lumileds
  - Samsung
  - Bridgelux + Toshiba
  - Epistar
  - Lattice Power
  - TSMC…

*Osram 6" LED Epiwafer*



Bridgelux 8" LED Epiwafer



Lattice Power Led-On-Si chip

- **Multiple startups (e.g.: Aledia…)**
- **Bridgelux/Toshiba, Lattice Power, Plessey committed to Si transition. Samsung also has strong incentive (CMOS fabs available)**
- **Most still undecided or in "defensive mode"**
- **New LED industry business models?**
  - **Azzurro offering GaN on Si templates or full LED epiwafers → fabless LED makers.**

# Players and Recent News

## Mixed signals at TSMC and Epistar:

### TSMC:

- *"it is difficult for 8-inch Si-substrate GaN wafers to replace sapphire wafers to become mainstream LED material because the former's manufacturing process is complicated and brightness of LED chips is lower"* – Jacob Tam, President TSMC Solid State Lighting, January 2013.
- *"It is understood that in the current stage, TSMC Solid State Lighting GaN-on-Silicon and sapphire substrate LED production line revenue is 50%, differentiated by using high-power and low-power LEDs"* – Digitime April 2013.

### EPISTAR:

- *Epistar transferred its GaN LED structure to an Si with Azzurro templates in just 16 weeks. While Epistar has not announced plans for production of GaN-on-Si LEDs* – PR Oct 2012
- *Chairman Lee Biing-jye, indicated that yield rates for Si-substrate GaN wafers are still low and Epistar is developing production technology for breakthrough".* - Digitime. Jan 2013

# Players and Recent News

## But others moving on:

### Bridgelux (US)/ Toshiba (JP):

- December 2012: Toshiba says it is shipping GaN-on-SI LEDs but no evidence yet of products that use the LEDs have been verified on the market
- April 2013: Bridgelux sells silicon IP to Toshiba.

### Plessey (UK)

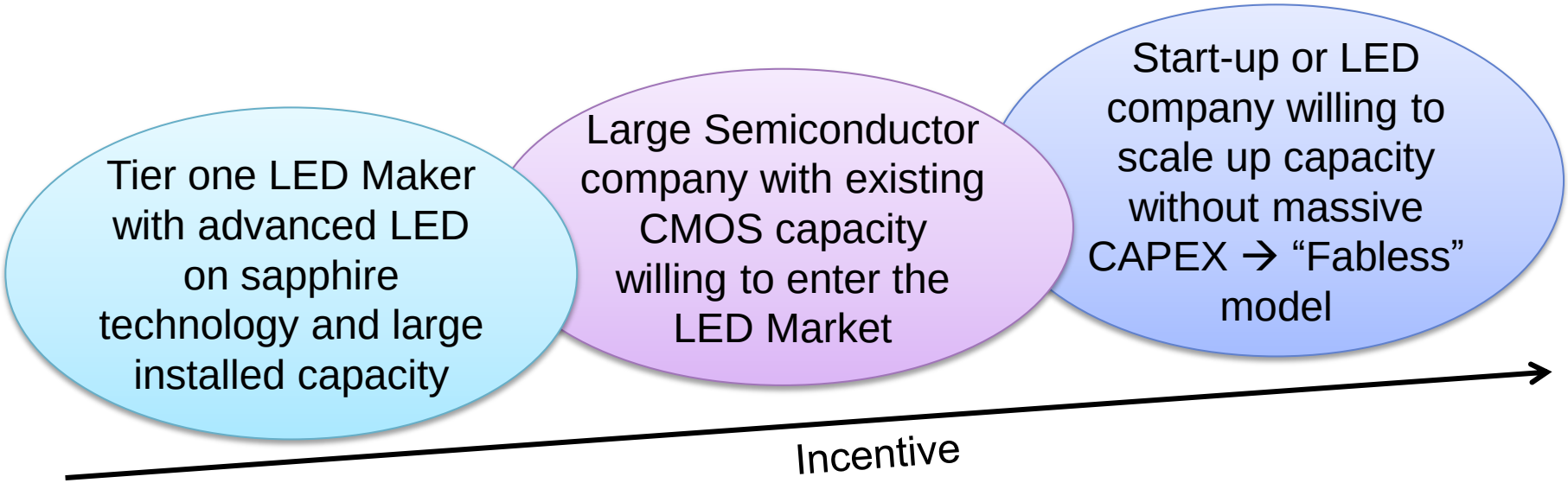
- March 2013: Plessey announces shipment of GaN-on-Si LEDs using 6-in wafers but first products only offer flux output in the 1-3-lm range  15-36 lm/W at 3.3V / 25 mA)
- Target for next product release: 60-70 lm/W

### Lattice Power:

- Feb 2013: volume production of high power chips but still on 2” Si wafers. Not much cost saving vs. sapphire but plan to switch to 6” soon.
- Currently run 15k to 20k wafers per month.

# Will LED-on-Si Happen?

- **Still some technology hurdles: yields, full CMOS compatibility.**
- **LED on Si better suited for some type of LEDs than others and breakeven point not the same for all manufacturers.**

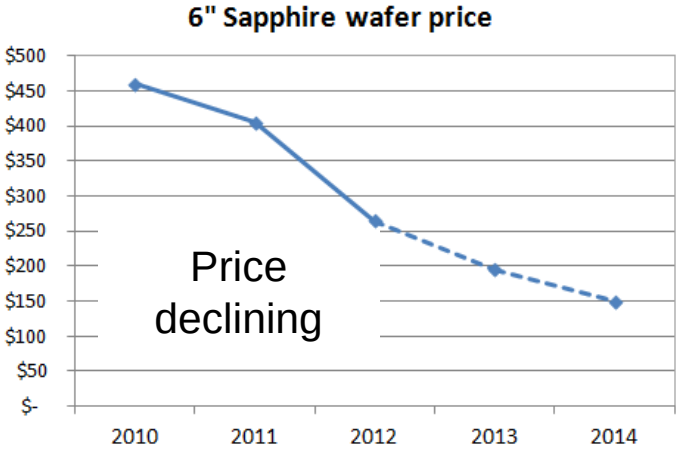



**<u>If</u> technology hurdles are cleared, LED-On-Si will be adopted by <u>some</u> LED manufacturers but not necessarily become the standard.**

# Will LED-on-Si Happen?

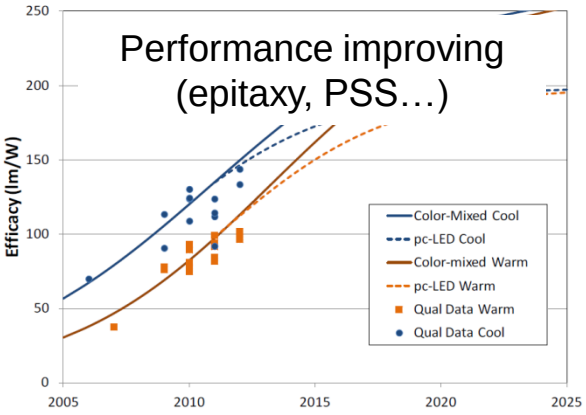
## Maybe…

- **It's a cost game ($/lumen)!**
- **Si enables 200 mm in CMOS fabs**
- **Sapphire/SiC = moving targets!**




*(Yole Developpement)*


*Monocrystal*




*DOE Roadmap*

# Our Scenario

- If technology hurdles are cleared, LED-on-Si will be adopted by some LED maker, but not necessarily become the industry standard.

**Scenario #1**:
Current LED-on-Si proponent fails to move to mass manufacturing.

Industry refocuses attention on Sapphire, stimulating adoption of 6” wafers and possibly resuming R&D effort on 8”

**Scenario #2**:
Current LED-on-Si proponent successfully moves to mass manufacturing but fails to generate massive cost benefits and differentiations

LED-On Si adoption remains limited to these few companies. The bulk of the industry continues leveraging on its sapphire (or SiC) platform

**Scenario #3**:
Current LED-on-Si proponent are successful and demonstrate differentiating cost benefits

The rest of the industry tries to emulate this success and eventually massively switches to LED-on-Si → complete disruption of the sapphire wafer industry

# THANK YOU!


Contacts (US):
Michael McLaughlin: mclaughlin@yole.fr
650-931-2552

*www.i-**micronews**.com*
www.yole.fr