Next Gen Packaging & Integration Panel

ECTC 2012

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SEMI

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Packaging Supply Chain

- Market Trends
- Material Needs and Opportunities

Market Trends

Packaging Materials Market- *Increasing Material "Intensity"*

Packaging Materials Revenue

US$ Billions: 0, 5, 10, 15, 20, 25

% of Semiconductor Revenues: 0%, 1%, 2%, 3%, 4%, 5%, 6%, 7%, 8%, 9%, 10%

1988, 1989, 1990, 1991, 1992, 1993, 1994, 1995, 1996, 1997, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011

Packaging Materials — **Pkg. Mat. as a % of Semi. Revenues**

Source: Rose Associates (through 1999), WSTS, SEMI

Traditional Materials- *Large Supplier Base Remains*

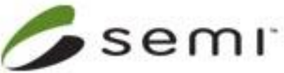
	Laminate Substrates	Underfill	Die Attach	Leadframe	Solder Balls	Molding Compounds
# of Suppliers	22	~30	~18	~40	26	~16
Est. Share of Top Five	~55-60%	>50%	~75 – 80%	~45%	One supplier has ~50%	~75 – 80%

Source: SEMI and TechSearch International, Global Semiconductor Packaging Materials Outlook, November 2011

Material sets have changed and evolved with new packaging form factors and market needs:

- *Green materials*
- *Die attach films*
- *Copper wire*
- *Etc.*

Korean Material Suppliers- *An Emerging Supplier Base*



Combined Total Sales and Percentage Export for Seven Korean Packaging Material Suppliers

	2003	2004	2005	2006	2007	2008	2009	2010	2011
Combined Revenues (US$ million)	$498	$634	$700	$821	$930	$950	$900	$1,090	$1,220
% Export Sales	**40%**	**48%**	**41%**	**51%**	**58%**	**56%**	**60%**	**67%**	**65%**

Source: SEMI and TechSearch International, Global Semiconductor Packaging Materials Outlook, November 2011

Other suppliers active in new die attach, encapsulant, and underfill materials

Materials for WLP and TSV- *New materials and Processes*

Advanced packaging technologies are becoming increasingly more *"front-end/fab"* oriented:

- Silicon technologies are becoming more and more brittle with ultra-low-k materials, meaning the choice of packaging can have a big impact on the device reliability, performance, etc.

- Front-end and back-end companies need to closely collaborate to understand the constraint of each other.
  - Pad design, UBM design and materials, eventual passivation, PI opening, substrate material finishing, bump metallurgy and shape, underfill type… all need to be assessed very seriously.

A number of technologies cannot anymore be easily put in front- or back-end category. There is an overlap, thus there are lot of technologies in what is called "mid-end".

"An Equipment Digression"- *Convergence of Fab and Packaging*

- TEL → NEXX Systems (deposition equipment, 2012)
- AMAT → Semitool (deposition equipment, 2009)
- KLA Tencor → ICOS (backend inspection, 2008)
- Ricmar → NanoPhotonics AG, (backend inspection 2008)
- Nanometrics → Zygo (backend inspection, 2009)
- AMEC (China) introduced TSV etch system

Material Needs and Opportunities

Materials for WLP and TSV- *New materials and Processes*

- Temporary bonding materials
- CMP slurries
- Underfill and encapsulant materials
- Dielectrics
- Interposers
- Thermal materials

Materials compatible with high-volume manufacturing of high yielding and high reliability packages

Temporary Bonding Materials

Wafer thinning and wafer bonding/debonding are a critical process step:

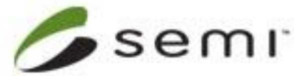
- Low temperature bonding
- Ease of debond and cleaning
- Minimal total thickness variation (TTV)
- Adhesion to various substrates and surfaces
- Mechanical strength and adhesion during wafer thinning and backside processing
- Thermal stability and chemical resistance to withstand backside processing
- What process: chemical? thermal? mechanical?

CMP Materials

- TSV is among the next big target markets for Cu CMP slurry.
- Different slurry formulations and process conditions for front side planarization and back side reveal.
- Product development expenses are fixed and relatively high compared to the volume of slurry that will be sold for each step
  - *Though TSV benefits from a somewhat lower product development cost as it can leverage what we've learned in formulating Cu interconnect slurry.*
- The biggest differences between Cu interconnect and Cu TSV are the control of dishing in the larger TSV feature sizes, and the higher Cu removal rate due to the thickness of the TSV Cu over burden.

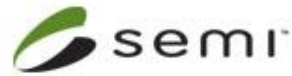
Source: Techcet Group (www.techcet.com)

Underfill



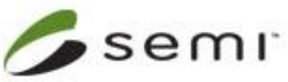
- ~$220M market currently forecasted to reach $300M by 2015
- Micro bumps for 3D IC or silicon interposer connections require new material formulations
- Address fine pitch bumps and smaller die gaps
  - Smaller (*nano-sized*) filler materials are needed
  - Vacuum assist to improve the flow of the underfill?
- No-flow underfill formulations are in vogue again
  - Applied prior to chip placement, either on the wafer or substrate
  - Use non-conductive pastes (NCP) or films (NCF)
    - *Copper pillar- Fill the small gaps; good fillet control, etc.*
    - *Simplifies the process, e.g. cure at the same time as the bonding operation*

Dielectrics



- ~$60M market currently forecasted to reach $120M by 2015
- Requirements for new materials include:
  - Good adhesion/no delamination
  - Low moisture absorption (reduced outgassing at elevated temperatures)
  - Low stress (to match the CTE of the chip) and/or low modulus (for less wafer bow)
  - Low temperature cure (200 to 250°C)
  - Lower dielectric constant
  - Higher resolution at thicker layers
  - Wide process windows
  - Enhanced board-level reliability performance

Supply Chain
Opportunities and Issues



- New materials and processes to improve package performance and reliability
- Large material supplier base exists
- How large will the material markets be?
- Cost reduction pressures