BRIDGING THE GAP BETWEEN SILICON AND PACKAGING

GREGG BARTLETT
CHIEF TECHNOLOGY OFFICER
GLOBALFOUNDRIES

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What has Changed?

Technology Challenges

Technology Solutions

The New Supply Chain

Summary

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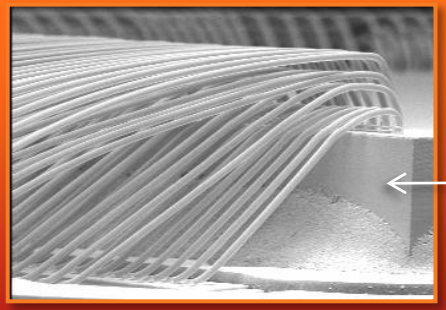
Silicon Interconnect Evolution

Interconnect process optimized by assembly provider with little or no Foundry involvement

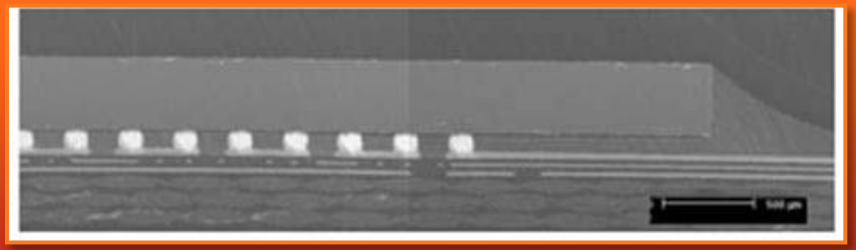
Wire Bond: 2D

Typically 25-1000ea per IC



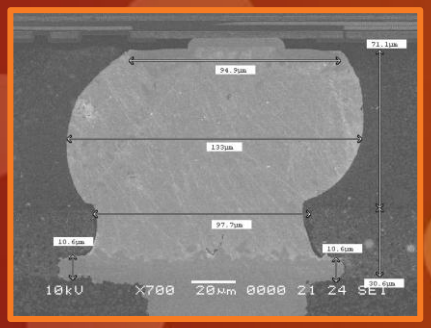
Flip Chip: 2D

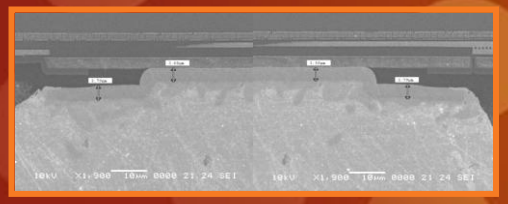
Typically 250-10,000 per IC



Evolution to Flip Chip and Pb Free Bump:
Driven by Performance and Interconnect Density

Increasing collaboration between Foundry and assembly provider for optimum solutions





Impacts:

Increased I/O density

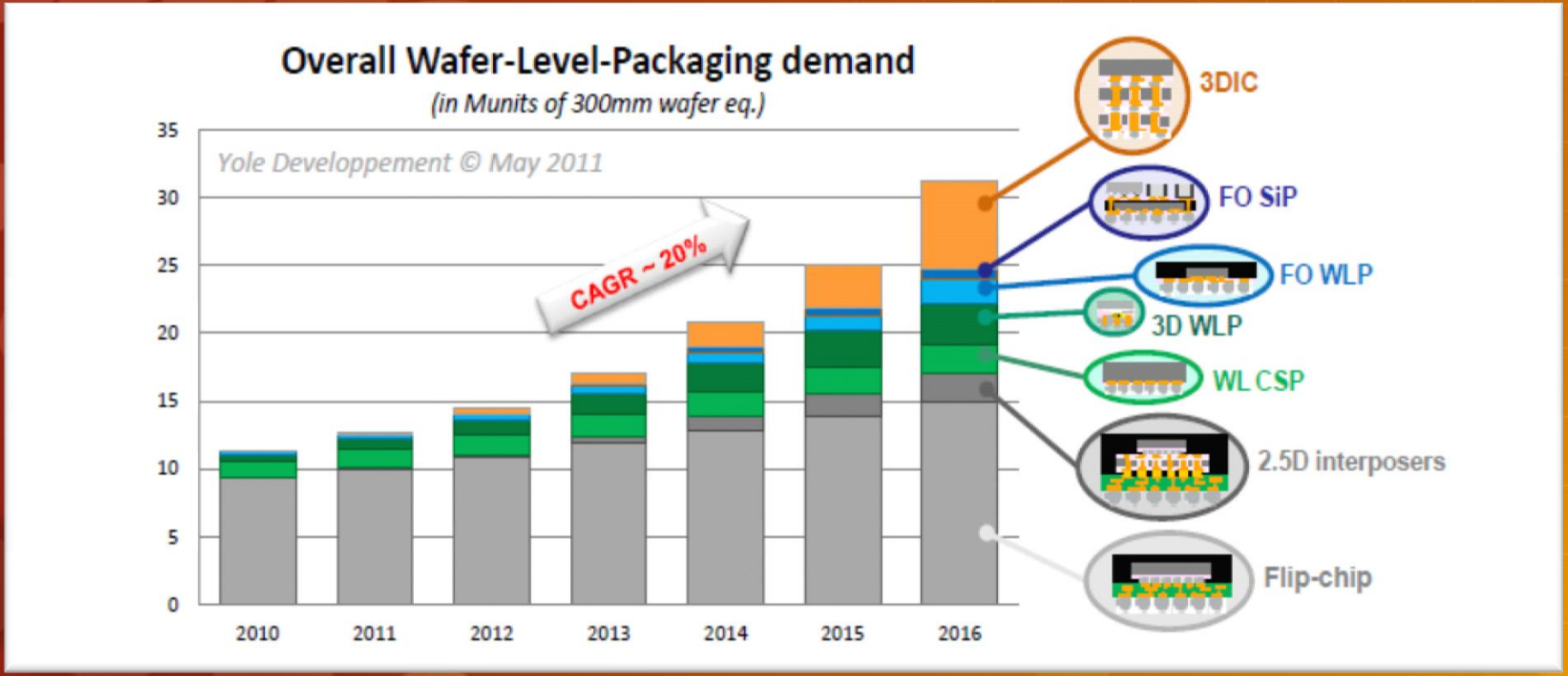
Improved electrical performance

Higher modulus interconnect

Weaker low K dielectric

Substrate thickness and CTE have increasing role

Explosion of Wafer Level Products:
Driven by I/O Density, Performance, Form Factor



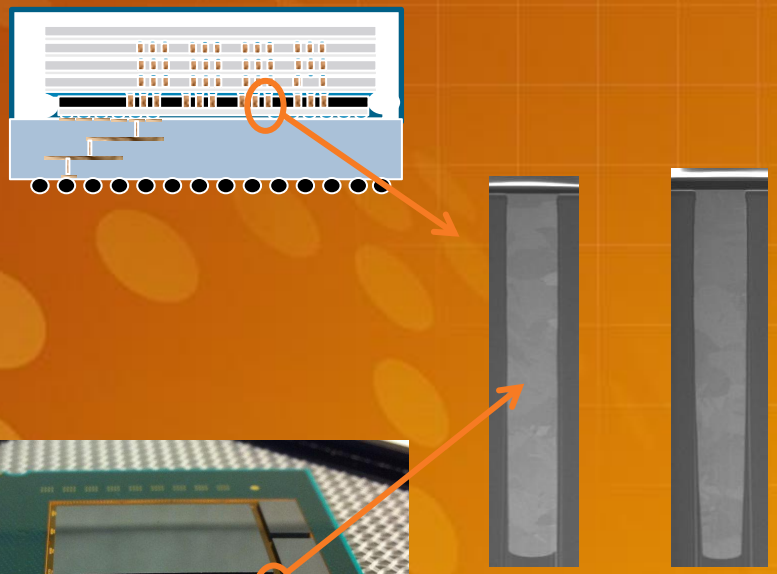
Courtesy of Yole

Driving Revolution to Silicon Interconnect

Interconnect solutions require high collaboration between Foundry-OSAT

Through Silicon Via (TSV): 3D

Typically 1000-50,000 per IC



Through Silicon Via (TSV): 2.5D

TSV's in interposer

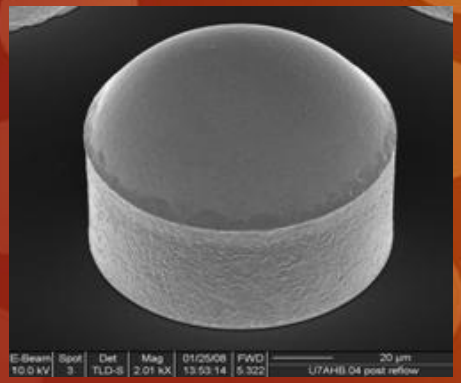
Requiring New Technologies

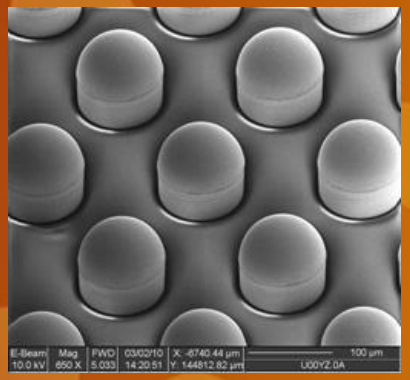
New interconnect at much finer pitch

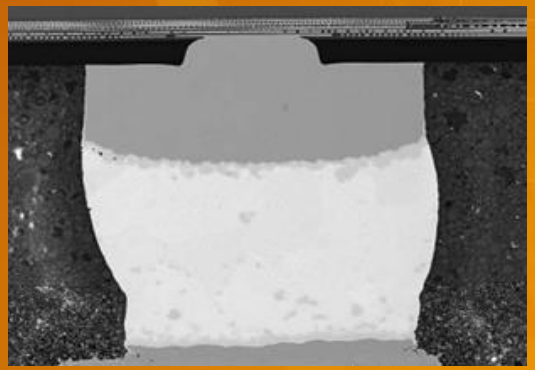
Probe (wafer test) as fine pitch

Thin wafer handling

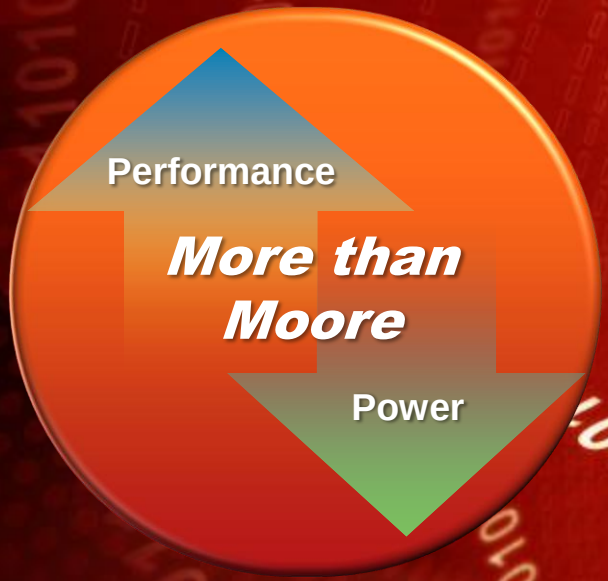
New assembly technologies and design rules to manage warpage

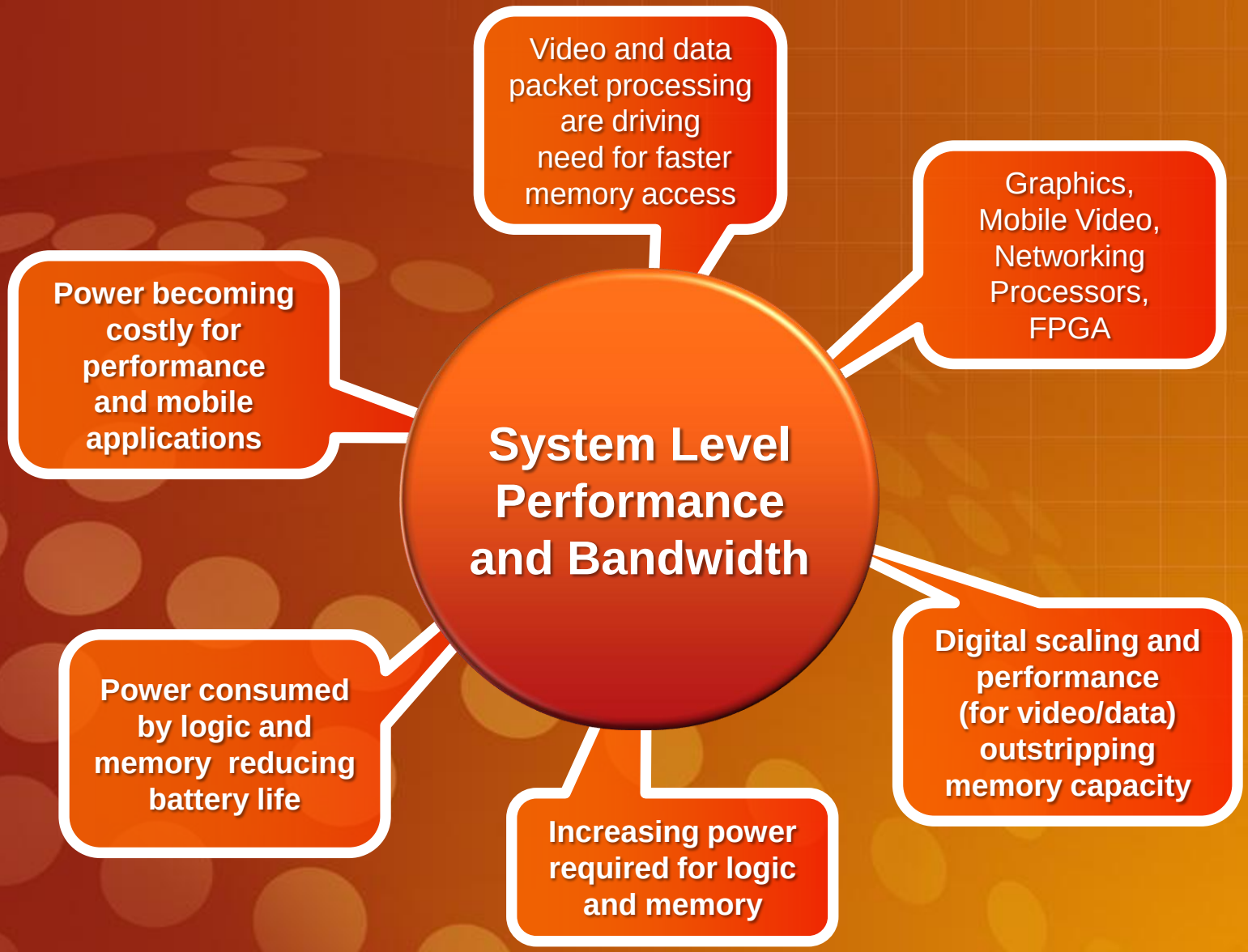




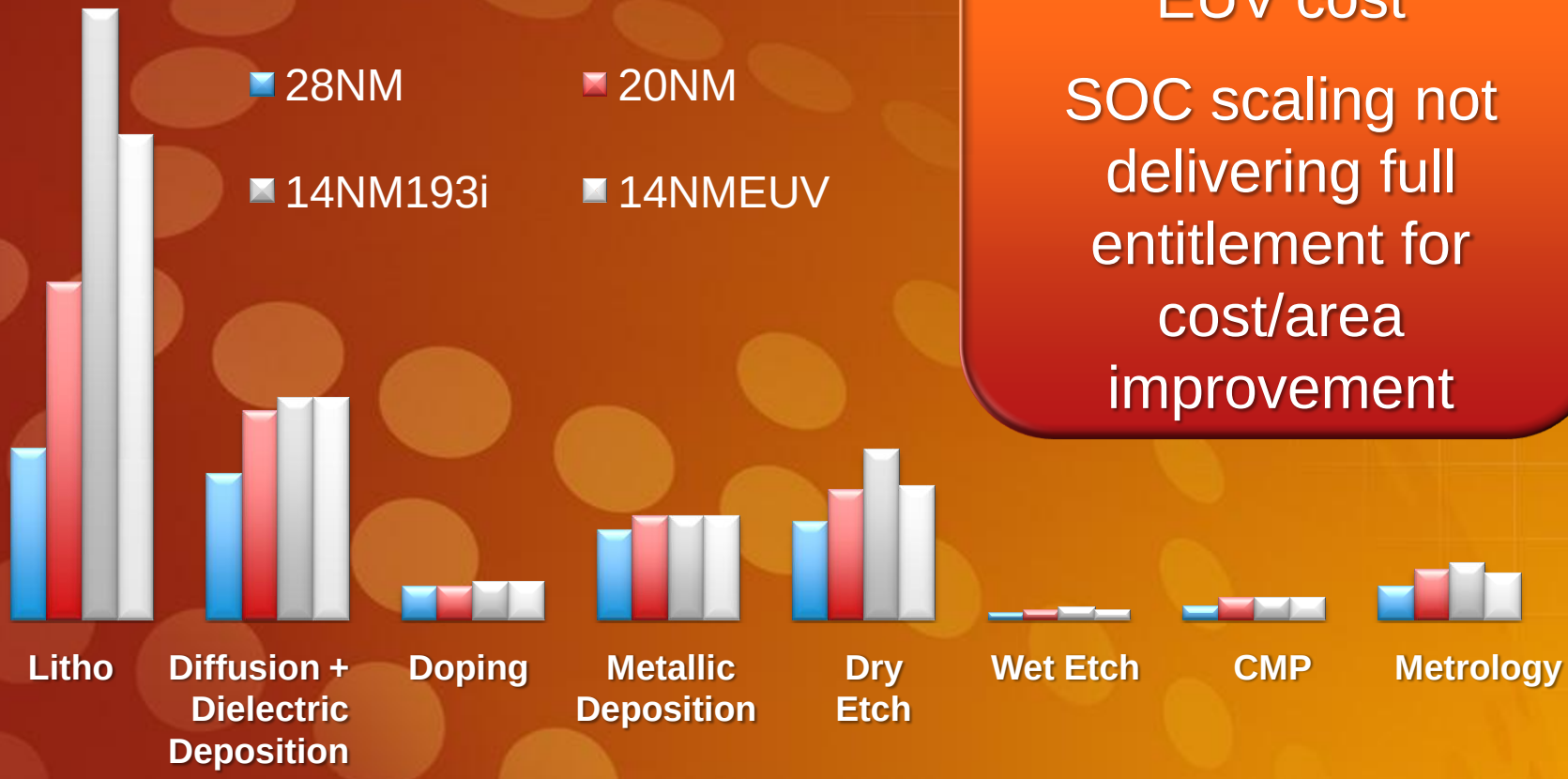


Technology Challenges




System Level Performance and Bandwidth
Video and data packet processing are driving need for faster memory access
Graphics, Mobile Video, Networking Processors, FPGA
Digital scaling and performance (for video/data) outstripping memory capacity
Increasing power required for logic and memory
Power consumed by logic and memory reducing battery life
Power becoming costly for performance and mobile applications

Increasing Cost, Reducing Benefit of Scaling



Double patterning, EUV cost

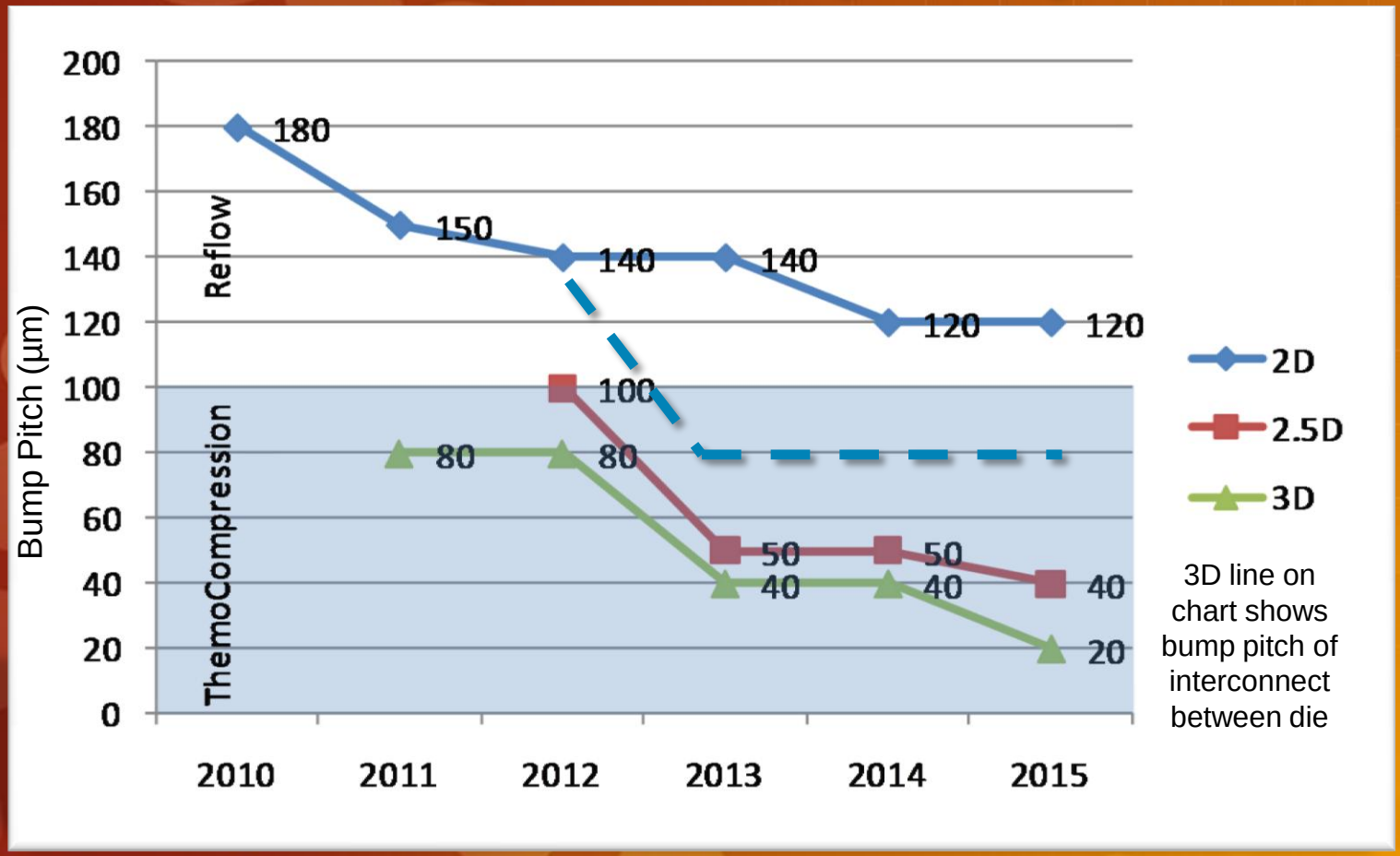
SOC scaling not delivering full entitlement for cost/area improvement

Source: IMEC INSITE program in collaboration with partners

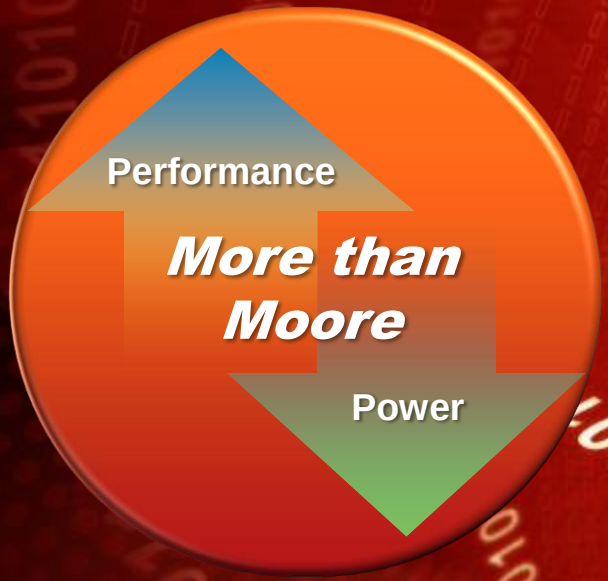
I/O Density Trend Drives Packaging

Shrinking pitch drives non-collapsing and smaller bumps

Smaller bumps increase warpage management risk



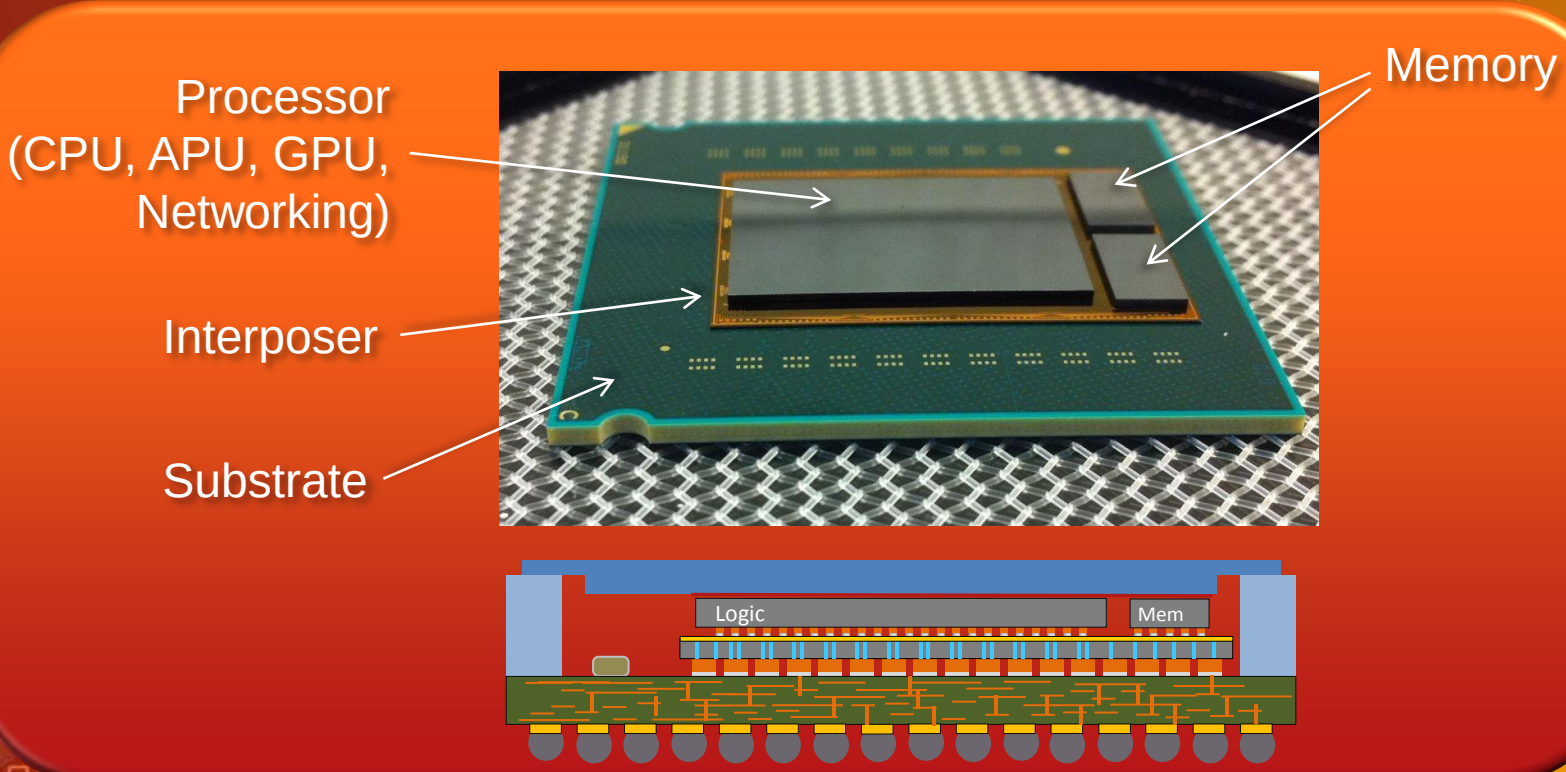
Solutions:
Innovation, Cost, Collaboration



Memory Bandwidth Solution for High Power Applications: 2.5D

Interposer is “passive silicon” with TSV’s used for high density interconnect.

Main challenges are warpage of thin interposer and yield.



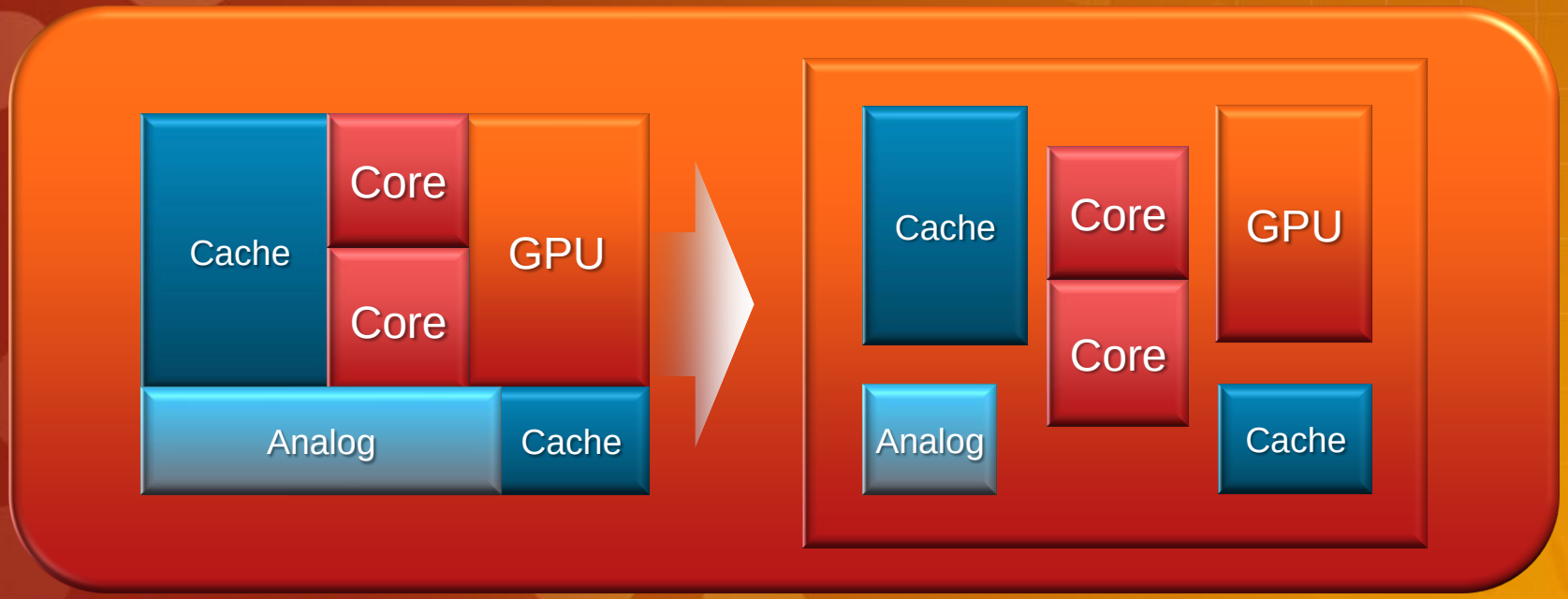
2.5D Enables “Fission”

Smaller die, higher yield, lower cost

Utilize process which is optimal for each function

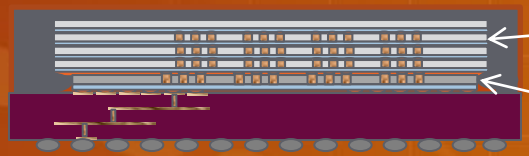
Scale each function when required, not whole SOC

Derive savings at system level as well: board, substrates, power



Memory Bandwidth Solution for Low Power Applications: 3D

3D: Vertical stacking of (mostly) logic and memory die. TSV's in logic die.



TSV's (Through-Silicon-Vias): Vertical connections through silicon, for very high interconnect density between IC's.

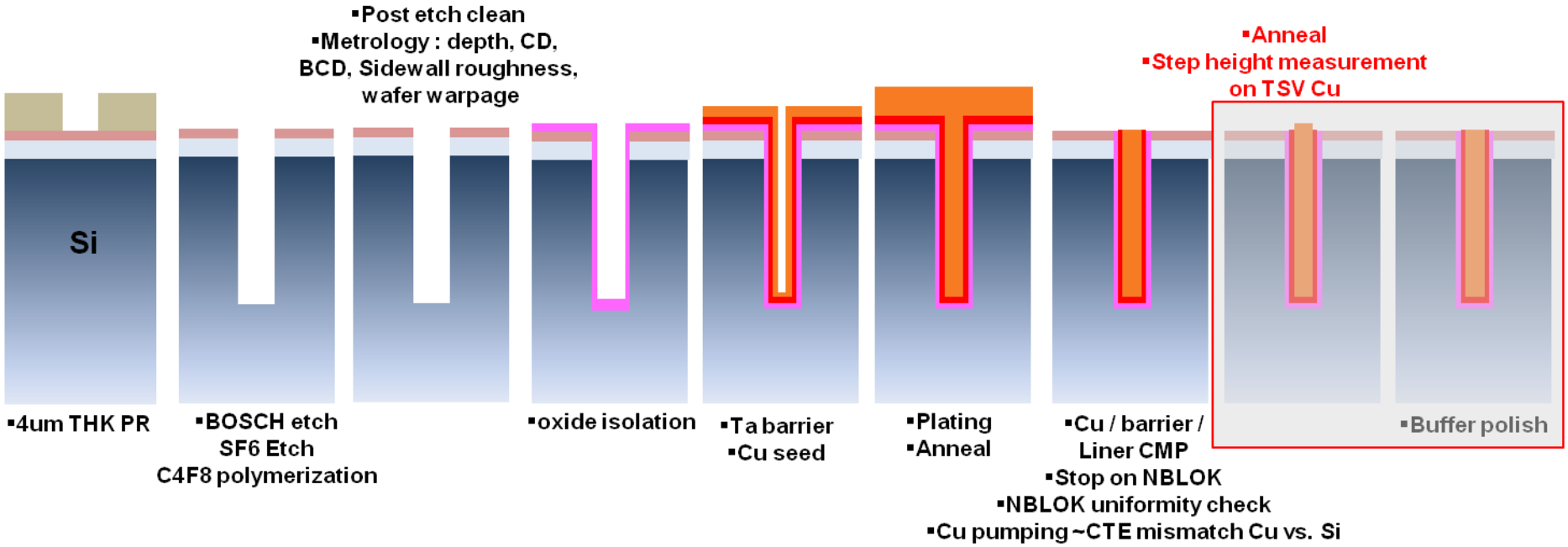
Wide I/O standard is 6um diameter with pitch 40-100um

Much higher interconnect density increases bandwidth

Much shorter interconnect improves performance

Increased bandwidth reduces power

TSV Formation



Step height measurement for Cu pumping detection, Buffer polish and 2nd anneal can be skipped

TSV Process Development

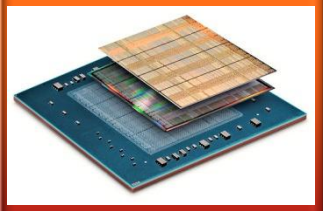
Module development at consortia

Integration in Foundry

Collaboration between consortia, foundry, tool manufacturer critical

TSV Etch installed, Fab 8, NY

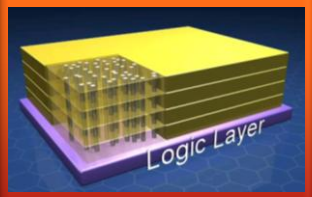
Packaging Roadmap



Silicon Partitioning with Interposers

Market: FPGA

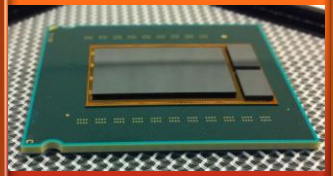
2011



Memory Cube

Market: Server and Computing

2013



Logic + Memory on Interposer

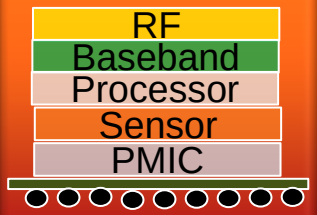
Market: GPU, CPU, Network Processors

2013/14

Wide I/O Memory on Apps Processor

Market: Mobile, Tablet

2014



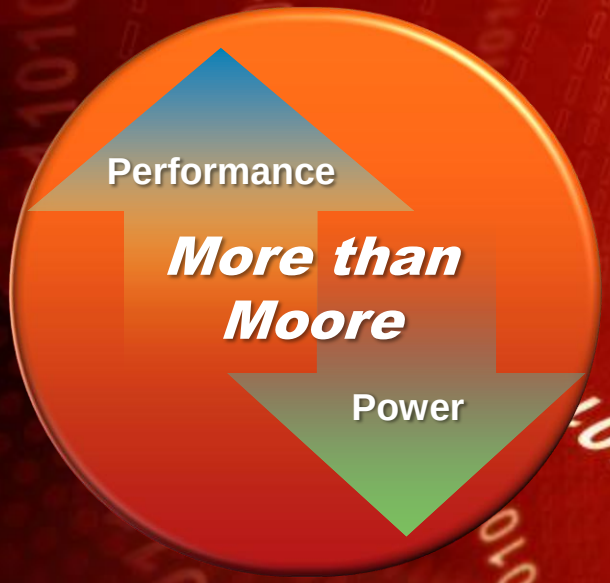
Heterogeneous Stacking

Market: Mobile, CPU

2017?

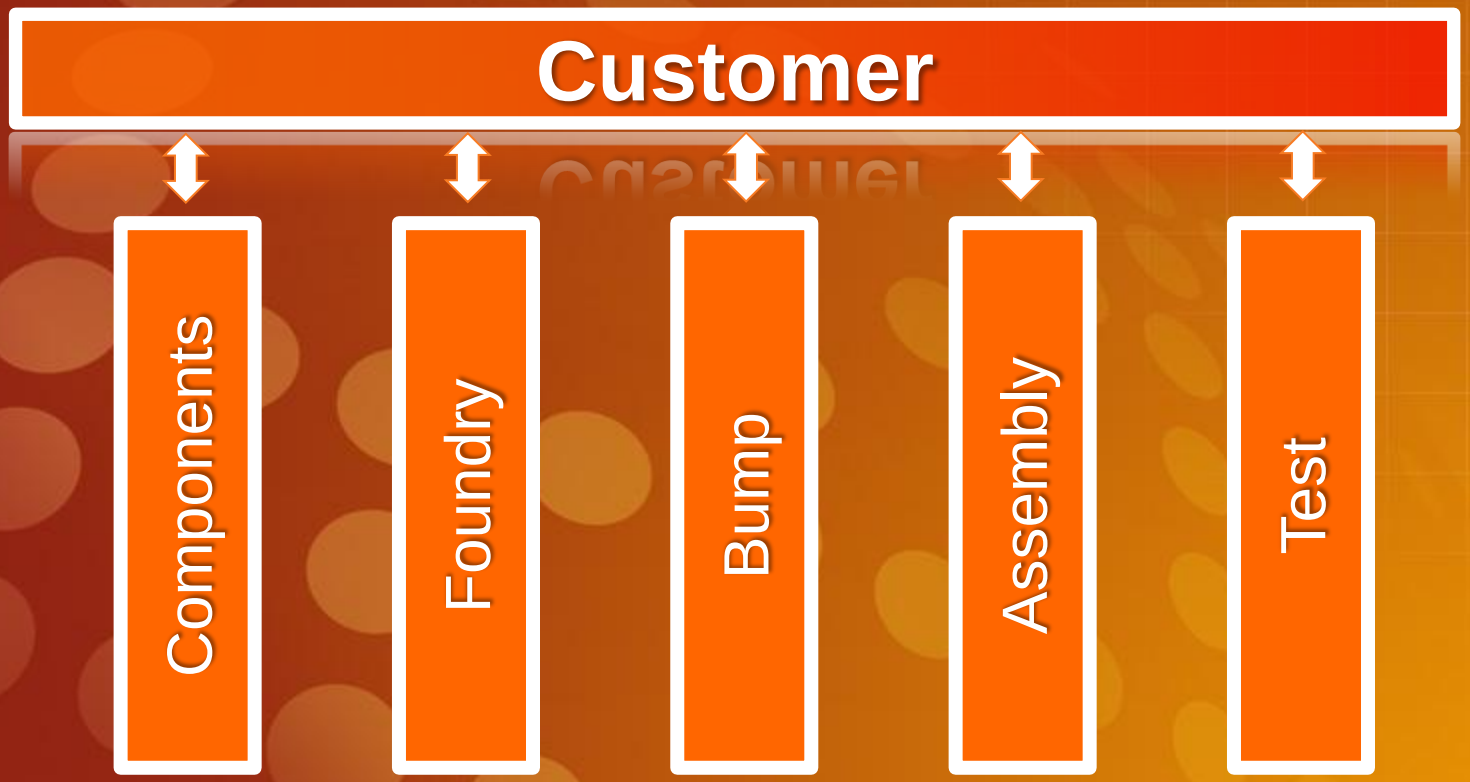
Time

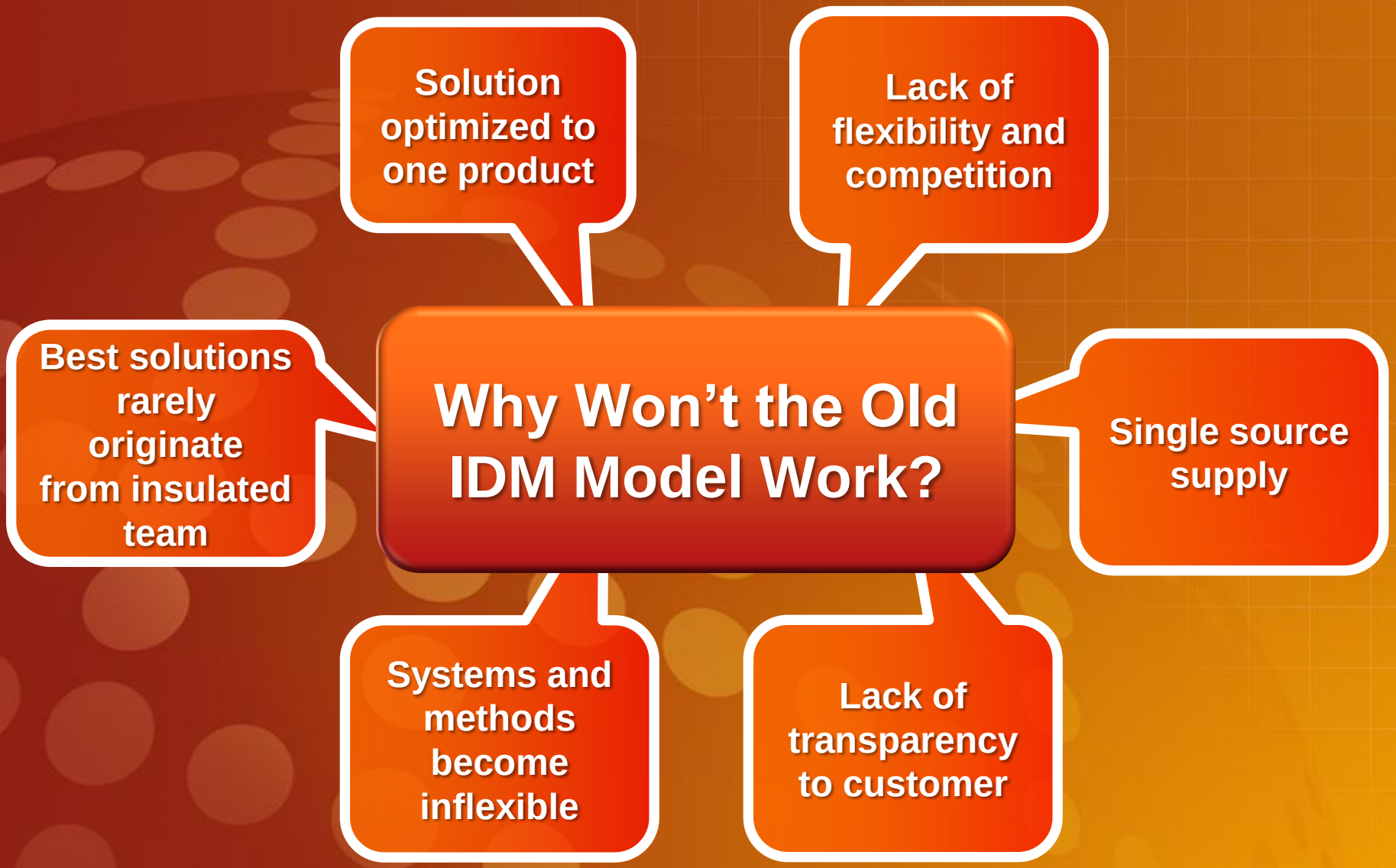
The New Supply Chain



Why Won't the Current Model Work?

Solutions developed in isolation are no longer adequate to address the complexity of high-silicon content packaging

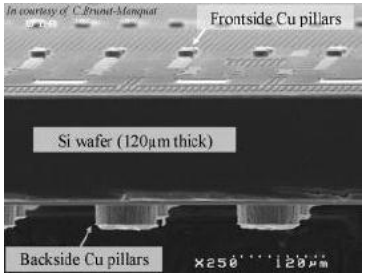



Why Won't the Old IDM Model Work?
Solution optimized to one product
Lack of flexibility and competition
Best solutions rarely originate from insulated team
Single source supply
Systems and methods become inflexible
Lack of transparency to customer

The New Model

Will Likely See Supply Chain Alliances Within the Industry

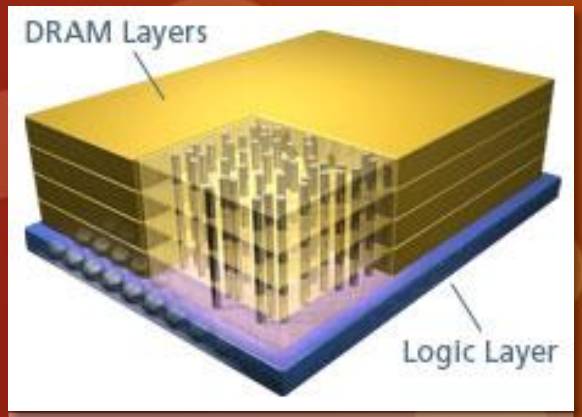
Collaborative Solutions Utilizing the Best Minds



	Optimize Block Placement	Optimize TSV/Bump Placement	PDKs	Reference Flow	TSV Development	TSV Metrology	TSV Impact on Transistors	Thinning Impact on Transistors	KGD Methods	Fine Pitch Probe	Thin Wafer Handing	Assembly Development	Test Strategy and IP	Test Repairability
Consortia	■	■			■	■	■	■	■	■	■	■	■	■
Customers	■	■	■	■	■	■	■	■	■	■				■
EDA Tool Suppliers	■	■	■	■	■									
MOL Tool Suppliers					■	■	■	■			■			
Assm Tool Suppliers											■	■	■	■
Foundry	■	■	■	■	■	■	■	■	■	■	■	■	■	■
OSATs			■			■	■	■	■	■	■	■	■	■
Memory Suppliers	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Test Tool Suppliers									■	■	■		■	■

Collaboration:
Design for Yield

Co-Locate to Develop Solutions for Customers



Bring foundry and partners together to develop new tools, processes, and technologies for joining silicon

Fast learning cycles

Develop BEOL, bump, BSI, 3D assembly, test, and metrology together in one location for best collaborative ideas and evaluation of potential solutions

Development of thin wafer (50µm) handling tools and methods

Value Creation:
Deliver Solutions to Customers

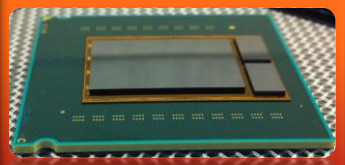
Aligned Design Rules, Metallurgy

Design Enablement

Design for Manufacturing

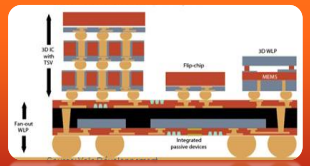
CPI, Assembly, Test

Supply Chain

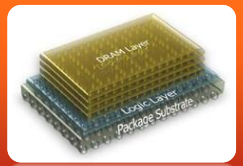


Interposers

Center of Excellence



OSAT



Memory

Aligned Metrology and Quality Systems

IP / EDA

Consortia Partners

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Conclusions:
Technology, supply chain and business model collaboration required
Customers need transparency to commit to new technologies
Packaging innovations beyond scaling
Open supply chain
Interconnected technical solutions require a new business model
Supply chain alliances enable solutions
Leading customers highly involved
Collaborative development, common location fast learning cycles
Yield => cost => success

Thank You