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1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – Indium Corporation

Course Objectives:

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMCs) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail, and novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whisker growth will also be discussed. Furthermore, the reliability of through-hole solder joints will be reviewed, and recommendations will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

Course Outline:

1. Implementation Status
2. Prevailing Materials: Alloys and Finishes
3. Surface Finish Issues: ENIG, Immersion Ag, and Immersion Sn
4. Mechanical Properties: Shear, Pull, and Creep
5. Intermetallic Compounds: Effect of Cu, Ni, Other Additives, and Heat History
6. Failure Modes: Grain Deterioration, Orientation, Mixed Alloys, and Interfacial Voiding
7. Thermal Cycle Reliability: Effect of Cycling Condition, Surface Finishes, and Reflow Temperature
8. Reliability of Through-Hole Joints: Large and Thick Boards and Partially Filled Through-Holes
9. Fragility: Effect of Surface Finishes, Alloys, Reflow, Strain Rate, Aging, Cycling, and IMC
10. Electromigration: Effect of Current Density, Back Stress, and Cu UBM Thickness
11. Corrosion: SAC and Performance of Surface Finishes under Harsh Conditions
12. Tin Whiskers: Causes of Formation, Methods for Control

Who Should Attend:

Anyone interested in achieving high reliability leadfree solder joints should take this course.

2. WAFER LEVEL CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – Texas Instruments, Inc.

Course Objectives:
Wafer Level-Chip Scale Packaging (WL-CSP) has gained so much success as a packaging form factor in the consumer arena in the past few years that it is almost considered as a "technology commodity". It has been driven by needs for cost reduction, size shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The standard configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability.

Course Outline:
1. Market Drivers for WLPs: Handsets, Medical, Automotive, Space, Imaging Sensors, MEMS, and HBLEDs
2. Key WLP Technologies
3. Equipment & Materials Toolbox
4. Infrastructure Service Providers
5. PCB Pitch Reduction
6. Cost, Benefits, and Drawbacks of WLPs.
7. Reliability: Thermal Cycling, Drop, Flex Testing, and Electromigration
8. Fan-Out WLP
9. Equipment & Materials Toolbox
10. Supply Chain
11. Challenges
12. Embedded Die
13. Equipment & Materials Toolbox
14. Chip First vs. Chip Last
15. Single Die Embedding vs. SiP Module
16. Challenges and Evolution to Large Format Processing

Who Should Attend:
The course will be useful to the following three groups of engineers and scientists: Newcomers to the field who would like to obtain a general overview of WL-CSP, R&D practitioners who would like to learn new methods for solving CSP problems, and those considering WL-CSP as an alternative for their interconnect systems.

3. LED PACKAGING, SYSTEM, AND RELIABILITY CONSIDERATIONS
Course Leader: Xuejun Fan – Lamar University

Course Objectives:
Light emitting diode (LED) has now emerged as promising technology to replace conventional lighting, such as incandescent bulbs and compact fluorescent lamps, due to its superior energy efficiency, environmental friendliness, and particularly long lifetime (in the range of 25,000–100,000 hours). This course will present a comprehensive overview of recent advances in LED packaging, system integration, and reliability issues. Unlike the traditional IC failure that is mainly characterized by catastrophic mode, LED performance is characterized by a dual-degradation mode: light output (lumen maintenance) degradation and color shift. Packaging structure, system integration, and materials play a very important role in LED efficacy and reliability.

Course Outline:
1. Basics of LED Photometry and Colorimetry
    - LED Packaging Evolution
    - LED Packaging Materials: Chip, Phosphor, Silicone, Reflector, Substrate, and System Integration
2. Overview of LED Lumen Maintenance Testing, Related Standards, Accelerated Testing, and Lifetime Prediction
3. LED Color Shift Mechanism, Accelerated Test, and Lifetime Prediction
4. LED Thermal Management
5. LED Driver Reliability: Failure Modes, Lifetime Prediction, and the Interactions with LED Degradation
6. LED System Reliability

Who Should Attend:
The course is designed for staff members, technical managers, LED system reliability, design and manufacturing personnel, reliability engineers, and students who are interested in LED packaging, material selection, and LED reliability. The course does not assume prior knowledge in LED areas.

4. SYSTEM SCALING FOR NEW ERA OF SELF-DRIVING, INFOTAINING AND ELECTRIC CARS

Course Leaders: Rao Tummala and Venky Sundaram – Georgia Institute of Technology

***Course Objectives**:*
Automotives are becoming “electronic devices,” unlike in the past, when they were mainly mechanical devices. Automotive electronics are expected to account for about a third of the total cost of the entire car, about $10,000 for each car. This is a huge market. This course is consistent with three major new drivers in automotive electronics: (1) autonomous driving, (2) secure, high-speed communications and infotainment, and (3) all-electric cars with high-power and high temperature electronics. These drivers require electrical, mechanical and thermal designs; new digital, RF, sensors, millimeter-wave, radar, laser and power technologies. Such systems must integrate many disparate technologies such as high-speed digital, optical, RF, and wireless sensing and wireless power and data processing from hundreds of sensors as well as ultra-high power electronics. The intent of this course is to educate the global R&D community with the market need for the new era of automotive electronics, present technical challenges, and to review the status in the relevant branches of electronics.

Course Outline:
1. Global Need, Vision, and Strategy
2. Computing and Communication Electronics
3. Sensors and Sensor Integration Electronics
4. High-Power Electronics
5. High-Temperature Electronics

Who Should Attend:
Senior marketing and R&D executives as well as engineering specialists who are performing R&D in any one or more of the above areas of the new era of automotive electronics should attend this course.

5. POLYMERS AND NANOCOMPOSITES FOR ELECTRONIC AND PHOTONIC PACKAGING

Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu –Henkel Corporation

Course Objectives:
Polymers and nanocomposites are widely used in electronic and photonic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds, and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance novel no-flow underfills, reworkable underfills for ball grid array (BGA), chip scale packaging (CSP), system in a package (SIP), direct chip attach (DCA), flip-chip (FC), paper-thin IC and 3D packaging, conductive adhesives (both ICA and ACA), embedded passives (high K polymer composites), and nano particles and nanofunctional materials such as CNTs (some with graphenes). It is imperative that material suppliers, formulators, and their users have a thorough understanding of polymeric materials and the recent advances on nano materials and their importance in the advances of the electronic packaging and interconnect technologies.

Course Outline:
1. Fundamentals of Polymers and Materials Science and Engineering
2. Material Needs for Next Generation Electronic Packaging
3. Novel Nanocomposites for Flip-Chip Underfill Applications
4. Recent Advances on Nano Lead-Free Alloys for High Performance Components Interconnects
5. Low-Cost High-Performance Lead-Free Interconnect Materials and Processes
6. Recent Advances on CNTs as Thermal Interface Materials (TIMs)
7. Lotus Effect Coating for Self-Cleaning Applications
8. Fundamentals of Electrically Conductive Adhesives (ECAs)
9. Recent Advances on Conductive Adhesives
10. Recent Advances on Nano Conductive Adhesives

Who Should Attend:
Engineers, scientists, and managers involved in the design, process, and manufacturing of IC electronic components and hybrid packaging, and electronic material suppliers involved in materials manufacturing and research and development should attend.

6. INTEGRATED THERMAL PACKAGING AND RELIABILITY OF POWER ELECTRONICS

Course Leaders: Patrick McCuskey and Avi Bar-Cohen – University of Maryland

Course Objectives:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics. Following a quick review of heat transfer principles and thermal management techniques, along with prognostic health management approaches to assess and ensure reliability, this short course will present the latest developments in the materials (e.g. organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS and systems, along with modeling and testing techniques. This course will emphasize thermal

packaging techniques capable of addressing performance limits and reliability concerns associated with increased power levels and power density in power electronic components.

Course Outline:
1. Introduction to Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques
3. Application of Thermal Management Techniques to Commercial Power Systems/Data Centers
4. Durability Assessment: Failure Modeling, Simulation, Testing, and Health Monitoring
5. Reliability and Thermal Packaging of Active Devices (Si, SiC, GaN) and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, Including Encapsulants
7. Reliability in Assembly Packaging: Rigid PCBs, Solders, Passives, OLED, Flex Circuits
8. MEMS and Sensor Packaging

Who Should Attend:
This course is intended for new and established engineers and technical managers in the field of electronic packaging who would like to learn more about the mechanical and thermal issues involved in reliably packaging devices and circuits for applications involving high voltage, current, and power loss.

7. FUNDAMENTALS OF ELECTRICAL DESIGN AND FABRICATION PROCESSES OF INTERPOSERS, INCLUDING THEIR RDLs

Course Leaders: Ivan Ndip and Michael Töpper – Fraunhofer IZM

***Course Objectives**:*
As a result of their myriad of advantages in system-integration, glass and silicon interposers will continue to play a crucial role in the development of future electronic systems. The fabrication processes and electrical performance of these interposers, including their re-distribution layers (RDLs), will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and electrical design of glass and silicon interposers, including their RDLs. An overview of advanced packaging technologies and the role of interposers will first be given. This will be followed by a thorough discussion of silicon interposers, through-silicon vias (TSV) generation process and tools, as well as glass interposers and options for through-glass vias (TGV) generation and metallization. Major challenges of RDL build-up on thin interposer substrates will be presented and advanced RDL materials and technologies to realize routing down-to 3µm in interposers will be discussed. The fundamentals of efficient electrical design of interposers and RDLs up to millimeter wave frequencies will be given. Finally, the RF performance of transmission lines and vias in these interposers will be compared. Examples of interposers designed and fabricated at Fraunhofer IZM will also be discussed.

Course Outline:
1. Introduction to Advanced Packaging Technologies and the Role of Interposers
2. Silicon Interposers: Illustration of TSV Generation Process and Tools
3. Glass Interposers: Illustration of Technology Options for TGV Generation and Metallization
4. Presentation of Thin Substrate Handling and Temporary Bonding
5. Comparison between Glass, Silicon, and Organic-Based Interposers
6. Illustration of RDL Generation and Their Role in CSP and FO-WLP
7. Discussion of Major Challenges of RDL Build-Up on Thin Interposer Substrates
8. Advanced RDL Materials/Technologies to Realize Routing down to 3µm in Interposers
9. Electrical Design Challenges of Interposers and RDLs: Signal/Power Integrity and EMI Issues

10. New Design Approach for Applications up to Millimeter-Wave Frequencies
11. Explanation of Fundamental Electrical Design Concepts: Impedance, RLCG Parasitics, and S-Parameters
12. Electrical Design, Measurement, and Comparison of Transmission Lines on RDLs and Interposers
13. Electrical Design, Measurement, and Comparison of TSVs and TGVs
14. Examples of Interposers Designed, Fabricated, and Characterized at Fraunhofer IZM

Who Should Attend:
Engineers, researchers, designers, technical managers, and graduate students involved in the process of electrical design, layout, processing, fabrication, and/or system-integration of interposers and electronic packages.

8. INTRODUCTION TO MECHANICS BASED QUALITY AND RELIABILITY ASSESSMENT METHODOLOGY

Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation

Course Objectives:
This course presents a unique integrated methodology that combines two essential domains, engineering mechanics and reliability statistics, to perform standards based or knowledge-based risk assessment to meet the dynamic market demand for electronic devices. To ensure that corporate quality and reliability goals are met, it is vital to have a comprehensive understanding of device usage and complete characterization of physics of failure. This course discusses key elements of Q&R like use condition (UC), accelerated life tests, statistical data analysis methods, acceleration factor models, DPM risk assessment at UC, FA tools/techniques, design for reliability and experiment planning. It also provides an overview of the basic concepts of solid mechanics such as stress-strain curves, characterization of material behavior, stress analysis methods including Finite-Element Analysis (FEA) with specific application to packaging, material characterization metrologies, and FEA model validation techniques. The course offers a deeper dive into key mechanisms like Si-package interactions, package delamination, solder joint reliability, package warpage, etc. to highlight successful application of this integrated methodology. Benefits of driving proactive product risk assessment at UC and optimizing product design/process/materials for reliability are highlighted. The course will also explore the application of this integrated methodology in traditional and new markets like wearables and Internet of Things. Multiple hands-on exercises throughout the duration of the course enhance student learning reinforcing the skills learned.

Course Outline:
1. Packaging Technology: Trends and Challenges
2. Introduction to Quality and Reliability
3. Overview of Key Components of Reliability Statistics and Accelerated Testing
4. Hands-On Class Exercise I
5. Introduction to Solid Mechanics
6. Key Components of Solid Mechanics: Stress/Strain Curves, Failure Theories, and Finite Element Analysis
7. Material Characterization Metrologies and Analysis Validation Techniques
8. Key Failure Mechanisms and Failure Analysis Tools/Techniques.
9. Overlapping Areas between Reliability and Mechanics
10. Overview of the Unified Reliability Assessment Methodology Using Mechanics
11. Application of Methodology to Key Organic Package Failures
12. Hands-On Class Exercise II

13. Summary of Key Learning Elements

Who Should Attend:
Packaging engineers involved in design, development, production, and reliability testing of semiconductor packages would benefit from the course.

9. THERMO-ELECTRIC COOLERS: CHARACTERIZATION, RELIABILITY, AND MODELING

Course Leader: Jaime Sanchez – Intel Corporation

Course Objectives:
Thermo-electric coolers are devices widely used in the semiconductor industry as the main thermal engines for thermal control during test of integrated circuit devices. They offer the ability to both heat and cool a device under test to mimic worst case platform conditions and defect screening at different temperatures. In this short course, we will review fundamental characterization techniques of thermoelectric coolers that allow the direct measurement of relevant properties such as the effective Seebeck coefficient, electrical resistivity, and thermal impedance. A detailed numerical modeling approach will be discussed that utilizes user-defined functions in Fluent that allows a close representation of these devices matching experimental conditions. Experimentation and numerical analysis techniques will be discussed that enable the full characterization of a thermal solution based on thermoelectric coolers both in steady and transient state. A comprehensive overview of modeling and experimentation techniques will be provided that capture the dynamic behavior of a thermal solution connected to a closed loop control algorithm: the impact of various approaches of controlling the junction temperature of a device under test under different conditions, as well as the sensitivity of the dynamic response of the full system including the effect of active power management of the device under test. Finally, experimental techniques based on reliability statistics will be covered that have a direct application into predicting the life of a thermo-electric cooler under various test conditions.

Course Outline:
1. Introduction
    - State-Of-The-Art in Thermo-Electricity
    - Research What is Thermo-Electricity
    - General Industrial Applications
2. TEC Modules Governing Principles
    - Single Peltier Couple to a TEC Module
    - Governing Equations and Relationships
    - Example of TEC Module Selection Based on a Static Cooling Application
3. TEC Module Characterization and Modeling
    - Experimental Setups and Methodology
    - Overview of Analytical Approaches
    - Overview of Transient Characterization
4. Operation of TEC Modules in Dynamic Closed Loop Control
    - Applications to Test ICs
5. Reliability of TECs
    - Overview of Failure Modes
    - Improvements for Test Application
6. Summary and Future Directions
7. References

Who Should Attend.

This course is intended for students and engineers in the electronics cooling industry specifically, but should be of interest for those working with thermo-electric modules in general. The class will cover experimental and numerical methods.

10. FLIP CHIP FABRICATION AND INTERCONNECTION

Course Leaders: Eric Perfecto – GLOBALFOUNDRIES; Shengmin Wen – Synaptics Inc.

Course Objectives:

This course will cover all aspects of lead free solder bumping and highly customized Cu pillar bumping technologies used in today's flip chip products. Single chip, multichip, single unit based BGA packages as well as strip based chip scale packages, Chip-on-Chip, Chip-on-Wafer, and 2.5D/3D flip chip packages will all be discussed and demonstrated. It will detail and compare the various UBM (electroplating, electroless plating, and sputtering) and solder (electroplating, ball drop, IMS, and solder screening) deposition methods. It will include process considerations when joining the various method bumped dies to various types of substrate (organic laminate, ceramic, and Si substrates). This course will cover the accelerated reliability tests currently used to qualify the flip chip connections, the failure types and the analytical tools used to identify defect root cause. A substantial portion of this course will be covering the Cu pillar flip chip technologies with highly customized bumping and assembly process that are applied to flip chip packages inside today's mobile devices. Failure modes, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc. will be included dispersedly in the related subjects of the whole course. The students are encouraged to bring topics and technical issues from their daily job function for group discussions. A 20-minute group exercise at the end of the class is planned to make sure the students can apply the course knowledge to their daily job function.

Course Outline:

1. Introduction to Flip Chip
2. UBM Metal Selection
3. Flip Chip Solder Deposition Processes
4. C4 Fabrication Issues
5. Flip Chip Plastic Ball Grid Array (FCPBGA) Assembly Process Flow
6. Chip/Package Interaction and Electromigration
7. Cu Pillar Flip Chip Summary
8. Cu Pillar Structures
9. Cu Pillar 2D and 3D Assembly: Mass Reflow and Thermal Compression
10. Substrates Technologies for Cu Pillar Flip Chip Assembly
11. Integration Options in Cu Pillar Assembly and Failure Modes
12. Cu Pillar Reliability Assessment
13. Flip Chip Technology Design and Assembly Failure Examples

Who Should Attend:

The targeted audience includes scientists, engineers, and managers currently using flip chip (with solder or Cu pillar) or considering to move from wirebonding and reliability, and product or applications engineers who need a deeper understanding of flip chip advantages, limitations, and failure mechanisms.

11. FAN-OUT WAFER LEVEL PACKAGING

Course Leader: Beth Keser – Qualcomm Technologies, Inc.

Course Objectives:

Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 8 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking. This course has been updated with over 10% new material compared to the first time it was offered last year at ECTC.

Course Outline:
1. Current Challenges in Packaging
2. Definitions and Advantages
3. Applications
4. Package Structures Including Advanced FO Technologies
5. Process
6. Material Challenges
7. Equipment Challenges
8. Design Rules
9. Technology Roadmap
10. Reliability
11. Benchmarking

Who Should Attend:
Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability, and package design should attend this course. Both newcomers and experienced practitioners are welcome.

12. OPERATION, DESIGN, CHARACTERISTICS, AND KEY PARAMETERS OF INTEGRATED SILICON ANALOG COMPONENTS

Course Leader: Badih El-Kareh –Consultant

Course Objectives:
As digital processing extends to more products, an ever-increasing number of analog integrated chips are required to interface with the “real world”. At the root of analog technologies are active components–CMOS, bipolar transistors, high-voltage, junction field-effect transistors–and integrated passive components–capacitors, resistors, varactors, and inductors. The components must satisfy requirements for transistor gain and output resistance, mismatch, and noise which are typically not as important to digital applications. This course provides an overview of integrated analog components, their mode of operation, characteristics, key parameters, and reliability considerations.

Course Outline:
1. Analog/RF CMOS and Differences from Digital CMOS
2. High-Voltage and Power Transistors
    - Laterally Double-Diffused MOSFET (LDMOS)
    - Drain-Extended MOSFET (DEMOS)
3. Component Mismatch
4. Bipolar Transistors (BJTs)
5. Junction Field-Effect Transistors (JFETs)

6. Passive Components
    - Precision Capacitors
    - Precision Resistors
    - Varactors
    - Inductors
7. Component Mismatch and Noise
8. Reliability Considerations

Who Should Attend:
Engineers, managers, and high-level technicians practicing in the field of analog, mixed-signal, power, and RF integrated technologies should attend this course.

13. DESIGN AND ANALYSIS OF HIGH-PERFORMANCE MEMORY SYSTEMS

Course Leader: Wendem Beyene –Rambus

Course Objectives:
This tutorial starts with an introduction to memory systems in computing devices such as computers, tablets, and smartphones. Then, an in-depth analysis of standard memory systems for low-power and high-performance applications is provided. The interactions between the signaling, clocking architecture and packaging technology of a memory interface as well as how these interactions determine the achievable data rates and power efficiency are discussed. Signaling and clocking schemes for standard memories, including DDR3 and DDR4, and mobile memories, including LPDDR3 and LPPDR4 are detailed and compared against each other. Emerging 2.5D/3D memory systems such as WideIO1/2, HBM1/2, and HMC1/2 and packaging options such as BGA, PoP, and the emerging 2.5D/3D are also discussed. Different state-of-the-art memory interfaces will be compared using the metrics such as cost, power efficiency, bandwidth, design complexity, signal and power integrity, thermal solution, and form factor that can help attendees implement or select a solution which best fits their specific application.

Course Outline:
1. Review of Standard Memory Systems: Workstations, Desktops, Laptops, Tablets, and Smartphones
    - DDR, LPDDR, GDDR, HMC, and HBM Memory Interfaces
2. Design Challenges of Low-Power and High-Performance Memory Interfaces in Overall System
3. Design and Optimization of Signaling and Clocking Architectures, Packaging Solutions, Channel, and Power Distribution Systems
4. Dependence of Memory Channels on Different System Environments
    - Examples: DDR4, LPDDR4, and WideIO2 Memory Systems
5. Driver and Receiver Complexity and Resulting Power Consumption in These Memory Systems
    - Channel Attenuation, Dispersion, and Reflection
6. Traditional Wirebond Based Packaging Technologies for Memory Applications
    - Chip-Scale Package (CSP) for DDRx
    - System-in-Package (SiP) and Package-on-Package (PoP) for LPDDRx
7. Advanced 2.5D/3D Memory Packaging Technology Solutions
    - TSV Technology and Si/Glass Interposer for WideIO1 and WideIO2
    - Hybrid Memory Cube (HMC)
    - High Bandwidth Memory (HBM)
8. Analysis and Comparison of Different State of-the-Art Memory Interfaces: Cost, Power

Efficiency, Bandwidth, Design Complexity, Signal and Power Integrity, Thermal Solution, and Form Factor

Who Should Attend:
Package, board, and system designers as well as signal and power integrity engineers of high performance memory systems.

14. POLYMERS FOR ELECTRONIC PACKAGING

Course Leader: Jeffrey Gotro –InnoCentrix, LLC

Course Objectives:
The course will provide a broad overview of polymers used in semiconductor packaging and the important structure-property-process performance relationships. We will cover in more depth the chemistries, material properties, and process considerations for adhesives, underfills, coatings, and mold compounds. Additionally, we will provide an introduction to common thermal analysis methods (DSC, DMA, TMA, and TGA) for the characterization of thermoset polymers used in semiconductor packaging. Finally, the course will provide an introduction to the rheological performance of polymer-based materials used in packaging semiconductors. In most cases, adhesives, underfills, mold compounds, and coatings are applied as a viscous liquid and then cured. The flow properties of these materials are critical to performance in high volume manufacturing. The course will provide an introduction to rheology measurements and examples of rheology issues in semiconductor packaging.

Course Outline:
1. Thermoset Polymers versus Thermoplastics
2. Temperature Dependence of Physical Properties
3. Thermoset Polymers: Curing, Curing Mechanisms, Network Formation
4. Overview of Key Chemistries Used: Epoxies, Acrylates, Polyimides, and Bismaleimides
5. Chemistry of Die Attach Adhesives and Capillary Underfills
6. Chemistries Used in Mold Compounds
7. Packaging Substrate Materials
8. Encapsulants (Mold Compounds) and Coatings
9. Introduction to Rheological Characterization Methods: Types of Rheometers and Basic Techniques
10. Introduction to the Rheological Properties of Adhesives
11. Key Rheology Properties: Shear Thinning, Viscosity, Rheology Changes during Curing

Who Should Attend:
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

15. NOVEL INTERCONNECT AND SYSTEM INTEGRATION ARCHITECTURES

Course Leader: Muhannad Bakir – Georgia Institute of Technology

Course Objectives:
Interconnects have emerged as a critical bottleneck to the realization of lower-power and higher-performance electronics. Coupled with this, the need for ever more tightly integrated systems presents unique cooling and power delivery challenges for next-generation electronics. This short course will present an overview of emerging technologies to address these need

areas and present key modeling results to help guide technology development. The modeling effort presented in the short course will not only help us understand the design considerations of the technologies discussed but will also help benchmark the performance of the various technologies so that optimal systems can be developed.

Course Outline:
1. 3D-TSV Based System Integration
2. Monolithic 3D Based System Integration
3. Advances in Silicon Interposer Technologies (Digital and RF)
4. Photonic Silicon Interposer Technologies
5. Advanced Cooling Technologies, Including Microfluidic Cooling for Interposer and 3D Systems
6. Thermal and Power Delivery (Power Supply Noise) Modeling for 3D Systems
7. Advanced Emerging Concepts in Biotechnology Using 3D Technology

Who Should Attend:
This short course will be of value to those working in the areas of interconnects, packaging, 3D technology, and heterogeneous integration.

16. PACKAGE FAILURE MECHANISMS, RELIABILITY, AND SOLUTIONS

Course Leader: Darvin Edwards –Edwards Enterprises

Course Objectives:
This course explores past and present reliability failure modes and mechanisms that plague semiconductor packages. Primary reliability challenges in TSV and WLCSP packaging, as well as major failure mechanisms for FC-BGA, plastic leaded, no lead, and selected MEMS package types will be described. The class will cover reliability concerns such as TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and wire bonds, Cu vs. Au wire bond reliability challenges, problems associated with delamination in packages, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mechanism, the failure modes and failure analysis techniques needed to verify the mechanisms will be summarized. Recommended failure analysis fault isolation techniques will be described. This solutions focused course concentrates on process parameters, design techniques, and material selections that eliminate the failures and improve reliability to ensure participants can design in reliability and design out failures. The development and characterization of design guidelines that enable reliable products will be described and encouraged. A test structure methodology combined with qualification by similarity will be highlighted as a process for early detection of chip/package reliability risks.

Course Outline:
1. Introduction and Description of IC Package Types
2. Failure Analysis Techniques and Fault Isolation Flow
3. Package Failure Mechanism: FC-BGA
4. Package Failure Mechanism: Molded and Leaded
5. Package Failure Mechanism: WLP
6. Package Failure Mechanism: Embedded Die/Molded WLP
7. Package Failure Mechanism: TSV
8. Package Failure Mechanism: MEMS
9. Materials, Modeling, Design Rules, and Reliability
10. Common Test Structures for Failure Mechanism Identification

11. Qualification by Similarity (QBS) Methods
12. Summary

Who Should Attend:
This class is intended for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms will prove useful. Both beginning engineers and those skilled in the art will benefit from the holistic description of the failure mechanisms and proven solutions.

17. 3D IC INTEGRATION AND 3D IC PACKAGING

Course Leader: John Lau – ASM Pacific Technology Ltd.

Course Objectives:
3D IC packaging and 3D IC integration are different. In general, the TSV (through-silicon via) separates 3D IC packaging from 3D IC integration because the latter use TSVs, but 3D IC packaging does not. TSV is the heart of 3D IC integration. The potential high volume manufacturing of 3D IC integration is: (1) memory-chip stacking; (2) Wide I/O memory (or logic-on-logic); (3) Wide I/O DRAM, Wide I/O 2, Hybrid Memory Cube (HMC), and High Bandwidth Memory (HBM); and (4) Wide I/O interface (or 2.5D IC integration). In this presentation, the supply chains and the critical steps such as FEOL, MOL, BEOL, TSV, MEOL, assembly, and test and their ownerships for high-volume manufacturing for those four groups of 3D IC integration will be discussed. The 3D IC packaging, which has been keeping 3D IC integration away from volume production, will be briefly mentioned first. Key enabling technologies such as TSV forming and filling, front and backside metallization, RDL, temporary bonding and de-bonding, and micro bumping, assembly, and reliability will be presented and discussed.

Course Outline:
1. TSMC's InFO-PoP vs. Samsung's ePoP
2. TSV Technology including Via Formation, Dielectric, Barrier, and Seed Layer Deposition, Cu Plating, and CMP
3. Micro Bumping, Assembly, and Reliability
4. 3D IC Integration such as Samsung's Memory-Chip Stacking, Wide I/O 2, HMC, and HBM
5. 3D IC Integration examples: HMC (Intel, Fujitsu, Altera, Pico Computing)
6. 3D IC Integration examples: HBM/HBM2 (AMD, NVIDIA, Open-Silicon, Hynix/Samsung), and Samsung's Widcon
7. 2.5D IC Integration (Interposers): TSMC's CoWoS
8. 2.5D IC Integration (TSV-less Interposers): ITRI's TSH, Intel's EMIB, Xilinx/SPIL's SLIT, Amkor's SLIM
9. Supply Chains and Ownership for 2.5D/3D IC Integration
10. Re-Distribution Layers; Polymer and Cu Damascene Methods
11. Thin-Wafer Handling and Cu Revealing
12. Embedded 3D Hybrid Integration

Who Should Attend:
If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer's books, *Reliability of RoHS Compliant 2D and 3D IC Interconnects*, *TSV for 3D Integration*, and *3D IC Integration and Packaging*.

18. THERMO-ELECTRICAL CO-DESIGN OF 3D CHIP STACKS

Course Leaders: Ankur Srivastava and Avi Bar-Cohen – University of Maryland

Course Objectives:
3D integration provides significant improvements in device density, interconnect delays, system integration, and computational efficiency but is expected to lead to higher heat densities, along with decreased thermal management access to individual chips and on-chip hotspots. To achieve the inherent computational advantages of 3D integration it will, thus, be necessary to unify the thermal and electrical design of 3D chip stacks and explore new thermal management paradigms for such packaging form factors. This PDC will begin with a brief review of chip packaging, placing 3D chip stacks in the context of packaging history and identifying the form factors and heat dissipation loads expected in homogeneous and heterogeneous 3D integration. Attention will then turn to thermal-electrical "co-design," unifying the circuit layout with the thermal and fluidic aspects of the design to create an integrated co-design environment that enables designers to estimate the impact of the cooling solutions on the electrical aspects and vice versa. Recognizing the growing popularity of FPGAs, especially those which exploit 3D integration, the discussion shall pay attention to the nuances of FPGA design, as well as the more-traditional ASICs. It will be shown that relying on conventional "remote cooling" techniques for 3D integration could have catastrophic consequences, necessitating use of embedded cooling solutions, including integrated micro-fluidics, to achieve the performance goals. The PDC will close with several co-design case studies which demonstrate the potential impact of such a design activity on the performance and energy efficiency of 3D ICs

Course Outline:
1. Thermal Packaging History and Trends
2. Thermal Management Requirements for Chips, Chip Stacks, and MMICs
3. Gen-3 Embedded Cooling Options: Microfluidics, Conductive Substrates, Thermal Interconnects, Thermoelectric Coolers
4. Electronic Design Automation
5. Thermo-Electrical Co-Design Case Studies
    - 3D Unified Micro-fluidic Thermal Interconnect Networks
    - Gate Level Optimizations Unlocked by Co-Design
    - 3D CPU Architectures Enabled by Co-design: Impact on Performance and Energy Efficiency
    - Microfluidic Cooling and Reconfigurable Platforms: FPGAs
6. Future Challenges and Opportunities

Who Should Attend:
IC package design engineers and managers that are looking to learn about the electrical performance design challenges and techniques as well as those packaging SI/PI engineers wanting to refresh their conceptual understanding of the fundamentals and the challenges posed by process limitations should attend this class.