4. Moore’s Law for Packaging to Replace Moore’s Law for ICs

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Course Objective:

This course proposes Moore’s Law for Packaging to replace Moore’s Law for ICs, as this is seen as coming to an end. Moore’s Law for ICs is about scaling transistors to ever smaller sizes, from node to node and interconnecting and integrating these to result in more transistors in smaller chips at lower cost from 300 mm wafers. As transistor scaling and integration comes to an end due to physical, material and electrical limitations, Moore’s Law for Packaging (MLP) can be viewed as interconnecting and integrating smaller chips with the highest transistor density with the highest performance at the lowest cost. Package or system scaling is proposed to be one and the same, as the end goal of packaging is a system. Just as Moore’s Law has two components: number of transistors and cost of each transistor, Moore’s Law for Packaging is proposed to have two components as well: the number of interconnections or I/Os and the cost of each I/O. This course lays the ground work for Moore’s Law for Packaging by showing how I/Os have evolved from one package family node to the next, starting with <16 I/Os in 1960s to the current silicon interposers with about 200,000 I/Os. It proposes a variety of ways to extend Moore’s Law such as extending Si interposers and beyond, using glass in panel embedding. As Moore’s Law for Electronic Packaging comes to its own end, this article proposes 3D opto-electronic packaging as the next Moore’s Law for Packaging.

Moore’s Law has been the driving force behind transistor scaling and integration as well as reduction in cost of transistors during the last six decades. But electronic systems such as smartphones, self-driving electric cars and machines mimicking human brains, are more than transistors and ICs. Moore’s Law for ICs brought electronics to more than a trillion-dollar industry. But Moore’s Law, which includes both increased transistor integration and cost reduction every two years, is being predicted to come to an end, at least in cost, if not in transistors. What will take its place then for electronics systems of the future? This article proposes Moore’s Law for Packaging to replace Moore’s Law for ICs, at least, in cost, in the short term. While reducing transistor size, referred to as transistor scaling, along with their interconnections and integration, was the basis of Moore’s Law for ICs. Component size reduction for both active and passive system components, referred to as system scaling, along with their interconnections and integration, can become Moore’s Law for Packaging to form packaged systems.

Just as Moore’s Law has both a doubling of transistors and a simultaneous cost reduction from node to node every 18-24 months, Moore’s Law for Packaging must do the same. Interconnections have been driven by computing systems and within computing systems, between logic and memory. The new era of artificial intelligence, mimicking human brains, is yet another reason for Moore’s Law for System Interconnections.
Currently, the most advanced Moore’s Law for Packaging is with wafer-based silicon packaging. But silicon-based packaging has many limitations at material, substrate or interconnect and system levels. At material level, its electrical loss and its dielectric constant are very high. At interconnect level, its capacitance and resistance are very high, leading to so-called RC delays. In addition, Si-based packaging doesn’t conform to Moore’s Law for cost. Cost, of course, is the basis for going away from Moore’s Law for ICs. At system levels, Si interposers, while they are perfectly matched to ICs, they are totally mismatched to boards, requiring additional packaging, thus making system level interconnections even longer. So, what are future technologies beyond Si interposers to drive Moore’s Law for packaging. This course will present and discuss a variety of options.

Course Outline:

1. Current Approach to Devices and Systems
2. Moore's Law for ICs, Its Evolution and Its Future
3. Three Eras of Moore's Law: For ICs, Packaging or Interconnections and for Systems
4. Moore's Law for Packaging: Observation and Proposal
5. Evolution of Package Interconnections(I/Os) from 1960s consistent with Moore's Law
6. Future of Moore's for Packaging

Who Should Attend:
R&D executives as well as senior technical and marketing managers involved in all aspects of electronics from academic and industry R&D, supply-chain IC, Package and systems manufacturing, marketing, investments and users who deal with strategic directions for their company.

Bio:

Rao Tummala is the Joseph M. Pettit Chair Professor and Director in 3D Systems Research Center in the School of Electrical and Computer Engineering and Materials Science and Engineering at Georgia Tech. He is also the Founding Director of the first NSF ERC in the U.S. He is a world-renowned packaging expert and has developed several major technologies from concept to manufacturing including the industry's first 100-chip ceramic modules, first plasma display and thin film magnetic storage devices for which contributions he was named an IBM Fellow. Prior to joining Georgia Tech, he was Director of Packaging for IBM.