

2. Introduction to Fan-Out Wafer Level Packaging

Course Leader: Beth Keser – Intel Corporation

Course Objective:

Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 10 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wire bond and bump interconnections, substrates, lead frames, and the traditional flip chip or wire bond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking.

Course Outline:

1. Current Challenges in Packaging
2. Definition and Advantages
3. Applications
4. Package Structures
5. Process
6. Material Challenges
7. Design Rule Roadmap
8. Reliability
9. Benchmarking

Who Should Attend:

Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Suppliers who are interested in supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

Bio:

BETH KESER, Ph.D., a recognized global leader in the semiconductor packaging industry with over 20 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 28 patents and patents pending and over 40 publications in the semiconductor industry. For over 7 years, Beth led the Fan-Out and Fan-In Wafer Level Packaging Technology Development and NPI Group at Qualcomm where she and her team qualified over 50 products resulting in over 8 billion units shipped--technology consumers around the world enjoy in cell phones today. Beth is also an IEEE EPS Distinguished Lecturer who chaired IEEE EPS's 2015 ECTC and is currently EPS's VP of Education. Based in Munich, Germany, Beth currently leads the Packaging & Systems Technology department in Intel's Platform Engineering Group.