17. From Wafer to Panel Level Packaging

Course Leaders: Tanja Braun and Michael Töpper – Fraunhofer IZM

Course Objective:

Panel Level Packaging (PLP) is one of the latest trends in microelectronics packing. Besides technology developments towards heterogeneous integration including multiple die packaging, passive component integration in package and redistribution layer or package-on-package approaches also larger substrates formats are targeted. Manufacturing is currently done on wafer level up to 12”/300 mm and 330 mm respectively. For higher productivity and therewith lower costs larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP has the opportunity to adapt processes, materials and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when moving from wafer to panel level is not possible. Materials, equipment and processes have to be further developed or at least adapted. The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging including Fan-out Panel Level Packaging substrate embedding approaches. This will include material discussion, technologies, applications and market trends as well as cost modelling.

Course Outline:

1. Introduction Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-out Wafer Level: Material, Processes, Applications
4. Introduction and Definition Level Packaging
5. Fan-out Panel Level Packaging: Technologies, Challenges and Opportunities
6. Substrate Embedding Technologies
7. Cost Modelling.

Who Should Attend:

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging. Engineers and manages are welcome as detailed technology descriptions as well as market trends, applications and cost modelling are presented.

Bio:

Tanja Braun is from Fraunhofer IZM. She studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins.

Michael Töpper, Fraunhofer IZM, has a M.S. degree in Chemistry and a PhD in Material Science. Since 1994 he is with the Packaging Research Team at TU Berlin and Fraunhofer IZM. In 1997 he became head of a research group. In 2006 he was also a Research Associate

Professor of Electrical and Computer Engineering at the University of Utah, Salt Lake City. The focus of his work was Wafer Level Packaging applications with a focus on materials. Since 2015 he is part of the business development team at Fraunhofer IZM. Michael Töpper is Senior Member of IEEE-EPS and has received the European Semi-Award in 2007 for WLP. He has published several book chapters and is author and co-author of over 200 publications.