13. Fan-Out Wafer/Panel Level Packaging and 3D IC Heterogeneous Integration

Course Leader: John Lau – ASM Pacific Technology Ltd.

Course Objective:

Recent advances in, e.g., fan-out wafer/panel level packaging (TSMC's InFO-WLP and Fraunhofer IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration, 3D CIS/IC integration, and 3D MEMS/IC integration will be discussed in this presentation. Emphasis is placed on various FO-WLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FO-WLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor, SPIL/Xilinx, ASE, MediaTek, Intel, ITRI, Shinko, Cisco/eSilicon, Sony's TSV-less CIS, and Samsung/Hynix (HBM3) will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:

1. FOW/PLP: Chip-First (Die-Up/Down), Chip-Last (RDL-First)
2. RDL Fabrications: Polymer, PCB/LDI, Cu Damascene Methods
3. InFO-WLP, TSMC InFO-PoP vs. Samsung ePoP
4. Dielectric and Epoxy Mold Compound
5. Semiconductor and Packaging for IoTs (SiP)
6. Wafer vs. Panel Carriers, WLSiP and PLSiP
7. TSV formation
8. Memory Chip Stacking with TSV: Samsung's DDR4
9. Hybrid Memory Cube (HMC) with TSV: Intel's Knights Landing with Micron's HMC
10. High Bandwidth Memory (HBM) with TSV: AMD/Nvidia's GPU, Hynix/Samsung's HBM
11. Memory + Logic with TSV: Samsung's Widcon
12. 3D IC/MEMS Integration and 3D IC/CIS Integration
13. Embedded 3D Hybrid Integration
14. 2.5D IC Integration: TSMC/Xilinx's CoWoS (Chip-on-Wafer-on-Substrate)
15. TSV-Less Interposer: Xilinx/SPIL's SLIT, Amkor's SLIM, ASE's FOCoS, Intel's EMIB, ITRI's TSH, Shinko's i-THOP, Cisco's Organic Interposer, Sony's CIS, SPIL/Xilinx's NTI, Samsung's Organic Interposer, etc.
16. Semiconductor Packaging New Trends

Who Should Attend:

If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer's books and the papers published by others.

Bio:

John H. Lau has been a senior technical advisor of ASM since 2014 and a Senior Scientist/MTS at HP Lab/Agilent in California, US for more than 25 years. With more than 39 years of R&D and manufacturing experience in semiconductor packaging, he has published more than 480 peer-reviewed papers, 30 issued and pending US patents, and 19 textbooks on flip chip technologies, WLCSP, FOWLP, BGA, TSV for 3D integration, advanced MEMS packaging, lead-free solder and manufacturing, reliability of 2D and 3D IC interconnections.