10. Flip Chip Technologies

Course Leaders: Eric Perfecto – Independent Consultant and Shengmin Wen – Synaptics Inc.

Course Objective:
This course will cover the fundamentals of all steps and aspects of flip chip assembly process including wafer bumping, solder joint formation, underfill types, substrate selection, and reliability evaluation. The course is divided into two major sections. The first section is devoted to bumping technology. Two major bumping technologies that are used in today's flip chip assembly, i.e., lead-free solder bumping and highly customized Cu Pillar bumping, are discussed in depth, including the details and comparison of various UBM (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc. The second section focuses on the details of assembly processes and their applications to single, multi-die, and multi-level flip chip integration, as well as wire bond / flip chip mixed integration. For example, the chip scale packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages are all discussed with actual industrial leading application cases. In depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, and the important roles of electrical and mechanical simulation, Si die floor plan optimization and its consequence on packaging, among others. Students will understand the versatility of flip chip technologies and learn a range of criteria that they can apply to their daily work needs. This section also provides the trend in the flip chip assembly technologies.

The goal of this course is to provide the students with a list of options to apply to their particular flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. A substantial portion of this course will be covering the Cu Pillar flip chip technologies. The students are encouraged to bring topics and technical issues from their past, present and future job function for group discussions. A 20 minutes group exercise at the end of the class is planned to make sure the students can walk away with the course knowledge that applies to their daily job functions.

Course Outline:

1 Introduction to Flip-Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Flip Chip Si Package Co-Design and Chip-Package Interaction
5. Flip Chip New Trends: Wafer Level, Panel Level, and u-BGA
6. Substrate Technologies, Underfill, Package Warpage Control, and Yield
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7. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
8. Bumping General
9. Flip Chip Under-Bump Metal and Intermetallics
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration

14. Non-Solder Interconnects

Who Should Attend:
The targeted audience includes scientists, engineers, and managers currently using flip-chip (with solder or Cu pillar) or those considering moving from wire bonding to flip-chip, as well as reliability, product or applications' engineers who need a deeper understanding of flip-chip technologies: the advantages, limitations and failure mechanisms.

Bio:
Dr. Shengmen Wen is the Principal Package Architect at Synaptics Inc., has 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. Recent years, he focused on chip scale package (CSP) including wirebond, flipchip, wafer level Fan-In and Fan-out, and panel level packaging development. In particular, he has extensive and unique experiences in flip chip assembly technologies that uses fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, and advanced fine pitch flip chip assembly process. He previously worked at Amkor Technology where he was a director of 3D CSP Product Group. Dr. Wen received his Ph.D. in Theoretical and Applied Mechanics from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science based fatigue theory. Dr. Wen has been actively participating and contributing to industry technical conferences to learn, to share, and to contribute.

Eric Perfecto has over 36 years of experience working in the development and implementation of advanced packages, including Principal Member of the Technical Staff at GLOBALFOUNDRIES and C4 Development Chief Technologist at IBM. Responsivities included UBM and Pb-free solder definition for u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College. Eric has published over 75 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards and an IBM Outstanding Contribution Award for the Development of 3D Wafer Finishing Process (2014). Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. He has achieved senior member status from IMAPS and Society of Plastic Engineers. He is an IEEE Fellow, a Distinguish Lecturer, the Awards Program Director and elected board member of the Electronics Packaging Society of IEEE.