13. Fan-Out Wafer/Panel Level Packaging and 3D IC Heterogeneous Integrations

Course Leader: John Lau – Unimicron

Course Objective:

Recent advances in, e.g., fan-out wafer/panel level packaging (TSMC's InFO-WLP and Fraunhofer IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration, 3D CIS/IC integration, and 3D MEMS/IC integration will be discussed in this presentation. Emphasis is placed on various FO-WLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FO-WLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor, SPIL/Xilinx, ASE, MediaTek, Intel, ITRI, Shinko, Cisco/eSilicon, Sony's TSV-less CIS, and Samsung/Hynix (HBM3) will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:

1. Formation of FOWLP: (a) Chip-first (die face-down), (b) Chip-first (die face-up), and (c) Chip-last (or RDL-first)
2. Fabrication of Redistribution Layers (RDLs): (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu damascene + CMP, (c) Hybrid RDLs, and (d) ABF/LDI and PCB Cu-plating + Etching
3. Warpages: (a) Kinds of Warpages and (b) Allowable of Warpages
4. Reliability of FOWLP: (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations
5. TSMC InFO: (a) InFO-PoP, and (b) InFO_AiP/RF-Chip Driven by 5G
6. Samsung PLP: (a) PoP for Smart watches and (b) SiP SbS for Smartphones
7. Formation of FOPLP: (a) PCB + SAP, (b) PCB + LDI, (c) PCB + TFT-LCD, and (d) PCB/ABF/SAP + LDI
8. Wafer vs. Panel: (a) Application Ranges of FOWLP and FOPLP, and (b) Critical Issues of FOPLP
9. Trends in FOWLP and FOPLP
10. System-on-Chip (SoC)
11. Heterogeneous Integrations or SiPs
12. Heterogeneous Integrations vs. SoC
13. Heterogeneous Integrations on Organic Substrates
14. Heterogeneous Integrations on Silicon Substrates (TSV-Interposers)
15. Heterogeneous Integrations on Silicon Substrates (TSV-less Interposers)
16. Heterogeneous Integrations on Fan-Out RDL Substrates: STATSChipPac's FOFC-eWLB, ASE's FOCoS, MediaTek's FO-RDLs, Samsung's Si-Less RDL Interposer, and TSMC's InFO_oS, and InFO_MS
17. Heterogeneous Integration of (a) PoP, (b) Memory Stacks, (c) Chip-to-Chip Stacks, (d) CIS and Logic Chip, (e) LED and TSV-Interposers, (f) MEMS and Logic Chip, and (g) VESCL and PD
18. Trends in Heterogeneous Integrations

Who Should Attend:

If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer's books and the papers published by others.

Bio:
John H. Lau
If you are involved with any aspect of the electronics and optoelectronic industry, you should attend this course. The materials are from the papers from others and the instructor's books, Fan-Out Wafer-Level Packaging (Springer 2018) and Heterogeneous Integrations (Springer 2019). Each attendee will receive more than 250 pages of handouts.