5. INTRODUCTION TO MECHANICS BASED QUALITY AND RELIABILITY ASSESSMENT METHODOLOGY

Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation

Course Objective:
This course presents a unique integrated methodology that combines two essential domains, engineering mechanics and reliability statistics, to perform standards based or knowledge-based risk assessment to meet the dynamic market demand for electronic devices. To ensure that corporate quality and reliability goals are met, it is vital to have a comprehensive understanding of device usage and complete characterization of physics of failure. This course discusses key elements of Q&R: Use Conditions (UC), accelerated life tests, statistical data analysis methods, acceleration factor models, DPM risk assessment at UC, FA tools/techniques, design for reliability, and experiment planning. It also provides an overview of the basic concepts of solid mechanics such as stress-strain curves, characterization of material behavior, stress analysis methods including FEA with specific application to packaging, material characterization metrologies, and FEA model validation techniques.

The course offers a deeper dive into a few key mechanisms like Si-package interactions, package delamination, SJR, package warpage, etc. to highlight successful application of this integrated methodology. They highlight benefits of driving proactive product risk assessment at UC and optimizing product design/process/ materials for reliability. The course will also explore the application of this integrated methodology in traditional and new markets like Internet of Things, Automotive, Industrial and other harsh environment applications. Multiple hands-on exercises throughout the duration of the course enhance student learning reinforcing the skills learned.

Course Outline:
1. Packaging Technology: Trends and Challenges
2. Introduction to Quality and Reliability
3. Overview of Key Components of Reliability Statistics and Accelerated Testing
4. Hands-On Class Exercise 1
5. Introduction to Solid Mechanics
6. Key Components of Solid Mechanics: Stress/Strain Curves, Failure Theories, and Finite Element Analysis
7. Material Characterization Metrologies and Analysis Validation Techniques
8. Key Failure Mechanisms and Failure Analysis Tools/Techniques.
9. Overlapping Areas between Reliability and Mechanics
10. Overview of the Unified Reliability Assessment Methodology Using Mechanics
11. Application of Methodology to Key Organic Package Failures
12. Hands-On Class Exercise 2
13. Summary of Key Learning Elements

Who Should Attend:
Packaging engineers involved in design, development, production, and reliability testing of semiconductor packages would benefit from the course.

Bio 1:
Shubhada Sahasrabudhe is a Senior Engineering Manager at Assembly Test Technology Development Q&R, Intel. She manages Enabling TD Q&R team with focus on Solder Joint

Reliability, IMAX, Package Thermals and Thermal Enabling of bare die components. She graduated with Mechanical Engineering degree from University of Maryland, College park. Shubhada has been in Intel for 16 years and has worked on a range of Q&R areas like process/design/material based Q&R FMEAs and risk assessment strategies, use condition/physics based predictive reliability modeling, advanced statistical models, to enable faster, accurate Q&R risk assessments that drive product reliability-cost-performance optimization. Shubhada has over 30 publications and 11 patents/ trade secrets filed in the field of semiconductor packaging. She has taught packaging technology reliability courses at Arizona State University and several packaging conferences.

Bio 1:

Sandeep Sane is a Principal Engineer at Intel. He received his M.S./Ph.D. from California Institute of Technology, Pasadena in Aerospace Engineering with major in Solid Mechanics. He holds B.S. in Mechanical Engineering from Indian Institute of Technology, Bombay (Mumbai). Sandeep is currently responsible to drive novel technical solutions across packaging technologies in the Assembly and Test Technology Development (ATTD) organization, Intel Corp., Chandler. In the past he managed a technical team of 30 engineers with a charter to deliver fundamental understanding of various mechanical issues in electronic packaging, establish roadmaps for ATTD and work directly with Intel's customers (OEM/ODMs) and suppliers to resolve thermo-mechanical issues. Sandeep has filed for more than 15 patents and published several technical articles in various conferences and journal proceedings. He is also a recipient of numerous awards across Intel for his technical contributions.