4. FUTURE OF DEVICE AND SYSTEMS PACKAGING IN POST MOORE'S LAW

Course Leader: Rao Tummala – Georgia Institute of Technology

Course Objective:

Semiconductor and systems landscape is changing dramatically. ICs, on one hand, for the most part, are becoming commodities, providing much lower profit margins than ever before, leading to industry consolidation to less than ten manufacturing companies within the next decade, worldwide. In addition, the cost and complexity of transistor scaling is growing exponentially. There is no longer a cost reduction as the next node is introduced with higher transistor density. In addition, IC performance is being greatly impacted by interconnect delay and leakage.

The driving engines for electronic systems, on the other hand, are also changing dramatically to smart, wearable, wireless healthcare, wireless networks and new era of self-driving and electric cars, requiring an entirely different vision and strategy than transistor scaling alone that has been and continued to be practiced during the last 60 years. These systems are small to ultra-small systems and yet must perform dozens of functions that include high-speed digital, high-efficiency power, 5G and millimeter wave, MEMS and sensors. The new era of automotive electronics, in addition, requires a variety of sensing technologies for self-driving cars such as camera, LiDAR and radar, and ultra-high power for electric cars. All these emerging or next generation computing, communications, consumer and automotive systems pose device, packaging and integration barriers.

They require new role for packaging. Future Packaging must address these devices and systems' barriers by enabling better and cheaper devices and highly-integrated and ultra-miniaturized systems. The advances need to be more than Moore's (MTM) Law with on-chip transistor integration with 2D and 2.5D MCM, 3D stacked ICs with TSV and SIP. They require a new paradigm in systems packaging, referred to as "System Moore's" Law (SM) for complete systems. Such a concept requires new system package architecture beyond SIP, 2.5D and 3D with TSV.

The course will review the current approach to devices, device packaging and system packaging. These include traditional single and multi-chip packaging as well as the recent focus in embedded and fan-out packaging. This course describes IC and system packaging challenges and potential solutions that lie ahead in strategic technologies, manufacturing infrastructures and applications.

Course Outline:

1. Emerging Electronic System
2. Current Approach to Devices and Device Packaging
3. Strategic Packaging Technologies to Enable Future Devices
   - Integration of Homogeneous and Heterogeneous Devices in 2D, 2.5D, and 3D Multi-Chip Packaging which Requires I/O Scaling Similar to BEOL
4. Strategic Systems Packaging Technologies to Enable Future Systems
   - Envisioned is a System Scaling Concept that Includes Devices by Transistor Scaling but goes Beyond to include Components and Interconnections
5. Current vs. Future Packaging Manufacturing Infrastructure
   - Current: Limited to Wafer-Based with BEOL Tools with Low I/O Density
   - Future: Panel-Based BEOL-Like Packaging
6. Emerging and High-Growth Applications

7. Applications of Future Packaging to Emerging Systems

Who Should Attend:
Senior marketing and R&D executives as well as senior managers who are dealing with strategic issues facing the electronics industry should attend.

Bio:

Rao Tummala is the Joseph M. Pettit Chair Professor and Director in 3D Systems Research Center in the School of Electrical and Computer Engineering and Materials Science and Engineering at Georgia Tech. He is also the Founding Director of the first NSF ERC in the U.S. He is a world renowned packaging expert and has developed several major technologies from concept to manufacturing including the industry's first 100-chip ceramic modules, first plasma display and thin film magnetic storage devices for which contributions he was named an IBM Fellow. Prior to joining Georgia Tech, he was Director of Packaging for IBM.