17. SOLVING PACKAGE FAILURE MECHANISMS FOR IMPROVED RELIABILITY

Course Leader: Darvin Edwards – Edwards Enterprises

Course Objective:

This course explores past and present reliability failure modes and mechanisms that plague semiconductor packages. Primary reliability challenges and major failure mechanisms will be investigated in emerging and high-volume package types: TSV, FOWLP, WLCSP, FC-BGA, plastic leaded, no lead and selected MEMS packages. The class will detail reliability topics such as TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and wire bonds, Cu vs. Au wire bond reliability challenges, complications associated with package delamination, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mechanism, the prevalent failure modes and failure analysis techniques needed to verify the mechanisms will be summarized. Recommended failure analysis fault isolation techniques will be described. This solutions-focused course concentrates on process parameters, design techniques and material selections that eliminate failures and improve reliability to ensure participants can design-in reliability and design-out failures. Characterization and implementation of design guidelines that enable reliable products will be described and encouraged. A test structure methodology combined with qualification by similarity will be highlighted as a technique for early detection of chip/package reliability risks.

Course Outline:

1. Introduction and Description of IC Package Types
2. Failure Analysis Techniques and Fault Isolation Flow
3. Package Failure Mechanisms: FC-BGAs
4. Package Failure Mechanisms: Molded and Leaded Packages
5. Package Failure Mechanisms: WLCSPs
6. Package Failure Mechanisms: Embedded Die/Fan-Out WLPs
7. Package Failure Mechanisms: TSVs
8. Package Failure Mechanisms: MEMS
9. Materials, Modeling, Design Rules and Reliability
10. Common Test Structures for Failure Mechanism Identification
11. Qualification by Similarity (QBS)
12. Summary

Who Should Attend:

This class is intended for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms will prove invaluable. Beginning engineers and those skilled in the art will benefit from the holistic description of the failure mechanisms and the provided proven solutions.

Bio:

Darvin Edwards joined Texas Instruments in 1980 with a B.S. degree in Physics from Arizona State University. His responsibilities included developing integrated test structures to evaluate chip/package interactions, improving the thermal performance of TI's products, and leading the Dallas package modeling team for fifteen years. He wrote design rules to ensure package reliability, and helped develop such package technologies as flip-chip BGA, CSP, WCSP and TSVs. Along the way, he helped introduce HAST and standardized thermal tests. He was elected TI Fellow in 1999; he was most recently responsible for Analog Si/Pkg interactions

within the Semiconductor Packaging Group before retiring in 2013. Darvin formed Edwards' Enterprise Consulting LLC in 2014, specializing in helping companies solve package reliability and thermal problems, as well as providing training worldwide. He has served as Member at Large for the IEEE CPMT society and is currently co-chair of the Electronics Components and Technology Conference Applied Reliability committee of which he has been a member for 37 years. Darvin has authored and co-authored over 60 papers and articles in the field of IC packaging, has written two book chapters, and holds 26 US patents. He has been active with JEDEC, SRC, INEMI, and IMAPS.