15. CORROSION IN MICROELECTRONIC PACKAGES

Course Leader: Varughese Mathew – NXP Semiconductors

Course Objective:

Corrosion of various components of electronic packages (wires, bond pads, lead frames etc.) has been identified as a major contributor to semiconductor device failures. The objective of this course is to describe fundamental aspects of corrosion including basic principles of electrochemical corrosion, thermodynamic and kinetic factors and mechanisms of corrosion generally observed in packaging of microelectronic devices. Various types of corrosion occurring in package systems will be described. This will include Galvanic corrosion, Crevice corrosion, Pitting corrosion, Stress corrosion and Metal Dendrite formation.

1. Fundamental Aspects of Corrosion
   - Basic Principles of Electrochemical Corrosion
   - Thermodynamic and Kinetic Factors
   - Factors Affecting Corrosion
2. Types of Corrosion: Galvanic, Pitting, Crevice, and Stress
3. Illustration /Case Studies of Corrosion Induced Failures in Microelectronic Packages
   - Case I: Corrosion Reliability of Copper Wire-bonded Packages
   - Case I: Aluminum Bond Pad Corrosion of Wire-bonded Packages
   - Case I: Cu-Al Intermetallic Corrosion and Copper Wire-bond (CuWB) Reliability
   - Case II. Failures due to Electro Chemical Migration / Dendrite Formation
   - Case II: Corrosion Control and Protection
4. General Methods of Corrosion Control and Protection: Corrosion Inhibitors, Cathodic Protection, and Sacrificial Anodes

Who Should Attend?

Anyone interested in understanding corrosion reliability of electronic packaging is encouraged to attend this course. This course will be useful for Engineers and Managers responsible for package reliability, package quality, new packaging development and package characterization.

Bio:

Varughese Mathew joined Motorola Semiconductor Products Sector (later Freescale Semiconductor and now NXP Semiconductors), Austin, TX, in 1997 after being a Post-Doctoral fellow in the Department of Materials Science and Engineering, University of Arizona, Tucson, AZ, where he carried out research in the areas of Semiconductor processing and Chemical Mechanical Planarization. In Motorola /FSL/NXP he has worked on various areas of Electronic Package development including flip chip package development, electroplated bumps, lead free solder applications and leaded packages. He led multiple package reliability projects such as bump electromigration, soft error, solder joint, lead frame package reliability etc. He led semiconductor process/integration projects such as Copper Interconnect process development for advanced device nodes. He carried out extensive research and development work in the areas of corrosion, electrochemical and electroless metal deposition for semiconductor applications and Through –Silicon Via fill development (TSV) for 3D Interconnect applications. His recent focus is on the packaging material development and reliability for high temperature automotive applications. Recent work includes enablement of AEC (Automotive Electronic Council) Grade 0 and 1 capability for various types of packages including QFP, QFN and BGA and package reliability due to corrosion. Varghese Mathew has served as a member of the Packaging Technical Advisory Board (TAB) of IPS/GRC division of Semiconductor Research Corporation (SRC) from 2008 and was the 2012 TAB Chair. He has authored or co-authored

about 40 technical papers and Inventor/co-inventor of 27 U.S. patents. He is a member of Electrochemical Society and IEEE.