13. FAN-OUT WAFER-LEVEL PACKAGING AND 3D PACKAGING

Course Leader: John Lau – ASM Pacific Technology Ltd.

Course Objective:

Recent advances in, e.g., fan-out wafer/panel level packaging (TSMC's InFO-WLP and Fraunhofer IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights Landing CPU), 2.5D IC Integration (Xilinx/TSMC's CoWoS and TSV-less interconnects and interposers), embedded 3D hybrid integration (of VCSEL, driver, serializer, polymer waveguide, etc.), 3D CIS/IC integration, 3D MEMS/IC integration, and Cu-Cu hybrid bonding will be discussed in this presentation. Emphasis is placed on various FOWLP assembly methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FOWLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB/LDI will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor, SPIL/Xilinx, STATS ChipPac, ASE, MediaTek, Intel, ITRI, Shinko, Cisco/eSilicon, Samsung, and Sony will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:

1. Patents Impacting the Semiconductor Packaging
2. FOWLP Formations: Chip-First (Face-down), Chip-First (Face-up), and RDL-First
3. RDL Fabrication methods: Polymer, PCB/LDI, and Cu damascene
4. TSMC InFO-WLP and INFO-PoP vs. Samsung-ePoP
5. Wafer vs. Panel Carriers (WLSiP vs. PLSiP)
6. Notes on Dielectric, Epoxy Molding Compound, and Compression Molding
7. Memory Chip Stacking with TSVs – Samsung's DDR4
8. Hybrid Memory Cube (HMC) – Micron/Intel's Knights Landing for CPU
9. High Bandwidth Memory (HBM): Hynix/AMD's and Samsung/Nvidia's GPU
10. Integration: 3D IC/CIS, 3D IC/MEMS, and Embedded 3D Hybrid
11. TSMC/Xilinx's CoWoS
12. TSV-Less: Xilinx/SPIL's SLIT, NTI SLIM, and Amkor's SLIM
13. TSV-Less: STATS ChipPac's FOFC-eWLB and ASE's FOCoS
14. TSV-Less: Intel's EMIB
15. TSV-Less: Cisco/eSilicon's Organic Interposer
16. TSV-Less: Sony's CIS (Cu-Cu Hybrid Bonding)
17. New Trends in Semiconductor Packaging

Who Should Attend:

If you are involved with any aspect of the electronics assemblies, you should attend this course. All the materials are based on the papers and books published in the past 3 years and each participant will receive more than 200 pages of the lecture notes.

Bio:

John H. Lau has been a senior technical advisor of ASM in Hong Kong since 2014 and a Senior Scientist/MTS at HP Lab/Agilent in California for more than 25 years. With more than 39 years of R&D and manufacturing experience in semiconductor packaging, he has published more than 450 peer-reviewed papers, 30 issued and pending US patents, and 18 textbooks on flip chip technologies, WLCSP, BGA, TSV for 3D integration, advanced MEMS packaging, and reliability

of 2D and 3D IC interconnections. John received many awards and is an elected ASME and IMAPS Fellow and has been an IEEE Fellow since 1994.