11. WAFER LEVEL-CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – Texas Instruments, Inc.

Course Objective:

This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? Will it be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors?

Course Outline:

1. Market Drivers for WLCSPs: Handsets, Medical, Automotive, Space, Imaging Sensors, MEMS, HBLEDs
2. Key WLCSP Technologies
3. Equipment and Materials Tool Box
4. Infrastructure Service Providers
5. PCB Pitch Reduction
6. Cost, Benefits, and Drawbacks of WLPs
7. Reliability: Thermal Cycling, Drop, Flex Testing, Electromigration
8. Fan-Out WLP
9. Supply Chain
10. Embedded Die
11. Chip First vs. Chip Last
12. Single Die Embedding vs. SiP Module
13. Challenges and Evolution to Large Format Processing

Who Should Attend:

The course will be useful to the following groups of engineers: Newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and, those considering WLCSP as a potential alternative for their packaging solutions.

Bio:

Luu Nguyen is a TI Fellow at Texas Instruments, working on sensors, printed electronics, high voltage packaging, design-for-manufacturability, and wafer level packaging. He received his Ph.D. in Mechanical Engineering from MIT, and has worked at IBM Research and Philips Research. He co-edited two books on packaging, and has over 200 publications. He has over 70 patents and invention disclosures. He is a Fellow of IEEE and ASME, and a Fulbright Scholar (Finland 2002). He received two Best of Conference Awards, one Best Poster of Conference Award, and eight IMAPS and IEMT Best of Session Conference Awards. He

received the 2004 IEEE CPMT Outstanding Sustained Technical Contributions Award. Other awards also include the 2003, 2014, 2015, and 2016 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation in recognition of contributions to student mentoring, research collaboration, and technology transfer.