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## 1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

***Course Leader: Ning-Cheng Lee – Indium Corporation***

**Course Objective:**
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail, and novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whisker growth will also be discussed. Furthermore, the reliability of through-hole solder joints will be reviewed, and recommendations will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

**Course Outline:**
1. Implementation Status
2. Prevailing Materials: Alloys and Finishes
3. Surface Finishes Issues: ENIG, Immersion Ag, and Immersion Sn
4. Mechanical Properties: Shear, Pull, and Creep
5. Intermetallic Compounds: Effect of Cu, Ni, Other Additives, and Heat History
6. Failure Modes: Grain Deterioration, Orientation, Mixed Alloys, and Interfacial Voiding
7. Thermal Cycle Reliability: Effect of Cycling Condition, Surface Finishes, and Reflow Temperature
8. Reliability of Through-Hole Joints: Large and Thick Boards, Partially Filled Through-hole
9. Fragility: Effect of Surface Finishes, Alloys, Reflow, Strain Rate, Aging, Cycling, and IMC
10. Electromigration: Effect of Current Density, Back Stress, and Cu UBM Thickness
11. Corrosion: SAC and Performance of Surface Finishes Under Harsh Conditions
12. Tin Whisker: Causes of Formation, Methods for Control

**Who Should Attend:**
Anyone interested in achieving high reliability lead-free solder joints and wants to know how to achieve it should take this course.

## 2. WAFER LEVEL-CHIP SCALE PACKAGING

***Course Leader: Luu Nguyen – Texas Instruments, Inc.***

**Course Objective:**

This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? Will it be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors?

**Course Outline:**

1. Market Drivers for WLCSPs: Handsets, Medical, Automotive, Space, Imaging Sensors, MEMS, HBLEDs
2. Key WLCSP Technologies
3. Equipment and Materials Tool Box
4. Infrastructure Service Providers
5. PCB Pitch Reduction
6. Cost, Benefits, and Drawbacks of WLPs
7. Reliability: Thermal Cycling, Drop, Flex Testing, Electromigration
8. Fan-Out WLP
9. Supply Chain
10. Embedded Die
11. Chip First vs. Chip Last
12. Single Die Embedding vs. SiP Module
13. Challenges and Evolution to Large Format Processing

**Who Should Attend:**

The course will be useful to the following groups of engineers: Newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and, those considering WLCSP as a potential alternative for their packaging solutions.

## 3. LED PACKAGING, SYSTEM, AND RELIABILITY CONSIDERATIONS

***Course Leader: Xuejun Fan – Lamar University***

**Course Objective:**

Light emitting diode (LED) has now emerged as promising technology to replace conventional lighting, such as incandescent bulbs and compact fluorescent lamps, due to its superior energy efficiency, environmental friendliness, and particularly long lifetime (in the range of 25,000 – 100,000 hours). This course will present a comprehensive overview of recent advances in LED packaging, system integration, and reliability issues. Unlike traditional IC failure that is mainly characterized by catastrophic mode, LEDs' performance is characterized by a dual-degradation

mode: light output (lumen maintenance) degradation and color shift. Packaging structure, system integration, and materials play a very important role in LED efficacy and reliability. This course will cover the topics below:

**Course Outline:**

1. LED Introduction
2. LED Basics
3. LED Packaging and System Integration
4. Basics of LEDs' Photometry and Colorimetry
    - LED Packaging Evolution
    - LED Packaging Materials: Chip, Phosphor, Silicone, Reflector, Substrate, and System Integration
5. LED Packaging Materials and Degradation
6. LED Failure Mechanisms
7. LED Testing Standards and Specifications
8. Accelerated Testing and Lifetime Prediction
9. LED Driver and LED Driver Reliability
10. Thermal Management
11. Multi-Physics Modeling
12. Physics of Failure (PoF) Based Health Monitoring
13. System Reliability and Prediction
14. Conclusions

**Who Should Attend:**
The course is designed for staff members, technical managers, LED system reliability, design and manufacturing personnel, reliability engineers, and students who are interested in LED packaging, material selection, and LED reliability. The course does not assume prior knowledge in LED areas.

## 4. FUTURE OF DEVICE AND SYSTEMS PACKAGING: STRATEGIC TECHNOLOGIES, MFG. INFRASTRUCTURE, AND APPLICATIONS

***Course Leader: Rao Tummala – Georgia Institute of Technology***

**Course Objective:**
Semiconductor and systems landscape is changing dramatically. ICs, on one hand, for the most part, are becoming commodities, providing much lower profit margins than ever before, leading to industry consolidation to less than ten manufacturing companies within the next decade, worldwide. In addition, the cost and complexity of transistor scaling is growing exponentially. There is no longer a cost reduction as the next node is introduced with higher transistor density. In addition, IC performance is being greatly impacted by interconnect delay and leakage.

The driving engines for electronic systems, on the other hand, are also changing dramatically to smart, wearable, wireless healthcare, wireless networks and new era of self-driving and electric cars, requiring an entirely different vision and strategy than transistor scaling alone that has been and continued to be practiced during the last 60 years. These systems are small to ultra-small systems and yet must perform dozens of functions that include high-speed digital, high-efficiency power, 5G and millimeter wave, MEMS and sensors. The new era of automotive electronics, in addition, requires a variety of sensing technologies for self-driving cars such as camera, LiDAR and radar, and ultra-high power for electric cars.  All these emerging or next

generation computing, communications, consumer and automotive systems pose device, packaging and integration barriers.

They require new role for packaging. Future Packaging must address these devices and systems' barriers by enabling better and cheaper devices and highly-integrated and ultra-miniaturized systems. The advances need to be more than Moore's (MTM) Law with on-chip transistor integration with 2D and 2.5D MCM, 3D stacked ICs with TSV and SIP. They require a new paradigm in systems packaging, referred to as "System Moore's" Law (SM) for complete systems. Such a concept requires new system package architecture beyond SIP, 2.5D and 3D with TSV.

The course will review the current approach to devices, device packaging and system packaging. These include traditional single and multi-chip packaging as well as the recent focus in embedded and fan-out packaging. This course describes IC and system packaging challenges and potential solutions that lie ahead in strategic technologies, manufacturing infrastructures and applications.

**Course Outline:**

1. Emerging Electronic Systems
2. Current Approach to Devices and Device Packaging
3. Strategic Packaging Technologies to Enable Future Devices
    - Integration of Homogeneous and Heterogeneous Devices in 2D, 2.5D, and 3D Multi-Chip Packaging which Requires I/O Scaling Similar to BEOL.
4. Strategic Systems Packaging Technologies to Enable Future Systems
    - Envisioned is a System Scaling Concept that includes Devices by Transistor Scaling but Goes Beyond to include Components and Interconnections.
5. Current vs. Future Packaging Manufacturing Infrastructure
    - Current: Limited to Wafer-Based with BEOL Tools or Panel-Based Tools with Low I/O Density
    - Future: Panel-Based BEOL-Like Packaging
6. Emerging and High-Growth Applications
7. Applications of Future Packaging to Emerging Systems

**Who Should Attend:**

Senior marketing and R&D executives as well as senior managers who are dealing with strategic issues facing the electronics industry should attend.

## 5. POLYMERS AND NANOCOMPOSITES FOR ELECTRONIC AND PHOTONIC PACKAGING

***Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu –Henkel Corporation***

**Course Objective:**

Polymers and nanocomposites are widely used in electronic and photonic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance novel no flow underfills, reworkable underfills for ball grid array (BGA), chip scale packaging (CSP), system in a package (SIP), direct chip attach (DCA), flip-chip (FC),

paper-thin IC and 3D packaging, conductive adhesives (both ICA and ACA), embedded passives (high K polymer composites), nano particles and nanofunctional materials such as CNTs (some with graphenes). It is imperative that both material suppliers, formulators and their users have a thorough understanding of polymeric materials and the recent advances on nano materials and their importance in the advances of the electronic packaging and interconnect technologies.

**Course Outline:**

1. Fundamental of Polymers and Materials Science and Engineering
2. Material Needs for Next Generation Electronic Packaging
3. Novel Nanocomposites for Flip-Chip Underfill Applications
4. Recent Advances on Nano Lead-Free Alloys for High Performance Components Interconnects
5. Low-Cost High Performance Lead-Free Interconnect Materials and Processes
6. Recent Advances on CNTs as Thermal Interface Materials (TIMs)
7. Lotus Effect Coating for Self-Cleaning Applications
8. Fundamentals of Electrically Conductive Adhesives (ECAs)
9. Recent Advances on Conductive Adhesives
10. Recent Advances on Nano Conductive Adhesives

**Who Should Attend:**
Engineers, scientists and managers involved in designing, processing and manufacturing of microelectronic and optoelectronic components and packages, material suppliers, and students and researchers on electronic packaging should attend.

## 6. INTEGRATED THERMAL PACKAGING AND RELIABILITY OF POWER ELECTRONICS

***Course Leaders: Patrick McCuskey and Avi Bar-Cohen – University of Maryland***

**Course Objective**:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics. Following a quick review of active heat transfer techniques, along with prognostic health management approaches to assess and ensure reliability, this short course will present the latest developments in the materials (e.g. organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems along with modeling and testing techniques. Thermal isolation, glass substrates, heterogeneous integration, and non-traditional module structures will be included. This course will emphasize thermal packaging techniques capable of addressing performance limits and reliability concerns associated with increased power levels and power density in power electronic components.

**Course Outline:**

1. Introduction to Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques: Air, Single Phase Liquid, Two Phase, Phase Change Materials, Thermal Interface Materials

3. Application of Thermal Management Techniques to Commercial Power Systems/Data Centers including Embedded Cooling
4. Durability Assessment: Failure Modeling, Simulation, Testing, Prognostics and Health Monitoring
5. Reliability and Thermal Packaging of Active Devices: Si, SiC, and GaN and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, including Organic Encapsulates
7. Reliability in Rigid Assembly Packaging: PCB, Solders, and Glass Interposers
8. Flexible Materials, Packaging, and Thermal Management: Flex Circuit, OLED, Wearables
9. Reliability of 3D Power Packaging including Additive Manufacturing
10. MEMS and Sensor Packaging

**Who Should Attend:**
This course is intended for Power Electronic Systems designers and managers who would like to add heat transfer, manufacturability and reliability criteria to their designs for longer life products with improved performance. In addition, it would be useful to thermal, mechanical, and materials engineers active in the power electronic communities who want to see the latest research developments.

## 7. FUNDAMENTALS OF ELECTRICAL DESIGN AND FABRICATION PROCESSES OF INTERPOSERS, INCLUDING THEIR RDLs

***Course Leaders: Ivan Ndip and Michael TÖpper – Fraunhofer IZM***

**Course Objective:**
As a result of their myriad of advantages in system-integration, glass and silicon interposers will continue to play a crucial role in the development of future electronic systems. The fabrication processes and electrical performance of these interposers, including their re-distribution layers (RDLs), will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and electrical design of glass and silicon interposers, including their RDLs. An overview of advanced packaging technologies and the role of interposers will first be given. This will be followed by a thorough discussion of silicon interposers, Through-silicon via (TSV) generation process and tools, as well as glass interposers and options for though-glass vias (TGV) generation and metallization. Major challenges of RDL build-up on thin interposer substrates will be presented and advanced RDL materials and technologies to realize routing down to 3 µm in interposers will be discussed. The fundamentals of efficient electrical design of interposers and RDLs up to millimeter-wave frequencies will be given. Finally, the RF performance of transmission lines and vias in these interposers will be compared. Examples of interposers designed and fabricated at Fraunhofer IZM will also be discussed.

**Course Outline:**
1. Introduction to Advanced Packaging Technologies and the Role of Interposers
2. Silicon Interposers: Illustration of TSV Generation Process and Tools
3. Glass Interposers: Illustration of Technology Options for TGV Generation and Metallization
4. Presentation of Thin Substrate Handling and Temporary Bonding
5. Comparison between Glass, Silicon and Organic-Based Interposers
6. Illustration of RDL Generation and their Role in CSP and FO-WLP
7. Discussion of Major Challenges of RDL Build-Up on Thin Interposer Substrates

8. Advanced RDL Materials/Technologies to Realize Routing Down to 3 µm in Interposers
9. Electrical Design Challenges of Interposers and RDLs: Signal/Power Integrity and EMI Issues
10. New Design Approach for Applications up to Millimeter-Wave Frequencies
11. Explanation of Fundamental Electrical Design Concepts: Impedance, RLCG Parasitics, S-Parameters
12. Electrical Design, Measurement and Comparison of Transmission Lines on RDLs and Interposers
13. Electrical Design, Measurement and Comparison of TSVs and TGVs
14. Examples of Interposers Designed, Fabricated and Characterized at Fraunhofer IZM

**Who Should Attend:**
Engineers, researchers, designers, technical managers and graduate students involved in the process of electrical design, layout, processing, fabrication and/or system-integration of interposers and electronic packages.

## 8. INTRODUCTION TO MECHANICS BASED QUALITY AND RELIABILITY ASSESSMENT METHODOLOGY

***Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation***

**Course Objective:**
This course presents a unique integrated methodology that combines two essential domains, engineering mechanics and reliability statistics, to perform standards based or knowledge-based risk assessment to meet the dynamic market demand for electronic devices. To ensure that corporate Q&R goals are met, it is vital to have a comprehensive understanding of device usage and complete characterization of physics of failure. This course discusses key elements of Q&R like Use Conditions (UC), accelerated life tests, statistical data analysis methods, acceleration factor models, DPM risk assessment at UC, FA tools/techniques, design for reliability and experiment planning. In addition, it provides an overview of the fundamental concepts of solid mechanics such as stress-strain curves, characterization of material behavior, stress analysis methods including FEA with specific application to packaging, material characterization metrologies and FEA model validation techniques. The course offers a deeper dive into a few key mechanisms such as Si-package interactions, SJR, die cracking, etc. to highlight successful application of this integrated methodology. They highlight benefits of driving proactive product risk assessment at UC and optimizing product design/process/ materials for manufacturability/quality/reliability. The course will explore the application of this integrated methodology in traditional and new markets like wearables and Internet of Things. Students will perform multiple hands-on exercises throughout the duration of the course to reinforce the fundamental concepts and the value of integrated methodology.

**Course Outline:**
1. Packaging Technology: Trends and Challenges
2. Introduction to Quality and Reliability
3. Overview of Key Components of Reliability Statistics and Accelerated Testing
4. Hands-On Class Exercise 1
5. Introduction to Solid Mechanics
6. Key Components of Solid Mechanics: Stress/Strain Curves, Failure Theories, Finite Element Analysis
7. Material Characterization Metrologies and Analysis Validation Techniques
8. Key Failure Mechanisms and Failure Analysis Tools/Techniques.
9. Overlapping Areas between Reliability and Mechanics

10. Overview of the Unified Reliability Assessment Methodology Using Mechanics
11. Application of Methodology to Key Organic Package Failures
12. Hands-On Class Exercise 2
13. Summary of Key Learning Elements

**Who Should Attend:**
Packaging engineers involved in design, development, production, and reliability testing of semiconductor packages would benefit from the course.

## 9. THERMO-ELECTRIC COOLERS: CHARACTERIZATION, RELIABILITY, AND MODELING

***Course Leader: Jaime Sanchez – Intel Corporation***

**Course Objective:**
Thermo-electric coolers are devices widely used in the semiconductor industry as the main thermal engines for thermal control during test of integrated circuit devices. They offer the ability to both heat and cool a device under test to mimic worst case platform conditions and defect screening at different temperatures. In this short course, we will review fundamental characterization techniques of thermoelectric coolers that allow the direct measurement of relevant properties such as the effective Seebeck coefficient, electrical resistivity, and thermal impedance. A detailed numerical modeling approach will be discussed that utilizes user-defined functions in Fluent that allows a close representation of these devices matching experimental conditions. Experimentation and numerical analysis techniques will be discussed that enable the full characterization of a thermal solution based on thermoelectric coolers both in steady and transient state. A comprehensive overview of modeling and experimentation techniques will be provided that capture the dynamic behavior of a thermal solution connected to a closed loop control algorithm: the impact of various approaches of controlling the junction temperature of a device under test under different conditions, as well as the sensitivity of the dynamic response of the full system including the effect of active power management of the device under test. Finally, experimental techniques based on reliability statistics will be covered that have a direct application into predicting the life of a thermo-electric cooler under various test conditions.

**Course Outline:**

1. Introduction
   - State-of-the-Art in Thermo-Electricity Research
   - What is Thermo-Electricity
   - General Industrial Applications
2. TEC Modules Governing Principles
   - Single Peltier Couple to a TEC Module
   - Governing Equations and Relationships
   - Example of TEC Module Selection Based on a Static Cooling Application
3. TEC Module Characterization and Modeling
   - Experimental Setups and Methodology
   - Overview of Analytical Approaches
   - Overview of Transient Characterization
4. Operation of TEC Modules in Dynamic Closed Loop Control
   - Applications to Test ICs
5. Reliability of TECs
   - Overview of Failure Modes
   - Improvements for Test Application

6. Summary and Future Directions
7. References

**Who Should Attend?**

This course is intended for students and engineers in the electronics cooling industry specifically, but should be of interest for those working with thermo-electric modules in general. The class will cover experimental and numerical methods.

## 10. FLIP CHIP TECHNOLOGIES

***Course Leaders: Eric Perfecto – GLOBALFOUNDRIES; Shengmin Wen – Synaptics Inc.***

**Course Objective:**

This course will cover the fundamentals of flip-chip assembly process that involves wafer bumping, solder joint formation, substrate and/or redistribution selection, and underfill processes. All aspects of bumping technologies, including lead-free solder bumping and highly customized Cu Pillar technologies used in today's flip-chip are addressed in depth, including the details and comparison of various UBM (electroplating, electroless plating and sputtering) and solder (electroplating, ball drop, IMS, and solder screening) depositions methods. Solder joint formation technologies used in single and multi-die assembly of chip scale packages, wafer-level packages, chip-on-chip, chip-on-wafer, and 2.5D/3D flip chip packages are discussed and demonstrated through industrial's leading application examples. The course provides a list of items to consider when choosing a particular flip-chip assembly process for a specific application such that a reliably and cost effective solution can be planned out of various methods to bump the wafer and different substrates types (organic laminate, ceramic, and Si substrates). Chip package interaction (CPI), package warpage control, and yield detractors for flip-chip assembly are discussed in detail. Advanced and current trend of flip-chip assembly processes are provided briefly. This course will cover the reliability tests commonly used to qualify the flip-chip assembled packages, the failure types and the analytical tools used to identify defect root cause. A substantial portion of this course will cover Cu Pillar flip-chip technologies. Failure modes, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc. will be included dispersedly in the related subjects of the whole course. The students are encouraged to bring topics and technical issues from their past, present and future job function for group discussions. A 20 minute group exercise at the end of the class is planned to make sure the students can walk away with the course knowledge that applies to their daily job function.

**Course Outline:**

1. Introduction to Flip-Chip Technologies
2. UBM Metal Selection
3. Flip-Chip Solder Deposition Processes
4. Cu Pillar Bumping
5. C4 and Cu Pillar Fabrication Issues
6. Electromigration
5. Flip-Chip Plastic Ball Grid Array (FCPBGA) Assembly Process Flow
6. Cu Pillar Assembly: Mass Reflow and Thermal Compression

7. Flip-Chip Ball Grid Array (FCBGA) Assembly Process Flow
8. Cu Pillar Assembly: Mass Reflow and Thermal Compression
9. Flip-Chip Technology New Trends: Wafer Level, Panel Level and u-BGA
10. Flip-Chip Si Package Co-Design and Chip-Package Interaction
11. Substrate Technologies, Underfill, Package Warpage Control, and Yield
12. Flip-Chip Reliability Assessment, Failure Modes, Examples, and Modeling

**Who Should Attend**:
The targeted audience includes scientists, engineers, and managers currently using flip-chip (with solder or Cu pillar) or those considering moving from wire bonding to flip-chip, as well as reliability, product or applications' engineers who need a deeper understanding of flip-chip technologies: the advantages, limitations and failure mechanisms.

## 11. PACKAGE FAILURE ANALYSIS - FAILURE MECHANISMS AND ANALYTICAL TOOLS

***Course Leaders: Rajen Dias – Amkor Technology and Deepak Goyal – Intel Corporation***

**Course Objective:**
The technical course will provide an overview of the failure modes and mechanisms observed in organic semiconductor packages. A brief introduction to the methodology of failure analysis for these packages will be described. The focus of the course will be on package failure mechanisms highlighted by case studies, analytical tools and techniques currently used, and the future direction for analytical tools and techniques required for successful and timely failure analysis of next generation package technologies. A discussion on the strategies for using these techniques and a flow chart for failure analysis will be included.

**Course Outline:**
1. Package Technology: Trends, Drivers and Challenges
2. Failure Analysis Challenges Offered by Package Technology Roadmaps
3. Introduction to the Methodology of Failure Analysis of Packages
4. Current Analytical Capabilities for Package Fault Isolation and Failure Analysis
5. Strategies to Use these Techniques to Identify Failures and Understand Failure Mechanisms
6. Analytical Capabilities to Support Next-Generation Packaging Technologies
7. Typical Failure Analysis Flow Charts for Opens and Shorts
8. Failure Modes/Mechanisms including Chip/Package Interactions, 1st/2nd Level Interconnections and Package/Board Substrates
9. Failure Analysis Case Studies: Flip-Chip, Wire Bond, 3D Stacked Die, WLFO and MEMS Package Technologies

**Who Should Attend:**
Engineers and technical managers who are involved in package technology development, reliability assessment of packages and failure analysis should attend.

## 12. 3D IC INTEGRATION AND 3D IC PACKAGING

***Course Leader: John Lau – ASM Pacific Technology Ltd.***

**Course Objective:**
Recent advances in, e.g., fan-out wafer/panel level packaging (TSMC's InFO-WLP and Fraunhofer IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights

Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration, 3D CIS/IC integration, and 3D MEMS/IC integration will be discussed in this presentation. Emphasis is placed on various FO-WLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FO-WLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor, SPIL/Xilinx, ASE, MediaTek, Intel, ITRI, Shinko, Cisco/eSilicon, Sony's TSV-less CIS, and Samsung/Hynix (HBM3) will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

**Course Outline:**

1. FOW/PLP: Chip-First (Die-Up/Down), Chip-Last (RDL-First)
2. RDL Fabrications: Polymer, PCB/LDI, Cu Damascene Methods
3. InFO-WLP, TSMC InFO-PoP vs. Samsung ePoP
4. Dielectric and Epoxy Mold Compound
5. Semiconductor and Packaging for IoTs (SiP)
6. Wafer vs. Panel Carriers, WLSiP and PLSiP
7. TSV formation
8. Memory Chip Stacking with TSV: Samsung's DDR4
9. Hybrid Memory Cube (HMC) with TSV: Intel's Knights Landing with Micron's HMC
10. High Bandwidth Memory (HBM) with TSV: AMD/Nvidia's GPU, Hynix/Samsung's HBM
11. Memory + Logic with TSV: Samsung's Widcon
12. 3D IC/MEMS Integration and 3D IC/CIS Integration
13. Embedded 3D Hybrid Integration
14. 2.5D IC Integration: TSMC/Xilinx's CoWoS (Chip-on-Wafer-on-Substrate)
15. TSV-Less Interposer: Xilinx/SPIL's SLIT, Amkor's SLIM, ASE's FOCoS, Intel's EMIB, ITRI's TSH, Shinko's i-THOP, Cisco's Organic Interposer, Sony's CIS, SPIL/Xilinx's NTI, Samsung's Organic Interposer, etc.
16. Semiconductor Packaging New Trends

**Who Should Attend:**

If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will received more than 200 pages of handout materials from the lecturer's books and the papers published by others.

## 13. FLEXIBLE HYBRID TECHNOLOGIES

***Course Leader: Pradeep Lall – Auburn University***

**Course Description:**

In this course, manufacture, design, assembly, and accelerated testing of flexible hybrid electronics for applications in some of the emerging areas will be covered. Flexible hybrid electronics opens the possibilities for the development of stretchable, bendable, foldable form-factors in electronics applications which have not been possible with the use of rigid electronics technologies. Flexible electronics may be subjected to strain magnitudes in the neighborhood of 50-150 percent during normal operation. The integration processes and semiconductor packaging architectures for flexible hybrid electronics may differ immensely in comparison with those used for rigid electronics. The manufacture of thin electronic architectures requires the integration of thin-chips, flexible encapsulation, compliant interconnects, and stretchable inks for metallization traces. A number of additive manufacturing processes for the fabrication and assembly of flexible hybrid electronics have become tractable. Processes for handling, pick-

and-place operations of thin silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes for development of robust process parameters which will allow for acceptable levels of yields in high-volume manufacture. Modeling of operational stresses in flexible electronics requires the material behavior under loads including constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear and abrasion. The strains imposed on flexible stretchable electronics may far exceed those experienced in rigid electronics requiring the consideration of finite-strain formulation in development of predictive models. The failure mechanisms, failure modes, acceleration factors in flexible electronics under operational loads of stretch, bend, fold and loads resulting from human body proximity are significantly different than rigid electronics. The testing, qualification and quality assurance protocols to meaningfully inform manufacturing processes and ensure reliability and survivability under exposure to sustained harsh environmental operating conditions, may differ in flexible electronics as well. A number of product areas for the application of flexible electronics are tractable in the near-term including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring and automotive electronics.

**Course Outline:**

1. Ultra-Thin Chips
2. Die-Attach Materials for Flexible Semiconductor Packaging
3. Compliant Interconnects
4. Flexible Encapsulation Materials
5. Inkjet and Aerosol-Jet Printing Processes
6. Dielectric Materials for Large-Area Flexible Electronics
7. Flexible Substrates
8. Stretchable Inks for Printed Traces
9. Pick-and-Place and Material Handling Processes
10. Additive Technologies in Flexible Electronics
11. Reflow and Printing Processes
12. Accelerated Testing Protocols

**Who Should Attend:**

The course is intended to introduce the attendees to the general area of flexible hybrid electronics.

## 14. POLYMERS FOR ELECTRONIC PACKAGING

***Course Leader: Jeffrey Gotro –InnoCentrix, LLC***

**Course Objective:**

The course will provide a broad overview of polymers used in semiconductor packaging and the important structure-property-process-performance relationships. We will cover in more depth the chemistries, material properties, and process considerations for adhesives, underfills, coatings and mold compounds. Additionally, we will provide an introduction to common thermal analysis methods (DSC, DMA, TMA, and TGA) used to characterize thermosetting polymers used in semiconductor packaging. Finally, the course will provide an introduction to the rheological performance of polymer-based materials used in packaging semiconductors. In most cases, adhesives, underfills, mold compounds and coatings are applied as a viscous liquid and then cured. The flow properties of these materials are critical to performance in high volume manufacturing. The course will provide an introduction to rheology measurements and examples of rheology issues in semiconductor packaging.

**Course Outline:**

1. Thermosetting Polymers Versus Thermoplastics
2. Temperature Dependence of Physical Properties
3. Themosetting Polymers: Curing, Curing mechanisms, Network Formation
4. Overview of Key Chemistries Used: Epoxies, Acrylates, Polyimides, Bismaleimides
5. Chemistry of Die Attach Adhesives: Paste, Film and Wafer Applied
6. Chemistry and Physics of Capillary Underfills, Pre-Applied Underfills, Wafer Level Underfills,
7. Polymers used in Wafer Level Packaging, ewLP, and Other Fan-Out Packages
8. Packaging Substrate Materials and Process
9. Encapsulants (Mold Compounds) and Coatings
10. Introduction to Rheological Characterization Methods: Types of Rheometers and Basic Techniques
11. Introduction to the Rheological Properties of Adhesives
12. Key Rheology Properties: Shear Thinning, Viscosity, Rheology Changes during Curing

**Who Should Attend:**
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

## 15. EMERGING INTERCONNECT AND SYSTEM INTEGRATION TECHNOLOGIES

***Course Leader: Muhannad Bakir – Georgia Institute of Technology***

**Course Objective:**
Interconnects have emerged as a critical bottleneck to the realization of lower-power and higher-performance electronics. Coupled with this, the need for ever more tightly integrated systems present unique cooling and power delivery challenges for next-generation electronics. This short course will present an overview of emerging technologies to address these need areas and present key modeling results to help guide technology development. The modeling effort presented in the short course will not only help us understand the design considerations of the technologies discussed but will also help benchmark the performance of the various technologies so that optimal systems can be developed.

**Course Outline:**

1. Advances in 2.5D Chip Integration, including Silicon-Bridge Based Approaches
2. 3D Integration Approaches, including Monolithic 3D ICs
3. Photonic Interposer and Package Technologies, including the Modeling of Diffractive Grating Couplers and the Impact of Misalignment
4. Thermal and Power Delivery (Power Supply Noise) Physical Modeling and Learning
5. Advanced Cooling and Thermal Decoupling Technologies in Multi-Die Interconnected Systems, including Microfluidic Cooling
6. Mechanically Flexible Interconnects in Assembly of High-I/O Density Chips
7. Example Bioelectronic Systems Enabled by Advanced Interconnection and Packaging

**Who Should Attend:**
This short course will be of value to those working in the areas of interconnects, packaging, 3D technology, and heterogeneous integration.

## 16. PACKAGE FAILURE MECHANISMS, RELIABILITY, AND SOLUTIONS

***Course Leader: Darvin Edwards –Edwards Enterprises***

**Course Objective:**

This course explores past and present reliability failure modes and mechanisms that plague semiconductor packages. Primary reliability challenges in TSV and FOWLP packaging, as well as major failure mechanisms for FC-BGA, WLCSP, plastic leaded, no lead, and selected MEMS package types will be described. The class will cover reliability concerns such as TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and wire bonds, Cu vs. Au wire bond reliability challenges, problems associated with delamination in packages, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mechanism, the failure modes and failure analysis techniques needed to verify the mechanisms will be summarized. Recommended failure analysis fault isolation techniques will be described. This solutions focused course concentrates on process parameters, design techniques and material selections that eliminate the failures and improve reliability to ensure participants can design in reliability and design out failures. The development and characterization of design guidelines that enable reliable products will be described and encouraged. A test structure methodology combined with qualification by similarity will be highlighted as a process for early detection of chip/package reliability risks.

**Course Outline:**

1. Introduction and Description of IC Package Types
2. Failure Analysis Techniques and Fault Isolation Flow
3. Package Failure Mechanisms: FC-BGAs
4. Package Failure Mechanisms: Molded and Leaded Packages
5. Package Failure Mechanisms: WLCSPs
6. Package Failure Mechanisms: Embedded Die/Fan-Out WLPs
7. Package Failure Mechanisms: TSVs
8. Package Failure Mechanisms: MEMS
9. Materials, Modeling, Design Rules and Reliability
10. Common Test Structures for Failure Mechanism Identification
11. Qualification By Similarity (QBS)
12. Summary

**Who Should Attend:**

This class is intended for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms will prove useful. Both beginning engineers and those skilled in the art will benefit from the holistic description of the failure mechanisms and proven solutions.

## 17. AGEING OF POLYMERS AND THE INFLUENCE ON MICROELECTRONIC PACKAGE RELIABILITY

***Course Leaders: Tanja Braun and Ole Hölck – Fraunhofer IZM***

**Course Objective:**

Many electronic products used in different applications, such as automotive, medical, and some consumer are exposed to extreme loading profiles. High temperatures, random vibrations or humid and or wet environments affect system and materials. Lifetime demands of 10 years and above in combination with these challenging environments requires well known materials and broad knowledge on their behavior over the entire lifetime. Polymers are widely used in

microelectronics packaging e.g. as interconnect material, encapsulant or substrate. But polymers age with time, temperature and humidity. Ageing entails a change in properties including mechanical, thermo-mechanical or adhesion characteristics, all of which are key factors for reliable package solutions. Hence, knowledge on materials and their ageing behavior is essential for developing reliable microelectronics packages and systems.

**Course Outline:**

1. Introduction of Polymers used in Microelectronics
2. Important Aspects of Encapsulation Technologies for Reliable Packaging
3. Ageing Mechanisms of Polymers
4. Adhesion and Interface Degradation
5. Test Methods and Selection Criteria for Polymers in Microelectronics Packaging
6. Overview of State-of-the-Art Measurement Equipment
7. Moisture and Temperature Induced Changes in Material Properties
8. Lifetime Simulation by FEM taking Polymer Degradation into Account
9. Failure Mechanisms Related to Polymer Ageing

**Who Should Attend:**

The course is targeted for engineers and engineer management in the field of microelectronic package design, development and reliability engineering. The attendees will learn about material selection, polymer ageing and the related influence on package reliability and will gain knowledge on how to build high reliable packages.

## 18. THERMO-ELECTRICAL CO-DESIGN FOR 3D INTEGRATION

***Course Leaders: Ankur Srivastava - University of Maryland, Avram Bar-Cohen - Raytheon***

**Course Objective:**

3D integration of computational and RF components – in both homogeneous and heterogeneous combinations - provides significant improvements in functional efficiency, device density, and interconnect delays but is expected to lead to higher heat densities, along with decreased thermal management access to individual chips and on-chip hotspots. To fully achieve the inherent advantages of 3D integration it will, thus, be necessary to implement “embedded cooling” approaches and unify the thermal, mechanical, and electrical design of chip stacks and other integrated packaging configurations. Thermo-electrical co-design for 3D integration is the theme of this CPMT Professional Development Course

The PDC will begin with a brief review of 3D and 2.5D packaging form factors and the expected areal and volumetric heat extraction rates. It will be shown that conventional “remote cooling” techniques are incapable of meeting these thermal requirements, necessitating the use of “embedded cooling” solutions, including on-chip thermal vias, micro-fluidics, and thermoelectrics. Attention will then turn to creating an integrated co-design environment that will enable designers to perform the electrical-thermal-mechanical trade-offs needed to create computational and RF modules that achieve the highest functional throughput and efficiency. The PDC will close with presentation and discussion of several co-design case studies which demonstrate the added value of an integrated co-design environment. Co-Design for two distinct and significant integrated systems will be discussed: high performance computational modules and integrated Power Amplifier MMICs **.** For the computational modules we will discuss how greater performance and energy efficiency can be extracted by exploiting the unique interplay between power, performance and reliability for CPUs, ASICs and FPGA. For Power Amplifier MMICs we will discuss co-design techniques for generating greater Gain, Power-Added Efficiency, and output power thru the application of embedded cooling technologies.

**Course Outline:**
1. 3D/2.5D Packaging Trends
2. Embedded Cooling State-of-the-Art
3. Electronic Design Automation
4. Integrated Co-Design Environment
5. Thermo-Electrical Co-Design Case Studies: Computation
6. Thermo-Electrical Co-Design Case Studiers: MMICs
7. Review and Lessons Learned

**Who Should Attend:**
The growing use of integrated co-design environments is blurring the line between IC designers and packaging engineers and creating a new class of EDA practitioners. This course will provide an introduction to this emerging EDA domain. The course is tailored to both IC designers and Packaging engineers seeking to better understand the interplay between electrical and thermo-mechanical aspects of component design and how to best manage the trade-offs needed to achieve the highest functional throughput and efficiency in computational and RF components.