

# First Call for Papers

## IEEE 69th Electronic Components and Technology Conference

[www.ectc.net](http://www.ectc.net)

To be held May 28 - May 31, 2019

at The Cosmopolitan of Las Vegas, Las Vegas, NV, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical program subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

### Advanced Packaging

Fan-out, wafer & panel level processes; 2.5 & 3D, TSV & interposer; Heterogeneous integration; Embedded & advanced substrates; Advanced flip-chip, SiP, CSP, PoP, MEMS, sensors & IoT; Automotive & power electronics; Bio, medical, flexible, wearable.

### Applied Reliability

Reliability of TSV, 2.5D, 3D, fan-out, WLCS, WLFO, PLFO, SiP & MCM; Interconnect reliability in flip chip, wire bond and BGA; Product reliability including LED, IoT and automotive; Reliability/life test methods & models; Failure analysis techniques & materials characterization; Drop/dynamic mechanical reliability; System level reliability; Automotive & harsh environment reliability.

### Assembly and Manufacturing Technology

Embedded/hybrid package manufacturing; Wearable/IoT package assembly; Healthcare/fitness component assembly; Warpage management in board level assembly; Thin die/mold/package handling and assembly; Large package (SiP, SIM, MCP) integration and processing; Panel level manufacturing for fan-in, fan-out; Dicing and singulation technology.

### Emerging Technologies

Wearable and implantable medical electronics including sensors/actuators, flexible, stretchable, disposable, dissolvable, self-healing packaging; Emerging MEMS & NEMS; 3D printing, self-alignment, emerging assembly, lab-on-chip & novel additive technologies; Packaging for autonomous sensors, photovoltaic, and heterogeneous integration; Security, anti-counterfeiting & smart electronics.

### High-Speed, Wireless & Components

Electrical modeling, analysis, design, integration, and characterization of novel electronic packages, interconnects, components, modules, and systems; High-speed or wireless applications from digital to analog to RF, low to high power, DC to THz, nano to microscales and beyond; Corresponding simulation and measurement methods.

### Interconnections

Interconnections for fan-out & fan-in wafers & panels; Interconnects and TSV for 2.5D/3D, SiP, Si/glass/organic interposers, PoP & WLP; Flip chip, solder bumping, Cu pillar & thermocompression bonding

technology; IMC interfaces, wirebonds & conductive adhesives; Interconnects for bio-medical, automotive, datacenters, cloud, network and harsh environments.

### Materials & Processing

Wafer & panel level packaging materials; Materials for harsh environments; Packaging substrates; Flexible, stretchable, bendable & wearable electronics; Battery materials; Wafer bond/debond materials; TSV; Emerging electronic materials & processes; Novel conductive and non-conductive adhesives; Solder metallurgy; Dielectrics and under-fill; Molding compounds; Thermal interface materials; Optoelectronic materials; Advanced wirebonding.

### Thermal/Mechanical Simulation & Characterization

Component, board & system level modeling for microelectronics; 3D/2.5D; TSV; Interposer; SiP; WLP; BGA; Embedded actives/passives; Power modules; LEDs; MEMS; Thin wafer/die handling; Wire bonding & assembly processes; Modeling of fracture mechanics, fatigue, electro-migration, warpage, delamination, drop test & material attributes; Novel modeling including multi-scale and multi-physics; Novel characterization methodologies.

### Optoelectronics

Wafer & panel level photonic packaging; Photonic integrated circuits; Photonic interposers; Optical interconnects; Waveguide technology; Optical printed circuit boards; Optical sensors; Silicon and III-V photonics; Micro-optical systems; Photonic SiP; 3D photonics; Novel LEDs & high power lasers; MicroLED; Visible light communication; Optoelectronic assembly, materials and reliability.

### Interactive Presentations

Highly encouraged at ECTC, presenter and attendee often communicate more efficiently here than in oral presentations. Abstracts can relate to any electronics packaging topic. Interactive presentation session papers are published and archived in equal merit with the other ECTC papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at [www.ectc.net](http://www.ectc.net).

If you have any questions, contact:

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Abstracts must be received by October 8, 2018. All abstracts must be submitted electronically at [www.ectc.net](http://www.ectc.net). You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

### Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at [www.ectc.net](http://www.ectc.net) by October 8, 2018.

If you have any questions, contact:  
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