The 2024 IEEE 74th Electronic Components and Technology Conference

May 28 – 31, 2024

2024 Conference Program & Exhibitor Listings

Gaylord Rockies Resort & Convention Center
Denver, Colorado, USA

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

For more information visit www.ECTC.net

WELCOME TO THE 74th ECTC FROM THE GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program and Executive Committee, it is our pleasure to welcome you to IEEE's 74th Electronic Components and Technology Conference (ECTC), which is held at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, from May 28 to 31, 2024.

The IEEE Electronics Packaging Society (EPS) sponsors this premier international conference annually. ECTC serves as a global gathering for all major players in the microelectronic packaging industry. This includes semiconductor and electronics manufacturers, design houses, semiconductor foundries, outsourced semiconductor assembly/testing (OSAT) service providers, substrate producers, equipment manufacturers, material suppliers, research institutions, universities, and investors. The ECTC 2023 conference was a fully in-person event that attracted over 1,600 attendees. ECTC 2024 is another exclusively in-person conference.

At the 74th ECTC, approximately 375 technical papers are scheduled to be presented by authors from many countries across 36 oral sessions and 5 interactive presentation sessions. Key topics include advancements in packaging technologies, heterogeneous integration, systems design (Sessions 1, 7), and next-generation substrate manufacturing (Session 13). Reliability aspects will cover advanced substrates, high-density packages, and harsh environment reliability (Sessions 4, 16, 29, 35). Topics in assembly and manufacturing technology include 3D integration, bonding, and die bond/board-level reliability (Sessions 10, 23, 27). Topics about RF, high speed components and systems include antenna-in-package design, signal integrity, and chiplet interconnect validation (Sessions 18, 22, 26). Emerging technologies topics include digital healthcare, AI, quantum computing, and additive manufacturing for printed electronics (Sessions 5, 11, 17). Interconnection technology sessions cover topics like die-to-wafer hybrid bonding, ultra-fine pitch technologies, and copper hybrid bonding (Sessions 2, 8, 14, 32). Materials and processing topics include advanced processes for chip stacking, hybrid bonding materials, polymer packaging innovations, and fine-pitch materials/processes (Sessions 9, 15, 21, 33). Thermal/mechanical simulation and characterization topics include reliability simulations, AI in modeling, advances in flex and redistribution layer technologies, process/hybrid bonding modeling, and thermal management solutions (Sessions 6, 12, 24, 30, 36). Photonics topics include co-packaged optics, optical interconnections, and photonics integration, materials, and processes (Sessions 3, 28, 34). Interactive presentations (Sessions 37-41) include innovations in bonding, power delivery systems, optimization algorithms, packaging for specific semiconductor devices, and reliability assessments. The 74th ECTC offers a platform for exploring cutting-edge microelectronic packaging advancements, fostering innovation, and addressing critical challenges.

The ECTC this year presents seven special sessions with industry experts, including five on Tuesday, each lasting 90 minutes. One session, chaired by Przemyslaw Gromala (Robert Bosch GmbH) and Erik Jung (Fraunhofer IZM), delves into Industry-Government Co-Investments for the Advanced Electronics Sector globally. Another, chaired by Ran Tao (NIST) and Benson Chan (Binghamton University), focuses on advancing metrology for next generation microelectronics. An afternoon session on Thermal Management for AI, chaired by Zhi Yang (Groq) and Sevket Yuruker (Tesla), explores innovative solutions for power-hungry AI/ML applications. Following that, an RF Packaging session above 100 GHz, chaired by Maciej Wojnowski (Infineon Technologies AG) and Ivan Ndip (Fraunhofer IZM/Brandenburg University of Technology), is scheduled. Additionally, a Young Professionals Networking Event on May 28, 2024, from 7:00 p.m. to 7:45 p.m., chaired by Aakrati Jain (IBM), and an IEEE EPS Seminar on Substrates for Chiplets from 7:45 p.m. to 9:15 p.m., chaired by Takashi Hisada and Yasumitsu Orii (Rapidus Corporation), are scheduled for Tuesday.

On the morning of Wednesday, May 29, 2024, ECTC's keynote presentation on "Petascale photonic chip connectivity for energy-efficient AI computing" is scheduled, presented by Prof. Keren Bergman (Columbia University) and invited by Karlheinz Bock (TU Dresden), the conference's General Chair. Additionally, a Diversity and Career Growth Panel and Reception on May 29, 2024, from 6:30 p.m. to 7:30 p.m., chaired by Cristina Amon (University of Toronto) for ITherm and Vidya Jarayam (Intel) for ECTC. A Plenary Session, styled as a start-up pitch competition on the Future of Semiconductor Industry, is planned for Thursday, May 30, 2024, from 8:00 a.m. to 9:15 a.m., chaired by Rozalia Beica (LQDX) and Farhang Yazdani (BroadPak). A panel session on Workforce Challenges in Education and Workforce Development in the New Chips Economy, organized by the IEEE EPS President, includes chairs Patrick Thompson (Texas Instruments), Mark Poliks (Binghamton University), Jeff Suhling (Auburn University), and Kitty Pearsall (Boss Precision Inc.), and is planned for Friday, May 31, from 8:00 a.m. to 9:15 a.m..

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and ECTC Exhibits. Co-located with the IEEE ITherm Conference, the 74th ECTC offers 16 CEU-approved PDCs, organized by Kitty Pearsall (Boss Precision Inc.) and Jeffrey Suhling (Auburn University). The PDCs take place on Tuesday, May 28th and are taught by distinguished experts in their respective fields.

The Exhibits at ECTC run from Wednesday May 29th to Thursday May 30th and showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred exhibiting companies are present Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We invite you to make your plans now to join us for the 74th ECTC and to be a part of all the exciting technical and professional opportunities.

We want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 74th ECTC a success. We look forward to meeting you at the Gaylord Rockies Resort & Convention Center, Denver, Colorado.

Michael Mayer
74th ECTC Program Chair
mmayer@uwaterloo.ca

Karlheinz Bock
74th ECTC General Chair
karlheinz.bock@tu-dresden.de

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, I am delighted to welcome you to the 74th Electronic Components and Technology Conference – the world's premier event for electronics packaging. Starting 74 years ago, ECTC continues to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging. Building upon the outstanding event held in 2023 and the very positive feedback from attendees and sponsors, we expect attendance at ECTC 2024 to well exceed 1,500 packaging professionals. This is a fantastic achievement. Our conference portfolio continues to find innovative ways to grow and serve our community. Together with ECTC and our Asia-Pacific flagship conference EPTC, to be held in December, EPS expects to reach similar well attended in-person conferences world-wide in 2024. These achievements would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year's exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community. May I also thank our authors, presenters, and sponsors for their contributions to this year's event. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members. In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website. Finally, may I thank you for attending this year's ECTC. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Patrick Thompson, EPS President 2024 – 2026

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Conference organizers reserve the right to cancel or change this program without prior notice.

CONFERENCE POLICIES AND GUIDELINES

Badges

Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, seminars, meals, exhibits and interactive presentation areas, and all conference sponsored social functions.

Medical Services

For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property

The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy

Please follow hotel policies and signs regarding this. Smoking is NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, seminars, meals, exhibits and interactive presentation areas, and all conference social functions. Thank you for your consideration and cooperation.

REGISTRATION AND GENERAL INFORMATION

REGISTRATION LOCATION AND HOURS

The ECTC Registration Desk is located in The Gaylord Rockies Resort & Convention Center in the Rockies Square area, behind the Convention Center Coffee Shop (lobby level).

Monday, May 27, 2024 – 3:00 p.m. - 6:00 p.m.
Tuesday, May 28, 2024 – 6:45 a.m. - 7:45 p.m.*
(From 6:45 a.m. – 8:15 a.m. registration is for morning session PDC and Special Session Attendees)*
Wednesday, May 29, 2024 – 6:45 a.m. - 4:00 p.m.
Thursday, May 30, 2024 – 7:30 a.m. - 4:00 p.m.
Friday, May 31, 2024 – 7:30 a.m. - 12:00 p.m.

On Tuesday, May 28th light morning refreshments will be provided from 6:45 a.m. – 7:30 a.m. Come pick up your registration materials EARLY and grab a bite to eat before our PDCs and Special Sessions start!

The above schedule for Tuesday will be vigorously enforced to prevent attendees from being late for their courses and sessions. Please make sure to take advantage of the 6:45 am start time as registration becomes very congested prior to the start of the morning program.

DOOR REGISTRATION FEES

Door Registration with Proceedings Download

IEEE Members

JOINT Registration (full ECTC + ITHERM conference) $1665
IEEE Member Full Registration $1265
IEEE Member Speaker / Session Chair Full Registration $1135
IEEE Member One Day $835
IEEE Member Speaker / Session Chair One Day $735

Non-Members

JOINT Registration (full ECTC + ITHERM conference) $1995
Non-Member Full Registration $1530
Non-Member Speaker / Session Chair Full Registration $1135
Non-Member One Day $835
Non-Member Speaker / Session Chair One Day $735

Student $455
Student Speaker $455

Tuesday Professional Development Courses

IEEE Members

Tuesday AM or PM Course with Luncheon $440
Tuesday All-Day (2 Courses) with Luncheon $625

Non-Members

Tuesday AM or PM Course with Luncheon $490
Tuesday All-Day (2 Courses) with Luncheon $675
Tuesday Student All-Day (2 Courses) with Luncheon $150

Extra Luncheon Tickets for Each Day $100

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS AND PROCTORS BREAKFAST

7:00 a.m. Tuesday
Room Location: Summit 10 & 11
PDC Instructors and Proctors are required to attend a briefing breakfast.

SESSION CHAIRS AND SPEAKERS BREAKFAST

7:00 a.m. Wednesday thru Friday
Room Location: Crest 3-5
Session Chairs and speakers are requested to attend a complimentary continental breakfast with briefing on the morning of their sessions/ presentations. During the breakfast, presentations are transferred to the conference PC.

SPEAKER PREP ROOM

7:00 a.m. – 5:00 p.m., Tuesday – Friday
Room Location: Valley 3
Speakers should prepare and review their digital presentations within the allotted times above.

It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.

GENERAL INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Conference Wi-Fi
Attendees can access the internet via a shared conference Wi-Fi connection included in the registration. Please note, this connection is intended for light use e.g. for the conference app or email. It is not intended for video streaming, video meetings, large file downloads, and other high bandwidth uses.

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

LUNCHEONS

Room Location: Aurora A & C
ECTC offers a daily luncheon from Tuesday to Friday for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $100 to replace. Please come and enjoy lunchtime with other attendees and colleagues in the industry!

Lunch times vary for each day:

Tuesday: 12:00 Noon – 1:15 p.m.

Wednesday: 12:45 p.m. – 1:45 p.m.

Thursday: 12:45 p.m. – 1:45 p.m.
Sponsored by: The IEEE Electronics Packaging Society

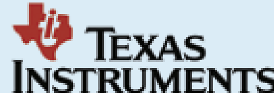
Friday: 12:45 p.m. – 1:45 p.m.
Don't miss out on this lunch! We will be raffling off several prizes including a hotel stay, free conference registrations, and many other industry gadgets!

General Chair's Speakers Reception

Tuesday, May 28, 2024 • 6:00 p.m. – 7:00 p.m.
(by invitation only)

ECTC Student Reception

Tuesday, May 28, 2024 • 5:00 p.m. – 6:00 p.m.
Location: Summit Foyer



Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

Exhibition Reception

Wednesday, May 29, 2024 • 5:30 p.m. – 6:30 p.m.
Location: Aurora 1
Open to all conference attendees.

74th ECTC Gala Reception

Thursday, May 30, 2024 • 6:30 p.m.
Location: Outside on the Front Range Lawn (Lower Level)

Sponsored by Koh Young Technologies, Inc.

Open to all conference attendees.

EPS Worldwide Chapter Officer Meeting

Please attend in person if you are an officer of EPS Chapter or EPS student Chapter.

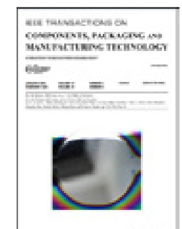
(Online by invitation)
Thursday May 30, 2024 • 7:00 a.m. – 8:00 a.m.
Room: Summit 3

Chapter Program Director: Toni Mattila
Reg 1-7 and 9: Annette Teng
Reg 8: Steffen Kroehnert
Reg 10: Andrew Tay

All EPS Worldwide Chapter Officers are invited to sit together for lunch to meet each other. Look for table with Chapter Signage.

ECTC Mobile App

ECTC is pleased to announce that a free mobile app "Whova" is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and venue maps. The app also features tools to set your schedule, so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching "Whova". After downloading the Whova app please log in using the email address you used to register for ECTC, and the ECTC content will appear automatically. Alternatively, a generic app invitation code will be made available onsite at the conference for attendees.



IEEE Transactions on Components, Packaging, and Manufacturing Technology

IEEE ELECTRONICS PACKAGING SOCIETY

If you are an author of a 74th ECTC paper, consider submitting an updated version of your conference paper after the conference as a journal manuscript to be peer reviewed by IEEE Transactions on Components, Packaging, and Manufacturing Technology. An updated version adds more significance and can include more references, discussions, or results that are still unpublished. For more details, see under "Papers Presented at Conferences" on https://eps.ieee.org/publications/ieee-transactions-on-cpmt/information-and-resources-for-authors.html

74th ECTC CONFERENCE OVERVIEW

2024 ECTC Special Session on Industry-Government Co-Investments

Exploring the Impact of Industry-Government Co-Investments for the Advanced Electronics Sector in North America, Asia and Europe

Tuesday, May 28, 2024, 8:30 a.m. – 10:00 a.m. • Aurora B

Chairs: Przemyslaw Gromala, Robert Bosch GmbH, and Erik Jung, Fraunhofer IZM

Essential to the global economy and innovation landscape, the semiconductor and microelectronics packaging industries are seeing government led investment programs. The introduction of the CHIPS and Science Act (Creating Helpful Incentives to Produce Semiconductors for America) in the United States has been inspiring similar programs, e.g. in Europe the European Chips Act. Speakers in this special session discuss programs and co-investments for the United States, Europe, India and East Asia, including job creation, supply chain resilience, and enhanced technological innovation. We will examine the prospects of global collaborations and partnerships between national semiconductor and microelectronic packaging centers and industry leaders. The session will also discuss mechanisms for knowledge exchange, joint research initiatives, and mutually beneficial outcomes.

Elisabeth Steimetz, EPoSS, Europe; Rao Tummala, Advisor to the Government of India; Eric Lin, CHIPS Research and Development Program, USA; David Lynch, CMC Microsystems, Canada; Kwang-Seong Choi, Electronics and Telecommunications Research Institute, Korea

2024 ECTC Special Session on Metrology

Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Tuesday, May 28, 2024, 10:30 a.m. – 12:00 p.m. • Aurora B

Chairs: Ran Tao, NIST, and Benson Chan, Binghamton University
Moderator: Jan Vardaman, TechSearch International

Metrology plays a pivotal role in semiconductor research and manufacturing and is critical to the success of this industry. Advancements in measurement science, material characterization, instrumentation, testing, and manufacturing capabilities are critically needed to drive product innovation and ensure quality, yield, and manufacturing efficiency. During the panel discussion, experts will share their insights on the metrology challenges and opportunities that today's semiconductor industry is facing across every segment of the supply chain, with a focus on advanced semiconductor packaging for next-generation microelectronics (e.g., heterogeneous integration, wafer level packaging, hybrid bonding, etc.).

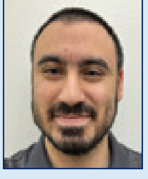
Paul Hale, NIST; Gaurang Choksi, Intel Corporation; Zhihua Zou, TSMC; CP Hung, ASE; Chet Lenox, KLA Corporation

2024 ECTC Special Session on Thermal Management for AI

Efficient and Innovative Thermal Management for Power Hungry AI/ML Applications: Challenges and Opportunities

Tuesday, May 28, 2024, 1:30 p.m. – 3:00 p.m. • Aurora B

Chairs: Zhi Yang, Groq and Sevket Yuruker, Tesla



The rapid advancement of artificial intelligence (AI) and machine learning (ML) technologies has led to the proliferation of high-power AI/ML applications in various domains, such as autonomous vehicles, high performance computing and natural language processing. However, this growth is accompanied by escalating thermal challenges that can critically impact the performance, reliability, and lifespan of entire systems. The non-uniform distribution of heat sources on AI/ML hardware further complicates cooling strategies. Moreover, the reliance on traditional thermal management techniques may prove inadequate in addressing emergent challenges.

To address these challenges, several industry and academia experts are discussing the current status and opportunities for innovative thermal management developments/methodologies in this special session.

Ki Wook Jung, Samsung; Igor Arsovski, Groq; Mudasir Ahmad, Google; Tiwei Wei, Purdue; University; Christopher Ortiz, Ansys

2024 ECTC Special Session on RF Packaging for above 100 GHz

RF Packaging for Communication and Sensing Applications above 100 GHz – Technologies, Design Challenges and Emerging Solutions

Tuesday, May 28, 2024, 3:30 p.m. – 5:00 p.m. • Aurora B

Chairs: Maciej Wojnowski, Infineon Technologies AG, and Ivan Ndip, Fraunhofer IZM/Brandenburg University of Technology

In this session, experts from industry and academia will present the latest developments in RF packaging for communication and radar sensing applications above 100 GHz. The panel will begin with a presentation of emerging applications, resulting challenges and opportunities for RF packaging. The experts will share the latest developments in RF packaging materials and technologies. Emerging RF system integration platforms will be presented, stressing the importance of material characterization and modeling as well as co-design and co-simulation techniques. The panel will conclude with examples of recent R&D results for novel D-band waveguide interfaces in packages for 6G data links over plastic microwave fiber (PMF), antennas-in-package (AiP) and phased array front-end AiP modules.

Swaminathan Sankaran, Texas Instruments; Martin Letz, Schott AG; Alberto Valdes-Garcia, IBM Research; Madhavan Swaminathan, Penn State University; Uwe Maass, Fraunhofer IZM

2024 ECTC Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 28, 2024, 8:00 a.m. – 5:00 p.m. • Aurora D

Chairs: William Chen, ASE, and Ravi Mahajan, Intel

Heterogeneous Integration uses packaging technology to integrate dissimilar chips, devices or components with different materials and functions, and from different fabless design houses, foundries, wafer materials, feature sizes and companies into a system or subsystem. In this workshop, 23 Technical working groups present on their areas of expertise. This workshop is a full-day event. Schedule:

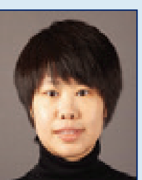
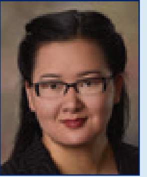
8:00 a.m. – 8:30 a.m. Welcome & Agenda Review
8:30 a.m. – 10:00 a.m. Challenges and Innovations in Thermal Engineering from Fan-out to 2.5D and 3D Stacking
10:30 a.m. – 12:00 p.m. Engineering Chiplets for the AI Era
1:30 p.m. – 3:00 p.m. CHIPS & Science Act Roundtable Chat
3:30 p.m. – 5:00 p.m. Packaging Challenges and Innovation for Future Communication Systems

2024 ECTC Young Professionals Networking Event

2024 Young Professionals Meetup

Tuesday, May 28, 2024, 7:00 p.m. – 7:45 p.m. • Aurora D

Chairs: Aakrati Jain, IBM, Rui Chen, Eastern Michigan University, and Zhangming Zhou, Auburn University

Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2024 IEEE EPS Seminar on Substrates for Chiplets

Substrate-Scaling Challenges in Chiplet Integration

Tuesday, May 28, 2024, 7:45 p.m. – 9:15 p.m. • Aurora A

Chairs: Takashi Hisada, Rapidus Corporation, and Yasumitsu Orii, Rapidus Corporation

Chiplet is driving performance scaling and cost efficiency of advanced semiconductor systems. There are difficult challenges for the substrates in chiplet integration such as very large size of the substrates, fine line and space ground rule with multiple layers, mechanical stress, reliability, and complexity of design.

The EPS Seminar organized by TC6 (High-Density Substrate and Board) will discuss technical and business challenges of chiplet on large substrates. We will have 7 panelists, and each panelist will give a short talk presenting insights on technology trends, technical challenges, application requirements, recent technical updates and more covering package form factors, design tools, materials, manufacturing tools, and assembly processes for advanced chiplet integration, followed by a panel discussion.

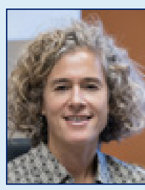
Gang Duan, Intel; Kinya Ichikawa, TSMC; Kenneth Larsen, Synopsys; Masahisa Ose, Resonac; Harish Penmethsa, AMAT; Yu-Po Wang, SPIL; Rozalia Beica, LQDX

2024 ECTC Keynote

Petascale Photonic Chip Connectivity for Energy Efficient AI Computing

Wednesday, May 29, 2024, 8:00 a.m. - 9:15 a.m. • Aurora A

Prof. Keren Bergman, Columbia University



High-performance data centers are increasingly bottlenecked by the energy and communications costs of interconnecting numerous compute and memory resources. Current systems face a gap of nearly two orders of magnitude between on-chip, intra-socket, communication capacities, and the capacities of links transporting data over longer distances. The per bit energy cost of data movement dominates that of data processing, as does density, throughput, and latency. Integrated silicon photonics offer the opportunity of optical connectivity that delivers high off-chip communication bandwidth densities with low power consumption. To realize these benefits deeply embedded packaging of photonics with the compute and memory is critical. This talk will cover these multi-chip packaging challenges as well as approaches for leveraging dense wavelength-division multiplexing photonic IO that can scale to realize Petabit/s chip escape bandwidths with sub-picojoule/bit energy consumption.

2024 ECTC/ITherm Diversity and Career Growth Panel and Reception

Effective Practices to Attract, Promote and Retain a Diverse Workforce

Wednesday, May 29, 2024, 6:30 p.m. – 7:30 p.m. • Aurora A

Chairs: Cristina Amon, University of Toronto / iTherm, and Vidya Jarayam, Intel / ECTC

Semiconductor, electronic packaging and energy-related companies are planning to grow their workforces to meet the current and expected demands due to policy incentives and domestic investments, including the CHIPS Act. To achieve business and economic success, we will need to attract a broader group of students to the relevant fields and expand beyond the traditional pool of candidates to include women and underrepresented minorities from rural candidates to veterans and mid-career retrainees. This panel will focus on how best practices in Diversity, Equity and Inclusion have been implemented and can be used to attract students and hire, develop, promote and retain employees within organizations to meet their goals.

The panelists will introduce some of the challenges faced by women, minorities , and underrepresented groups, as well as share their organization's strategies for professional development, promotion, retention, and success. This will be followed by an interactive Q&A with the audience.

After the panel session, a social and networking reception will be held. All ECTC and ITherm attendees are invited to join in on this engaging discussion and the reception afterwards.

Ramona Prioleau, CHIPS; Margaret Kindling, SEMI Foundation; Allyson Stewart, Marvell Inc; Al Ortega, Villanova University; Tina Herrera, NREL; Ravi Mahajan, Intel

2024 ECTC Plenary Session on Future of Semiconductor Industry

The Future of Semiconductor Industry. Emerging Start-ups and Material Innovations in Advanced Packaging

Thursday, May 30, 2024, 8:00 a.m. – 9:15 a.m. • Aurora A

Chairs: Rozalia Beica, LQDX, and Farhang Yazdani, BroadPak; Chair of Jury Panel: Jean-Christophe Eloy, Yole Group

Styled as a start-up competition, this session looks at next generation materials and companies.

It features presentations from start-up companies and reviewed by a panel of judges from the industry and investment community. Topics include Materials & Processes for MicroLED and System-In-Package, Thermal Management, Dielectrics & Metallization for High End IC Substrates.

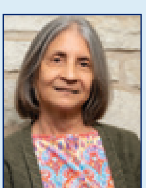
Victor Chiriac, Global Cooling Technology Group; Mohsen Asad, Hyperlume; Wayne Rickard, Terecircuits; Tristan El Bouayadi, Thintronics

2024 IEEE EPS President's Panel Session on Workforce

Challenges in Education and Workforce Development in the New Chips Economy

Friday, May 31, 2024, 8:00 a.m. – 9:15 a.m. • Aurora A

Chairs: Patrick Thompson, Texas Instruments; Mark Poliks, Binghamton University; Jeff Suhling, Auburn University; Kitty Pearsall, Boss Precision Inc.



The semiconductor and packaging industries are currently experiencing unparalleled growth, driven by demand in areas such as AI, transportation electrification, digital manufacturing, data centers, mobile devices, hybrid flexible electronics, virtual reality, and photonics and MEMS. This expansion has prompted substantial global investments in new fabs and packaging infrastructure, supported by government spending in North America, Europe, and Asia.

However, the parallel surge in demand for skilled labor poses a considerable challenge, with estimates indicating a threefold increase in headcount required over the next five years. The industry is seeking individuals with multidisciplinary education, ranging from technician degrees to Ph.D. degrees. The panel will explore workforce needs, industry perspectives on student preparation, global approaches to electronics packaging education, and innovative strategies to attract students to the semiconductor packaging field.

John Oakley, Semiconductor Research Corporation; Toni Mattila, Business Finland; Robert Geer, SUNY Polytechnic University; Wenhui Zhu, Central South University; Jim Wieser, Texas Instruments

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 28, 2024

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Summit 5 **1. High Reliability Soldering in Semiconductor Packaging** *Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech*	Summit 5 **9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability** *Course Leader: Pradeep Lall – Auburn University*
Summit 6 **2. Photonic Technologies for Communication, Sensing, and Displays** *Course Leader: Torsten Wipiejewski – Huawei Technologies*	Summit 6 **10. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level and Advanced RF Packages** *Course Leaders: Ivan Ndip – Fraunhofer IZM/ Brandenburg University of Technology and Markus Wöhrmann – Fraunhofer IZM*
Summit 7 **3. From Wafer to Panel Level Packaging** *Course Leaders: Tanja Braun and Piotr Mackowiak – Fraunhofer IZM*	Summit 7 **11. Advanced Packaging – Fan-Out, Chiplet, and Heterogeneous Integration** *Course Leader: John Lau – Unimicron*
Summit 8 **4. Eliminating Failure Mechanisms in Advanced Packages** *Course Leader: Darvin Edwards – Edwards Enterprises*	Summit 8 **12. Analysis of Fracture and Delamination in Microelectronic Packages** *Course Leader: Andrew Tay – National University of Singapore*
Summit 9 **5. Navigating Thermal and Reliability Challenges in Chip Components for Automotive High-Performance Compute Systems** *Course Leader: Fen Chen – Automotive Reliability/Validation Consultation Services*	Summit 9 **13. Advanced Packaging for MEMS and Sensors** *Course Leader: Horst Theuss – Infineon Technologies AG*
Crest 3 **6. Polymers for Advanced Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*	Crest 3 **14. Nano Materials and Polymer Composites for Electronic Packaging** *Course Leaders: C.P. Wong – Georgia Tech and Daniel Lu – Henkel Corporation*
Crest 4 **7. Flip Chip Technologies** *Course Leader: Shengmin Wen – SiMa Technologies, Inc.*	Crest 4 **15. Design-On-Simulation for Advanced Packaging Reliability and Life Prediction** *Course Leaders: Kuo-Ning Chiang – National Tsing Hua University*
Crest 5 **8. Reliable Integrated Thermal Packaging for Power Electronics** *Course Leaders: Patrick McCluskey – University of Maryland and Damena Agonafer – NEIT Laboratory, University of Maryland*	Crest 5 **16. Thermal Spreading and Contact Resistance** **Course Leaders: Yuri Muzychka – Memorial University of** *Newfoundland and Marc Hodes – Tufts University*

Refreshment Breaks
10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Summit and Crest Foyers

COMMITTEE MEETINGS

ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday May 28, 2024

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Summit 2

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Summit 3

Wednesday May 29, 2024

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Summit 2

7:00 a.m. – 8:00 a.m.
EPS Materials & Process TC
Summit 3

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
Summit 10 & 11

6:00 p.m. – 7:00 p.m.
ECTC Program Subcommittee Chairs & Assistant Chairs Reception
(by invitation only)

Thursday, May 30, 2024

7:00 a.m. – 8:00 a.m.
EPS Chapter Chairs Meeting
Summit 3

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Summit 2

7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
Summit 1

7:00 a.m. – 8:00 a.m.
EPS EDMS TC
Summit 10 & 11

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
Crest 1 & 2

8:00 a.m. – 9:00 a.m.
EPS Conference Organizers
Summit 10 & 11

4:30 p.m. – 6:00 p.m.
EPS BoG Information Session
Summit 10 & 11

5:30 p.m. – 6:30 p.m.
ECTC 2025 Program Committee Meeting
Aurora D

9:00 p.m.
74th ECTC Governing/ Executive Committee Reception
(by invitation only)

Friday May 31, 2024

7:00 a.m. – 8:00 a.m.
EPS RF & THz Tech. TC
Summit 3

7:00 a.m. – 8:00 a.m.
EPS Photonics TC
Summit 1

7:00 a.m. – 8:00 a.m.
EPS Emerging Tech TC
Summit 2

9:00 a.m. – 10:00 a.m.
EPS T-CPMT SAE/AE's
Summit 10 & 11

2:15 p.m. – 5:15 p.m.
ECTC Executive Committee
Crest 1 & 2

5:30 p.m. – 6:30 p.m.
ECTC / EPS Steering Committee
Crest 1 & 2

ECTC 2023 BEST PAPER AWARDS

BEST SESSION PAPER

Fine Pitch Die-to-Wafer Hybrid Bonding

Thomas Workman, Jeremy Theil, Gill Fountain, Dominik Suwito, Cyprian Uzoh, Guilian Gao, K. M. Bang, Bongsub Lee, Laura Mirkarimi – Adeia

OUTSTANDING SESSION PAPER

A New Adhesive for CoW Cu-Cu Hybrid Bonding with High Throughput and Room Temperature Pre-Bonding

Yasuhisa Kayaba, Yuzo Nakamura, Wataru Okada, Takuo Shikama, Kahori Tamura, Satoshi Inada – Mitsui Chemicals, Inc.

BEST INTERACTIVE PRESENTATION PAPER

50 nm Overlay Accuracy for Wafer-to-Wafer Bonding by High-Precision Alignment Technologies

Hajime Mitsuishi, Hiroshi Mori, Hidehiro Maeda, Mikio Ushijima, Atsushi Kamashita, Masashi Okada, Masanori Aramata, Takashi Shiomi, Shinya Sakamoto, Kishou Takahata, Tomohiro Chiba, Minoru Fukuda, Masahiro Kanbayashi, Toshimasa Shimoda, Isao Sugaya – Nikon Corporation

OUTSTANDING INTERACTIVE PRESENTATION PAPER

Optimization of the Cu Microstructure to Improve Copper-to-Copper Direct Bonding for 3D Integration

Ralf Schmidt, Christian Schwarz – Atotech (MKS Instruments)

INTEL BEST STUDENT PAPER

Thermal-Aware SoC Macro Placement and Multichip Module Design Optimization with Bayesian Optimization

Michael Molter, Elyse Rosenbaum – University of Illinois Urbana-Champaign; Rahul Kumar, Madhavan Swaminathan – Penn State University; Sonja Koller – Intel Deutschland GmbH; Nikita Ambasana – DPE, DCAI, Intel India

INTEL OUTSTANDING STUDENT PAPER

Scalable Fiber-Array-to-Chip Interconnections With Sub-Micron Alignment Accuracy

Shengtao Yu, Thomas K. Gaylord, Muhannad S. Bakir – Georgia Institute of Technology

TI BEST IP STUDENT PAPER

Simulation, Prediction, and Verification of the Corrosion Behavior of Cu-Ag Composite Sintered Paste for Power Semiconductor Die-attach Applications

Xinyue Wang, Zhoudong Yang, Pan Liu – Fudan University; Guoqi Zhang – TU Delft; Jing Zhang – Heraeus Materials Technology Shanghai Ltd.

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To sign-up for sponsorship or to get more details, please contact Alan Huffman at alan.huffman@ieee.org or +1-336-380-5124.

PROGRAM SESSIONS: WEDNESDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 1: Advances in Fan-Out, Wafer-Level, and Panel-Level Packaging Technologies Enabling New Applications	Session 2: Advanced Die-to-Wafer Hybrid Bonding for Heterogeneous Integration	Session 3: Co-Packaged Optics
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Photonics**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: **Beth Keser - ZeroASIC** **bethk@kesers.com** **Steffen Kroehnert - ESPAT Consulting** **steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs:** **Katsuyuki Sakuma - IBM Research** **ksakuma@us.ibm.com** **Tiwei Wei - Purdue University** **tiwei@purdue.edu**	**Session Co-Chairs:** **Richard Pitwon - Resolute Photonics** **richard.pitwon@resolutephotonics.com** **Nicolas Boyer - Ciena** **nboyer@ciena.com**
1. 9:30 AM - How to Manipulate Warpage in Fan-Out Wafer and Panel Level Packaging *Tanja Braun, Ole Hölck, Marius Adler, Mattis Obst, Steve Voges, Karl-Friedrich Becker, Rolf Aschenbrenner - Fraunhofer IZM; Marcus Voitel, Marc Dreissigacker, Martin Schneider-Ramelow - Technical University Berlin*	***1. 9:30 AM - Direct Die-to-Wafer Hybrid Bonding Using Plasma Diced Dies and Bond Pad Pitch Scaling Down to 2 µm*** *Ye Lin, Pieter Bex, Koen Kennes, Jaber Derakhshandeh, Prathamesh Dhakras, Samuel Suhard, Carine Gerets, Sven Dewilde, Violeta Georgieva, Anne Jourdain, Gerald Beyer, Eric Beyne - imec*	***1. 9:30 AM - High Density Integration of Silicon Photonic Chiplets for 51.2T Co-Packaged Optics*** *Sukeshwar Kannan, Ray Chang, Hari Potluri, Sheng Zhang - Broadcom, Inc.; Jay Li, Bruce Xu, Hsi-Chang Hsu - Siliconware Precision Industries Co., Ltd.*
2. 9:50 AM - Advanced FO-PLP with Multi-chip for Wearable Application *Jooyoung Choi, Hyungmin Kim, Jaehoon Choi, Eun Seok Choi, Hwanpil Park, Gyunghwan Oh, Seungsoo Ha, Wonkyung Choi, Dong Wook Kim - Samsung Electronics Co., Ltd.*	***2. 9:50 AM - Multi-Functional Self-Assembled Monolayer for Chip-to-Chip and Chip-to-Wafer Hybrid Bonding*** *Murugesan Mariappan, H Hashimoto, T Fukushima - Tohoku University; K Mori - T-Micro; A Kurachi, T Imori - JX Metals Corporation*	***2. 9:50 AM - Ultra Low-Loss Ion-Exchange Waveguides in Optimized Alkali Glass for Co-Packaged Optics*** *Lars Brusberg, Matthew J. Dejneka, Chukwudi A. Okoro, David J. McEnroe, Aramais R. Zakharian, Chad C. Terwilliger - Corning Research and Development Corp.*
3. 10:10 AM - Transcending the Reticle Limit in On-Wafer Die Integration and Advanced Packaging: Full-Wafer Patterning With High-Productivity Electron Beam Lithography *Andrew Ceballos, Kenneth MacWilliams, Ted Prescop, Tsenguun Byambadorj, David Lam - Multibeam Corporation; Timothy Michalka - TLM Technologies, LLC; Craig Bishop, Cliff Sandstrom, Tim Olson - Deca Technologies, Inc.*	***3. 10:10 AM - 3D Heterogeneous Integration With Sub-3 µm Bond Pitch Chip-to-Wafer Hybrid Bonding*** *Yi Shi, Haris Niazi, Michael Baker, Yuan Meng, Ashish Dhall, Xavier Brun - Intel Corporation*	***3. 10:10 AM - A Surface-Mount Photonic Package With a Photonic-Wire-Bonded Glass Interposer as a Hybrid Integration Platform for Co-Packaged Optics*** *Hiroshi Uemura, Taichi Misawa, Yasutaka Mizuno, Hajime Arao, Tetsuya Nakanishi, Keiji Tanaka, Tomomi Sano, Katsumi Uesaka - Sumitomo Electric Industries, Ltd.; Mami Miyairi, Yoshikatsu Ishizuki, Taiji Sakai - FICT LIMITED; Yoichiro Kurita - Tokyo Institute of Technology*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Aurora 1		
4. 11:15 AM - 600 mm x 600 mm Fan-Out Panel Level Package (FOPLP) as an Alternative to Lead-Frame-Free Quad Flat No Lead (QFN) Package *Jacinta Aman Lim, Yoon Muk Park, Brett Dunlap, Jane Lee - nepes Corporation; Robin Davis - DECA*	***4. 11:15 AM - Novel Three-Layer Stacking Process With Face-To-Back CoW 6 µm-Pitch Hybrid Bonding*** *Akihiro Urata, Takahiro Kamei, Akihisa Sakamoto, Hirotaka Yoshioka, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation*	***4. 11:15 AM - Development of All-Photonics-Function Embedded Package Substrate Using 2.3D RDL Interposer for Co-Packaged Optics*** *Akihiro Noriki, Fumi Nakamura, Satoshi Suda, Takayuki Kurosu, Takeru Amano - National Institute of Advanced Industrial Science and Technology; Hirotaka Uemura, Haruhiko Kuwatsuka, Naoki Matsui, Reona Motoji, Dan Maeda, Tomoya Sugita - Kyocera Corporation*
5. 11:35 AM - Challenges and Analysis for Pitch 25 µm - 100 µm Mixed Micro Bumps and Interconnection in Fan-Out Embedded Bridge Die With TSV Package (FO-EB-TSV) *Kuei Hsiao Kuo, Jia Han Li, Chia Shing Wu, Feng Lung Chien - Siliconware Precision Industries Co., Ltd.*	***5. 11:35 AM - Dielectric Stack Optimization for Die-Level Warpage Reduction for Chip-to-Wafer Hybrid Bonding*** *Chandra Rao Bhesetti, Dileep Kumar Mishra, Nagendra Sekhar Vasarla, Sasi Kumar Tippabhotla, Ismael Cereno Daniel, Ser Choong Chong, King Jien Chui, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR*	***5. 11:35 AM - Advanced 3D Packaging of 3.2Tbs Optical Engine for Co-Packaged Optics (CPO) in Hyperscale Data Center Networks*** *Aparna Prasad, Sandeep Razdan, Paul Ton, Cristiana Muzio - Cisco Systems, Inc.*
6. 11:55 AM - High Precision and Productivity Bridge-Die-Last Bonding Process and Its Reliability for Pillar-Suspended Bridge (PSB) Architecture *Ichiro Kono, Yoshihiro Kometani, Atsushi Kuroha - AOI Electronics; Yoichiro Kurita - Tokyo Institute of Technology*	***6. 11:55 AM - Low Temperature Wafer Level Hybrid Bonding Enabled by Advanced SiCN and Surface Activation*** *Fumihiro Inoue, Junya Fuse, Sodai Ebiko, Ryosuke Sato - Yokohama National University; Atsushi Nagata, Yoshihiro Kondo - Tokyo Electron Kyushu, Ltd.; Kenichi Saito, Takuo Kawauchi - Tokyo Electron, Ltd.; Junghwan Park, Chiwoo Ahn, Myeonghyeon Kim, Jiho Kang - SK Hynix, Inc.*	***6. 11:55 AM - 3D-Printed Beam Expanding Lens for Chip to Fiber Vertical Coupling*** *Yasutaka Mizuno, Hiroshi Uemura, Tomoya Saeki, Keiji Tanaka, Katsumi Uesaka - Sumitomo Electric Industries, Ltd.*
7. 12:15 PM - Vertical Fan-Out (VFO) Package With Enhanced Form Factor and Performances for Mobile Applications *Kijun Sung, Kyoungtae Eun, Seowon Lee, Sungwon Yoon, Ho-Young Son, Kang-Wook Lee - SK Hynix, Inc.*	***7. 12:15 PM - A Study on D2W Hybrid Cu Bonding Technology for HBM Multi-Die Stacking*** *Hyeonmin Lee, Jihoon Kim, Hyungchul Shin, Wonil Lee, Aeni Jang, Hyuekjae Lee, Byungchan Kim, Ilhwan Kim, Dongjoon Oh, Jumyong Park, Un-Byoung Kang, Dae-Woo Kim - Samsung Electronics Co., Ltd.*	***7. 12:15 PM - Characterization of QSFP and OSFP CPO ELS Modules Employing an 8-channel CWDM TOSA in Practical Air-Cooling Conditions*** *Kohei Umeta, Taketsugu Sawamura, Kyoko Nagai, Yuki Shiroishi, Hideyuki Nasu - Furukawa Electric Co., Ltd.*

PROGRAM SESSIONS: WEDNESDAY, MAY 29, 9:30 A.M. - 12:35 P.M.

Session 4: Reliability of Advanced Substrates and Interconnects	Session 5: Digital Healthcare: Wearable Sensors, and Flexible Electronics	Session 6: Thermal-Mechanical Reliability Simulations
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: Christian Schmidt – NVIDIA Corporation christians@nvidia.com Keith Newman - AMD keith.newman@amd.com	**Session Co-Chairs: Rabindra N. Das - MIT Lincoln Labs rabindra.das@ll.mit.edu Hee Seok Kim - University of Washington Tacoma heeskim@uw.edu**	**Session Co-Chairs: Wei Wang - Qualcomm Technologies, Inc. weiwang.cu@gmail.com Karsten Meier - TU Dresden karsten.meier@tu-dresden.de**
1. 9:30 AM - Reliability Assessment of Stacked-Vias With Different Configurations Through a Unit Cell-based Substrate Design *Krishna Tunga, Joseph Ross, Shidong Li, Sushumna Iruvanti, Bakul Parikh - IBM Corporation*	***1. 9:30 AM - Three-Dimensional Integration of a Flexible Battery and a Flexible Wireless Charger for Powering Wearables*** *Guangqi Ouyang, Subramanian Iyer - University of California, Los Angeles*	***1. 9:30 AM - Modeling and Optimization of Thermal Cycling Performance to Reduce Ratcheting-Induced Passivation Cracking in High-Voltage Power Modules*** *Bill Chen, Yong Liu - ON Semiconductor*
2. 9:50 AM - Enhanced Biased HAST Reliability of Polyimide for High-Density Redistribution Layers *Takumi Onuma, Daisaku Matsukawa, Takahiro Tanabe - HD MicroSystems LLC*	***2. 9:50 AM - Ferrite-Based NFC Antenna and Sensor Package Module Development for Implantable Continuous Glucose Monitor*** *Gaurav Mehrotra, Young Kim, Marko Mailand - Renesas Electronics Corporation; James Masciotti - Senseonics, Inc.; Ginger Huang, Jackson Chen, Ryan Lai - Advanced Semiconductor Engineering, Taiwan*	***2. 9:50 AM - Interfacial Reliability and Predictive Models for Potted Board Assemblies in Inclined 25000 g Mechanical Shock*** *Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Jeff Suhling - Auburn University; Ken Blecker - US Army*
3. 10:10 AM - Effect of Lamination Process-Induced Residual Stress on the CTE of Advanced Prepregs Before and After Solder Reflow Process *Byoung-Phil Kang - Chungbuk National University/ SIMMTECH; Jong-Yun Lee - Chungbuk National University; Jaesung Kim, Jongwoo Park, Kyu-Jin Lee - SIMMTECH; Yongrae Jang, Bongtae Han - University of Maryland*	***3. 10:10 AM - Design and Development of Sustainable Low-Cost Single-Use Electrode Leads for Wearable Medical Devices*** *Babatunde Falola, Riadh Al-Haidari, Udara Somarathna, Bryan Cabrera, Mohammed Alhendi, Mark D Poliks - Binghamton University; Nancy Stoffel - General Electric Global Research; Gurvinder Khinda, Tzu-Jen Felix Kao - General Electric Healthcare; Rafael Tudela - Tapecon, Inc.*	***3. 10:10 AM - A Novel Approach to Assess Board Level Solder Joint Reliability for Flip Chip on Leadframe Package Using Finite Element Analysis*** *Guangxu Li, Siva Gurrum, Frank Mortan, Li Jiang, Carlos Arroyo - Texas Instruments, Inc.*
Refreshment Break: 10:30 a.m - 11:15 a.m. – Exhibition Hall – Aurora 1		
4. 11:15 AM - Fan-Out PoP Solder Joint Reliability Investigation by System Power Cycling *Chi Ko Yu, Techi Wong, Hank Hsieh, P. H. Tsao, M.Z. Lin, Liham Chu - MediaTek, Inc.*	***4. 11:15 AM - Conformal Skin Patch for Dehydration Monitoring in Dementia Patients*** *Musafargani Sikkandhar, Ramona B. Damalerio, Wei Da Toh, Ming-Yuan Cheng - Institute of Microelectronics A*STAR*	***4. 11:15 AM - A Robust Mesh Size Control Technology Suitable for Various Empirical Equations for Predicting Solder Joint Reliability*** *Kuo-Ning Chiang, C. E Lee - National Tsing Hua University; Cadmus Yuan - Feng Jia University*
5. 11:35 AM - Fatigue-Fracture Propensity Measurement and Competing Risk Model for FCBGA Interfaces Under Sustained Humidity and Temperature Exposure *Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Madhu Kasturi, Jeff Suhling - Auburn University*	***5. 11:35 AM - Silicon-Based Membrane Pressure Sensor for Inline Monitoring of Pressure and Hermeticity of Small-Volume Bonded Packages*** *Jannik Koch, Levin Brinkmann, Alexander Kassner, Folke Dencker, Marc Wurz - Institute of Micro Production Technology*	***5. 11:35 AM - Multi-Material Corner Singularity in Electronic Packaging: Avoiding Mesh Dependence in Analyzing Stress*** *Yaxiong Chen, Torsten Hauck - NXP Semiconductor, Inc.; Ganesh Subbarayan - Purdue University*
6. 11:55 AM - Evaluation of Vapor Pressure Induced Debonding Failure in Fan-Out Package Under Reflow Condition *Bo-Shuo Chen, Tz-Cheng Chiu - National Cheng Kung University; Wei-Jie Yin, Chin-Li Kao - Advanced Semiconductor Engineering, Taiwan*	***6. 11:55 AM - Using Flexible Hybrid Electronics on a Miniaturized Non-invasive Bio-optical Sensor For Hemoglobin Detection*** *Yu-Chih Lee, Kai-Lun Yu, Shu-An Tsai, Pai-Sheng Shih, Guo-Sin Huang, Tien-Chia Liu, Hung-I Lin, Jen-Chun Chen, Jen-Kuang Fang, Harrison Chang - Advanced Semiconductor Engineering, Inc.; Tzyy-Wei Fu, Sheng-Hao Tseng - National Cheng Kung University*	***6. 11:55 AM - Bayesian Optimization of Large Glass Package Architecture for System-Level Reliability in High-Performance Computing Applications*** *Emanuel Torres Surillo, Christian Molina-Mangual, Pratik Nimbalkar, Hyunggyu Park, Ramon Sosa, Vanessa Smet - Georgia Institute of Technology*
7. 12:15 PM - Characterization and Sensitivity Analysis of Piezoresistive Stress Sensor for Thermal and Mechanical Loads and Implementation for In-Situ Health Monitoring of Solder Bumps *Adwait Inamdar, Willem van Driel, GuoQi Zhang - Delft University of Technology; Varun Thukral, Letian Zhang, Jeroen Zaal, Michiel van Soestbergen, Hanz Tuinhout - NXP Semiconductor, Inc.*	***7. 12:15 PM - A Multi-Channel, Embedded, and Geometrically Optimized Filter Bank Utilizing Advanced Packaging Topologies for Miniaturized RF Modules in IoT and Wearable Systems*** *Hani Al-Jamal, Marvin Joshi, Manos M. Tentzeris - Georgia Institute of Technology; Nick Kingsley - Teradyne*	***7. 12:15 PM - Prediction of Moisture Absorption Characteristics Under Normal/ Accelerated Preconditioning Condition in Multi-Chip Packages*** *Hyunggyun Noh, Jinsoo Bae, Keunho Rhew, Soojin Yoo, Jiyoung Lim, Yuchul Hwang, Sangwoo Pae - Samsung Electronics Co., Ltd.*

PROGRAM SESSIONS: WEDNESDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 7: Heterogeneous Integration: Systems Design, Signal & Power Delivery, and Process Optimization	Session 8: Sub-Micron Scaling in Wafer-to-Wafer Hybrid Bonding	Session 9: Advanced Processes for Chip Stacking
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: Materials & Processing**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: Lihong Cao - ASE lihong.cao@aseus.com Subhash L. Shinde - Notre Dame University sshinde@nd.edu	**Session Co-Chairs: Jean-Charles Souriau - CEA Leti jcsouriau@cea.fr Matthew Yao - GE Aerospace matthew.yao@ge.com**	**Session Co-Chairs: Qianwen Chen – IBM Research chenq@us.ibm.com Vidya Jayaram - Intel vidya.jayaram@intel.com**
1. 2:00 PM - Next Generation Large Size High Interconnect Density CoWoS-R Package *Chien-Hsun Lee, C.L. Lai, M. Liu, J. Hu, S.L. Tsai, H.Y. Chen, J. Lin, C.C. Hsieh, C.K. Hsu, Kathy Yan, Shin-Puu Jeng, Jun He - Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 2:00 PM - Study of Ultra Fine 0.4 µm Pitch Wafer-to-Wafer Hybrid Bonding and Impact of Bonding Misalignment*** *Yukako Ikegami, Takumi Onodera, Masanori Chiyozono, Akihisa Sakamoto, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation*	***1. 2:00 PM - IR Laser Release for 3D Stacked Devices: Effect of the Release Stack Structure on the Debonding Mechanism*** *François Chancerel, John Slabbekoorn, Steven Brems, Alain Phommahaxay, Eric Beyne - imec; Peter Urban, Julian Bravin, Thomas Uhrmann, Markus Wimplinger - EV Group, Inc.*
2. 2:20 PM - World's First UCIe Interoperability Silicon Enabling Open Standards Heterogeneous Integration *Xavier Brun, Stephen Wong - Intel Corporation; Manuel Mota - Synopsys, Inc.*	***2. 2:20 PM - 3-Layer Fine Pitch Cu-Cu Hybrid Bonding Demonstrator With High Density TSV for Advanced CMOS Image Sensor Applications*** *Stephane Nicolas, Jerzy-Javier Suarez-Berru, Nicolas Bresson, Carole Socquet-Clerc, Myriam Assous, Stephan Borel - Grenoble Alps University/CEA-LETI*	***2. 2:20 PM - High Performance 3D Package Technology for Mobile Application Processor (AP)*** *Sun Jae Kim, Cheol Kim, Huiyeong Jang, Jongpa Hong, Seongyo Kim, Yongwon Choi, Chajea Jo, Sun-Kyung Seo, Dong Kwan Kim, Dae-Woo Kim - Samsung Electronics Co., Ltd.*
3. 2:40 PM - Scalable Advanced DBHi Chiplet Package Using Silicon Bridge With 30 µm-Pitch Solder Joints *Akihiro Horibe, Takahito Watanabe, Chinami Marushima, Sayuri Kohara, Hiroyuki Mori - IBM Research, Tokyo; Divya Taneja, Thomas Wassick, Isabel de Sousa - IBM Infrastructure; Qianwen Chen, Eric Perfecto, Aakrati Jain, Joseph Ross - IBM Research*	***3. 2:40 PM - Scaling Cu/SiCN Wafer-to-Wafer Hybrid Bonding Down to 400 nm Interconnect Pitch*** *Boyao Zhang, Soon-Aik Chew, Michele Stucchi, Sven Dewilde, Serena Iacovo, Liesbeth Witters, Tomas Webers, Koen Van Server, Joeri De Vos, Andy Miller, Gerald Beyer, Eric Beyne - imec*	***3. 2:40 PM - Room Temperature Bonding of CVD Polycrystalline Diamond Wafers to Semiconductor and Piezo-Electric Single Crystalline Wafers*** *Tadatomo Suga, Junsha Wang Suga - Meisei University; Kazuya Yamamura - Osaka University; Izumi Kataoka - IIPT Inc.*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Aurora 1		
4. 3:45 PM - Performance Evaluation of UCIe-Based Die-to-Die Interface on Low-Cost 2D Packaging Technology *Srujan Penta - Marvell Technology, Inc. / Georgia Institute of Technology; Ting Zheng, Eric Tremble, Aatreya Chakravarti, Anthony Sigler, Carl Benes, Wolfgang Sauter - Marvell Technology, Inc.; Zhonghao Zhang, Muhannad Bakir - Georgia Institute of Technology*	***4. 3:45 PM - Fine Pitch and Low Temperature Nanocrystalline-Nanotwinned Cu and SiCN-to-SiO2 Wafer-to-Wafer Hybrid Bonding*** *Wei-Lan Chiu, Ou-Hsiang Lee, Chia-Wen Chiang, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo - Industrial Technology Research Institute; James Yi-Jen Lo, Chiang-Lin Shih, Hsih-Yang Chiu - Nanya Technology Corporation*	***4. 3:45 PM - Bump-Less Interconnect With Room Temperature Pre-Bondable Adhesive and Solder for High Throughput Chip Stacking*** *Wataru Okada, Yuzo Nakamura, Yasuhisa Kayaba, Takuo Shikama, Yutaka Hisamune, Kahori Tamura, Satoshi Inada, Rikia Furusho - Mitsui Chemicals, Inc.*
5. 4:05 PM - Signal & Power Integrity Optimization Utilizing Silicon Core Substrate *Seann Ayers, Steven Verhaverbeke, Han-Wen Chen, Liu Jiang, El Mehdi Bazizi - Applied Materials, Inc.*	***5. 4:05 PM - Single-Grain Cu µ-Joint Formation Induced by Selective Under-Seed-Metallurgy for Hybrid Bonding*** *Murugesan Mariappan, Hiroyuki Hashimoto, Takafumi Fukushima - Tohoku University; Kiyoharu Mori - T-Micro; Masahiro Sawa, Jinta Nampo - JCU Corporation*	***5. 4:05 PM - IR Laser Debond From Silicon Carrier Wafers With Inorganic Thin Film Release Layers for High-Density 2.5D and 3D Integration*** *Thomas Sounart, Tushar Talukdar, Henning Braunisch, Paul Nordeen, Kimin Jun, Aleksandar Aleksov, Adel Elsherbini, Shawna Liff, Johanna Swan - Intel Corporation*
6. 4:25 PM - Package Power Delivery Architecture for High Performance Computing Systems With a 1 kW IVR Operated in CCM-DCM Boundary Mode Condition *Ramin Rahimzadeh Khorasani, Madhavan Swaminathan - Pennsylvania State University; Xingchen Li, Joon Woo Kim, Prahalad Murali - Georgia Institute of Technology; Rohit Sharma - Indian Institute of Technology Ropar*	***6. 4:25 PM - 0.5 µm Pitch Wafer-to-Wafer Hybrid Bonding at Low Temperatures With SiCN Bond Layer*** *Kai Ma, Nikos Bekiaris, Sesh Ramaswami - Applied Materials, Inc.; Taotao Ding, Gernot Probst, Tobias Wernicke, Thomas Uhrmann, Markus Wimplinger - EV Group, Inc.*	***6. 4:25 PM - Backside Thinning Process Development for High-Density TSV in a 3-Layer Integration*** *Renan Bouis, Lionel Vignoud, Jerome Dechamp, Damien Hebras, Paul Valentin, Jeremy Marchand, Stephan Borel - Grenoble Alps University/CEA-LETI; Myriam Assous - CEA-LETI*
7. 4:45 PM - Study for Realization of the Next Generation High Density RDL Packaging for 2.5D Large Silicon Interposer *Masaki Mizutani, Yusuke Tokuyama, Noriyuki Shiozawa, Mizuma Murakami, Hiromi Suda, Ken-Ichiro Shinoda, Ken-Ichiro Mori - Canon, Inc.; Douglas Shelton - Canon USA, Inc.*	***7. 4:45 PM - Development of Double Cantilever Beam Technique for Wafer-to-Wafer Bond Energy Measurement*** *Guohua Wei, Matthew Gerber, Derik Rudd, Robert Sibley, Pengfei Nie, Logan Battrell, Andrew Bayless, Sam Ireland, Mark Fischer, Dan Markowitz, David Palsulich - Micron Technology, Inc.*	***7. 4:45 PM - Process Development and Characterization of Ru-Based UBM for In Bumps Integration for Quantum Computing Applications*** *Harold Le Tulzo, Diane Bijou, Thér`ese Souza, Anthony Gallegos, Jérôme Daviot - Technic France; Candice Thomas, Edouard Deschaseaux, Céline Feautrier, Jean Charbonnier, Alain Gueugnot - CEA-LETI; Jaber Derakhshandeh, Tassawar Hussain - imec*

PROGRAM SESSIONS: WEDNESDAY, MAY 29, 2:00 P.M. - 5:05 P.M.

Session 10: Novel 3D Integration and Hybrid Bonding Solutions	Session 11: Next-Generation Artificial Intelligence, Quantum Computing, and Secure Packaging	Session 12: Artificial Intelligence and Advanced Modeling Approaches
Committee: Assembly & Manufacturing Technology	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: Zia Karim - Yield Engineering Systems zkarim@yieldengineering.com Wenhao (Eric) Li - Intel wenhao.li@intel.com	**Session Co-Chairs: Rohit Sharma - IIT Ropar rohit@iitrpr.ac.in Santosh Kudtarkar - Analog Devices santosh.kudtarkar@analog.com**	**Session Co-Chairs: Yong Liu - OnSemi Yong.Liu@onsemi.com KN Chiang - National Tsinghua University knchiang@pme.nthu.edu.tw**
1. 2:00 PM - Investigation of Distortion in Wafer-to-Wafer Bonding With Highly Bowed Wafers *Shuo Kang, Serena Iacovo, Koen D'havé, Stefaan Van Huylenbroeck, Joeri De Vos, Gerald Beyer, Eric Beyne - imec; Thomas Plach, Gernot Probst, Taotao Ding, Markus Wimplinger, Thomas Uhrmann - EV Group, Inc.*	***1. 2:00 PM - Reworkable Superconducting Qubit Package for Quantum Computing*** *Rabindra Das, John Cummings, Thomas Hazard, Danna Rosenberg, David Conway, Shireen Warnock, Michael Gingras, Cyrus Hirjibehedin, Bethany Huffman, Steven Weber, Jonilyn Yoder, Mollie Schwartz - MIT Lincoln Laboratory*	***1. 2:00 PM - Machine-Learning Guided Strain-Relief Patterns for Maximizing Stretchability of Printed Conductors*** *Rui Chen - Eastern Michigan University; Suresh Sitaraman - Georgia Institute of Technology*
2. 2:20 PM - Development of 0.5 µm Pixel 3-Wafers Stacked CMOS Image Sensor With Through Silicon Deep Contact and In-Pixel Cu-Cu Bonding Process *Do Yeon Kim - Samsung Electronics Co., Ltd.*	***2. 2:20 PM - Key Technologies and Design Aspects for Wafer Level Packaging of High Performance Computing Modules*** *Kai Zoschke, Hermann Oppermann, Michael Schiffer, Ivan Ndip, Karl-Friedrich Becker, Marius Adler, Alexander Gäbler, Uwe Maass - Fraunhofer IZM; Gianna Paulin - Swiss Federal Institute of Technology; Walter Kocon - GlobalFoundries, Inc.*	***2. 2:20 PM - Development of Real-Time Thermal Monitoring of GaN-based Power Inverter Modules Using Digital Twin*** *Bin He, Gongyue Tang - Institute of Microelectronics A*STAR; Jaydeep Saha, Rahul Sadanand Bhujade, Sanjib Kumar Panda - National University of Singapore*
3. 2:40 PM - Non-TCB Process Cu/ SiO2 Hybrid Bonding Using Plasma-Free Hydrophilicity Enhancement With NaOH for Chip-to-Wafer Bonding *Yu-An Chen, Jia-Juen Ong, Wei-You Hsu, Shih-Chi Yang, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute*	***3. 2:40 PM - Fine Pitch Nb-Nb Direct Bonding for Quantum Applications*** *Pablo Renaud, Christophe Dubarry, Nicolas Bresson, Edouard Deschaseaux, Frank Fournel, Christophe Morales, Anne-Marie Papon, Candice Thomas - Grenoble Alps University/CEA-LETI; Jean Charbonnier - CEA-LETI*	***3. 2:40 PM - Creep Parameters for Solder Interconnects by Nanoindentation Inverse-FEA Method*** *Shidong Li, Christine Taylor, Charles Arvin - IBM Corporation*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Aurora 1		
4. 3:45 PM - A Novel Approach to Low Temperature Bonding Using Single Wafer Thermal Processing System *Masha Gorchichko, Shashank Sharma, Ben Ng, Tyler Sherwood, Yoocharn Jeon, Kun Li, Sarabjot Singh, Evan Iler, Raghav Sreenivasan, Sid Krishnan - Applied Materials, Inc.*	***4. 3:45 PM - Si Interposer With Cu TSVs on Cu Substrate Thermally and Electrically Anchoring Qubit Chips in Millikelvin Assembly*** *Misato Taguchi, Takaaki Okidono, Takuji Miki, Makoto Nagata - Kobe University*	***4. 3:45 PM - Deep Convolution Neural Networks for Automatic Detection of Defects Which Impact Hybrid Bonding Yield*** *Oliver Zhao, Dominik Suwito, Bongsub Lee, Thomas Workman, Laura Mirkarimi - Adeia*
5. 4:05 PM - Moving Towards Microchannel- Based Chip Cooling *Paul Semenza, Gity Samadi - SEMI; Dave Thomas - SPTS Technologies, Ltd.; Garrett Oakes, Dave Kirsch - EV Group, Inc.; Yin Hang - Meta Platforms, Inc.; Kuo-Chung Yee - Taiwan Semiconductor Manufacturing Company, Ltd.; Michael Cumbie, Paul Benning - HP Inc.; Madhusudan Iyengar - Google; Lihong Cao, William Chen - Advanced Semiconductor Engineering, Inc. (US)*	***5. 4:05 PM - Novel Approach for 3D Defect Detection and Metrology of HBMs Using Minimum Labeled Data*** *Ziyuan Zhao, Qiyu Wei, Jie Wang, Richard Chang, Ramanpreet Pahwa - Institute for Infocomm Research A*STAR; Xulei Yang - Institute of Microelectronics A*STAR*	***5. 4:05 PM - Experimentally Validated Thermal Modeling Prediction for BEOL and BSPDN Stacks*** *Xinyue Chang - imec/KU Leuven; Herman Oprins, Bjorn Vermeersch, Vladimir Cherman, Melina Lofrano, Seongho Park, Zsolt Tokei, Ingrid De Wolf - imec*
6. 4:25 PM - Novel Inorganic IR Release Process for High Temperature W2W and D2W Integration *Thomas Uhrmann, Peter Urban, Boris Považay, Michael Josef Gruber, Bernd Thallner, Markus Wimplinger - EV Group, Inc.*	***6. 4:25 PM - Design and Fabrication of 2.5D Cryogenic Interposer With Integrated Superconducting TSVs and Resonators*** *King Jien Chui, Hongyu Li - Institute of Microelectronics A*STAR*	***6. 4:25 PM - Analysis of Mechanical Behavior of Hybrid SAC-LTS Joints Under Temperature Cycling With a Modified Garofalo Creep Model Based on Bi Concentration*** *Souvik Chakraborty, Jeff Suhling - Auburn University; Yaxiong Chen, Gaurav Sharma, Abdullah Fahim, Torsten Hauck - NXP Semiconductor, Inc.; Ronit Das, Atif Mahmood, Peter Borgesen - Binghamton University*
7. 4:45 PM - D2W Hybrid Bonding System Achieving High-Accuracy and High-Throughput With Minimal Configurations *Kentaro Mihara, Takashi Hare, Hirofumi Sakai, Shimpei Aoki, Toyoharu Terada - Toray Engineering Co., Ltd.; Mariappan Murugesan, Hiroyuki Hashimoto, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima - Tohoku University; Fumihiro Inoue - Yokohama National University; Akira Uedono - University of Tsukuba*	***7. 4:45 PM - PQC-HI: PQC-enabled Chiplet Authentication and Key Exchange in Heterogeneous Integration*** *Md Sami Ul Islam Sami, Kimia Zamiri Azar, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor - University of Florida*	***7. 4:45 PM - ILD Crack Mechanical Reliability Mitigation*** *Yutaka Suzuki, Williamson Jaimal, Rajen Murugan - Texas Instruments, Inc.*

PROGRAM SESSIONS: THURSDAY, MAY 30, 9:30 A.M. - 12:35 P.M.

Session 13: Next-Generation Substrate Manufacturing Technologies	Session 14: Breakthrough Ultra-Fine Pitch Redistribution Layer and Solder Bumping Technologies	Session 15: Novel Materials and Process for Hybrid Bonding
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: **Markus Leitgeb - AT&S** **m.leitgeb@ats.net** **Kuldip Johal - MKS Instruments- MSD** **kuldip.johal@atotech.com**	**Session Co-Chairs:** **Seung Yeop Kook - GLOBALFOUNDRIES** **seung-yeop.kook@globalfoundries.com** **Wei Zhou - Micron** **zhouwei@micron.com**	**Session Co-Chairs:** **Ivan Shubin - Raytheon Technologies** **ishubin@gmail.com** **Dwayne Shirley - Marvel Semiconductor** **shirley@ieee.org**
1. 9:30 AM - Development of Next-Generation Chemical Mechanical Planarization Process for Panel-Level Heterogeneous Integration *Francoise Angoua, Aaditya Candadai, Daniel Rosales-Yeomans, Yosef Kornbluth, Dilan Seneviratne, Rahul Manepalli - Intel Corporation*	***1. 9:30 AM - A Study on Improvement and Extension of Fine-Pitch Micro-Bump Interconnects Technology: New Metallurgy & Flux-Less Oxide-Removal Laser Assembly (FLOLA)*** *Seok-Geun Ahn, Ju-Hyeon Oh, Gwang-Jae Jeon, Dae-Ho Lee, Seok-Hyun Lee - Samsung Electronics Co., Ltd.*	***1. 9:30 AM - Towards Standardization of Hybrid Bonding Interface: In-Depth Study of Dielectrics on Direct Bonding*** *Yi Yang, Xavier F. Brun - Intel Corporation; Marco Flores - Arizona State University; Marc Weber - Washington State University*
2. 9:50 AM - Dry Processes to Form Fine Features on Advanced Substrates *Wen Xiao, Qin Zhong, Cindy Mora, Anindarupa Chunder, Nicholas Loo, Sik Hin Chi, Cheng Sun, Weihua Qing, Harish V Penmethsa, Craig Rosslee, Jeff Turner - Applied Materials, Inc.*	***2. 9:50 AM - A Novel Copper Microporous-Assisted Bonding Method for Fine-Pitch Cu/Sn Microbump 3D Interconnects*** *Keyu Wang, Shuhang Lyu, Tiwei Wei - Purdue University*	***2. 9:50 AM - Demonstration of Low Temperature Cu-Cu Hybrid Bonding Using a Novel Thin Polymer*** *Yasuhisa Kayaba, Takuo Shikama, Wataru Okada, Kahori Tamura, Yuzo Nakamura, Yutaka Hisamune, Rikia Furusho - Mitsui Chemicals, Inc.*
3. 10:10 AM - Direct Laser Patterning Using Excimer Laser on Polyimide Compositions With Low Dielectric Properties and Good Flexibility for Redistribution Layer *Kanta Wataji, Akira Suwa, Junichi Fujimoto, Yasuhumi Kawasuji - Gigaphoton Inc; Takashi Yamaguchi, Taiyo Nakamura, Takashi Tazaki - Arakawa Chemical Industries, Ltd.; Masaru Sasago - ba2.so-net.ne.jp*	***3. 10:10 AM - Challenges and Innovations in Dual Damascene Polymer RDL With 2 µm Pitch and Beyond*** *Benjamin Briggs, Roger Quon, Chris Bencher, Ryan Ley, C.C. Chuang, Peng Suo, Andy Chang Bum Yong, Luisa Bozano, Jorge Fernandez, Prayundi Lianto, Niranjan Khasgiwale, Siddarth Krishnan - Applied Materials, Inc.*	***3. 10:10 AM - Process Challenges in Thin Wafers Fabrication With Double Side Hybrid Bond Pads for Chip Stacking*** *Dileep Kumar Mishra, Nagendra Sekhar Vasarla, Chandra Rao Bhesetti, Ser Choong Chong, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Aurora 1		
4. 11:15 AM - New Power Delivery Network (PDN) Approach for Extremely Large FC-BGA With Organic Substrate Based on Over 1 mm-Thick Core *Kyojin Hwang, Woobin Jung, Junghwa Kim, Heeseok Lee, Jisoo Hwang, Heejung Choi - Samsung Electronics Co., Ltd.*	***4. 11:15 AM - Void Migration Kinetics in Fine Line Cu RDL Under Electric Current Stressing and the Improvement of Electromigration Reliability by Polyimide Passivation*** *Yen-Cheng Huang, Kwang-Lung Lin - National Cheng Kung University; Min-Yan Tsai, Ting-Chun Lin, Yung-Sheng Lin - Advanced Semiconductor Engineering, Inc. (US); Chih-Pin Hung, Chen-Chao Wang - Advanced Semiconductor Engineering, Inc.*	***4. 11:15 AM - Development of Low Temperature Processable Polyimides for Organic Hybrid Bonding Applications*** *Kota Nomura, Masaya Jukei, Hitoshi Araki, Tomoyuki Honda, Yu Shoji - Toray Industries, Inc.; Takenori Fujiwara - Toray Singapore Research Center*
5. 11:35 AM - X-Ray Photoelectron Spectroscopy (XPS) Investigations to Monitor the Surface Chemistry During Palladium-Free Colloidal Copper Activation *Ibbi Ahmet, André Beyer, Laurence J. Gregoriades, Julia Lehmann, Yvonne Welz - Atotech (MKS Instruments)*	***5. 11:35 AM - Reliable Chiplet Integration on High Density Laminate (2.X D) for AI Hardware*** *Divya Taneja, Jonathan Pouliot-Grenier, Isabel de Sousa - IBM Canada, Ltd.; Joseph Ross, Sathya Raghavan, Griselda Bonilla - IBM Research; Horiyuki Mori - IBM Research, Tokyo; Brian Quinlan Quinlian, Thomas Wassick - IBM Systems*	***5. 11:35 AM - Effect of (111) Surface Ratio on the Bonding Quality of Cu-Cu Joints*** *Huang Jian-Yuan, Chen Chih - National Yang Ming Chiao Tung University*
6. 11:55 AM - Development of Glass Core Substrate With the Stress Analysis, Transmission Characteristics and Reliability *Koji Fujimoto, Yashuhiro Okawa, Takahiro Tai, Satoru Kuramochi - DNP Co., Ltd.*	***6. 11:55 AM - Zero-Misalignment Technology Achieves 333 IO/mm/Layer on Mold*** *Veronica Strong, Trianggono Widodo, Holly Sawyer, Carolyn Aubertine, Aleksandar Aleksov, Johanna Swan - Intel Corporation*	***6. 11:55 AM - Copper Microstructure Optimization for Fine Pitch Low Temperature Cu/SiO2 Hybrid Bonding*** *Marie Maubert, Mathilde Gottardi, Pierre-Emile Philip, Emilie Fragnaud, Gilles Romero, Arnaud Cornelis, Hadi Hijazi - Grenoble Alps University/CEA-LETI; Frank Fournel, Maria-Luisa Calvo-Mu~noz - CEA-LETI*
7. 12:15 PM - High Aspect Ratio (AR) Through Glass Via (TGV) Etch Performance on Glass Core Substrates for High Density 3D Advanced Packaging Applications *Venugopal Govindarajulu, Coby Tao, Zia Karim, Aneelman Brar - Yield Engineering Systems; Sung Jin Kim - Absolics*	***7. 12:15 PM - Additive Manufacturing of High-Density (2.5 µm L/S) Ag-Cu Stacked Interconnects on Organic Substrates*** *Shrivani Pandiya, Serge Ecoffey, Yann Beilliard, Dominique Drouin - University of Sherbrooke; Christophe Sansregret - Centre de Collaboration MiQroInnovation (C2MI); Isabel De Sousa - IBM Canada, Ltd.*	***7. 12:15 PM - Multi-Tier Die Stacking Through Collective Die-to-Wafer Hybrid Bonding*** *Koen Kennes, Ye Lin, Samuel Suhard, Pieter Bex, Dieter H. Cuypers, Alain Phommahaxay, Gerald Beyer, Eric Beyne - imec; Alice Guerrero - Brewer Science, Inc.; Dennis Bumueller - SUSS MicroTec GmbH*

PROGRAM SESSIONS: THURSDAY, MAY 30, 9:30 A.M. - 12:35 P.M.

Session 16: Reliability of High-Density and High-Power Packages	Session 17: Advanced Additive Manufacturing for Printed Electronics and Integrated Systems	Session 18: Radio Frequency Antenna-in-Package and Component Design
Committee: **Applied Reliability**	**Committee:** **Emerging Technologies**	**Committee:** **RF, High-Speed Components & Systems**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: **Scott Savage - Medtronic Microelectronics** **scott.savage@medtronic.com** **Nokibul Islam - JCET Group** **Nokibul.ISLAM@jcetglobal.com**	**Session Co-Chairs:** **Xinpei Cao - Henkel Corporation** **xinpei.cao@henkel.com** **Tengfei Jiang - University of Central Florida** **Tengfei.jiang@ucf.edu**	**Session Co-Chairs:** **Amit P. Agrawal - AMD** **ap_agrawal@yahoo.com** **Sungwook Moon - Samsung** **sw2013.moon@samsung.com**
1. 9:30 AM - Structural Characterization of 2.5D System in Package Combined With High Bandwidth Memory for Enhanced Quality and Reliability *Byoungdo Lee, Jinwoo Choi, Sangyong Lee, Jinwoo Park, Gyujei Lee, Kangwook Lee - SK Hynix, Inc.*	***1. 9:30 AM - Embedded RF Packaging Via Ceramic 3D Printing and Printed Electronics Additive Manufacturing*** *Abdullah Obeidat, Mohammed Abdelatty, Ashraf Umar, Zhi Dou, Firas Alshatnawi, Riadh Al-Haidari, Waleed Al-Shaibani, Mohammed Alhendi, Mark Poliks - Binghamton University; Cathleen Hoel, Jason Case, Joseph Iannotti - GE Aerospace*	***1. 9:30 AM - Design and Simulation Study of 300-GHz Molded Patch Antenna in Packaging Substrate*** *Harshpreet Singh Phull Bakshi, Rajen Murugan, Sylvester Ankamah-Kusi - Texas Instruments, Inc.*
2. 9:50 AM - Reliability Investigations of Advanced Photosensitive Polymer Based RDL Processes Protected by Inorganic Capping Layers *Emmanuel Chery, Nelson Pinho, Eric Beyne - imec; Ritwik Bhatia, Ganesh Sundaram - Veeco*	***2. 9:50 AM - A CMOS Nanosensing System for Continuous Brain Multianalyte Monitoring*** *Yue Gu, Jesus Maldonado Vazquez, De-Shaine Murray, Hitten Zaveri, Dennis Spencer - Yale University*	***2. 9:50 AM - Wideband Antennas on Thin-Film Packaging Substrates for 140 GHz 6G Applications*** *Thi Huyen Le, Michael Phillip Kaiser, Julia-Marie Köszegi, Kavin Senthil Murugesan, Lutz Gerhold, Ivan Ndip, Martin Schneider-Ramelow - Fraunhofer IZM; Habib Hichri - Ajinomoto Fine-Techno USA Corporation; Ryohei Oishi, Reki Nakano - Ajinomoto Co., Inc.*
3. 10:10 AM - Alternative Techniques for Cross-Sectioning and Quality Analysis of Solder-TIM Joints With Soft Indium Alloys *Peter McClure, Daniel VanHart, Ali Davoodabadi - Universal Instruments Corp.*	***3. 10:10 AM - Novel Sub-THz Antenna SoP Modules Enabled by Micrometer-Scale Metal 3D Printing for B5G/6G Applications*** *Genaro Soto Valle Angulo, Kexin Hu, Manos M. Tentzeris - Georgia Institute of Technology*	***3. 10:10 AM - Miniaturized Highly-Efficient Substrate Integrated Waveguide (SIW) Cavity Slot Antenna at 28 GHz Based on Through Fused-Silica Via (TFS) Technologyy*** *Hanna Jang, Payman Pahlavan, Yong-Kyu Yoon - University of Florida*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Exhibition Hall – Aurora 1		
4. 11:15 AM - Fusing Current Characterization of Various Cu RDL Designs in Wafer Level Packages *JeongMin Ju, JiYeon Yoon, EunSook Sohn - Amkor Technology Korea/Amkor Technology, Inc.; Nathan Whitchurch - Amkor Technology, Inc.*	***4. 11:15 AM - Direct-Write NiO RRAM Cells*** *Jordan Howard-Jennings, Riadh Al-Haidari, Emuobosan Enakerakpo, Stephen Gonya, Mohammed Alhendi, Mark Poliks - Binghamton University; Kevin Bell, Tom Rovere - Lockheed Martin*	***4. 11:15 AM - A Compact mmWave 1x4 Antenna Array Design With Shorted Parasitic Elements for 5G AiP Applications*** *Sheng-Chi Hsieh, Cheng-Yu Ho - Advanced Semiconductor Engineering, Inc. (US)*
5. 11:35 AM - Electromigration Failure Mechanisms of Cu-Cu Joints at Low Stressing Temperatures *Shih-Chi Yang - Department of Materials and Science Engineering; Chih Chen - National Yang Ming Chiao Tung University*	***5. 11:35 AM - Micro-3D-Printed Packaging Substrates With Embedded Through Holes for Organic Interposers*** *Nahyeon Kim, Haksoon Jung, Yongwoo Lee, Sungmin Eum, Yechan Han, Jimin Kwon - Ulsan National Institute of Science and Technology; Hyunjin Park - Korea Research Institute of Chemical Technology; Yunsik Park - Korea Electronics Technology Institute*	***5. 11:35 AM - High-Performance Polymer Microwave Fiber Coupler in eWLB Package for Sub-THz Communication*** *Vasileios Liakonis - Infineon Technologies AG/National Technical University of Athens; Yannis Papananos - National Technical University of Athens; Maciej Wojnowski, Walter Hartner - Infineon Technologies AG*
6. 11:55 AM - A Data-Driven Machine Learning Model for the Stress-Strain Behavior of Single Grain SAC305 Solder Joints *Debabrata Mondal, Jeffrey Suhling, Elham Mirkoohi, Pradeep Lall - Auburn University*	***6. 11:55 AM - A Novel Fully Additive Fabrication Approach for Creating Double-Stacked Copper Spiral Inductors*** *Roghayeh Imani, Shailesh Chouhan, Jerker Delsing - Lulea University of Technology; Sarthak Acharya - University of Oulu*	***6. 11:55 AM - RF Modelling and Characterization of TSVs and Inductive Links of Hybrid Bonded Devices*** *Xiao Sun, Chin-Ya Su, Shih-Hung Chen, Soon Aik Chew, Boyao Zhang, Eric Beyne - imec*
7. 12:15 PM - BGA Electromigration Behavior and Why It Has Become the Bottleneck *Riet Labie, Chinmay Nawghane, Dimitrios Tsiakos, Jan Mertens - imec; Wolfgang Sauter, Eric Tremble, Richard Graf - Marvell Technology, Inc.*	***7. 12:15 PM - A Flexible Composite Heat Sink Embedded Ag Microchannels for Potential Flexible Electronic Applications*** *Han Cai, Yongjin Wu, Yanxin Zhang, Yunna Sun, Zhuoqing Yang, Guifu Ding - Shanghai Jiao Tong University; Jiangbo Luo - Shanghai Aerospace Electronic and Communication Equipment Research Institute*	***7. 12:15 PM - Terahertz Metasurfaces on Flex Using Aerosol Jet Printing and a Novel Parylene Lift-off Process*** *Sambit Kumar Ghosh, Ethan Kepros, Yihang Chu, Bhargav Avireni, Brian Wright, Premjeet Chahal - Michigan State University*

PROGRAM SESSIONS: THURSDAY, MAY 30, 2:00 P.M. - 5:05 P.M.

Session 19: 3D Integration Copper-Copper Hybrid Bonding	Session 20: Novel High-Density 3D & Thru-Via Structures and Processes	Session 21: Innovations in Polymer Packaging Materials Committee:
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: John Knickerbocker - IBM Corporation knickerj@us.ibm.com Peng Su - Juniper Networks pensu@juniper.net	Session Co-Chairs: David Danovitch - University of Sherbrooke David.Danovitch@USherbrooke.ca Yoshihsia Kagawa - Sony Yoshihisa.Kagawa@sony.com	Session Co-Chairs: Zhanhming Zhou - Qualcomm zhou.zhming@gmail.com Mark Poliks - Binghamton University mpoliks@binghamton.edu
1. 2:00 PM - A Study of Low Temperature SoIC Targeting 200 nm Bond Pitch *Wei-Ming Wang, C.W. Yeh, Han-Jong Chia, R.F. Tsui, Ji James Cui, Chih-Hang Tung, Kuo-Chung Yee, Douglas C.H. Yu - Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 2:00 PM - Integration of Planarized Nb-Based Vias to Form a Multi-Level Superconducting Back-End-of-Line*** *Candice Thomas, Edouard Deschaseaux, Rémi Vélard, Giovanni Romano, Jean-Philippe Michel, Norman Vivien, Richard Souil, Cassandre Beluffi, Catherine Pellissier, Jean Charbonnier - Grenoble Alps University/CEA-LETI*	***1. 2:00 PM - Novel Sheet Molding Compound Technology for Wafer Level Packaging to Overcome Wafer Warpage Issue*** *Yuki Sugiura, Daisuke Mori, Yasuhito Fujii, Takashi Yagihashi, Eiichi Nomura - Nagase ChemteX Corporation; Kenta Imamura - Nagase America LLC; Ippei Yamai - Nagase & Co., Ltd.*
2. 2:20 PM - Low Resistance and High Isolation HD TSV for 3-Layer CMOS Image Sensors *Stéphan Borel, Myriam Assous, Rémi Velard, Jerzy-Javier Suarez-Berru, Stéphane Nicolas, Jérôme Dechamp, Renan Bouis, Lionel Vignoud, Paul Valentin, Jérémy Marchand, Antonio Roman, Messaoud Bedjaoui - Grenoble Alps University/CEA-LETI*	***2. 2:20 PM - Observation of Thermal Expansion Behavior of Nanotwinned-Cu/ SiO2 & Regular-Cu/SiO2 Hybrid Structure Via In-Situ Heating AFM*** *Huai-En Lin, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute*	***2. 2:20 PM - Development of UV-Curable Molding Materials With Minimum Die-Shift for FOWLP/FOPLP*** *Markus Schindler, Severin Ringelstetter - DELO Industrial Adhesives; Mariana Pires, Mikhail Begel, Andrea Kneidinger, Markus Wimplinger, Thomas Uhrmann - EV Group, Inc.*
3. 2:40 PM - Integrated Hybrid Bonding System for the Next Generation Advanced 3D Packaging *Raymond Hung, Gilbert See, Ying Wang, Chang Bum Yong, Ke Zheng, Yauloong Chong, Avi Shantaram, Ruiping Wang, Arvind Sundarrajan - Applied Materials, Inc.; Nithyananda Hedge, Setfan Schmid, Manfred Glantschnig - Besi NL*	***3. 2:40 PM - 3D Interconnects for Quantum Computing*** *Jaber Derakhshandeh - imec*	***3. 2:40 PM - Temperature-Dependent Dielectric Characterization of Low Loss Thin Film Polymers up to Sub-THz Bands*** *Kavin Senthil Murugesan, Jens Schneider, Michael Kaiser, Julia-Marie Köszegi, Lutz Gerhold, Ivan Ndip, Martin Schneider-Ramelow - Fraunhofer IZM; Habib Hichri, Ryohei Oishi, Reki Nakano - Ajinomoto Fine-Techno USA Corporation*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Aurora 1		
4. 3:45 PM - Process Development and Performance Benefits of 0.64-0.36 µm Pitch Hybrid Bonding on Intel Process *Tushar Talukdar, Adel Elsherbini, Kimin Jun, Brandon Rawlings, Richard Vreeland, William Brezinski, Haris Niazi, Siyan Dong, Yi Shi, Pilin Liu, Xavier Brun, Johanna Swan - Intel Corporation*	***4. 3:45 PM - Laser Micro Drilling of Around 3 Microns into Ajinomoto Build-up Film*** *Toshio Otsu, Shuntaro Tani, Hiroharu Tamaru, Yohei Kobayashi - University of Tokyo; Shoko Nagayama, Ryo Miyamoto - Ajinomoto Fine-Techno Co., Inc.; George Okada - Spectronix Corp., Ltd.; Naoyuki Nakamura, Junichi Nishimae - Mitsubishi Electric Corporation*	***4. 3:45 PM - Low-Temperature Polymer Hybrid Bonding with Nanoparticulated Cu and Photosensitive Acrylic Adhesive*** *Hirokatsu Sakamoto, Tadashi Teranishi, Rumi Nagai, Ryo Itaya, Akihiko Happoya - Daicel Corporation; Hideaki Tamate - T-Micro; Takafumi Fukushima - Tohoku University*
5. 4:05 PM - Methodologies for Characterization of W2W Bonding Strength *Mario Gonzalez, Kris Vanstreels, Oguzhan Orkut Okudur, Serena Iacovo, Eric Beyne - imec*	***5. 4:05 PM - Thermo-Mechanical Reliability Analysis and Raman Spectroscopy Characterization of Sub-micron Through Silicon Vias (TSVs) for Backside Power Delivery in 3D Interconnects*** *Shuhang Lyu, Thomas Beechem, Tiwei Wei - Purdue University*	***5. 4:05 PM - Development of New Concept Photo Imageable Dielectric Materials for Next Generation Advanced Packaging*** *Kazuki Sato, Kazuaki Ebisawa, Makiko Irie, Yiyang Zhan, Atsushi Kubo - Tokyo Ohka Kogyo Co., Ltd.*
6. 4:25 PM - 3.5D Advanced Packaging Enabling Heterogenous Integration of HPC and AI Accelerators *Chandra Sekhar Mandalapu, Chintan Buch, Priyal Shah, Roden Topacio, Patrick Cheng, Liwei Wang, Raja Swaminathan, Alan Smith, John Wuu, Kaushik Mysore, Arsalan Alam - Advanced Micro Devices, Inc.*	***6. 4:25 PM - Organic Interposers Using Zero-Misalignment-Via Technology and Silicon Wafer Carriers for Large Area Wafer-Level Package Applications*** *Alekdandar Aleksov, Tushar Talukdar, Veronica Strong, Holly Sawyer, Carolyn Aubertine, Johanna Swan, Thomas Sounart - Intel Corporation*	***6. 4:25 PM - Development of Thick-Core Substrate Material for Cutting-Edge IC Packaging*** *Tomo Mugurma, Tom Shin - Panasonic Industrial Devices Sales Company of America; Masafumi Honma, Teppei Washio, Yuichi Ishikawa, Yutaka Tashiro, Hirosuke Saito, Jun Yasumoto, Genki Takahashi, Yoshiki Okushima - Panasonic Industry Co., Ltd.*
7. 4:45 PM - Facile Wafer-to-Wafer Hybrid Bonding Integration at Sub 0.5 µm Pitch *Hemanth Kumar Cheemalamarri, San Sandra, Arvind Sundaram, Anh Tran Van Nhat, Chen Gim Guan, Chandra Rao Bhesetti, Steven Lee Hou Jang, Raju Mani, Nandini Venkataraman, King Jien Chui, Srinivasa Rao Vempati, Singh Navab - Institute of Microelectronics A*STAR*	***7. 4:45 PM - Bendability Enhancement and Miniaturization of Through-X Via (TXV) Based on Flexible Fan-Out Wafer-Level Packaging With Additive Tiny Cu Pillar Assembly*** *Atsushi Shinoda, Chang Liu, Akihiro Tominaga, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima - Tohoku University*	***7. 4:45 PM - Development of Magnetic Molding Compound for Low Pressure Molding Inductors With Both Good Magnetic Properties and High Reliability*** *Hiroki Sonokawa, Yoshinori Endo, Mika Tanaka, Takashi Inagaki, Teruo Ito - Resonac Corporation*

PROGRAM SESSIONS: THURSDAY, MAY 30, 2:00 P.M. - 5:05 P.M.

Session 22: Signal & Power Integrity for Advanced Packages and Systems	Session 23: Novel Bonding Technology for Advanced Assembly Substrates and Integration	Session 24: Advances on Flex and Redistribution Layer Technologies and Warpage
Committee: RF, High-Speed Components & Systems	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: Hideki Sasaki - Rapidus hideki.sasaki@rapidus.co.jp Srikrishna Sitaraman - Marvell srikrishna. sitaraman@gmail.com	Session Co-Chairs: Valerie Oberson - IBM voberson@ca.ibm.com Pascale Gagnon - IBM pgagnon@ca.ibm.com	Session Co-Chairs: Ning Ye - Western Digital ning.ye@wdc.com Rui Chen - Eastern Michigan University rchen7@emich.edu
1. 2:00 PM - High Bandwidth and Energy Efficient Electrical-Optical System Integration Using COUPE Technology *Chih-Hsin Lu, Chia-Chia Lin, Tzu-Chun Tang, Chung-Yi Lin, Jay Chang, Chung-Hao Tsai, Harry Hsia, J.C. Twu, C.S. Liu, Gene Wu, Kuo-Chung Yee, Douglas Yu - Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 2:00 PM - Advanced Thermocompression Bonding on High Density Fan-Out Embedded Bridge Technology for HPC/AI/ML Applications*** *Wiwy Wudjud, Lihong Cao - Advanced Semiconductor Engineering, Inc. (US); ShuYu Lin, Yungshun Chang, Jean Yen, Reno Liao, Leo H.S. Cheng, YiHsien Wu, Simon Y.L. Huang, Ivan R.C. Chen, ChengYu Lee, Joey C.I. Huang - Advanced Semiconductor Engineering, Inc.*	***1. 2:00 PM - Accurate Prediction of Solder Stresses/Strains in Multi-Layered Electronics Packages During Temperature Cycling*** *Xuejun Fan, Mukunda Khanal, Jiang Zhou - Lamar University*
2. 2:20 PM - High Frequency Assessment of Djordjevic-Sarkar Model for Low Loss Package Dielectrics *Cemil Geyik, Michael Hill, Zhichao Zhang, Kemal Aygun - Intel Corporation*	***2. 2:20 PM - Various Defect Mechanism Analysis for Optimization of Vacuum Fluxless Solder Reflow Performance Using 10 µm or Below Microbumps*** *Lei Jing, Alvin Lin, Xinxuan Tan, Anderson Chen, Vladimir Kudriavtsev, Lucky Murugesh, Zia Karim - Yield Engineering Systems*	***2. 2:20 PM - Comparison of Sustainable and Non-Sustainable Ink Process-Performance Interactions for Additively Printed Circuits*** *Pradeep Lall, Ved Soni, Sabina Bimali, Daniel Karakitie - Auburn University; Scott Miller - NextFlex*
3. 2:40 PM - System Level Analysis and Design Optimization of Back-Side Power Delivery Network for Advanced Nodes *Kyunghwan Song, Sungwook Moon, Minseok Kang, Yongho Lee, Duhyoung Ahn, Hyeonjin Kim - Samsung*	***3. 2:40 PM - Chip-on-Wafer (CoW) Technology Utilizing Laser-Assisted Bonding With Compression (LABC) for Bump Counts Exceeding 500,000 at a 20 µm Pitch*** *Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Jungho Shin, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ho-Gyeong Yun, Seok Hwan Moon, Ji Eun Jung, Gaeun Lee, Yong-Sung Eom - Electronics and Telecommunications Research Institute*	***3. 2:40 PM - Simulation and Metrological Applications for RDL Patterning Development of Glass Substrate*** *Chang-Chun Lee - National Tsing Hua University; Jui-Chang Chuang - National Tsing Hua University/Industrial Technology Research Institute; Chen-Tsai Yang, Chung-I Li - Industrial Technology Research Institute; Shih-Hsien Lee, Shih-Hao Kuo - Applied Materials, Inc.*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Exhibition Hall – Aurora 1		
4. 3:45 PM - PDN Impedance Optimization of AR/VR Systems: A Trade-off in VRM Bandwidth and Board Decoupling *Wendem Beyene, Ling Jiang, Koichi Yamaguchi, Xiaoping Liu, Ashkan Hashemi - Meta Platforms, Inc.*	***4. 3:45 PM - Novel Molded FCBGA Package Platform for Highly Reliable Automotive Applications*** *Inrack Kim, Nari Kim, Gayoung Shin - Amkor Technology Korea; Youngdo Kweon - Amkor Technology, Inc.*	***4. 3:45 PM - Monitoring of Wafer Thinning Induced In-Die Mechanical Stress With Embedded Sensors for Heterogeneous Integration*** *Alberto Piadena, Michele Quarantelli, Sharad Saxena, Christopher Hess, Larg Weiland, Rakesh Vallishayee, Yuan Yu, Tomasz Brozek, Andrzej Strojwas - PDF Solutions*
5. 4:05 PM - Physical-Based Verification of High-Speed Channel Crosstalk and Correlation with BER Measurements *Po-Wei Chiu, Chao-Chin Lee, Guan-Yu Lin, Jinsung Youn, Youngsoo Lee, Hong Shi, Alan Fang, Santiago Asuncion - Advanced Micro Devices, Inc.*	***5. 4:05 PM - Study of Fabrication and Reliability for 120 mm x 120 mm Extremely Large Advanced 2.5D Package*** *Kazue Hirano, Dongchul Kang, Masaki Takahashi, Takahiro Iseki, Kosuke Murai, Sadaaki Katoh - Resonac Corporation*	***5. 4:05 PM - Investigation of Mechanical Reliability of Flexible/Stretchable Electronic Materials Using Multi-Axial Stretch Techniques*** *Kaushik Godbole, Benjamin Stewart, Suresh Sitaraman - Georgia Institute of Technology; Nicholas Ginga - University of Alabama in Huntsville*
6. 4:25 PM - An Energy Efficient DDR5 I/O Performance Boost in Clamshell Configuration by Charge Pumping From Non-Target Device *Ryuichi Oikawa - Renesas Electronics Corporation*	***6. 4:25 PM - Thin Substrate Bonding*** *Partia Naghibi - HRL Laboratories, LLC*	***6. 4:25 PM - Optimized Simulation Methodology of Warpage and Localized Stress Hotspot Prediction for Assembly Risk Assessment*** *Zhi Yang, Igor Arsovski, Clint Harames, Jim Miller - Groq; Krishna Mellachervu - ANSYS, Inc.*
7. 4:45 PM - Signal Integrity Analysis and Design Optimization Using Neural Networks *Juhitha Konduru, José Schutt-Ainé - University of Illinois; Oleg Mikulchenko, Loke Yip Foo - Intel Corporation*	***7. 4:45 PM - High-Throughput Characterization of Nanoscale Topography for Hybrid Bonding by Optical Interferometry*** *Bongsub Lee, Oliver Zhao, Arianna Avellán, Suhail Sadiq, Gill Fountain, Dominik Suwito, Guilian Gao, Laura Mirkarimi - Adeia*	***7. 4:45 PM - Analyzing the Influence of RDL Stack-Up on Wafer Warpage in FOWLP Through Experimental and Numerical Investigations*** *Saskia Huber, Philipp Scheibe, Sükrücan Mutlu, Olaf Wittler, Martin Schneider-Ramelow - Fraunhofer IZM*

PROGRAM SESSIONS: FRIDAY, MAY 31, 9:30 A.M. - 12:35 P.M.

Session 25: High-Performance Computing, Design Challenges, and Solutions	Session 26: Chiplet Interconnect Design and Validation	Session 27: Advanced Die Bond and Board Level Reliability
Committee: Packaging Technologies	**Committees: Interconnections and RF, High-Speed Components & Systems**	**Committees: Materials & Processing and Assembly & Manufacturing Technology**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: Eric Tremble - Marvell etremble@marvell.com Young-Gon Kim - Renesas Electronics America young.kim.jg@renesas.com	**Session Co-Chairs: Gang Duan - Intel gang.duan@intel.com Jaemin Shin - Qualcomm jaemins@qti.qualcomm.com**	**Session Co-Chairs: Jason Rouse - Taiyo America jhrouse@taiyo-america.com Omkar Gupte - AMD Omkar.Gupte@amd.com**
1. 9:30 AM - An Energy-Efficient Si-Integrated Micro-Cooler for High Power and Power-Density Computing Applications *Yu-Jen Lien, Cheng-Chieh Hsieh, Terry Ku, Li Wang, Po-Ju Chen, Kcyee Yee, C. H. Douglas Yu - Taiwan Semiconductor Manufacturing Company, Ltd.*	***1. 9:30 AM - Impact of Pitch Scaling on 3D Die-to-Die Interconnects*** *Nicolas Pantano, Michele Stucchi, Geert Van Der Plas, Eric Beyne - imec*	***1. 9:30 AM - Impact of Chip-Package Parameters on the Thermomechanical Reliability of High Thermal Die Attach Materials in RF, Power, and Automotive Applications*** *A R Nazmus Sakib, Ruther Ricon - Renesas Electronics America; Jake Eom, Yoshitsugu Kawashima, Kosuke Azuma, Ganesh Tharumalingam, Young Kim - Renesas Electronics Corporation*
2. 9:50 AM - High Power Thermal Test Vehicle With 2-Phase Cooling for AI Datacenters, 5G RAN, and EDGE Compute Nodes *Yang Liu, Nagesh Basavanhally, Mark Earnshaw, Todd Salamon, Rick Papazian, Ting-Chen Hu, Mark Cappuzzo, Rose Kopf, David Apigo, Bob Farah - Nokia Bell Labs*	***2. 9:50 AM - A 32 Gb/s Full Duplex Bi-Directional Transceiver With Crosstalk Cancellation for Chiplet Interconnections*** *Jae-Woo Park, Jung-Hoon Chun - Sungkyunkwan University; Nicolas Pantano, Geert Van Der Plas, Eric Beyne - imec*	***2. 9:50 AM - The Challenges of High-Temperature Lead-Free Solder Paste for Power Discrete Applications*** *Hongwen Zhang, Kyle Aserian, David Hu, Tyler Richmond, Leo Hu - Indium Corporation; Bo Chen, Kaiyuan Zhu, Mary Jane R. Alin - Alpha and Omega Semiconductor Ltd.*
3. 10:10 AM - Block Level and Package Level Thermal Assessment for Back Side Power Delivery Network *Melina Lofrano, Herman Oprins, Vladimir Cherman, Liesbeth Witters, Anne Jourdain, Geert Van der Plas, Eric Beyne - imec*	***3. 10:10 AM - Modeling and Analysis of Heterogeneously Integrated Chiplet-to-Chiplet Communication Link in 2.5D Advanced Packaging*** *Haofeng Sun, Bobi Shi, Thong Nguyen, Jose Schutt-Aine - University of Illinois*	***3. 10:10 AM - Reliability Analysis of Cu Sintered Die-Attach for SiC Power Devices: Mechanical, Electrical, and Thermal Evaluation*** *Xu Liu, Shaogang Wang, Dong Hu, Paddy French, Guoqi Zhang - Delft University of Technology; Chenshan Gao, Qianming Huang, Huaiyu Ye - Southern University of Science and Technology*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Aurora, Crest, and Summit Foyers		
4. 11:15 AM - CoaxMIL 2.0 – Next Generation Coaxial Magnetic Integrated Inductors for Higher Efficiency Fully Integrated Voltage Regulator *Beomseok Choi, Jaeil Baek, Brandon Marin, Shuren Qu, Siddharth Kulasekaran, Jose Chavarria, Leigh Wojewoda, Kaladhar Radhakrishnan - Intel Corporation*	***4. 11:15 AM - Signal, Power and Thermal Co-Optimization Methodology for FPGA Advanced Package*** *Wei Liu, Guang Chen, Brian Wang, Jenny Xiaohong Jiang, Ed Milligan - Intel Corporation*	***4. 11:15 AM - Complex Board Via Structure Induced Uneven Stress/Strain Impact on Interconnect Stability: SAC305, Full and Hybrid LTS Comparison*** *Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna - Cisco Systems, Inc.; Jonghyun Nam, Daljin Yoon, Heera Roh - SK Hynix, Inc.*
5. 11:35 AM - Integrated Design Ecosystem for Chiplets Heterogeneous Integration and Chip-to-Chip Interconnects in Advanced Packaging Technology *Lihong Cao - Advanced Semiconductor Engineering, Inc. (US); Chen-Chao Wang, Chih-Yi Huang, Hung-Chun Kuo - ASE Corporate R&D Center*	***5. 11:35 AM - An Advanced Packaging Figure of Merit (AP-FoM) for Benchmarking of Heterogeneous Integration Technologies*** *Chuei-Tang Wang, Shu-An Shang, Yu-Ming Hsiao, Mirng-Ji Lii, Kam Heng Lee, Jun He - Taiwan Semiconductor Manufacturing Company, Ltd.*	***5. 11:35 AM - Mitigating Solder Beading in Non-Eutectic Low-Temperature Solder: Mechanism and Solution*** *Lip Teng Saw, Mutharasu Devarajan - Western Digital Corporation; Puurnaraj A/L Nadarajah, Chye Yang Soo - Western Digital*
6. 11:55 AM - Thermal and Mechanical Simulations of 3D Packages With Custom High Bandwidth Memory (HBM) *Kamalika Chatterjee, Yan Li, Pouya Asrar, WooPoung Kim - Samsung Semiconductor, Inc.*	***6. 11:55 AM - Signal Integrity Designs at Organic Interposer CoWoS-R for HBM3-9.2Gbps High Speed Interconnection of 2.5D-IC Chiplets Integration*** *Sheng-Fan Yang, Wei-Chiao Wang, Yi-Tzeng Lin, Chih-Chiang Hung, Hao-Yu Tung, Justin Hsieh - Global Unichip Corporation*	***6. 11:55 AM - Thermal Aging Reliability of Socketable BGA Packages With Bi-Au-Coated Sn Spheres*** *Jaewon Lee, Vanessa Smet - Georgia Institute of Technology*
7. 12:15 PM - A Novel DC-DC Converter Module Using the Integrated Package Solution (iPaS) Substrate for Next Generation High Performance Computing (HPC) Applications *Shuhei Yamada, Nobuyoshi Adachi, Kazuki Itoyama, Tatsuya Kitamura, Koshi Himeda, Atsushi Yamamoto - Murata Manufacturing Co., Ltd.; Keito Yonemori - Murata Electronics North America, Inc.*	***7. 12:15 PM - Effective Interface Simulation Approach Based on Peak Distortion Analysis for UCIe IPs*** *Joonhyun Kim, Seungki Nam, Sungwook Moon, Taeyun Kim, Sangin You, Chanmin Jo, Yongho Lee - Samsung Electronics Co., Ltd.*	***7. 12:15 PM - Develop New Solder Alloy for High Reliability Device*** *Albert T. Wu, Wei Ting Lin - National Central University; Watson Tseng, Chang-Meng Wang - Shenmao Technology, Inc.*

PROGRAM SESSIONS: FRIDAY, MAY 31, 9:30 A.M. - 12:35 P.M.

Session 28: Optical Interconnections	Session 29: Reliability in Harsh Environments Including Automotive	Session 30: Process and Hybrid Bonding Modeling and Characterization
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: Ping Zhou - LDX Optronics pzhou@ldxoptronics.com Masao Tokunari - IBM tokunari@jp.ibm.com	**Session Co-Chairs: Varughese Mathew - NXP Semiconductors varughese.mathew@nxp.com Tae-Kyu Lee - Cisco Systems taeklee@cisco.com**	**Session Co-Chairs: Pradeep Lall - Auburn University lall@auburn.edu Xuejun Fan - Lamar University xuejun.fan@lamar.edu**
1. 9:30 AM - Fiber Array Attach for Co-Packaged Optics: High-Volume Production Process Control and Performance *Paul Gond-Charton, Sebastien Gouin, Steve Pellerin, Louis-Michel Collin, Michelle Sevigny, Patrick Jacques, Elaine Cyr - IBM Canada, Ltd.*	***1. 9:30 AM - Transitioning From Warpage "Control" to Warpage "Design": A Paradigm Shift*** *Sukrut Prashant Phansalkar, Bongtae Han - University of Maryland*	***1. 9:30 AM - Modeling of Copper Hybrid Bonding Anneal*** *Joshua Hooge, Chris Netzband - Tokyo Electron, Ltd.*
2. 9:50 AM - Photonic Building Blocks for Board-Level Disaggregation in Hyperscale Systems *Richard Pitwon - Resolute Photonics, Ltd.; Bernard Lee, Tiger Ninomiya, Michael O'Farrell - Senko Advance Components*	***2. 9:50 AM - Under Bump Metallization and the Stability of Solder Interconnect Assembly under Thermal and Electrical Load: Refreshed Understanding*** *Hariram Mohanram - University of Texas, Arlington; Choong Un Kim - United Test and Assembly Center, Ltd.; Patrick Thompson, Qiao Chen, Sylvester Kusi - Texas Instruments, Inc.*	***2. 9:50 AM - Investigating Sintering Mechanism of 100 nm Ag Nanoparticles via In-Situ SEM Observation and Phase Field Simulation*** *Xiao Hu, Dong Hu, Willem Van Driel, Guoqi Zhang - Delft University of Technology; René Poelma - Nexperia; Jianlin Huang - Ampleon B.V.*
3. 10:10 AM - Interfacing Silicon Photonics for CPO *Geert Van Steenberge, Jef Van Asch, Viktor Geudens, Toon De Baere, Nele De Moerlooze, Jeroen Missinne - imec/ Ghent University; Joris Van Campenhout - imec*	***3. 10:10 AM - Additively Printed In-Mold Electronics Circuits and Sensors and Process-Performance Interactions for Automotive Applications*** *Pradeep Lall, Hyesoo Jang, Ved Soni, Fatahi Musa, Md Golam Sarwar - Auburn University; Scott Miller - NextFlex*	***3. 10:10 AM - Elucidating the Mechanism of Four Corner Voids in Chip-on-Wafer Hybrid Bonding*** *Takaaki Hirano, Tatsumasa Hiratsuka, Hirotaka Yoshioka, Naoki Ogawa, Suguru Saito, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation*
Refreshment Break: 10:30 a.m. - 11:15 a.m. – Aurora, Crest, and Summit Foyers		
4. 11:15 AM - High Power Performance Assessment of Low-Loss Spot Size Converter based on Self-Aligned Passive Fiber Attach Process *Arpan Dasgupta, Jae Kyu Cho, Yusheng Bian, Takako Hirokawa, Zahidur Chowdhury, Farid Barakat, John Garant, Yarong Lin, Thomas Houghton, Arman Najafi, Ryan Sporer, Michelle Zhang - GlobalFoundries, Inc.*	***4. 11:15 AM - Enhancing Cu Wire-Bonding Reliability by a Cu-Selective Passivation Coating*** *Dinesh Kumar Kumaravel, Logan Estridge, Kevin Antony Jesu Durai, Khanh Tran, Oliver Chyan - University of North Texas; John Alptekin - Texas Instruments, Inc.; Varughese Mathew - NXP Semiconductor, Inc.*	***4. 11:15 AM - Fan-Out Embedded Bridge Structure for Co-Packaged Optics Characterization and Evaluation*** *Vito Lin, Teny Shih, Andrew Kang, Yu-Po Wang - Siliconware Precision Industries Co., Ltd.*
5. 11:35 AM - A Compact, High Performance Passive Optical Network Transceiver Integration Approach *Mark Earnshaw, Cris Bolle, Robert Farah, Rose Kopf, Mark Cappuzzo, Tzu-Yung Huang, Cuong Tran, Tam Huynh - Nokia Bell Labs*	***5. 11:35 AM - High Acceleration Dynamic Methodology for Board-Level Shock Solder Joint Reliability Approach*** *Min-Cheng Yu, Nan-Yi Wu, Wu-Lung Wang, Hsin-Chih Shih, Wei-Hong Lai, Chin-Li Kao, Chen-Chao Wang - Advanced Semiconductor Engineering, Inc.; CP Hung - Advanced Semiconductor Engineering, Inc. (US)*	***5. 11:35 AM - Advanced Atomic-Scale Insights Into the Chemical Mechanical Polishing Process With Ceria Abrasives Using Molecular Dynamics and Neural Network Potential*** *Yoshishige Okuno, Teruo Hirakawa, Fukiko Ota, Hiromu Kubo, Yuuto Kurata, Akihiro Orita, Satoyuki Nomura - Resonac Corporation*
6. 11:55 AM - Characterization of 224 Gbps/lambda Interconnects in Co-Packaged Optics for Hyperscale Data Centers and AI/ ML Clusters *Jiaqi Wu, Teck Guan Lim, Sajay Bhuvanendran Nair Gourikutty, Surya Bhattacharya - Institute of Microelectronics A*STAR; Xin Li, Jason Tsung-Yang Liow - Rain Tree Photonics Pte. Ltd.*	***6. 11:55 AM - Thermomechanical Degradation of Sintered Copper Under High-Temperature Thermal Shock*** *Paul Paret, Sreekant Narumanchi - National Renewable Energy Laboratory; Sri Krishna Bhogaraju - CuNex GmbH; Dirk Busse, Alexander Dahlbüdding - Budatec GmbH; Gordon Elger - Technical University of Applied Science Ingolstadt*	***6. 11:55 AM - Finite Element Modeling for Wafer-to-Wafer Direct Bonding Behaviors and Alignment Prediction*** *Kyungmin Baek, Min-soo Han, Il Young Han, Jung Shin Lee, Jaeuk Sim, Joongha Lee, Daeho Min, Kyeongbin Lim - Samsung Electronics Co., Ltd.; Minwoo Daniel Rhee - Samsung*
7. 12:15 PM - Hybrid Integrated Chip-Scale Laser Systems Based on Automated Assembly *Xiaolei Zhao, Taylor Levaur, Lance Sweatt, Md. Arefin Islam, Lin Zhu - Clemson University*	***7. 12:15 PM - Solder Reaction with Cu Alloy C7025 and Its Effect on Solder Joint Reliability*** *Kejun Zeng, Venu Chauhan, Lance Wright - Texas Instruments, Inc.*	***7. 12:15 PM - Measurement of the Interfacial Strength of Thin Metal Film by Laser Spallation Method for Advanced Wafer Level Package*** *Young-Min Ju, Jin-Young Kim, Hui-Jin Um, Se-Min Lee, Dukyong Kim, Woong-Kyoo Yoo, Seung Hwan Lee, Hak-Sung Kim - Hanyang University; Daewoong Lee, Yeontaek Hwang - SK Hynix, Inc.*

PROGRAM SESSIONS: FRIDAY, MAY 31, 2:00 P.M. - 5:05 P.M.

Session 31: Advances in Flip Chip and Chip Scale Packages	Session 32: Advancement in Copper Hybrid Bonding Technologies Common to Multiple Applications	Session 33: Fine-Pitch Materials and Processes
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Aurora B	**Aurora D**	**Crest 3-5**
Session Co-Chairs: **Luu Nguyen - Psi Quantum** **lnguyen@psiquantum.com** **Glenn Ning Ge - TetraMem** **greene.ge@gmail.com**	**Session Co-Chairs:** **Thom Gregorich - Infinera** **tmgregorich@gmail.com** **Vempati Srinivasa Rao - IME A-star** **vempati@ime.a-star.edu.sg**	**Session Co-Chairs:** **Praveen Pandojirao-S - Johnson & Johnson** **praveen@its.jnj.com** **Bo Song - HP Inc.** **bo.song@hp.com**
1. 2:00 PM - New Double Sided Molded Package Platform Development With Open Cavity Mold on One Side and Exposed Die Mold on the Other Side *MiKyeong Choi, HoSeung Seo, SeMin Gim, GyeongCheol Lee, JungHoon Na, GaHyeong Hwang, WonBae Bang, KiDong Sim, WonChul Do, KyungRok Park - Amkor Technology Korea; Ted Adlam, Jeff Davis - Amkor Technology, Inc.*	***1. 2:00 PM - A Microstructural Investigation of Sub-1 µm Copper Bonding Contact Structures in Die-to-Wafer Hybrid Bonding*** *Sari Al Zerey, Junghyun Cho - State University of New York at Binghamton; Roy Yu, Katsuyuki Sakuma - IBM Research*	***1. 2:00 PM - The Patterned Photosensitive Dielectric Organic Material/Cu Simultaneous Novel CMP Process for Fine Damascene RDL Based on Process Design Assisted by Deep Learning*** *Toshiaki Tanaka, Masaaki Yasuda, Takeyasu Saito, Masaru Sasago, Yoshihiko Hirai - Osaka Metropolitan University; Hideaki Nishizawa - Doi Laboratory, Inc.; Toshiro Doi - Doi Laboratory Inc.; Mitsuru Ozono, Hiroaki Kimuro, Hisatoshi Hirai - Advanced Industrial Science and Technology, Kyushu Center; Seiji Takahashi, Yoichi Minami - Lithotech Japan Corp.*
2. 2:20 PM - Package Miniaturization and Wiring Impedance Reduction for High-Bandwidth Memory Devices With Vertical Wire Bonding *Keita Mochizuki, Hiroyuki Wakioka, Tsutomu Fujita, Masatoshi Shomura, Takeori Maeda, Toshihiko Ohda, Yoshitaka Muto, Eiji Takano, Masahiro Inohara - KIOXIA Corporation*	***2. 2:20 PM - Low-Temperature Cu-Cu Bonding Using <111>-Oriented and Nanocrystalline Hybrid Surface Grains*** *Chen-Ning Li, Jia-Juen Ong, Shih-Chi Yang, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute*	***2. 2:20 PM - Novel Negative-Tone Dry Film Resist and Process for Fine Pitch Copper Wiring With L/S = 1.5/1.5 µm on Build-Up Substrate*** *Kei Togasaki, Natsuki Toda, Kensuke Yoshihara, Yosuke Kaguchi, Kanako Funai, Hitoshi Onozeki, Kenichi Iwashita - Resonac Corporation*
3. 2:40 PM - Ultra-Thin Double Side SiP Technology With Embedded Trace Substrate *Chehan (Jerry) Li, Jesus Mennen Belonio, Jon Gutierrez, Humi (Shih-Wen) Tang, Jessie (Yu-Shan) Wei - Renesas Electronics Corporation*	***3. 2:40 PM - Copper Microstructure Effect on Electromigration Investigated by In Situ SEM EBSD Technique*** *Yaqian Zhang, Sten Vollebregt, Guoqi Zhang - Delft University of Technology*	***3. 2:40 PM - 20 µm Pitch Cu-to-Cu Flip-Chip Interconnects Through Cu Nanoparticles Sintering*** *Xinrui Ji, Leiming Du, Henk van Zeijl, Guoqi Zhang - Delft University of Technology; Jaber Derakhshandeh, Eric Beyne - imec*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Aurora, Crest, and Summit Foyers		
4. 3:45 PM - High Accuracy Selective Patterning for EMI Shielding of 5G AiP *Ming-Hung Chen, Huei-Pin Chien, Yi-Chun Chou, Yu-Shuan Tsai, Kuan-Lin Kuo, Jei-Chieh Kao - Advanced Semiconductor Engineering, Inc. (US)*	***4. 3:45 PM - Achieving Sub-nm Copper Recess Controllability for Advanced 3D Integration: An Experimental and Atomic-Scale Simulation Study on Wet Atomic Layer Etching Process*** *Seung Ho Hahn, Wooyoung Kim, Bumki Moon, Minwoo Rhee - Samsung Electronics Co., Ltd.-Mechatronics Research; Kyeongbin Lim - Samsung Electronics Co., Ltd.*	***4. 3:45 PM - Ultra High Density RDL Patterning of High-Resolution Dielectrics by Maskless Exposure Technology for High Performance Computing and Artificial Intelligence*** *Ksenija Varga, Thomas Uhrmann, Roman Holly, Tobias Zenger - EV Group, Inc.; Dimitri Janssen, Niels Van Herck, Mario Reybrouck, Marieke Vandevyvere, Stefan Vanclooster - Fujifilm Electronic Materials Europe; Sanjay Malik - Fujifilm Electronic Materials*
5. 4:05 PM - Analysis of Thin Flip Chip Chip-Scale Package Warpage Causes and Variations *Chee S Foong, Nishant Lakhera, Trent Uehling - NXP Semiconductor, Inc.; Amirul Afripin - NXP Malaysia Sdn. Bhd.*	***5. 4:05 PM - Quantifying the Electrical Impact of Bonding Misalignment for 0.5 µm Pitch Hybrid Bonding Structures*** *Kevin Ryan, Christopher Netzband, Andrew Tuchman, Scott Lefevre, Ilseok Son, Hirokazu Aizawa, Kaoru Maekawa - TEL Technology Center, America, LLC; Nathan Ip - Tokyo Electron America, Inc.*	***5. 4:05 PM - Novel Photo Imageable Film for RDL Application*** *Meiten Koh, Kazuyoshi Yoneda, Kazutaka Nakada, Yuna Kawata, Yusuke Naka, Mitsuya Uchida - Taiyo Ink Mfg. Co., Ltd.*
6. 4:25 PM - Large Package Body Size Scaling With Two Novel Technologies: Multi Ball BGA and Liquid Metal Interconnect *Xiao Lu - Intel Corporation*	***6. 4:25 PM - Liquid Surface Tension-Driven Chip Self-Assembly Technology With Cu-Cu Hybrid Bonding for High-Precision and High-Throughput 3D Stacking of DRAM*** *Zehua Du, Tetsu Tanaka, Takafumi Fukushima - Tohoku University; Hiroshi Kikuchi, Hayato Hishinuma - YAMAHA ROBOTICS HOLDINGS CO., LTD.*	***6. 4:25 PM - Cu Nanowire Fine-Pitch Joints for Next Gen Heterogeneous Chiplet Integration*** *Steffen Bickel, Iuliana Panchenko, Manuela Junghaehnel - Fraunhofer IZM; Olav Birlem, Sebastian Quednau - Nanowired GmbH*
7. 4:45 PM - A Study About Direct Laser Reflow for Forming Stable and Reliable C4 Bump Interfaces on Semiconductor Substrates for Flip Chip Applications *Matthias Fettke, Anne Fisch, Alexander Frick, Georg Friedrich, Thorsten Teutsch - Pac Tech GmbH*	***7. 4:45 PM - Wafer-On-Wafer-On-Wafer (WoWoW) Integration Having Large-Scale High Reliability Fine 1 µm Pitch Face-To-Back (F2B) Cu-Cu Connections and Fine 6 µm Pitch TSVs*** *Masaki Haneda, Yukako Ikegami, Kengo Kotoo, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation*	***7. 4:45 PM - High-Planarity, Ultra-Low-Temperature-Curable Photosensitive Polyimide for Heterogeneous Integration*** *Atsutaro Yoshizawa, Akira Asada, Daisaku Matsukawa, Takahiro Tanabe - HD MicroSystems LLC*

PROGRAM SESSIONS: FRIDAY, MAY 31, 2:00 P.M. - 5:05 P.M.

Session 34: Photonics Integration, Materials, and Processes	Session 35: Reliability and Current Stressing of Solder Interconnections	Session 36: Thermal Management and Cooling Solutions
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Summit 8-9	**Summit 6-7**	**Summit 4-5**
Session Co-Chairs: **Takaaki Ishigure - Keio University** **ishigure@appi.keio.ac.jp** **Mark Earnshaw - Nokia** **mark.earnshaw@nokia-bell-labs.com**	**Session Co-Chairs:** **Paul Tiner - Texas Instruments** **p-tiner@ti.com** **Pei-Haw Tsao - Mediatek** **ph.tsao@mediatek.com**	**Session Co-Chairs:** **Patrick McCluskey - University of Maryland** **mcclupa@umd.edu** **Chris Bailey - Arizona State University** **christopher.j.bailey@asu.edu**
1. 2:00 PM - Packaged Tunable Single Mode III-V Laser Hybrid Integrated on a Silicon Photonic Integrated Chip Using Photonic Wire Bonding *Venkatesh Deenadayalan, Eric Thornton, Mario Ciminelli, Stefan Preble - Rochester Institute of Technology; George T. Nelson, Peter McGarvey - AIM Photonics; Justin Bickford - US Army Research Lab; Matthew Mitchell, Lukas Chrostowski, Sudip Shekhar - Dream Photonics; Juned N. Kemal, Sebastian Tobias Skacel - Vanguard Automation*	***1. 2:00 PM - Electromigration in Eutectic Tin-Bismuth Bottom-Terminated-Component Solder Joints*** *Prabjit Singh, Larry Palmer, Mehdi Hamid, Thomas Wassiac - IBM Corporation; Raiyo Aspandiar, Brian Franco - Intel Corporation; Haley Fu - iNEMI; Richard Coyle - Nokia Corporation; Vasu Vasudvan - Dell, Inc.; Aileen Allen - HP Inc.; Keith Howell - Nihon Superior Co.; Kei Muryayama - Shinko Electric Industries Co., Ltd.*	***1. 2:00 PM - Electrical-Thermal Analysis of TSV Embedded Microfluidic Pin-Fin Heatsink in 3D IC for High Heat Dissipation With High Bandwidth Density and Low Latency*** *Euichul Chung, Geyu Yan, Erik W. Masselink, Muhannad S. Bakir - Georgia Institute of Technology*
2. 2:20 PM - Collective Die-to-Wafer Assembly Process for Optically Interconnected System-on-Wafer *Koen Kennes, Anton Dvoretskii, Arnita Podpod, Pengfei Xu, Junwen He, Guy Lepage, Negin Golshani, Rafal Magdziak, Yoojin Ban, Filippo Ferraro, Andy Miller, Joris Van Campenhout - imec*	***2. 2:20 PM - Impact of Current Induced Joule Heating Variation on Long-Term Low Melting Temperature Solder Joint Stability*** *Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna - Cisco Systems, Inc.; Young-Woo Lee, Hui-Joong Kim, Seul-Gi Lee - MK Electron Co., Ltd.; Pushkar Gothe, Choong-Un Kim - University of Texas, Arlington*	***2. 2:20 PM - Thermal Mitigation Strategy for Backside Power Delivery Network*** *Feifan Xie, Tiwei Wei - Purdue University; Rongmei Chen - Peking University*
3. 2:40 PM - A Compact Wafer-Level Heterogeneously Integrated Scalable Optical Transceiver for Data Centers *Sajay Bhuvanendran Nair Gourikutty, Jiaqi Wu, Teck Guan Lim, Lai Yee Chia, Ser Choong Chong, Surya Bhattacharya - Institute of Microelectronics A*STAR; Liang Ding, Ronson Tan, Nagarajan Radhakrishnan - Marvell Semiconductor, Inc.; Xiaoguang Tu, Wanjun Wang, Chee-Keong Tan - Marvell Asia Pte Ltd*	***3. 2:40 PM - Reliability Concerns Due to Changes in the Microstructure and Electrical Resistance of Low Temperature, SnBi-Based Solder Joints During Current Stressing*** *Eric Cotts, Sitaram Panta, Eric Cotts, Babak Arfaei, Faramarz Hadian - State University of New York at Binghamton*	***3. 2:40 PM - Thermal Management of 6-in-1 SiC Power Module With Double-Sided Impingement Cooling*** *Yong Han, Gongyue Tang - Institute of Microelectronics A*STAR*
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Aurora, Crest, and Summit Foyers		
4. 3:45 PM - Scalable Fabrication of 3D Optical Redistribution for Co-Packaged Optics Using an Originally-Developed Nanoimprint Stepper *Fumi Nakamura, Kenta Suzuki, Akihiro Noriki, Satoshi Suda, Takayuki Kurosu, Takeru Amano - National Institute of Advanced Industrial Science and Technology*	***4. 3:45 PM - The Effect of Extended Dwell Time on Thermal Cycling Performance of Hybrid Low Temperature Solder Joints*** *Richard Coyle, Chloe Feng, Richard Popowich - Nokia Bell Labs; Martin Anselm - Rochester Institute of Technology*	***4. 3:45 PM - Thermal Performance of an Indium-Silver Alloy Metal TIM for a Large Body Lidded FCBGA After EOL and Long-term Reliability Tests*** *SangHyuk Kim, EunSook Sohn, KyungRok Park - Amkor Technology Korea; YoungDo Kweon - Amkor Technology, Inc.*
5. 4:05 PM - Laser Attach Process Development and Material Selection *Alexander Janta, Pascale Gagnon, Eric Turcotte, Elaine Cyr, Jason Zheng - IBM Corporation*	***5. 4:05 PM - Correlation of Mechanical and Microstructural Evolutions in Lead Free Solders Subjected to Various Thermal Exposures*** *Mohammad Al Ahsan, S M Kamrul Hasan, Souvik Chakraborty, Jeffrey Suhling, Pradeep Lall - Auburn University*	***5. 4:05 PM - AI-Driven Cold Plate Design and Optimization*** *Yue Wu, Eric Chu, Fiona Shiau, Nathan Ai, Albert Zeng, Hoa Pham - Cadence Design Systems*
6. 4:25 PM - Ultra-Compact Computing at the Edge Involving Unobtrusively Small Sub-Millimeter Heterogeneous Integration Packaging *Frank Libsch, Steve Bedell, Cyril Cabral, Arun Paidimarri, Chitra Subramanian, Seiji Munetoh - IBM Research*	***6. 4:25 PM - Pad Cratering and Pin Pull Strength for Large BGA and Connectors — How Are They Correlated?*** *Dongji Xie, Joe Hai, Vivienne Zou, Zhongming Wu, Minghong Jian - Nvidia Corporation*	***6. 4:25 PM - Heat Dissipation Measurement in Flip-Chip Package Using Microfabricated Temperature Sensors on Lid*** *Ars`ene Guédon, Nizar Bouguerra, Étienne Paradis, Dominique Drouin - University of Sherbrooke; Éric Duchesne, Stéphanie Allard - IBM Canada, Ltd.; Hél`ene Frémont - University of Bordeaux*
7. 4:45 PM - Sintering for High Power Optoelectronic Devices *Gordon Elger, Nihesh Mohan, Alberto Siligardi, Hamza Bin Aqeel, Hannes Schwan, Rocky Kumar Saha, Fabian Steinberger - Technical University of Applied Science Ingolstadt; Sri Krishna Bhogaraju, Rohan Ghosh - CuNex GmbH; Holger Klassen, Klaus Müller - ams OSRAM Group*	***7. 4:45 PM - Board Level Drop Reliability of Hybrid Solder Joints With Controlled Bismuth Mixing Ratio for Carbon Neutrality*** *Seahwan Kim, Jaejun Yoon, Taejoon Noh, Seung Boo Jung - Sungkyunkwan University; Kyung Deuk Min - Samsung Electronics Co., Ltd.*	***7. 4:45 PM - Innovative Two-Phase Immersion Cooling Solutions for High-Power Advanced Packages*** *Sumit Sharma, Aqbal Ahmad, Chi-Chuan Wang - National Yang Ming Chiao Tung University; ICheng Huang, Ying-Xu Lu, Hung-Hsien Huang, Chen-Chao Wang, Chih-Pin Hung - Advanced Semiconductor Engineering, Inc. (US)*

Wednesday May 29th

Session 37: Thermo-mechanical Stress and Reliability Analysis for Materials in Future Packaging

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Aurora A-C Corridor

Session Co-Chairs:
Mark Poliks - Binghamton University
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Jeffrey Lee - Integrated Service Technology Inc.
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Joshua Dillon - Marvell
jdillon@marvellgs.com

Venkata Mokkapati - AT&S
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1. Investigating the Adhesion Between Glass Core and Polymer Buildup Films
Preeya Kuray, Yoji Nakajima, Junko Konishi - AGC, Inc.

2. Long-Term Reliability Analysis of Crystal Oscillator Under Immersion Cooling With Various Coolants
Yangfan Zhong, Dan Liu, Fangzhi Wen, Honghao Cao - Alibaba Group; Tina Bao, Kai Wang - Intel Corporation

3. Impact of Bi-Content on the High Strain Rate Properties of SnAgCu Solders Under Sustained High-Temperature Operation
Pradeep Lall, Vishal Mehta, Mrinmoy Saha, Jeff Suhling - Auburn University; David Locker - US Army

4. Bond-Line Thickness Prediction for Thermal Interface Material Under Usage Conditions
Yangyang Lai, Jlefeng Xu, Karthik Deo, Jonghwan Ha, Junbo Yang, Seungbae Park - Binghamton University

5. Cu/Dielectric Hybrid Bonding Among Glass and Si
Hemanth Kumar Cheemalamarri, Arvind Sundaram, Anh Tran Van Nhat, Chen Gim Guan, Jae Ok Yoo, Vempati Srinivasa Rao, Navab Singh - Institute of Microelectronics A*STAR

6. Multiphysics Overlay Modeling of Monolithic 3D Fusion and Hybrid Bonding Processes
Christian Mühlstätter, Lukas Koller, Markus Wimplinger, Viorel Dragoi - EV Group, Inc.

7. Mitigating Cracking From RDL Stress in Glass Substrates With Low-CTE Electrodeposited Copper-Graphene Composites
Christian Molina-Mangual, Emanuel Torres-Surillo, Nithin Nedumthakady, Vanessa Smet - Georgia Institute of Technology

8. A Predictive Methodology for BGA Solder Joint Formation and Assembly Defects
Matt Bond, Mudasir Ahmad, Jin Kim, Sue Teng, Nima Shahidi, Yingshi Tang - Google

9. High-Performance Thermal and Electrical Characteristics of Via-Last (BBCube) Process in Multi-Layer 3D Integration
Norio Chujo - Hitachi, Ltd.; Hiroyuki Ryoson, Koji Sakui, Shinji Sugatani, Masao Taguchi, Takayuki Ohba - Tokyo Institute of Technology

10. Embedded Liquid Cooling of High-Power Microelectronics Using Liquid Metal
Huicheng Feng, Bin He, Gongyue Tang, Xiaowu Zhang, Boon Long Lau, Jason Au, Javier Ong, Ming Chinq Jong, King Jien Chui - Institute of Microelectronics A*STAR

11. A Development of Sensorized Ear Model for New Behind-The-Ear (BTE) Hearing Aid
Maria Ramona Ninfa Bautista Damalerio, Wei Da Toh, Ruiqi Lim, Ming-Yuan Cheng - Institute of Microelectronics A*STAR

12. Electrical Characterization and Reliability Studies of Nano-TSV
Ya-Ching Tseng, Daniel Lau, Simon Chun Kiat Goh, King Jien Chui - Institute of Microelectronics A*STAR

13. A Simulation-Led Board Level Reliability Assessment of High Speed Printed Circuit Boards for Advanced Networking Applications
Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Glasauer - Juniper Networks; Vishnu Shukla, Andrea Molina, Tengfei Jiang - University of Central Florida

14. Thermal Resistance Prediction Model for IC Packaging Optimization and Design Cycle Reduction
Guan-Wei Chen, Chung-Hsiang Hsu, Hung-Kai Wang, Yan-Cheng Lin - National Cheng Kung University; Tang-Yuan Chen, Chen-Chao Wang - Advanced Semiconductor Engineering, Inc.

15. Study of Stress and Warpage Estimate of FOWLP Under Hygro-Thermal Coupling Loading Condition
Yu-Wei Huang - Industrial Technology Research Institute; Ruchi A. K. Yadav, Hong-Yu Lin, Jian-Han Li, Chang-Chun Lee - National Tsing Hua University

16. Single and Multi NPU Chiplet Heterogeneous Integration Packaging Based on Fan-Out RDL Interposer With Silicon Bridge Technology
Insoo Kang, Jacinta Aman Lim - nepes Corporation

17. Thermal Transport Properties of Hybrid Bonding With Passivation
Hakjun Kim, Jae Young Hwang, Young-Chang Joo, Hyejin Jang - Seoul National University; Sangwoo Park, Sarah Eunkyung Kim - Seoul National University of Science and Technology

18. Optimization of Core Material Properties for Large Flip-Chip Ball Grid Array Substrate to Manage Both Warpage and Board Level Reliability
Hirokazu Noma, Masaki Takahashi, Nene Hatakeyama, Yuichi Yanaka, Akito Fukui, Keita Johno, Hitoshi Onozeki - Resonac Corporation

19. Embedded Cooling Method With Monolithic Dual-Layer Micro-Channel Cold Plate for High-Power Chips
Jianyu Du, Hongxu Wu, Huaiqiang Yu, Chi Zhang, Wei Wang - Peking University

20. Method to Evaluate the Adhesion Distribution on Wafers
Tatsumasa Hiratsuka, Takaaki Hirano, Kengo Kotoo, Nobutoshi Fujii, Suguru Saito, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation

21. Experimental and Numerical Investigation of Cu-Cu Direct Bonding Quality for 3D Integration
Sung-Hyun Oh, Hyun-Dong Lee, Jae-Uk Lee, Hoo-Jeong Lee, Eun-Ho Lee - Sungkyunkwan University; Sung-Ho Park, Won-Seob Cho, Yong-Jin Park, Alexandra Haag, Soichi Watanabe, Marco Arnold - BASF

22. Atomistic Simulation Investigation of Various Plasma Surface Activations in SiCN Dielectric Bonding
Hojin Kim, Andrew Tuchman, Yu-Hao Tsai, Toru Hisamatsu, Ilseok Son, Sitaram Arkalgud - TEL Technology Center, America, LLC

23. Reliability of Differently Shaped Solder Joints in Chip Resistor Under Drop Impact
Jonghwan Ha, Karthik Deo, Junbo Yang, Yangyang Lai, Seungbae Park - Binghamton University

24. Study of Damage Development in Under-Bump Interconnects by Thermo-Mechanical Stress in Package Interconnects
Jorge Mendoza, Choong-Un Kim - University of Texas, Arlington; Hung-Yun Lin - Texas Instruments, Inc.

25. Aging Behaviour and Environmental Impact of Under Bump Metallurgies for Wafer Level Balling
Arnaud Garnier, Laetitia Castagne, Stephane Moreau, Alexandra Fraczkiewicz, Theo Monniez, Daniel Mermin, Suzanne Guillou, Laura Vauche, Damien Saint-Patrice, Perceval Coudrain - Grenoble Alps University/CEA-LETI

26. Automated Solder Joint Failure Mode Analysis Based on Dry and Pry Image Processing
Yinan Lu, Chaolun Zheng, Andrew Huang, Hedan Zhang, Bee Chin Loke, Ning Ye, Bo Yang - Western Digital Corporation

Wednesday May 29th

Session 38: Photonics, mm-Wave Applications & Emerging Technologies

Time: 2:30 PM - 4:30 PM

Committee: Interactive Presentations

Aurora A-C Corridor

Session Co-Chairs:
Frank Libsch - IBM
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Saikat Mondal - Intel
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Pavel Roy Paladhi - IBM
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Yoichi Taira - Keio University
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1. Conformal Dry Electrode for ECG Monitoring
Riadh Al-Haidari, Babatunde Falola, Mohammed Alhendi, Mark Schadt, Mark Poliks - Binghamton University; Dan Balder, Andrew Stemmermann, Matthew Foster - SunRay Scientific, Inc.; Tzu-Jen Kao, Nancy Stoffel - General Electric Global Research

2. Reliability of Flexible Electronics Undergoing Vibration
Sara Lieberman, El Mehdi Abbara, Nathaniel Gee, Kankanige Udara Sandakelum Somarathna, Abhishek Navkar, Abdullah Obeidat, Zhi Dou, Mohammed Alhendi, Peter Borgesen, Mark Poliks - Binghamton University

3. Quantifying Uncertainties in the Correlation of Simulations and Measurements Using the IEEE EPS Packaging Benchmark Suite
Jonatan Aronsson - CEMWorks, Inc.; Kemal Aygun - Intel Corporation

4. Polymer Waveguides for Co-Packaged Optics
Yi Shen, Michael Gallagher, Ross Johnson, Jake Joo, Masaki Kondo, James Ryley, Rui Zhang, Zhebin Zhang - DuPont; Marika Immonen, Matthew Neely, Everett Sarauer, David Senk - TTM Technologies, Inc.

5. The Energy-Efficient 10-Chiplet AI Hyperscale NPU on Large-Scale Advanced Package
Jiwon Yoon, Hyunwoo Kim, Juhyeon Lee, Joungho Kim, Sungjin Kim - Korea Advanced Institute of Science and Technology; Youngsu Kwon, Yigyeong Kim, Minseok Choi - Electronics and Telecommunications Research Institute; Heejun Jang, Kyun Ahn, Jinhan Kim, TaeKyeong Hwang - Amkor Technology, Inc.

6. Development of Robust and Cost-Effective Electrical & Optical Interconnect Solution for High Performance Silicon Photonic Applications
Jae Kyu Cho, Takako Hirokawa, Yusheng Bian, Scott Pozder, Koushik Ramachandran, Arpan Dasgupta, Jason Kim, Zahidur Chowdhury, Norman Robson, Thomas Houghton - GlobalFoundries, Inc.

7. Low-Loss Non-Contact Interconnects Based on 3D Heterogeneous Redistribution Layer for Millimeter Wave Phased Arrays
Lichang Huang, Yunfei Cao - South China University of Technology; Yuting Tong, Sha Xu - Guangdong University of Technology; Xiaobin Xu, Jinxing Chen - Glorysky Electronic Technology Co., Ltd.

Wednesday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Aurora A-C Corridor

8. Thermal Performance and Reliability of Liquid Metal Alloys as Thermal Interface Materials for Computing Electronics Devices
Guangyu Fan, Jacob Wells - Indium Corporation; Michael Beam - SUNY Polytechnic Institute

9. Multi-Wideband Antenna in Package With Dual Polarizations
Mei Sun - Institute of Microelectronics A*STAR

10. Deep Reinforcement Learning-Based Power Distribution Network Design Optimization for Multi-Chiplet System
Weiyang Miao, Zhen Xie, Chuan Seng Tan - Institute of Microelectronics A*STAR/Nanyang Technological University; Mihai Dragos Rotaru - Institute of Microelectronics A*STAR

11. Novel Low Loss Polymer With High Thermal Resistance for Advanced IC Packaging
Hikaru Mizuno - JSR Micro, Inc.; Eri Mishima, Shunsuke Iizuka, Yuuichi Yashiro, Naoyuki Kawashima - JSR Corporation

12. Power Supply Design and Power Management in Complex System Design: Co-Packaged Optics-FPGA 3D SIP Module
Jugal Kishore Bhandari, Sandhya Dharavath, Venkata Ramana Pamidighantam, Mohd. Ubed, Anusha Veerandi, Rohin Kumar Yeluripati - LightSpeed Photonics Pte Ltd

13. Additively Manufactured SoP Modules for Smart Agriculture and Insect Pheromone Sensing Applications
Genaro Soto Valle Angulo, Manos M. Tentzeris - Georgia Institute of Technology; Andrew Fang - Walton High School

14. All-Cu 3D Interconnects as an Alternative to Hybrid Bonding
Tadatomo Suga, Kanji Otsuka - Meisei University

15. Additive Manufacturing of an Electronically Steerable Microstrip Leaky Wave Antenna on Thin Alumina Substrate
Ethan Kepros, Yihang Chu, Bhargav Avireni, Sambit Ghosh, Brian Wright, Premjeet Chahal - Michigan State University

16. Conductive Fabric Based RFID Wearable Textile Antennas for Product Authentication and Quality Control
Bhargav Avireni, Yihang Chu, Ethan Kepros, Sambit Kumar Ghosh, Premjeet Chahal - Michigan State University

17. Tire-Integrated Antennas for Wireless Sensors in Automotive Applications
Yihang Chu, Sambit Kumar Ghosh, Bhargav Avireni, Ethan Kepros, Premjeet Chahal - Michigan State University

18. Additively Manufactured Dissolvable Packaging for Recycle and Reuse of Chips for Sustainable Reduction of E-Waste
Dhiya Belkadi, Carl P Hahn, Hannah Lynn Houston, Sunehra Saleha, Min Sung Kim, Muhammad Mustafa Hussain - Purdue University

19. Experimental Study of Transmission Signal Performance of Sub-2-micron Fine Wiring With Novel Structure
Masaya Tanaka, Nobuyoshi Moriwaki, Satoru Kuramochi - Dai Nippon Printing Co., Ltd.

20. Comprehensive Socket Characterization and Correlation for High-Speed Interface Testing System
Varin Sriboonlue, Yeseul Jeon, Gerardo R. Luevano, Chris Ferguson, Ennai Ochoa - Qualcomm Technologies, Inc.

21. A Novel Method for LPDDR5 DRAM Jitter Measurement Through De-Embedding
Manho Lee, Chulhee Cho, Hyeongi Lee, Sehoon Park, Wonseok Hong, ByungSuk Woo, Woo-Shin Choi, Young-Chul Cho, Young-Soo Sohn, Jung-Hwan Choi - Samsung Electronics Co., Ltd.

22. An Effective Surface Roughness Extraction Method Using Particle Swarm Optimization (PSO) Algorithm and 2D Based Equations for High Speed Systems
Youngjae Lee, Kwangho Kim, Chulhee Cho, Sungjin Yoon, Hyeongi Lee, Wonji Hwang, Wooshin Choi, Young-Chul Cho, Jung-Hwan Choi, Young-Soo Sohn - Samsung Electronics Co., Ltd.

23. Ultimate Wafer-Level Lens Integration and Optimization Using Microlenses and Metalenses for High-End Active Pixel Sensor Applications
Hoi-Jin Lee, Sihun Han, Chanyeol Park, Sunyong Park, Woonphil Yang, Yitae Kim - Samsung Electronics Co., Ltd.

24. Microprinting Process Development Enabling Cost Effective, High Density and Flexible Electro-Optical Integration
Krzysztof Nieweglowski, David Weyers, Akash Mistry, Karlhenz Bock - TU Dresden

25. High Bandwidth Active Flexible Connector for Signaling in Wafer-Scale Systems
Randall Irwin, Joanna Fang, Subramanian Iyer - University of California, Los Angeles

Thursday May 30th

Session 39: Bonding Process and Analysis in Next-generation Interconnects

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Aurora A-C Corridor

Session Co-Chairs:
Rao Bonda - Amkor
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Karan Bhangaonkar - Intel
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Amanpreet Kaur - Oakland University
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Jin Yang - Samsung
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1. A Novel Detection Applied on Micro Defect in Bump Interface for 2.5DIC Package
Yi-Sheng Lin, Yu-Hsiang Hsiao, Cheng-Hsin Liu, Fan-Ju Hsiao - Advanced Semiconductor Engineering, Inc.

2. Hybrid Bonding Technology Chemical Mechanical Planarization Process Optimization Using Comprehensive 3D Modeling
Liu Jiang, El Mehdi Bazizi, Gregory Costrini, Prayudi Lianto, Gilbert See, Sefa Dag - Applied Materials, Inc.; Dimitrios Tsamados, Yves Saad - Synopsys, Inc.

3. Influence of Stiffener Design on Co-Packaged Optics (CPO) 2.5D Heterogeneous Packages
Karthik Arun Deo, Yangyang Lai, Jong Hwan Ha, Junbo Yang, Seungbae Park - Binghamton University

4. Adhesion Layer Influence on Thermomechanical Reliability of Electroplated Copper Through-Glass Via (TGV)
Junbo Yang, Ke Pan, Pengcheng Yin, Yangyang Lai, Seungbae Park - Binghamton University; Chukwudi Okoro - Corning, Inc.; Dhananjay Joshi, Scott Pollard - Corning Research and Development Corp.

5. A Study on the Surface Activation of Plasma Treatment for Hybrid Bonding Joint Interface
Chih-Jing Hsu, Hsu-Nan Fang, Tzu-Yu Su, Zhao-Ze Jiang, Yi-Hua Chen, Chien-Ching Chen, Yu-Bin Tsai, Che-Ming Hsu, Yuan-Feng Chiang, Jen-Chieh Kao, Yung-I Yeh - ASE Corporate R&D Center

6. Influence of Heat Treatment on the Quality of Die-to-Wafer Hybrid Bond Interconnects
Laura Wenzel, Catharina Rudolph, Adil Shehzad, Iuliana Panchenko, Manuela Junghnel - Fraunhofer IZM; Partha Mukhopadhyay, H. Jim Fulford - Tokyo Electron America, Inc.

7. Inverse Hybrid Bonding With Aluminum Oxide as Infill Using Atomic Layer Deposition
Rohan Sahay, Ashita Victor, Muhannad Bakir - Georgia Institute of Technology; Shreyam Natani, Dipayan Pal, Victor Wang, Chenghsuan Jimmy Kuo, Andrew Kummel - University of California, San Diego

8. Intelligent Design and Demonstration of Reliable All-Cu Interconnections on High-Density Glass Substrates at 10 Micron Pitch
Ramon Sosa, Antonia Antoniou, Vanessa Smet - Georgia Institute of Technology

9. Electromigration Kinetics of SAC/SnBiAg Hybrid Solder
Minhua Lu, Evan Colgan - IBM Research

10. Simulation of Bulge-Out Mechanism Enabling Sub-0.5 µm Scaling of Hybrid Wafer-to-Wafer Bonding
Jo De Messemaeker, Koen Van Sever, Yan Wen Tsau, Boyao Zhang, Kristof Croes, Eric Beyne - imec

11. Wet Cu Passivation for High Throughput Fluxless Thermal Compression Bonding of Cu-Sn bumps for Die-to-Wafer Stacking
Jens Rip, Jaber Derakhshandeh, Dieter H. Cuypers, Eric Beyne - imec; Ryo Negishi, Itsuro Tomatsu - MEC Co., Ltd

12. Low Temperature Nanocrystalline Cu/Polymer Hybrid Bonding With Tailored CMP Process
Lee Ou-Hsiang, Hsiang-Hung Chang, Wei-Lan Chiou, Chia-Wen Chiang, Shih-cheng Yu, Ting-Yu Ke, Yu-Min Lin - Industrial Technology Research Institute; Chia-Hsin Lee, Andrew Tan - Brewer Science, Inc.

13. A Novel FOPLP Structure With Chip First & RDL First Process for Automotive Chip Application
Terry Wang, Chih Wei Lu, Eric Feng, Yu-Jhen Yang, Cheng-Yueh Chang, Pei-Pei Cheng - Industrial Technology Research Institute; Fredrick Lie - Applied Materials, Inc.; Austin Cheng - FAVITE, Inc.; Hsin-Yi Huang - Everlight Chemical Industrial Corp.; Meiten Koh - Taiyo Ink Mfg. Co., Ltd.; Aneta Wiatrowska, ukasz Witczak - XTPL SA

14. A Unified and Adaptive Continual Learning Method for Feature Segmentation of Buried Packages in 3D XRM Images
Richard Chang, Jie Wang, Namrata Thakur, Ramanpreet Pahwa, Yang Xulei - Institute for Infocomm Research A*STAR

15. Low Thermal Budget Fine-Pitch Cu/Dielectric Hybrid Bonding With Cu Microstructure Modifications
Hemanth Kumar Cheemalamarri, Anh Tran Van Nhat, Gim Guan Chen, Arvind Sundaram, Binni Varghese, Nandini Venkataraman, Vempati Srinivasa Rao, Navab Singh - Institute of Microelectronics A*STAR

16. Fundamental Study on Reflow Mechanisms of Sn and Sn Alloys for Fine Bump Pitch Scaling
Chongyang Cai, Anup Panindre, Liang He, Jung Kyu Han, Gang Duan, Rahul Manepalli - Intel Corporation

17. Advanced Photo-imageable Dielectric Film Enabling Low CTE and sub-5-Micrometer Patterning for Next Generation Build-up Layer
Taku Ogawa, Ryuichi Okuda, Fumie Hattori, Hirokazu Ito - JSR Corporation

18. Glass Panel Process Integrated Low Stress Organic Dielectric RDL Structure
Chien Kang Hsiung, Sarah Wozny, Marvin L Bernt - Applied Materials, Inc.; Terry Wang - Industrial Technology Research Institute; Kuan-Nang Chen - National Yang Ming Chiao Tung University

19. A Warpage Investigation for a Large Panel-Sized Interposer With Embedded Dies
Katsuaki To, Daisuke Yamanaka, Masashi Minami, Shan Ho Tsai, Sadaaki Katoh - Resonac Corporation

Wednesday & Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Aurora A-C Corridor

20. Development of Two Different Molding Methods in 2.5D Package With 20 µm or Less Fine Bump Pitch CoW Structure
Takeshi Saito, Sadaaki Katoh, Keiko Ueno, Ryosuke Kimura, Tsai Shanho, Takahiro Iseki, Kan Donchoru - Resonac Corporation

21. Low Temperature Cu/SiO2 Hybrid Bonding With Protruding Copper Pads
Junpeng Fang, Qian Wang, Jiexun Yu, Ziqing Wang, Jian Cai - Tsinghua University; Yikang Zhou, Kai Zheng - Semiconductor Technology Innovation Center (Beijing) Corporation

22. Analysis of Vacancies in Wafer-Bonding Interface Via Positron Annihilation Lifetime Spectroscopy
Sotetsu Saito, Nobutoshi Fujii, Shunsuke Furuse, Naoki Ogawa, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation

23. Annealing Effects in Sub-8 µm Pitch Die-to-Wafer Hybrid Bonding
Partha Mukhopadhyay, Andrew Tuchman, Kevin Ryan, Adam Gildea, Sitaram Arkalgud, Anton deVilliers, Jim Fulford - TEL Technology Center, America, LLC; Laura Wenzel, Catharina Rudolph - Fraunhofer IZM; Chuck Woychik, Chris Nichols - SkyWater Technology; John Allgair - BRIDG

24. 3D Interconnect Technology With Serpentine and Trapezoidal Corrugation Using a Flexible Photosensitive Dielectric to Strengthen the Bendability of FHE
Chang Liu, Jiayi Shen, Atsushi Shinoda, Han Zhang, Tetsu Tanaka, Takafumi Fukushima - Tohoku University

25. Through Dielectric Via Etching in Magnetic Neutral Loop Discharge Plasma for 3D Chiplets Interconnect
Yasuhiro Morikawa - ULVAC, Inc.

26. A Novel Plasma Etching Technology of RIE-Lag Free TSV and Dicing Processes for 3D Chiplets Interconnect
Taichi Suzuki, Kenta Doi, Yasuhiro Morikawa - ULVAC, Inc.

27. Aluminum-to-Aluminum and Aluminum-to-Copper Thermal Compression Bonding for Heterogeneous Integration of Legacy Dielets
Krutikesh Sahoo, Randall Irwin, Golam Sabbir, Vineeth Harish, Subramanian Iyer - University of California, Los Angeles

28. Directional Atmospheric Plasma De-oxidation for Ultra Small Passive Component Assembly
Khouloud Ben Harzallah, David Danovitch, Malak Kanso - University of Sherbrooke; Christian Bergeron, Marc-Olivier Pion - IBM Canada, Ltd.

29. Exploring Bonding Mechanisms of SiCN for Hybrid Bonding
Sodai Ebiko, Fumihiro Inoue - Yokohama National University; Serena Iacovo, Soon-Aik Chew, Boyao Zhang - imec; Akira Uedono - University of Tsukuba

Thursday May 30th

Session 40: Materials, Manufacturing and Assembly Techniques in Advanced Packaging Solutions

Time: 2:30 PM - 4:30 PM

Committee: Interactive Presentations

Aurora A-C Corridor

Session Co-Chairs:
Mark Eblen - Kyocera
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Stephen Lee - NXP
stephen.lee@nxp.com

Kristina Young - Synopsys
kristina.youngfisher@gmail.com

Biao Cai - IBM
biaocai@us.ibm.com

1. Characterization of Warpage of Ultra-Low-K Dielectric Materials and Correlation With Modulus and Coefficient of Thermal Expansion
Mohanalingam Kathaperumal, Pragna Bhaskar, Austin Toro, Pratik Nimbalkar, Lila Dahal, Muhannad Bakir - Georgia Institute of Technology

2. A Highly-Reliable and Cost-Effective Approach by Reducing Flux Cleaning in Flip-Chip Processes Through Underfill Curing in a Pneumatic Ambient
Huan-Ping Su, Ming-Hua Hsu, Auger Horng - Ableprint Technology Co., Ltd.

3. 300 nm Pitch W2W HBI for CFET and 3D DRAM Through Module Co-Optimization
Tyler Sherwood, Raghav Sreenivasan, Masha Gorchichko, Amit Prakash, Raghuveer Patlolla, Sarabjot Singh, Yoocharn Jeon, Jason Appell, Ryan Ley, Kun Li - Applied Materials, Inc.; David Hafner - EV Group, Inc.

4. Mechanical Characterization and Modeling of iSAC Lead-Free Solder
Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Mohammad Al Ahsan, Jeffrey Suhling, Pradeep Lall - Auburn University

5. Novel SiO_2 Cables With Edge Launch Connectors for High Temperature RF Measurements
Firas Alshatnawi, Ashraf Umar, Emuobosan Enakerakpo, Mohamed Abdelatty, W.T. Alshaibani, Mohammed Alhendi, David Shaddock, Peter Borgesen, Mark Poliks - Binghamton University

6. Modeling and 3D Additively Manufactured Inductors on Complex Shape for Extreme High Temperature Electronics
Waleed Alshaibani, Ashraf Umar, Firas Alshatnawi, Emuobosan Enakerakpo, Mohamed Abdelatty, Mohammed Alhendi, Mark D. Poliks - Binghamton University; David Shaddock - General Electric Company

7. Underfill Selection Guideline for Fan-Out Heterogeneous Integration Package
Wen-Yu Teng, Liang-Yih Hung, Jackson Lee, Debby Li, Carl Chen, Don-Son Jiang, Yu-Po Wang - Siliconware Precision Industries Co., Ltd.

8. Comparison of Organic and Inorganic Dielectric Hybrid Bonding With Highly <111>-Oriented Nanotwinned Cu
Pin-Syuan He, Chih Chen - National Yang Ming Chiao Tung University

9. One-step Surface Modification for Boron Nitride and its Polymer Composite of Enhanced Thermal Conductivity for Advanced Packaging Applications
Zihao Lin, Jiaxiong Li, Zhijian Sun, Kyoung-Sik Moon, Ching-Ping Wong - Georgia Institute of Technology; Andrew Fang - Walton High School

10. Investigation on the Use of Al-Ge Eutectic Bonding in the Structural Part of a Multilayer Stacked MEMS Device
Jun Wang, Manuel Mannarino, Jakob Visker, Shuo Kang, Bivragh Majeed, Lan Peng, Gauri Karve, Luc Haspeslagh - imec; Günther Weidlinger, Tobias Wernicke, Jürgen Burggraf, Markus Wimplinger - EV Group, Inc.

11. Limits for Dicing Speed Based on Crack Stop Constructions With Different Levels of Robustness
Maria Heidenblut, Michael Goroll, Stefan Kaiser, Andreas Bauer, Kristina Hopfauf - Infineon Technologies AG

12. Vertical Stacking of Heterogeneous Chiplets of Duplexer on LNA/SOI
Tai Chong Chai, Rotaru Dragos Mihai, Xiangyu Wang, Pei Siang Sharon Lim, Lin Ji, Rathin Mandal, Raju Mani, Ming Chinq Jong, Yong Liang Ye - Institute of Microelectronics A*STAR

13. Multi Chip Stacked Memory Module Development Using Chip to Wafer (C2W) Hybrid Bonding for Heterogeneous Integration Applications
Nagendra Sekhar Vasarla, Dileep Kumar Mishra, Sasi Kumar Tippabhotla, Chandra Rao Bhesetti, Ser Choong Chong, King-Jien Chui, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR

14. Error Estimation in Immersion Cooling Liquid Dk-Df Extraction Using Different Methods
Saikat Mondal, Xenofon Konstantinou, Cemil Geyik, Zhichao Zhang, Kemal Aygun - Intel Corporation

15. Fluidic Self Alignment for Hybrid Bonding Using Intel Process
Feras Eid, Yi Shi, Golsa Naderi, Shashi Bhushan Sinha, Rob Jordan, Wenhao Li, Charles El Helou, Felipe Bedoya, Anandi Roy, Tayseer Mahdi, Jiun-Ruey Chen, Brandon M Rawlings - Intel Corporation

16. An Advanced Remote-Plasma Assisted Ozone-Ethylene-Radical (OER) Process for Cu-SiO2 Hybrid Bonding Yield Enhancement
Tatsunori Shino, Eitaro Toyama, Tetsuya Nishiguchi - MEIDEN NANOPROCESS INNOVATIONS, Inc.; Mariappan Murugesan, Kiyoharu Mori - NICHe; Bungo Tanaka, Takafumi Fukushima - Tohoku University

17. Influence of Temporary Rigid Carrier Structure on Warpage During Wafer/Panel Level Packaging
Yoshinori Matsuura, Joji Fujii, Vivek Dutta - Mitsui Mining & Smelting Co., Ltd.

18. Extremely Advanced Substrate as an Integrated Package Solution (iPaS) for Next Generation High Performance Computing (HPC) Applications
Tatsuya Kitamura, Takeshi Furukawa, Shuhei Yamada, Koshi Himeda, Atsushi Yamamoto - Murata Manufacturing Co., Ltd.

19. A CMP Process for Hybrid Bonding Application With Conventional / nt-Cu and SixNy / SixOy Dielectrics
Tri Widodo, Yi Shi, Xavier F Brun - Intel Corporation; Prayudi Lianto, Avery Tan, Joselyn Lie, Patrick Lim, Guan Huei See - Applied Materials, Inc.

20. Effect of Material Aging on the Reliability of an Automotive BGA Device Under Temperature Cycling Test Conditions
Abdullah Fahim, Ryan Zhang, Amar Mavinkurve, Sandeep Shantaram, Ali Rezaie Adli, Wiwat Tanwongwan, Torsten Hauck - NXP Semiconductor, Inc.

21. Overlay Challenges of Extremely Large Exposure Field, Fine Resolution Lithography Due to Alignment Solution Errors and a Solution Using Early Zone Corrections in Advanced IC Substrates
John Chang, Xin Song, Timothy Chang - Onto Innovation

22. World's Smallest, Membrane-Based Capacitive Differential Pressure Sensor- Package Structure, Material Selection, Assembly Challenges & Solutions
KM Rafidh Hassan, Gaurav Mehrotra, Hazel Caballero, Young Kim, Steven Lee - Renesas Electronics America; Karim Allidina, Tommy Tsang, Mohannad Elsayed, Hani Tawfik - MEMS Vision International, Inc.

23. Packaging Challenges and Solutions for Next Generation Low-Profile WLCSP
Humi (Shih-Wen) Tang, Jerry (Che-Han) Li, Jessie (Yu-Shan) Wei, Baltazar Canete, Leo (Hsin-Hung) Huang, Jesus Mennen Belonio - Renesas Electronics Corporation

24. A Study on Novel Low Temperature Soldering Process Using Vapor phase
Youngja Kim, Woojin Choi, Seungyeop Oh, Sinyeob Lee, Sunwon Kang - Samsung Electronics Co., Ltd.

25. Numerical Study on Hybrid Discontinuous Microchannel Heat Ink Combining Manifold With Pin Fins (DMC-MPF) for High Power Electronic Device
Jianyu Du, Lang Chen, Ran Hu, Chi Zhang, Wei Wang - Peking University; Huaiqiang Yu - 26th Research Institute of China Electronics Technology Group Corporation

26. Room-Temperature Hybrid Bonding of Via-Middle TSV Wafer Fabricated by Direct Si/Cu Grinding and Residual Metal Removal
Naoya Watanabe - National Institute of Advanced Industrial Science and Technology; Hiroshi Yamamoto, Takahiko Mitsui - Okamoto Machine Tool Works, Ltd.

Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Aurora A-C Corridor

27. Ultra Thin Fan-Out 3D WLCSP Heterogeneous Integration Packaging
Jay Li, Zen-Wei Zhang, Sam Lin, Vito Lin, Teny Shih, Nicholas Kao - Siliconware Precision Industries Co., Ltd.; Yu-Po Wang - SPIL

28. Panel Level Plasma Etching Characteristics for Advanced Packaging
Md Ishak Khan, Wei Wei, Haobo Chen, Xiyu Hu, Nicholas Haehn, Xiaoying Guo, Leonel Arana - Intel Corporation; Kensuke Akazawa - ULVAC, Inc.

29. Development of a Reusable Smart-Catheter System for Improved Urinary Health Monitoring
Zhi Dou, W.T. AlShaibani, Erika Solano Diaz, Mohammed Alhendi, Abdullah Obeidat, Riadh Al-Haidari, Mark Schadt, Mark Poliks - Binghamton University; Kara Allanach, Daniel Wollin, Souvik Paul - CathBuddy, Inc.

30. Focal Extension – A Novel Lithography Technique in Direct-Write Laser Lithography to Enable Fine-Pitch Patterning Over Large Topography
Golam Sabbir, Subramanian Iyer - University of California, Los Angeles

Friday May 31st

Session 41: Student Posters

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Aurora A-C Corridor

Session Co-Chairs:
Alan Huffman - Skywater
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Mohd. Enamul Kabir - Intel
enamul101b@yahoo.com

Ibrahim Guven - Virginia Commonwealth
iguven@vcu.edu

Jae Kyu Cho - Globalfoundries
jaekyu.cho@globalfoundries.com

1. Low Temperature Cu/SiO2 Hybrid Bonding Using Area-Selective Metal Passivation (Interface Metal) Technology for 3D IC and Advanced Packaging
Mu-Ping Hsu, Wen-Tsu Tsai, Chi-Yu Chen, Zhong-Jie Hong, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Ou-Hsiang Lee, Tzu-Ying Kuo, Hsiang-Hung Chang - Industrial Technology Research Institute

2. Vertical Power Delivery for High Performance Computing Systems with Buck-Derived Regulators
Sriharini Krishnakumar, Inna Partin-Vaisband - University of Illinois; Mingeun Choi, Satish Kumar - Georgia Institute of Technology; Ramin Rahimzadeh Khorasani, Madhavan Swaminathan - Pennsylvania State University; Rohit Sharma - Indian Institute of Technology Ropar

3. Multi-Objective Optimization of a 1200-V Fan-Out Panel-Level SiC MOSFET Packaging with Improved Genetic and Particle Swarm Algorithms
Xuyang Yan, Wei Chen, Jing Jiang, Jiajie Fan - Fudan University; Xuejun Fan - Lamar University; Guoqi Zhang - Delft University of Technology

4. Packaging of Photonic Neural Network Accelerators
Russell Schwartz, Nicola Peserico, Hamed Dalir, Volker Sorger - University of Florida

5. Comparison of Different Copper Nitride Passivation Layers Fabrication Methodology and Optimal Growth Condition for Low Temperature Copper-to-Copper Bonding in Advanced Packaging
Chiao-Yen Wang, Tzu-Heng Hung, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Ping-Jung Liu - Taiwan Semiconductor Manufacturing Company, Ltd.

6. Fabrication and Testing of In-Line Structures for Non-Destructive Study of Solder Electromigration: Applications to SnBi Low Temperature Solder
Chetan Jois, Pei-En Chou, Ganesh Subbarayan - Purdue University

7. Application of Elevated-Laser-Liquid-Phase-Epitaxy (ELLPE) Technique on Different Oriented Wafers for Monolithic 3DIC Integration
Bo-Jheng Shih, Yu-Ming Pan, Chiao-Yen Wang, Huan-Yu Chiu, Huang-Chung Cheng, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Chih-Chao Yang, Chang-Hong Shen - Taiwan Semiconductor Research Institute

8. Manufacturing and Characterization of Planar Transformers as Molded Interconnect Device Technology Component for an Industrial Production
Tim Nils Bierwirth, Folke Dencker, Marc Christopher Wurz - Leibniz University Hannover; Sebastian Bengsch, Michael Werner, Christian Henne, Stefan Bur - Ensinger GmbH; Rico Wachs - Tridelta Weichferrite GmbH

9. Hybrid Wiring Layers for Fine Pitch Integration
Vineeth Harish, Krutikesh Sahoo, Subramanian Iyer - CHIPS UCLA; Kai Zheng, Gilbert Park, Han-Wen Chen, Steven Verhaverbeke - Applied Materials, Inc.

10. Novel Single and Co-Ion Implantation Induced Backside Etch Stop Structures for 3D Multilayer Stacked Package
Yen-Shuo Chen, Hua-Tai Fan, Yu-Chien Ko, Fu-Hsiang Ko - National Yang Ming Chiao Tung University; Tzu-Wei Chiu - Thinchipway Co., Ltd.; Chun-Chi Chen - Taiwan Semiconductor Research Institute

11. New Method for Fluid Filling Through Silicon Vias With Silver Ink for Packaging Techniques
Zachary Nelson, Alice Mo, Luke Theogarajan - University of California, Santa Barbara

12. Electrospray Printed Silver Films for EMI Shielding of SiP Architectures
Emma Pawliczak, Paul Chiarot - Binghamton University

13. Latency Insertion Method for Accelerated Simulation of Memristor Crossbar Array in Neuromorphic Chip
Yi Zhou, Tahsin Shameem, Zohreh Salehi, Shaloo Rakheja, Jose Schutt-Aine - University of Illinois; Hanzhi Ma, Junwei Yu, Erping Li - Zhejian University

14. A Novel Parallel Interconnection Approach to Reduce Shading Losses on Submillimeter Concentrated Photovoltaic Technologies
Corentin Jouanneau, Thomas Bidaud, Artur Turala, David Danovitch, Gwenaelle Hamon, Maxime Darnon - University of Sherbrooke

15. Fabrication and Packaging of a Heterogeneously Integrated, Flexible Quantum Dot Enabled Micro-Display
Henry Sun, Harshal Sonagara, Subramanian Iyer - University of California, Los Angeles; Lisong Xu, Kai Ding, Mingwei Zhu - Applied Materials, Inc.

16. Intense Pulsed Light Soldering of SAC305 for Flip-Chip Package
Seong-Ung Ryu, Young-Min Ju, Jong-Whi Park, Seok-Hoon Jeong, Hak-Sung Kim - Hanyang University

17. Design Space Exploration for Power Delivery Network in Next Generation 3D Heterogeneous Integration Architectures
Madison Manley, Ankit Kaul, Muhannad Bakir - Georgia Institute of Technology

18. Hybrid Interconnect Infrastructure for Inter-Chiplet Communication in Wafer-Scale Systems
Yousef Safari, Rezvan Mohammadrezaee, Dima Al Saleh, Boris Vaisband - McGill University

19. Reliability of Indium Solder Joints using Laser-Assisted Bonding (LAB) Process at Room Temperature
Ji Eun Jung, Yoon Hwan Moon, Ga-Eun Lee, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-seok Jang, Jin-Hyuk Oh, Yong-Sung Eom, Jung-Ho Shin, Kwang-Seong Choi - Electronics and Telecommunications Research Institute; Seung-Yoon Lee - Hanbat National University

20. Tailored Multi-Mode, High-Q Superconducting Nb Resonators: Unique Platform for Magnon-Photon Coupling
Muntasir Mahdi, Bhargav Yelamanchili, Archit Shah, Sherman Peek, Michael Hamilton - Auburn University; Yuzan Xiong, Wei Zhang - University of North Carolina; Dan-Chi Nguyen - Ewha Womans University/The University of North Carolina; Tae Hee Kim - Ewha Womans University

21. Magnetic Cores for High Conversion Ratio Package Embedded Inductors
Sai Saravanan Ambi Venkataramanan, Prahalad Murali, Mohan Kathaperumal, Mark Losego - Georgia Institute of Technology; Dustin Allen Gilbert - University of Tennessee

22. Unveiling Mechanical Stress in Lithium-Metal Batteries for Flexible Electronics: A Novel Approach With Optical Techniques and Artificial Interfaces
Mayukh Nandy, Siyang Liu, Hongbin Yu - Arizona State University

23. Creep Properties of SAC305 Solder Specimens that Mimic the Microstructures of a Micro Solder Ball: Measurement and BLR Prediction
You-Gwon Kim, Heon-Su Kim, Tae-Wan Kim, Seong-Ung Ryu, Hak-Sung Kim - Hanyang University; Yongrae Jang, Bongtae Han - University of Maryland; Jun-Hyeong Lee, Jin-Kyu Kim - DUKSAN Hi-Metal Co., Ltd.

24. RF Energy Harvesting Hybrid RFID Based Sensors for Smart Agriculture Applications
Yihang Chu, Ethan Kepros, Bhargav Avireni, Sambit Kumar Ghosh, Premjeet Chahal - Michigan State University

25. Influence of Nickel and Bismuth Addition on the Mechanical Shear Strength of SAC+ Ni, Bi Solders Under Isothermal Aging and Multiple Reflows
Jyothsna Bandayagari, Dr. Darshil Patel, Dr. Yingge Zhou - Binghamton University; Dr. Santosh Kudtarkar, Dr. Arun Raj, Dr. Shafi Saiyed - Analog Devices, Inc.

26. Process Development of Manifold Microchannels Cooling for Embedded Silicon Fan-Out (MMC- eSiFO) Package
Zhou Yang, Yuchi Yang, Peijue Lyu, Jianyu Du, Lang Chen, Chi Zhang, Wei Wang - Peking University

27. Demystifying Edge Cases in Advanced IC Packaging Inspection Through Novel Explainable AI Metrics
Shajib Ghosh, Antika Roy, Md Mahfuz Al Hasan, Patrick Craig, Nitin Varshney, Sanjeev J. Koppal, Navid Asadizanjani - University of Florida

28. Effective Heat Dissipation of White Laser Diodes by Welding Metallized Phosphor-Sapphire on Ceramic Substrate With 3D Metal Dam
Zikang Yu, Jiuzhou Zhao, Qing Wang, Yang Peng, Mingxiang Chen - Huazhong University of Science and Technology

29. Impact of Non-Coplanarities on Microstructure and Properties of Sintered NP-Cu Interconnections
Ali Amirnasiri, Ramon A. Sosa, Mengkun Tian, Antonia Antoniou, Vanessa Smet - Georgia Institute of Technology

Friday Refreshment Break: 9:15 a.m. - 10:00 a.m. – Aurora A-C Corridor

2024 ECTC EXHIBITION

Exhibit Hall Hours

Wednesday, May 29

9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 6:30 p.m.

Thursday, May 30

9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 4:00 p.m.

Aurora 1 Ballroom

Booth 323
3D Systems Packaging Research Center
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The 3D Systems Packaging Research Center (PRC) at Georgia Tech is a graduated NSF Engineering Research Center focusing on advanced packaging and system integration leading to System on Package (SoP) technologies. The center conducts research and education in all aspects of packaging that includes design, materials, process, assembly, thermal management, and integration driven by applications including areas such as high-performance computing, artificial intelligence, automotive, broadband wireless and space. The team consists of 29 faculty from five schools, 11 research/administrative staff, 50+ graduate/undergraduate students and several visiting engineers. This is enabled through collaboration with over 40 industry/govt. organizations and 14 universities.

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Adeia invents, develops and licenses fundamental innovations that shape the way millions of people explore and experience entertainment and enhance billions of devices in an increasingly connected world. Leveraging the combination of highly experienced technologists, scientists, engineers and advanced R&D labs in San Jose, California and Raleigh, North Carolina, Adeia develops industry-leading 3D integration solutions such as hybrid bonding that meet the demand for greater functionality, higher performance and smaller size for next generation electronics.

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AI Technology, Inc. (AIT) specializes in electronic interconnection and microelectronic packaging materials, including adhesive films with low to zero interface stress for ultimate reliability and, as part of the company's line of Thermal Interface Materials (TIM), pads, greases, gels, waxes and phase change materials for unparalleled thermal dissipation in die, component and module levels of electronic packaging. Other AIT products include Conformal Coatings to combat UV, moisture and humidity corrosion.

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As the nation's first complete end-to-end silicon photonic manufacturing ecosystem, AIM Photonics provides our members and customers with crucial technology on-ramps and access to strategic U.S. government, industry, and academic communities to help advance their innovative ideas from concept to manufacturing-ready prototypes.
Our state-of-the-art test, assembly and packaging facility in Rochester, NY is the nation's only accessible 300 mm wafer facility offering both photonic and electronic packaging capabilities. Our extensive toolset comprises all standard processes such as wafer bumping, fiber attach, wire bonding, die attach, flip chip and dicing, as well as advanced packaging and heterogeneous integration capabilities.

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Ajinomoto Fine-Techno Co., Inc. (AFT) is a subsidiary of the Ajinomoto Group responsible for the fine chemicals division. AFT delivers materials that can suit a wide range of customer needs with our four main strengths: molecular design, formulation, process development, and solutions. We have grown to play a major part in the value chains for electronics, automotive, and a variety of other products. We strive to provide the highest quality products, services, and information for our customers. Beyond our Ajinomoto Build-up film®, we've expanded our material portfolio to include molding, photo dielectric, magnetic, and optoelectronics.

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Being a leading semiconductor equipment and wafer reclaim supplier in Taiwan, Scientech Corporation has launched the development of wet process equipment in 2003. Scientech has successively supported customers in Mini/Micro LED, compound semi and power components such as IGBT, SiC and GaN industries, as well as advanced packaging process such as Bumping, Fan-out, Chip-On-Wafer and so on. Our wet process equipment has been successfully verified in the latest Chiplet's 2.5D/3D packaging process technology and smoothly introduced into mass production. Scientech wet process equipment with single-wafer and wet-bench type, can be highly customized to adapt new process flow and operational interface.

Booth 731
SCREEN Holdings Co., Ltd.
+81-754147
screen.co.jp/en
Tenjinkita-machi 1-1, Teranouchi-agaru
4-chome,
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Kyoto, Kyoto 6028585, Japan
Contact: Yoshiteru Takaya
y.takaya@screen.co.jp
SCREEN is a leading supplier of equipment and process solutions for the global semiconductor industry and related markets. Our technologies enable innovation throughout the electronics industry, and our portfolio covers a wide range of products not only for semiconductor frontend cleaning but also for panel-level coating, direct imaging lithography for substrate etc. with its global infrastructure for wide application and service. We offer wafer bonding integrated our unique cleaning technology at this show. Please visit us at our Booth to discuss your advanced packaging requirements and challenges.

Booth 634
SEKISUI Chemical Co., Ltd.
+1-972-277-2950
sekisui.co.jp/electronics
1501 West LBJ Freeway, Suite 530
Dallas, TX 75234
Contact: Takaishi Hiratsuka
takaichi.hiratsuka@sekisui.com
SEKISUI is a Japanese chemical company established in 1947. Our various solutions are used in the electronics and mobility area. For the semiconductor market, our products like the interlayer insulation film are used in the high spec semiconductor, the thermal interface materials with unique and high dissipation using carbon fibers are used in high thermal management, and the specialty adhesives are used in the processing of materials with temporary adhesion and for easy peeling.

Booth 612
Semiconductor Equipment Corp
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Moorpark, CA 93021
Contact: Lester Salvatierra
lsalvatierra@semicorp.com
Semiconductor Equipment Corporation is a small innovative company that has designed and manufactured back end manual equipment for the semiconductor and related industries for more than 46 years. In that time we have expanded our business to distribute products for Nitto Denko and Hugle Electronics. We service everything we sell.

Booth 405
Senju Comtek Corp (SMIC)
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Contact: Derek Daily
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Senju Comtek Corp is the Americas subsidiary of Senju Metal Industry Co (SMIC) of Japan, a global leader in soldering materials and related equipment. Senju provides world class solder spheres (balls), solder pastes, attach flux and various other unique soldering technologies for your semiconductor application. Senju manufactures solder pastes in the USA at our Silicon Valley and Chicago regional facilities.

Booth 313 & 315
SETNA
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set-na.com
343 Meadow Fox Ln
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Contact: Matthew Phillips
mphillips@set-na.com
SETNA sells SET device bonders and Ontos atmospheric plasma equipment. SETNA has a long and rich history with-in the semiconductor packaging industry. Bonding chip to chip, chip to wafer using the most flexible platform for every type of bonding interface, including TCB/Reflow/Hybrid/Direct/High Force/Low Force. Both SET device bonders and OES plasma systems provide the most flexible platforms for cleaning and activating surfaces (removing oxides/Organics/Passivation of surfaces) while also successfully and consistently achieving the highest placement accuracy in the industry.

Booth 426
SHIKOKU CHEMICALS CORPORATION
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shikoku.co.jp
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Orange, CA 92868
Contact: Noritake Furuki
furukin@shikoku.co.jp
SHIKOKU CHEMICALS Co. has synthesized a number of unique resin crosslinking agents using our organic synthesis technology. Among them, we have discovered that the isocyanuric acid skeleton has excellent electrical properties, and are developing a new crosslinking agent with this skeleton as its core structure. Also, GliCAP is a new interface chemical developed based on our organic synthesis technology. Unique organic coating formed on copper surface directly improves adhesion between copper and resin effectively. SHIKOKU CHEMICALS Co. will continue to design and create materials that can balance the characteristics that have become issues in the market.

Booth 311
Shin-Etsu MicroSi
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Contact: Ian Holden
iholden@microsi.com
Founded in 1984 as a subsidiary of the General Electric Company, Shin-Etsu MicroSi is a driving force in both the semiconductor and microelectronics industries worldwide. By infusing science and chemistry with innovation and collaboration, we create leading-edge solutions that turn possibilities into realities–while providing the proven quality and time-tested dependability on which our customers rely. From computers to cell phones, 5G, automobiles, coatings, and more, our products are used by companies throughout the world to make the integrated circuits and semiconductor devices that power everyday living.

Booth 407
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Yamaha Robotics Holdings is a leading company in semiconductor manufacturing equipment. Under Yamaha Robotics Holdings are three Group companies; Shinkawa, APIC Yamada and PFA Corporation. Shinkawa: Wire Bonders, Die Bonders, Flip Chip Bonders, Bump Bonders. APIC Yamada: Molding System, Package Singulation System, Test Handler & Transport System, Trim & Form System, Precision DIE SET. PFA Corporation: Crystal oscillation manufacturing equipment, Camera module manufacturing equipment, Flat Panel inspection equipment (AOI), MEMS Related equipment & Other automatic assembly systems. We aim to provide a total solution that exceeds our customers' expectation as the "Turn-Key" provider in the field of semiconductors back-end processing.

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Shinko develops and produces Semiconductor Packages for the miniaturization, acceleration and performance of semiconductors. We aim to enrich and contribute to the lives of people all over the world by providing cutting-edge packaging for markets including AI/ML, HPC, Data and Networking, mobile and automotive

Booth 410
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Sigray is a San Francisco Bay Area based company, specializing in the development & integration of high-resolution, high-throughput 3D X-ray microscopes. Our team is comprised of x-ray professionals with extensive experience in x-ray source, optics, and instrumentation development, with a unified focus on bringing next-generation X-ray technologies to labs & fabs. The latest release, Apex XCT, is capable of producing sub-micron 3D X-ray images of large PCBs and wafers, with only minutes required for each data collection.

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SkyWater Technology is a U.S.-based semiconductor manufacturer and a DMEA-accredited Trusted supplier. SkyWater's Technology as a Service model streamlines the path to production for customers with development services, volume production and heterogeneous integration solutions in its world-class U.S. facilities. This pioneering model enables innovators to co-create the next wave of technology within diverse categories including mixed-signal CMOS, ROICs, rad-hard ICs, MEMS, superconducting ICs, photonics, and interposers. SkyWater serves growing markets including aerospace & defense, automotive, biomedical, cloud & computing, consumer, industrial and IoT.

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Smart High Tech is a Swedish company focusing on manufacturing and developing heat-dissipating materials reinforced with graphene with a focus on cooling electronics, processors, graphics cards, LEDs, and other heat-sensitive and heat-intensive products. We offer high-performance graphene-reinforced materials and associated process know-how. Our standard GT-TIM product line offers up to 90 W/mK through plane thermal conductivity and an effective thermal resistance below 6.5 Kmm^2/W at a mounting pressure of 40 Psi/275kPA with no plastic deformation, drying, or pump out in high power density

applications. Smart High Tech offers solutions for air cooled systems, immersion, aerospace, optoelectronics, automotive, and other sectors.

Booth 711
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Sono-Tek's ultrasonic coating technology is currently being used at the package level for EMI shielding coatings. Tested and approved using market-available EMI materials, our unique non-clogging spray coating systems, with a low temperature heat cure, offer a cost effective and faster alternative to costly sputtering equipment. Our FlexiCoat EMI system was designed to run continuously in production at a higher throughput than sputtering, at roughly 1/10th the cost. Sono-Tek's ultrasonic coating technology is known for thin, repeatable, and low waste coatings. Other applications include: Photoresist deposition, polyimide, flux dispensing for flip chip applications, and nano suspensions (CNT, graphene, nano-wires, etc).

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Contact: Graham Bay
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Founded in 1999, Surfx Technologies has developed and brought to market a true low-temperature, variable chemistry, atmospheric pressure plasma. Our products incorporate the most advanced plasma technology and are covered by multiple U.S. patents. Surfx's mission is to be the worldwide leader in the surface treatment of materials for the semiconductor, electronics assembly, aerospace, and medical device industries. We are driven by a total commitment to our customers. We take pride in our products and service. Our promise is to deliver to you the highest quality product for your manufacturing needs.

Booth 627
SUSS MicroTec Inc.
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suss.com
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Contact: Emyr Edwards
emyr.edwards@suss.com
SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring in the semiconductor industry and related markets. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. In close cooperation with research institutes and industry partners SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Imprint Lithography as well as key processes for Wafer-Level Packaging, MEMS and LED manufacturing. With its global infrastructure for applications and service, SUSS MicroTec supports more than 8,000 installed systems worldwide.

Booth 416
Taiyo Ink
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1731 Technology Dr, Suite 595
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Contact: Yuya Suzuki
yuyas@taiyo-america.com
High performance and high reliability materials showcased by TAIYO INK are beneficial for advanced IC packaging, as well as conventional packaging applications. Examples of the advanced materials include photo-imageable dry film dielectric, PVI-3 for high density packaging, and ultra-low loss dry film dielectric, Zaristo for high speed/frequency packaging. Taiyo also develops variety of new dielectric materials with special performances, such as magnetic, optical, or electrical, based on our industry-proven solder resist material technologies. Talk to you at our booth!

Booth 403
TATSUTA Electric Wire & Cable Co., Ltd.
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tatsuta.com
6-5-1 Kunimidai
Kizugawa, Kyoto 619-0216, Japan
Contact: Susumu Chiba
s-chiba@tatsuta.co.jp
Tatsuta Electric Wire & Cable Co., Ltd is a leading manufacturer of innovative advanced paste for high performance electronics. By using our electrically and thermally conductive paste, higher density interconnection, longer product life and outstanding reliability are achievable. With our knowledge of metal-resin formulation technology, our materials support your development cycles/process time shorten and process temperature lower as well, which enables lower carbon emission and eco-friendly process. For more information, please visit our website and you will find our latest developments.

Booth 436
TAZMO
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Fremont, CA 94538
Contact: Takashi Abe
takashi.abe@tazmo.co.jp
Tazmo is a semiconductor manufacturing equipment company, offering: (1) Temporary bonding and de-bonding tool for Silicon wafers and support glass for back grinding process. (2) Coater/Developer for semiconductor manufacturing processes. Coating with highly viscous materials and other materials that are difficult to work with while achieving good coating uniformity. (3) Cleaning tools and surface treatment for semiconductor manufacturing processes. Cleaning machines for manufacturing of semiconductor, slurry supply units, chemical supply units and phosphoric acid recycling. (4) Wafer transfer systems. Tazmo provides various wafer transfer systems to other semiconductor manufacturing equipment suppliers. These products include robots, aligners and EFEM.

Booth 501
TDK Corporation
+1-972-409-4519
product.tdk.com/en/products/fa/index.htm
475 Half Day Rd, Suite 300
Lincolnshire, IL 60069
Contact: Sara Lambeth
sara.lambeth@tdk.com
TDK is a leader in factory automation systems. Our products include TDK precision AFM 15 Thermosonic and AFM 15 Thermal Compression flip chip die bonders. TDK flip chip die bonders use a micro scrub process to lower heat required for die attach process. TDK micro scrub process eliminates flux and supports 5~10 mm line width and 3 mm spacing.

Additionally, TDK load ports feature high-performance that meet your needs for particle-free operation, high throughput and high durability of continual motion. In addition to the TAS300 load port, we also offer the TAS300 J1 and the TAS200.

Booth 606
Technic Inc.
+1-401-781-6100
technic.com
47 Molter St
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Contact: Felicity Moore
fmoore@technic.com
Technic supplies chemistry solutions for advanced semiconductor packaging. Marketed under the name Elevate, Technic's electrodeposition chemistries are well respected for innovation and high quality in such applications as RDL, pillars, microbumps, and LED packaging. Technic also supplies several high-performance photoresist strippers for liquid and dryfilm resists, as well as a full range of metal etchants and cleaners marketed under the names, TechniStrip®, TechniEtch, and Techniclean. For analytical controls, the Technic RTA 3D will be on display. The RTA has become the leading analytical control system for damascene copper processes and backend packaging applications for controlling TSV and copper pillar processes.

Booth 325
TechSearch International Inc.
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TechSearch International, Inc. has a 37-year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. Research topics include WLP, FO-WLP and panel-level processing, Flip Chip, CSPs, BGAs, 3DICs including hybrid bonding, Si Interposers, System-in-Package (SiP) and Heterogeneous Integration, embedded components, automotive electronics, and power devices. Multi-client and single client consulting services are offered. TechSearch International professionals have an extensive network of more than 24,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

Booth 537
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teikoku-taping.com
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robert.garrett@teikoku-taping.com
Manufacturer of tape lamination, tape removal, wafer/substrate mounting to film frame, and UV irradiation equipment for back-grinding, dicing, dry film resist and other taping applications.

Booth 435
Tektronix CSO
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tek.com/en/component-solutions
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Tektronix Component Solutions has a rich history of delighting customers by solving tough technical challenges through our microelectronics design, test, and manufacturing services. In addition, we take pride in – and are known for – our deep collaboration and responsiveness to delight customers. We have more than 50 years of manufacturing experience across a diverse range of products and customers, specializing in partnerships with the defense industry.

Booth 413
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TOK's Micro Processing Technology Creates Inspiration. TOK's state-of-the-art micro processing technology produces groundbreaking and innovative products. We have pioneered the development of polymer-containing functional photoresists based on photolithography technologies that are essential for the formation of semiconductor circuits. Along with advancement in the micro-fabrication of an electronic circuit, our sophisticated technologies provide solutions to enhance the functionality of semiconductors, such as miniaturization, high-integration, multi-functionality, and high-speed. We offer various new materials necessary for many device manufacturers, including advanced immersion photoresists enabling the formation of several tens nanometer scale features.

Booth 619
Toray International America Inc.
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Toray Industries is a leading Non-Conductive Film (NCF) provider for flip chip packages, photo-definable adhesive film for build-up substrates and packages with cavity structures. Toray's unique polyimide and film processing technologies provide excellent reliability and performance. "Photoneece" is Toray's photo-definable polyimide coatings for the front-end buffer layer and back-end re-distribution layer for WLP and TSV. We also offer environmentally friendly NMP-free materials. Toray Engineering Co., Ltd. provides state-of-the-art Flip Chip Bonding Equipment for semiconductor packaging with alignment accuracy. And Vacuum Encapsulation Equipment for void-free printing, Wafer Inspection Equipment with high speed, and a Coating system for substrate manufacturing are lined-up.

Booth 427
TOWA USA Corporation
+1-408-779-4440
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1430 Tully Rd, Suite 416
San Jose, CA 95122
Contact: Terence Koh
tkoh@towa-usa.com
TOWA is a leading company in the semiconductor molding equipment market. We offer equipment using our high quality / flow free compression molding method and our proven transfer molding method. We also manufacture ultra-precision molds that have been highly acclaimed by customers. Together with our molding equipment, our singulation system was developed from both aspects of the dicer and product handler to provide the optimal method of singulation for each product type. The result is high quality cutting whilst improving customers' productivity with high throughput. Located in the heart of Silicon Valley, TOWA USA San Jose Package Development Center was established to support customers' development programs. Our activities are centered around Compression Molding for Advanced Packaging and we collaborate with a broad spectrum of industry members from IDMs, OSATs, Fabless Companies, Government Contractors, Technical Institutes and Consortiums. Please contact us for more information.

Booth 508
TOYOCHEM Co., Ltd.
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Chuo-ku, Tokyo 1048379, Japan
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Leveraging its original resins, a core material used in Group products, the Polymers and Coatings segment develops a variety of solutions tailored to the needs of the times. Based on its synthesis and coating processing technologies, a large number of its functional products are used in many applications indispensable to everyday life, such as automotive and electronics, solar cells for energy, medical and healthcare, and many more.

Booth 718
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Toyota Tsusho America, Inc is the trading arm of Toyota Motor Group and we are developing the business in seven divisions such as Electronics & Chemical, Automotive, and the supporting administrative division. We have 35 locations in North America, in addition to 43 affiliate and subsidiary locations to provide valuable products and services for enterprise-level industries such as automotive, electronics, and more. As the Electronics & Chemical division, we are providing and developing services and cutting-edge products for semiconductor products such as Photoresist, CMP Slurry, High-frequency CCL, and Encapsulants to contribute to the growth of the electronics industries.

Booth 433
USHIO Inc.
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Established in 1964, USHIO INC. (TOKYO: 6925) is a leading manufacturer of light sources such as lamps, lasers, and LEDs, in a broad range from ultraviolet to visible to infrared rays, as well as optical equipment and cinema-related products that incorporate these light sources. It also makes products in the electronics field (such as semiconductors, flat panel displays and electronic

components) and in the visual imaging field (including digital projectors and lighting). Many of these products enjoy dominant market shares. In recent years, USHIO has undertaken business in the life science area, such as the medical and the environmental fields.

Booth 715
Vanguard Automation GmbH
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Headquartered in Karlsruhe, Germany, Vanguard Automation develops process technology and machines for creating low-loss photonic connections between passive and active components leveraging its unique IP portfolio for Photonic Wire Bonding and facet-attached micro-optics. Augmenting nano-print technology, Vanguard Automation's solutions enable high packaging density, increased design flexibility and fabrication throughput.

Booth 617
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With over 20 years of experience, XYZTEC has established our name as the technology leader in bond testing throughout the world. With 100% of our focus on bond testing, XYZTEC teams with customers to offer innovative solutions that address their specific bond test needs. Our mission is to take on the challenges of many different industries by offering customers products that improve their quality and increase their bottom line.

Booth 535
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Yole Group specializes in the strategic analysis of markets, the supply chain, and technological developments related to the semiconductor industry and adjacent industries. Leveraging our network in the field of semiconductors and the multidisciplinary profile (scientific, technical, and market-oriented) of our analysts, we support our clients in the understanding of markets, the evolution of technologies, and their implementation in industry.

Booth 730
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Zuken is a leading global software company specializing in electrical and electronic design solutions. Established in 1976, Zuken is consistently at the forefront of technology innovation, offering a comprehensive range of system-level 2D/3D electrical and electronic toolsets, including the CR-8000 and E3.series product families. With integrated design data management capabilities, Zuken empowers businesses with robust and efficient design solutions.

Booth 327
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Zymet manufactures Adhesives & Encapsulants and has been serving the electronics industry for over 30 years. Products include reworkable underfills and edgebond adhesives for high reliability and harsh environment applications. Other products include ultra-low stress adhesives, electrically conductive adhesives, thermally conductive adhesives, and non-conductive pastes. HDM's worldwide organization allows it to provide technical support and expertise to its customers with local personnel.

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FIRST CALL FOR PAPERS

IEEE 75th Electronic Components and Technology Conference • www.ectc.net
May 27 – May 30, 2025 at the Gaylord Texan Resort & Convention Center, Dallas, Texas, USA

The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee. Authors are encouraged to review the sessions of the previous ECTC programs to determine which committees to select for their abstracts.

Applied Reliability: Reliability of 2D, 2.5D, Si-bridge, 3D, chiplets, SiP, WLCSP, FOWLP, FOPLP & heterogeneous integration; interconnect reliability in micro-bump, micro-pillar, Cu-pillar, TSV, TGV, RDL, HDI, stacked-die, hybrid-bond, flip chip & wire bonded packages; novel reliability test methods, life models, FA techniques & materials characterization; component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays & memory; interfacial/bulk reliability of solder alloys, mold compound, epoxy, underfill, overcoat, build-up film, solder resist, & substrate laminate.

Assembly and Manufacturing Technology: Assembly and manufacturing challenges for new markets; Die bonding methods and processes; embedded packaging and modules; Wafer level process/materials technologies; Die and package singulation manufacturing; New & next generation substrates; Smart factory/manufacturing; Design for Manufacturing; Assembly related test/yield hardware development; Integrating advanced thermal solutions in manufacturing: Design/performance, integrating solutions, thermal materials, low stress/ high thermal; Process advancements/yield enhancements: Cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/ compression/injection mold; Heterogeneous integration and process: chiplets, 3D stacking, bridge technology, large body, warpage management; Shielding/ protection technologies and manufacturing and market requirements.

Emerging Technologies: Emerging, novel and unique packaging and material technologies for: soft and intelligent packaging, flexible/stretchable hybrid electronics, bioelectronics, extreme harsh environment, nanomanufacturing, AI electronics packaging and its application, EV Power electronics and energy storage,MEMS & NEMS, packaging for wide band gap devices, anti-tamper, cryptography, additive, subtractive or hybrid manufacturing, smart manufacturing industry 4.0, packaging for quantum computing and other cryonic application, electro-optical integration, green and sustainable electronics, green and sustainable electronics, net zero strategy/technology.

RF, High-Speed Components & Systems: 5G/6G, IoT, cloud computing, autonomous vehicles, AI/machine learning; Antennas, sensors, power transfer, electromagnetic compatibility, wired/wireless communications, RF to THz; Electrical/multi-physics modeling and characterization of interconnects, modules, and heterogeneous integration system; chiplet, heterogeneous Integration, chip-to-chip, die-to-die, SiP/MCM/system co-design (chip/pkg/board); opto-Electrical (OE) hybrid integration, analog packaging, power electronics modeling/ characterization; high-speed/frequency (RF, mmWave, THz) signal integrity, power integrity, and EMI/EMC

Interconnections: Interconnects for chiplets, heterogeneous integration, hybrid bonding, C2W, W2W, fan-out, panel-level, TSV; Interconnects for 2.5D/3D, Si/glass/organic interposers, fine-pitch/multi-layer RDL, SiP, ; Interconnects for thermo-compression/laser assisted/transient liquid phase bonding, low temperature solder, flip-chip, micro-bump, Cu pillar, Wirebond, Al ribbon bond ; Printable interconnects, flexible interconnect, quantum interconnects, optical interconnects ; Interconnection material, characterization and reliability ; Conductive/non-conductive adhesives, ACF, under-fill, molding compounds ; Thermal interface materials, thermal/mechanical/electrical tests and reliability; Interconnects for AI, Silicon photonics, HPC, mobile, 5G, IoT, power and rugged electronics, medical and health ; Interconnects for automotive, aerospace, flexible hybrid electronics, micro-LED display

Materials & Processing: Wafer/panel level packaging materials and process advancements; Advanced materials and processes for FOWLP, FOPLP, 2.5D/3D, SiP, TSV, chiplets, and advanced packaging architectures; Harsh environment resistant materials; Packaging substrates; Flexible, stretchable, & wearable electronics; Temporary wafer bond/debond materials/processes; Permanent adhesives; TCB and hybrid bonding; Adhesives, dielectrics and underfills; Emerging electronic materials & processes; Conductive and Non-Conductive adhesives; 3D Materials and Thin Wafer Processing, Novel solder metallurgies; Molding compounds; Thermal interface materials; Advanced wire bonding, Novel Materials and Processing, Emerging Materials.

Thermal/Mechanical Simulation & Characterization: Thermal/ mechanical simulation and characterization at component, board, and system levels for all packaging technologies: reliability related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); material constitutive relations; chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; novel modeling techniques including multi-scale physics, co-design approaches; quantum computing; measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; application of artificial intelligence on modeling, characterization, digital twin; and credible simulations for virtual release; CFD simulation including underfilling/molding process simulation.

Packaging Technologies: 2.xD/3D architecture/design of energy efficient C2C links, structures, thermal solutions, methods & processes for HPC; Heterogeneous (chiplet) integration for 2.5D / 3D-IC; Silicon / Glass / Organic Interposer & advanced package technology; DD Cu / Cu TSV / Hybrid Bonding; Embedded die / bridge, flexible, advanced substrates & modules; Fan-out wafer and panel level packaging; Advanced flip-chip, SiP, CSP, PoP & CPO; RF, wireless, MEMS sensors & IoT; Automotive, wireless power and power electronics; Bio, medical, flexible & wearable packaging.

Photonics: Assembly and packaging for all applications that leverages photonics components and circuits. Topics of Specific interest include Packaging of Photonics Integrated Circuits for telecom, datacom, and 5G, Co-packaged and Near-packaged optics, Heterogeneous integration, artificial intelligence, quantum systems, and sensors, medical devices, automotive/LIDAR, aerospace, defense, and cryogenic/harsh environment, RF/MW photonics, free-space optics, AR/VR, WDM, and high power lasers, micro-LEDs and 3D light-field displays, imaging and environmental sensors, new materials, connectors, EDA tools, and test methods/equipment.

Interactive Presentations: Abstracts may be submitted related to any of the topics listed. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract that describes the novelty, scope, content, and key points of your proposed manuscript via the website at www.ectc.net.

If you have any questions, contact:
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Abstracts cannot contain more than 700 words and must be received by October 7, 2024, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors with your submission. The authors are notified about the abstract selection outcome by December 13, 2024.

Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From proposals received, 16 PDCs are selected for offering at the 75th ECTC on Tuesday, May 27, 2025.

Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 20, 2024. Authors are notified of course acceptance with instructions by December 13, 2024.

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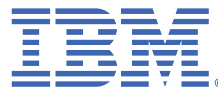

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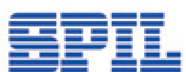

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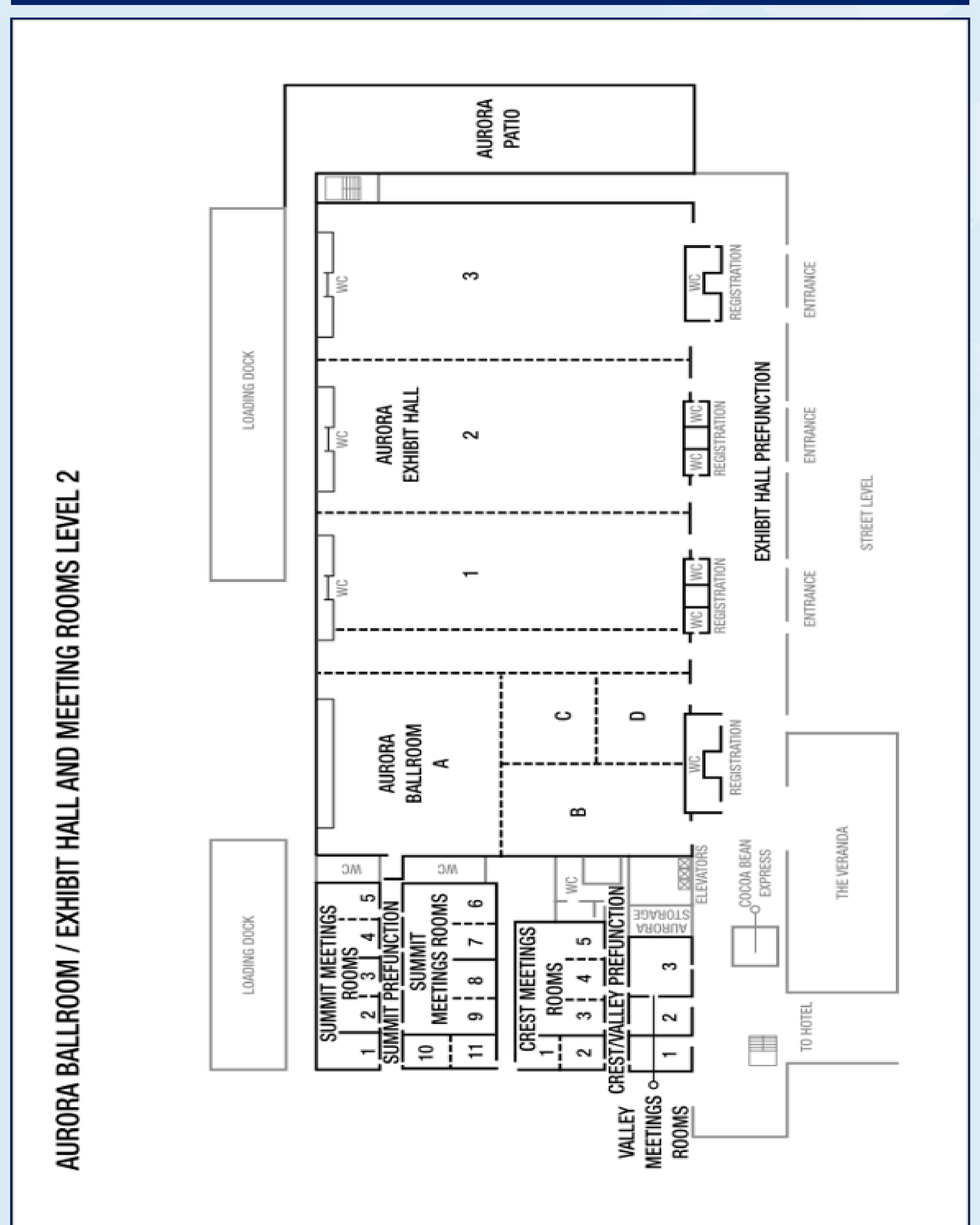
AURORA BALLROOM / EXHIBIT HALL AND MEETING ROOMS LEVEL 2
LOADING DOCK
LOADING DOCK
AURORA PATIO
AURORA EXHIBIT HALL
1
2
3
WC
REGISTRATION
ENTRANCE
EXHIBIT HALL PREFUNCTION
STREET LEVEL
AURORA BALLROOM
A
B
C
D
SUMMIT MEETINGS ROOMS
SUMMIT PREFUNCTION
SUMMIT MEETINGS ROOMS
CREST MEETINGS ROOMS
CREST/VALLEY PREFUNCTION
VALLEY MEETINGS ROOMS
AURORA STORAGE
ELEVATORS
COCOA BEAN EXPRESS
THE VERANDA
TO HOTEL

Gaylord Texan Resort & Convention Center, Dallas, TX
May 27 – 30, 2025

ECTC is turning 75 in 2025 and to celebrate we will be hosting the conference at the Gaylord Texan Resort & Convention Center! From the 10-acre Paradise Springs Water Park to an exciting lineup of family-friendly activities and entertainment, there's something for the entire family to enjoy. Guests can explore the four-and-a-half acres of airy, indoor garden atriums, four award-winning restaurants, bars, the world-class Relâche Spa, and a state-of-the-art fitness center.

Conference attendees will enjoy the resort's 490,000 sq. ft. of flexible meeting space, 1,814 beautiful guest rooms, and 127 spectacular suites as well as our lakeside events venue, Glass Cactus, perfect for live entertainment and events. Located near DFW Airport, LEGOLAND® Discovery Center, Cowboys Golf Club, Historic Downtown Grapevine, and water sports on Lake Grapevine itself, all are convenient so everyone can do more of what they love!

CONFERENCE AT A GLANCE

REGISTRATION

Monday, May 27, 2024
3:00 p.m. - 6:00 p.m.

Tuesday, May 28, 2024
6:45 a.m. - 7:45 p.m.*
*(AM PD Courses & Special Session Only)

Wednesday, May 29, 2024
6:45 a.m. - 4:00 p.m.

Thursday, May 30, 2024
7:00 a.m. - 4:00 p.m.

Friday, May 31, 2024
7:00 a.m. - 12:00 Noon

Rockies Square, behind Cocoa Bean Coffee Shop

EXHIBITION HALL

Wednesday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 6:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.

Thursday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 4:00 p.m.
Aurora 1

SPEAKER PREPARATION ROOM

Tuesday – Friday
7:00 a.m. – 5:00 p.m.
Valley 3

MAIN STAGE MORNING SESSIONS

Wednesday: ECTC Keynote

Thursday: EPS Plenary Session

Friday: IEEE EPS President Panel

8:00 a.m. - 9:15 a.m.
Aurora A

MAIN STAGE EVENING SESSIONS

Tuesday: IEEE EPS Seminar
7:45 p.m. - 9:15 p.m.

Wednesday: ECTC / ITherm Diversity Panel
6:30 p.m. - 7:30 p.m.
Aurora A

GALA RECEPTION

Thursday: 6:30 p.m.
OUTSIDE: Front Range Lawn (Lower Level)

TUESDAY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m. – 8:30 a.m.
Summit 10 & 11

Professional Development Courses (PDCs)
8:00 a.m. – 12:00 p.m.
1:30 p.m. - 5:30 p.m.
See page 8 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop
8:00 a.m. – 4:30 p.m.
Aurora D

ECTC Special Sessions
No. 1: 8:30 a.m. – 10:00 a.m.
No. 2: 10:30 a.m. – 12:00 p.m.
No. 3: 1:30 p.m. – 3:00 p.m.
No. 4: 3:30 p.m. – 5:00 p.m.
Aurora B

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Summit & Crest Foyers

Lunch
12:00 p.m. – 1:15 p.m.
Aurora A & C

ECTC Exhibition Setup
1:00 p.m. – 5:00 p.m.
Aurora 1

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Summit Foyer

General Chair's Speakers Reception
6:00 p.m. – 7:00 p.m.
Mountain Pass Restaurant, Upper Level
By invitation only

Young Professionals Networking Panel
7:00 p.m. – 7:45 p.m.
Aurora D

WEDNESDAY – FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Crest 3-5

Sessions
9:30 a.m. – 12:35 p.m. or
2:00 p.m. – 5:05 p.m.
see pages 10-21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Aurora B

Sessions 2, 8, 14, 20, 26, 32
Aurora D

Sessions 3, 9, 15, 21, 27, 33
Crest 3-5

Sessions 4, 10, 16, 22, 28, 34
Summit 8-9

Sessions 5, 11, 17, 23, 29, 35
Summit 6-7

Sessions 6, 12, 18, 24, 30, 36
Summit 4-5

Interactive Presentations
Sessions 37 - 41
10:00 a.m. - 12:00 p.m. or
2:30 p.m. - 4:30 p.m.
Aurora A-C Corridor
see pages 22 - 25 for specifics

Lunch
12:45 p.m. - 1:45 p.m.
Aurora A & C

Refreshment Breaks
10:30 a.m. – 11:15 a.m.
3:00 p.m. – 3:45 p.m.

Wednesday & Thursday
Aurora 1

Friday
Aurora, Crest, and Summit Foyers

Mark Your Calendars Now!

Gaylord Texan Resort & Convention Center
Dallas, Texas

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

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For more information visit www.ECTC.net